

# Formal Verification and Performance Analysis of Embedded Systems

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CISS, Aalborg U., DK



Michael R. Hansen

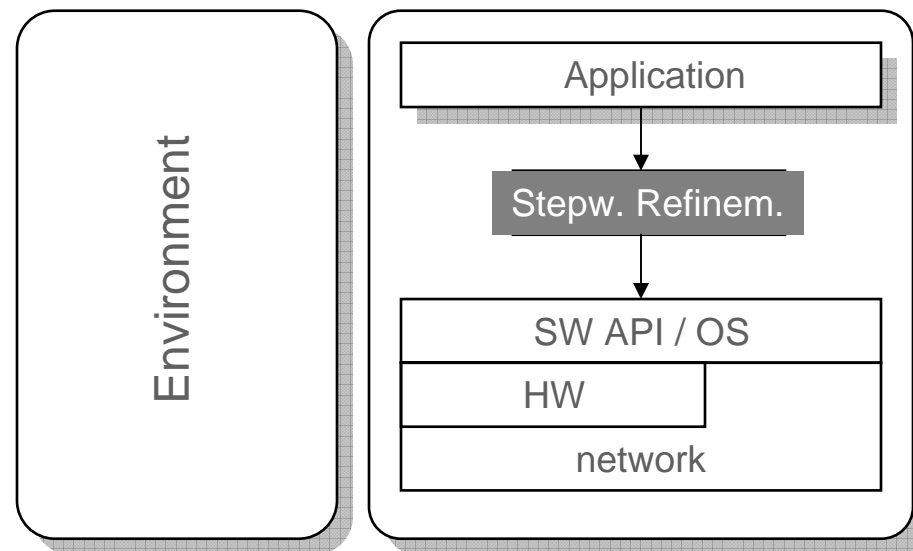
IMM, Technical U. of Denmark, DK



DaNES



# DaNES Challenges



# DaNES Challenges



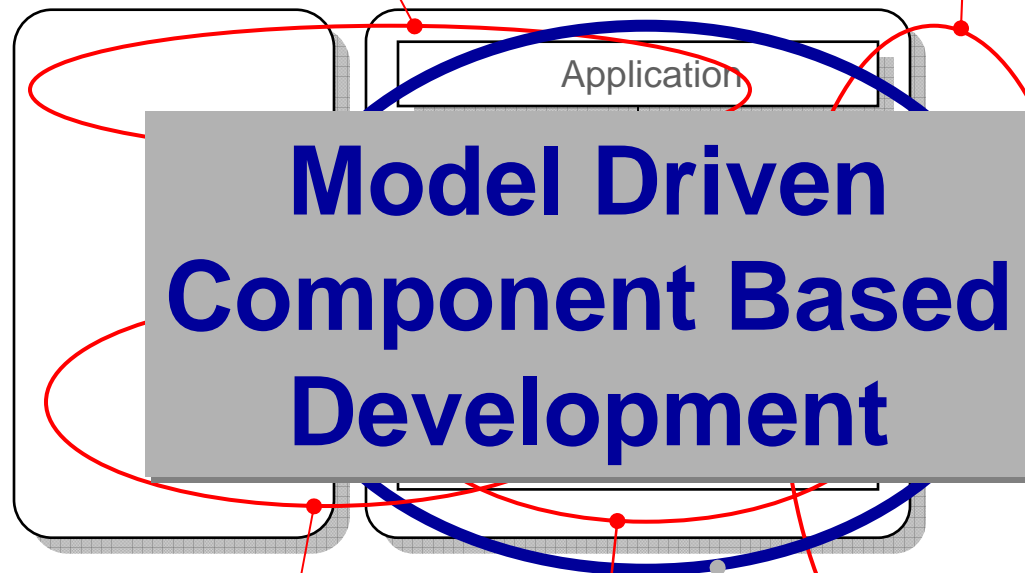
Selfdiagnostic & -repair



TERMA<sup>™</sup>



Test & Verificaiton



Embedded & Distributed Control



Informatik og Matematisk Modellering



Development



GATEHOUSE

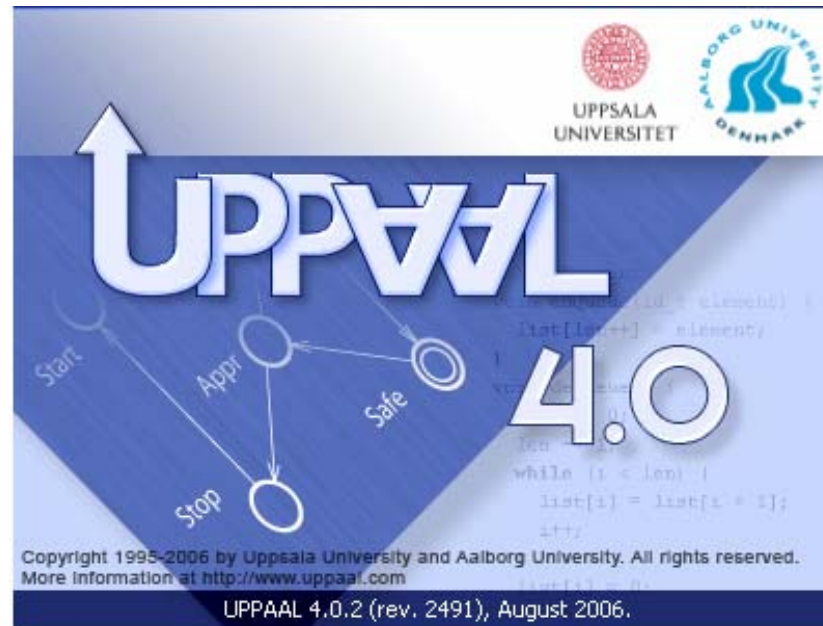
ice power



- Validation and Performance Analysis in UPPAAL / Kim G. Larsen
- Formalising the ARTS MPSoC Model in UPPAAL / Michael R. Hansen
- Discussion Points / KGL & MRH

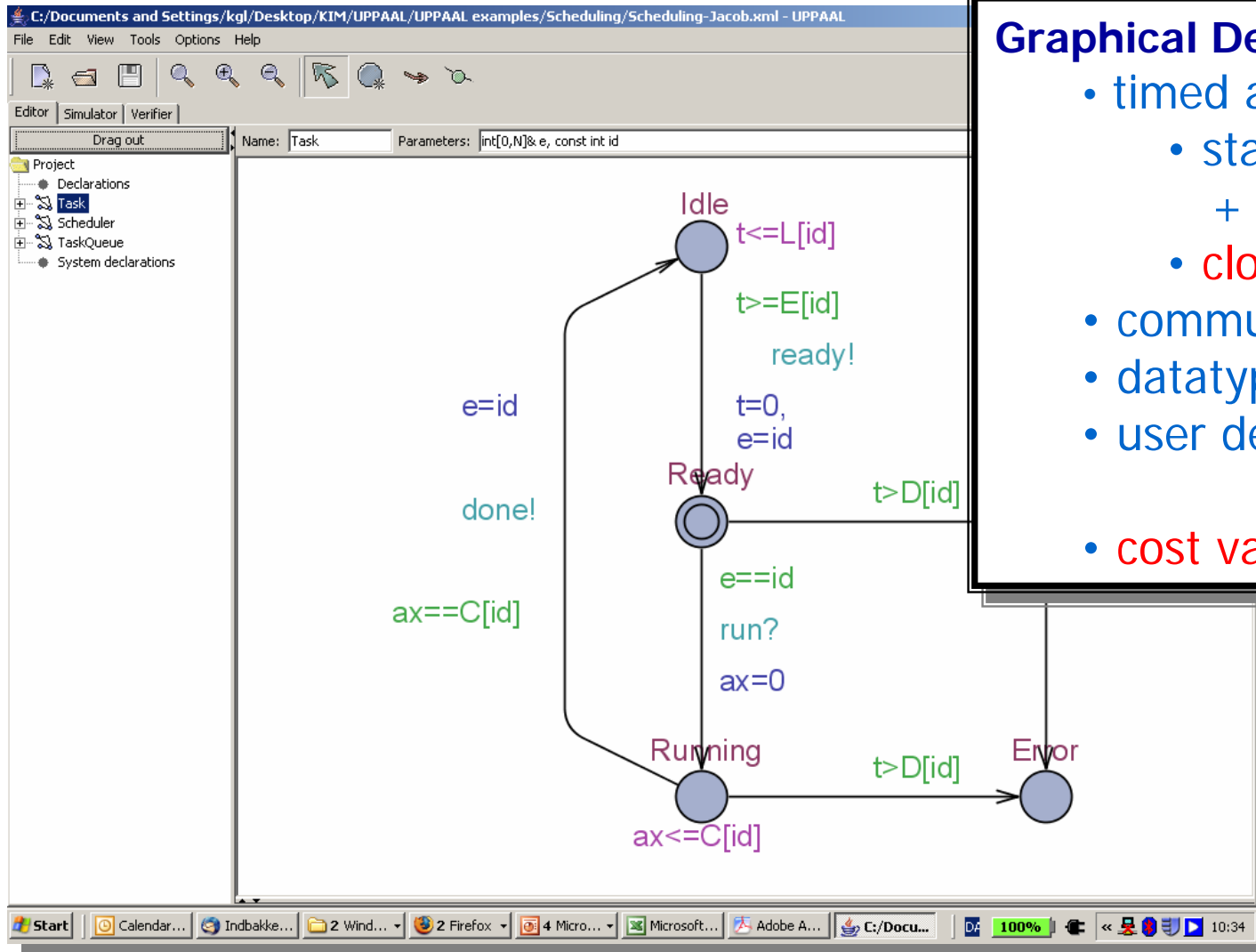


# Validation and Performance Analysis in UPPAAL



DaNES





## Graphical Design Tool

- timed automata =
  - state machines
  - +
    - **clocks**
- communication
- datatypes
- user defined functions
- **cost variable**



The screenshot displays the UPPAAL graphical simulator interface. It features several panels:

- Task0, Task1, Task2:** State machines for individual tasks. Task0 has states Idle, Ready, and Running. Task1 has states Idle, Ready, and Running. Task2 has states Idle, Ready, and Running. Transitions are labeled with events like  $t = E[i]$ ,  $t = D[i]$ , and  $ax = C[i]$ .
- Scheduler:** A state machine with states nonempty? and empty?. Transitions are labeled nonempty? and empty?.
- Simulation Trace:** A list of events such as Queue, nonempty: Queue --> Scheduler, run: Scheduler --> Task0, done: Task0 --> Scheduler, and rem: Scheduler --> Queue.
- Variables:** A window showing the current values of variables:  $el = 2$ ,  $E[0] = 20$ ,  $E[1] = 20$ ,  $E[2] = 10$ ,  $L[0] = 30$ ,  $L[1] = 25$ ,  $L[2] = 12$ ,  $D[0] = 30$ ,  $D[1] = 25$ ,  $D[2] = 12$ ,  $C[0] = 4$ ,  $C[1] = 2$ ,  $C[2] = 1$ ,  $P[0] = 1$ ,  $P[1] = 2$ ,  $P[2] = 3$ , and  $Queue.list[0] = 2$ .
- Task State Diagram:** A diagram at the bottom showing the states of Task0 (Ready, Running, Idle), Task1 (Ready, Running, Idle), Task2 (Ready, Running, Idle), Scheduler (Occ, Start), and Queue (Start). Red arrows indicate transitions between these states.

## Graphical Simulator

- visualization and recording
- inexpensive fault detection
- inspection of error traces
- Message Sequence Charts
- (Gantt Charts)

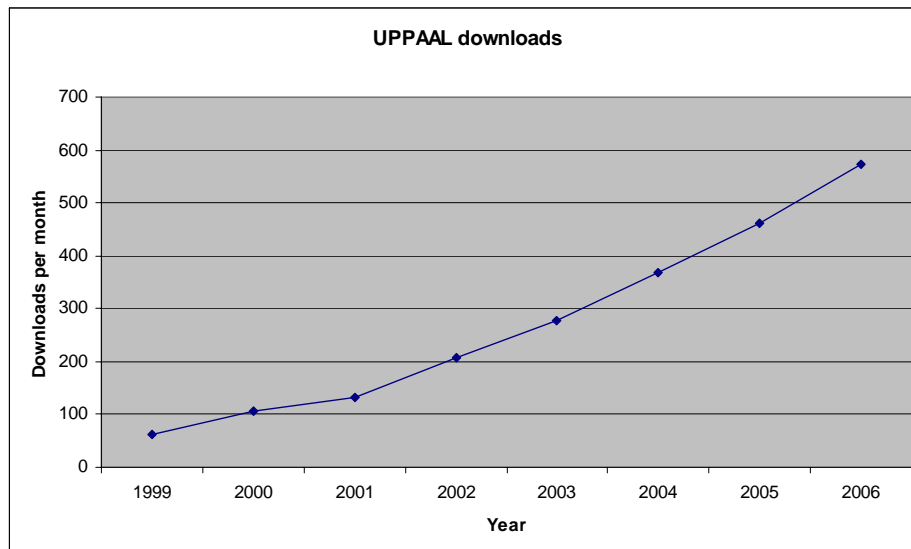
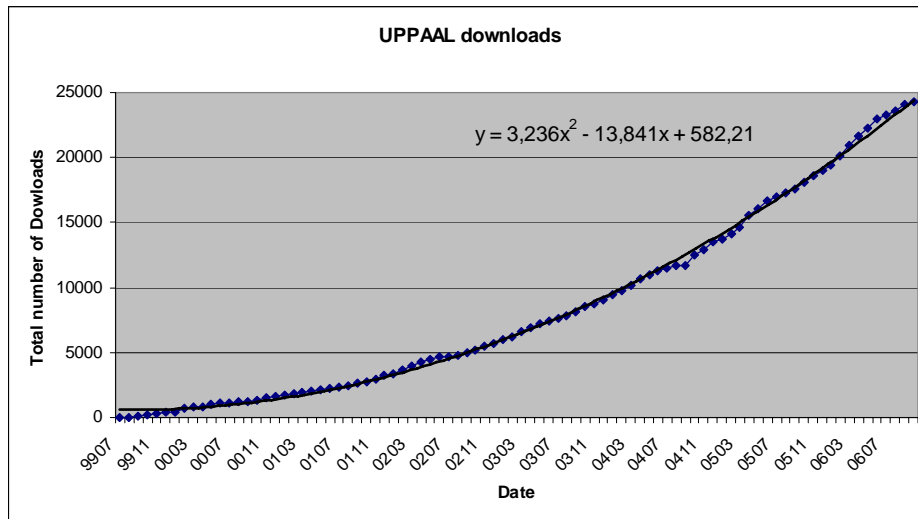


## Verifier

- Exhaustive & automatic checking of requirements
- .. including validating, safety, liveness, bounded liveness and response properties
- .. generation of debugging information for visualisation in simulator.
- **Optimal scheduling for cost models**



# “Impact”

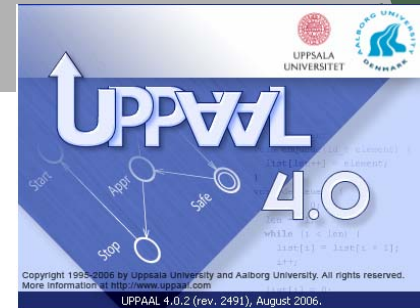


## Google:

|                |         |
|----------------|---------|
| UPPAAL:        | 134.000 |
| SPIN Verifier: | 242.000 |
| nuSMV:         | 57.700  |

> 1.500  
Google Scholar Citations  
(Rhapsody/Esterel < 3.500)

# Impact



## Academic Courses @

DTU, MCI, IT-U (DK)

Chalmers,

Linköping, Lund,

Chalmers,

Mälardalarn (S)

Nijmegen, Twente, CWI (NL)

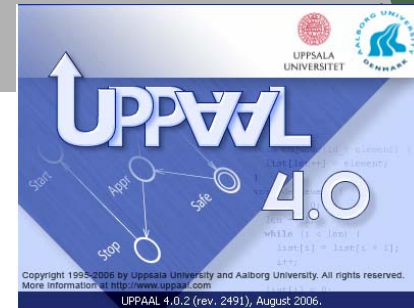
Upenn, Northumbria(US)

Braunschweig,

Oldenburg, Marktoberdorf (D)

Tsinghua, Shanghai, ISS, NUS (Asia)

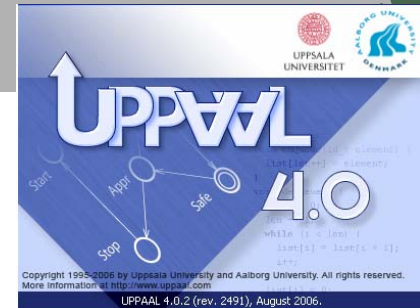
# Impact



## Company Downloads

- Mecel
- Jet
- Symantec
- SRI
- Relogic
- Realwork
- NASA
- Verified Systems
- Microsoft
- ABB
- Airbus
- PSA
- Saab
- Siemens
- Volvo
- Lucent Technologies
- Systematic

# Impact



## Tutorials Given @

Estonian School (01)

IPA Fall Days (01)

FTRTFT (02)

CPN (02)

SFM (02)

MOVEP (02)

DISC School

MOVEP (04)

PRISE (04)

PDMC (05)

ARTIST2 (05)

EMSOFT (05)

RTSS (05)

TECS week (05)

TAROT (06)

ARTS (06)

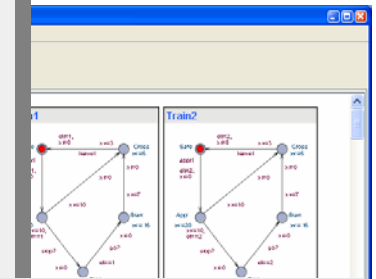
GLOBAN (06)

ARTIST ASIAN SCH (07)

.....

UPPAAL2k: Small Tutorial  
日本語版  
Ver.1.0

|     |                               |   |
|-----|-------------------------------|---|
| 1   | イントロダクション .....               | 2 |
| 2   | UPPAAL .....                  | 2 |
| 3   | UPPAAL を学ぶ .....              | 2 |
| 3.1 | 概要 .....                      | 3 |
| 3.2 | 排他制御アルゴリズム .....              | 4 |
| 3.3 | UPPAAL での時間 .....             | 7 |
| 3.4 | Urgent/Committed ロケーション ..... | 9 |
| 3.5 | 特性の検証 .....                   |   |
| 3.6 | モデリングのトリック .....              |   |



### 3.1 概要

UPPAALのメインウィンドウ(図 1) はメニューとタブから構成されています。

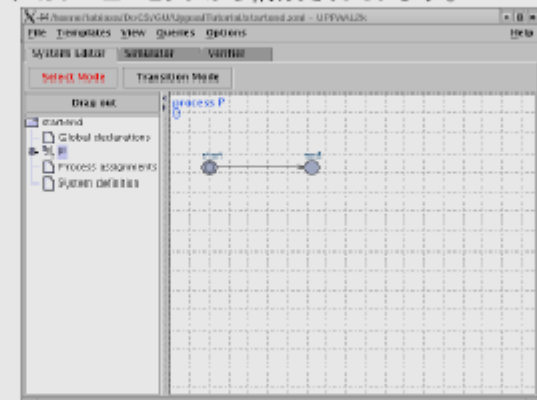
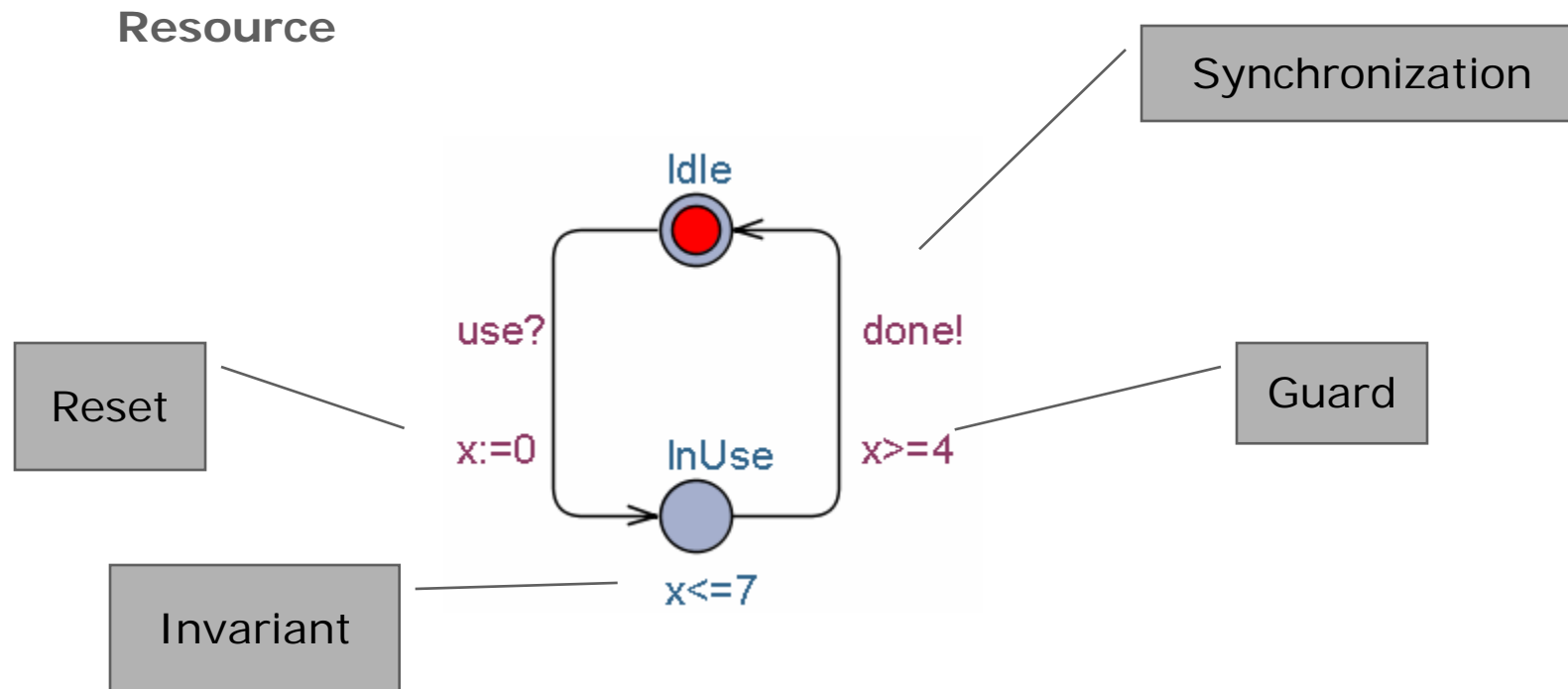


図 1: UPPAAL の画面

# Timed Automata

[Alur & Dill'89]

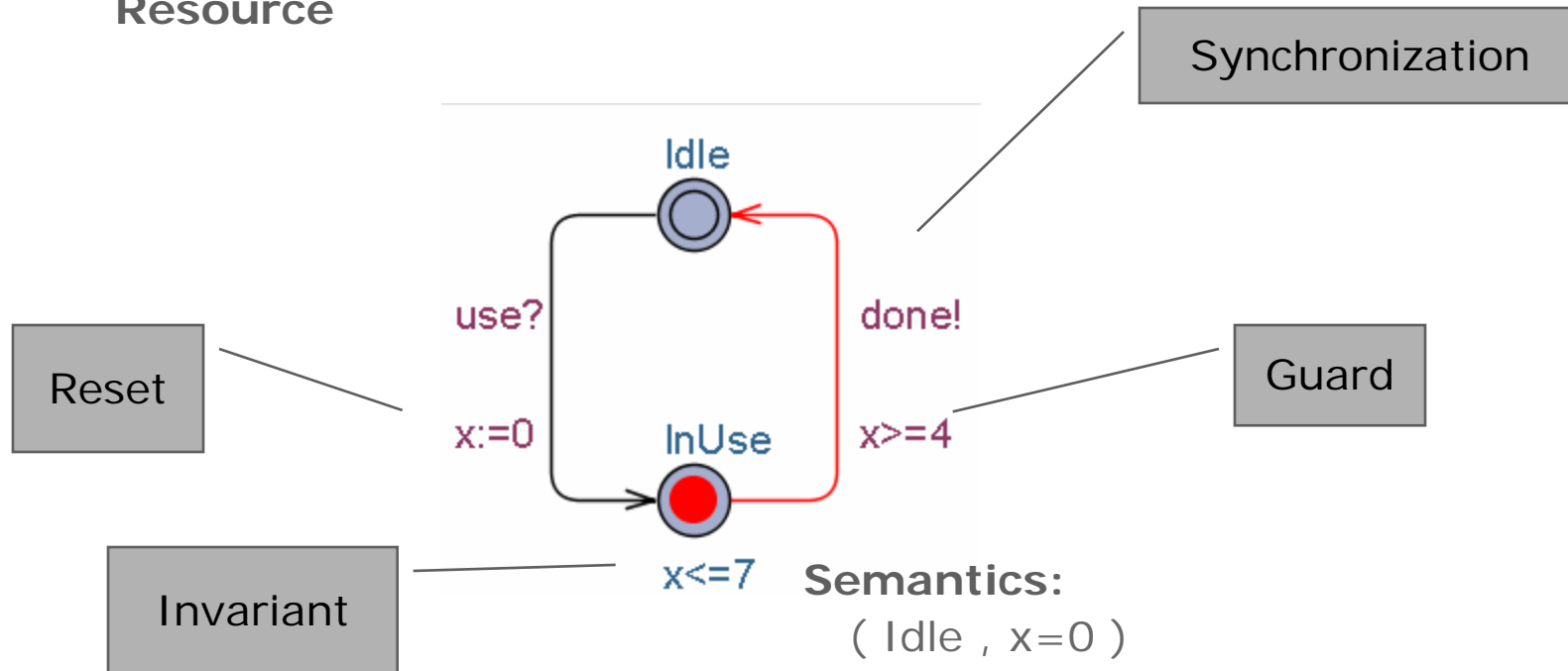


# Timed Automata

[Alur & Dill'89]



Resource



**Semantics:**

( Idle , x=0 )

→ ( Idle , x=2.5 )

d(2.5)

→ ( InUse , x=0 )

use?

→ ( InUse , x=5 )

d(5)

→ ( Idle , x=5 )

done!

→ ( Idle , x=8 )

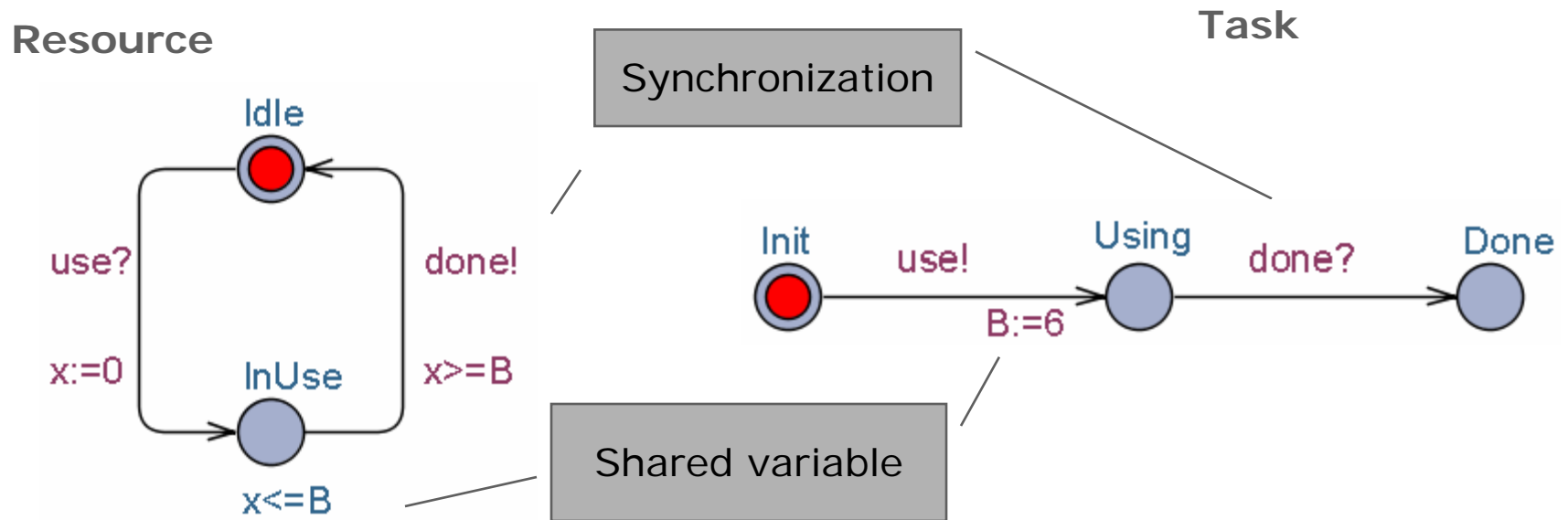
d(3)

→ ( InUse , x=0 )

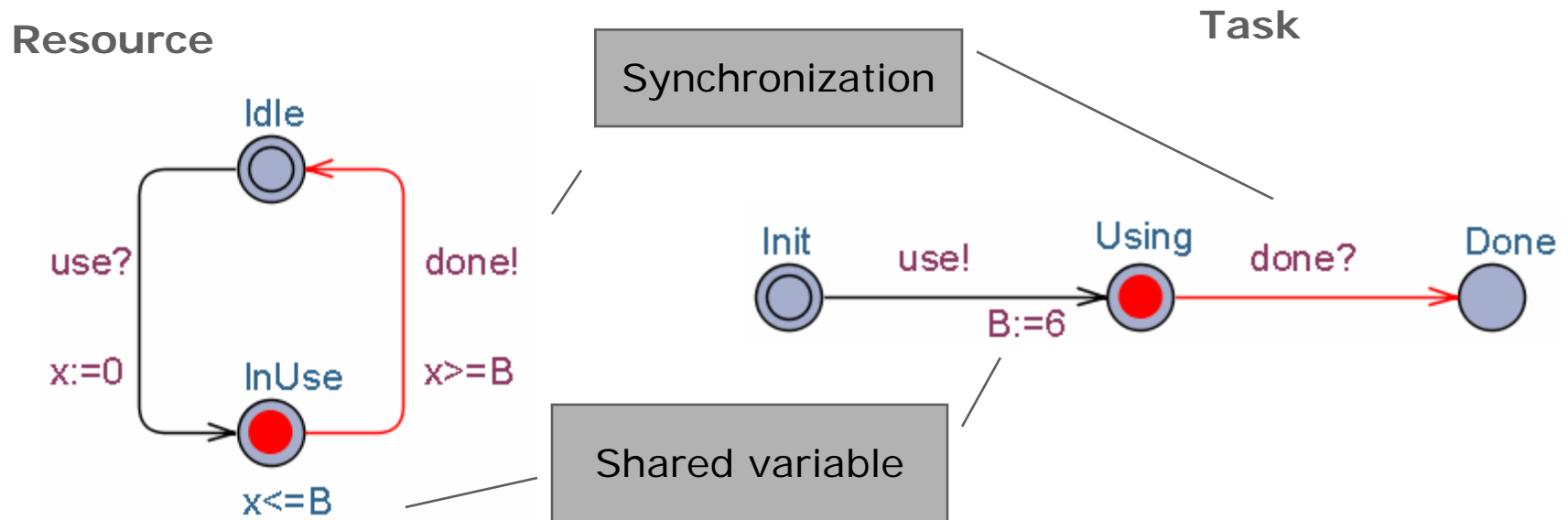
use?



# Composition



# Composition



## Semantics:

- ( Idle , Init , B=0 , x=0 )
- ( Idle , Init , B=0 , x=3.1415 )    d(3.1415)
- ( InUse , Using , B=6 , x=0 )    use
- ( InUse , Using , B=6 , x=6 )    d(6)
- ( Idle , Done , B=6 , x=6 )    done

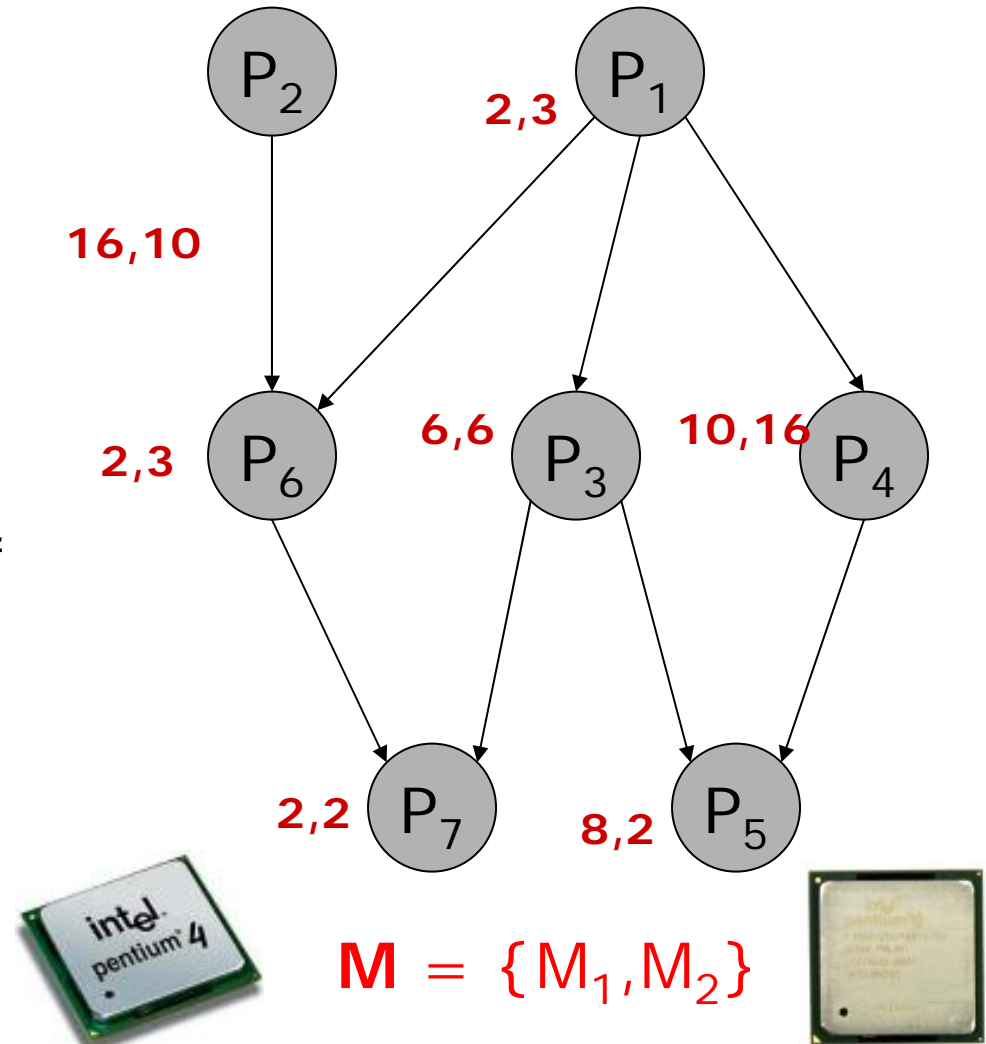


# Task Graph Scheduling

## Optimal Static Task Scheduling



- Task  $\mathbf{P}=\{P_1,\dots,P_m\}$
- Machines  $\mathbf{M}=\{M_1,\dots,M_n\}$
- Duration  $\Delta : (\mathbf{P}\times\mathbf{M}) \rightarrow \mathbf{N}_\infty$
- $< : \text{p.o. on } \mathbf{P} \text{ (pred.)}$
  
- A task can be executed only if all predecessors have completed
- Each machine can process at most one task at a time
- Task cannot be preempted.

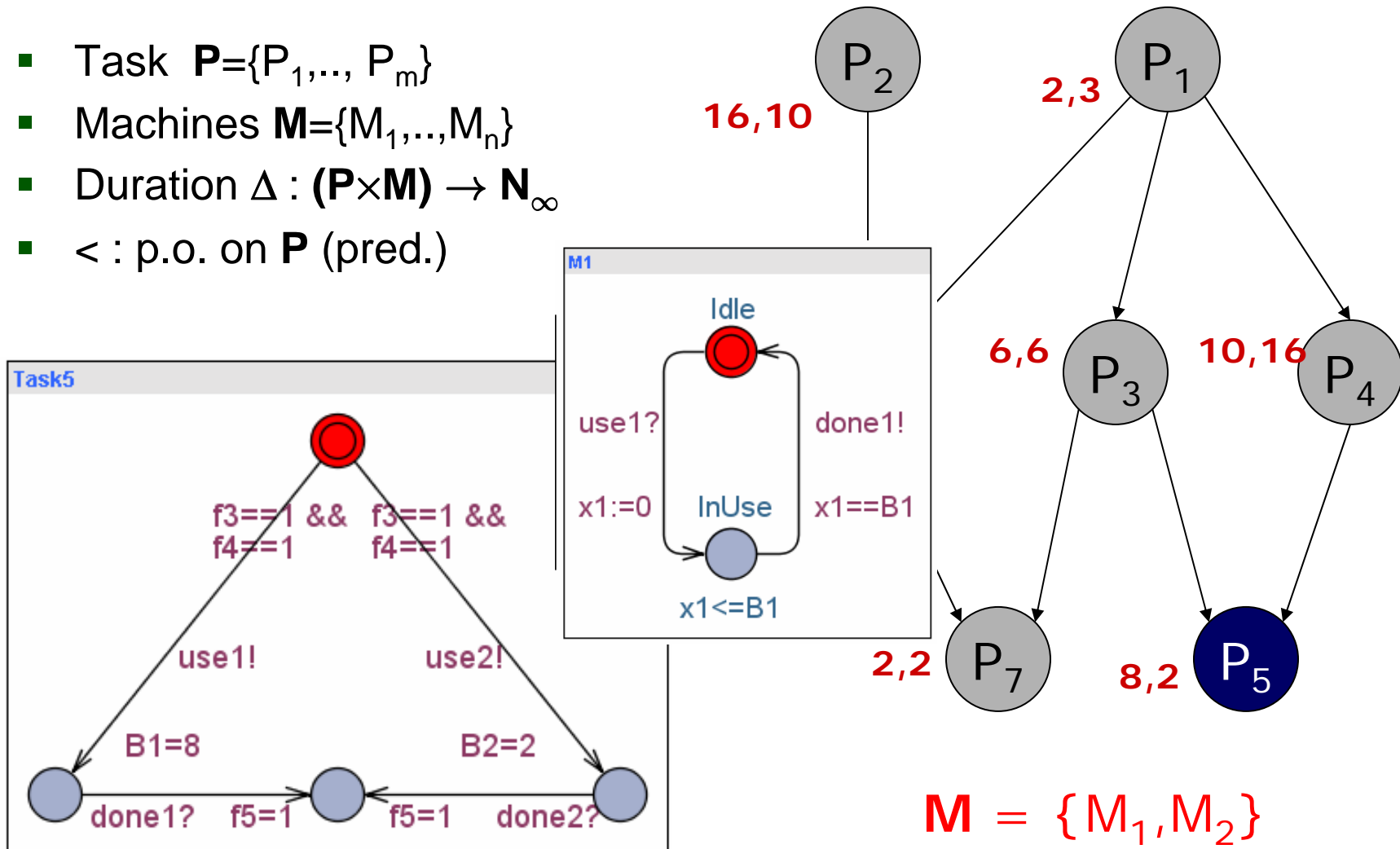


# Task Graph Scheduling

## Optimal Static Task Scheduling



- Task  $\mathbf{P}=\{P_1, \dots, P_m\}$
- Machines  $\mathbf{M}=\{M_1, \dots, M_n\}$
- Duration  $\Delta : (\mathbf{P} \times \mathbf{M}) \rightarrow \mathbf{N}_\infty$
- $<$  : p.o. on  $\mathbf{P}$  (pred.)



# Experimental Results



| name | #tasks | #chains | # machines | optimal | TA   |
|------|--------|---------|------------|---------|------|
| 001  | 437    | 125     | 4          | 1178    | 1182 |
| 000  | 452    | 43      | 20         | 537     | 537  |
| 018  | 730    | 175     | 10         | 700     | 704  |
| 074  | 1007   | 66      | 12         | 891     | 894  |
| 021  | 1145   | 88      | 20         | 605     | 612  |
| 228  | 1187   | 293     | 8          | 1570    | 1574 |
| 071  | 1193   | 124     | 20         | 629     | 634  |
| 271  | 1348   | 127     | 12         | 1163    | 1164 |
| 237  | 1566   | 152     | 12         | 1340    | 1342 |
| 231  | 1664   | 101     | 16         | t.o.    | 1137 |
| 235  | 1782   | 218     | 16         | t.o.    | 1150 |
| 233  | 1980   | 207     | 19         | 1118    | 1121 |
| 294  | 2014   | 141     | 17         | 1257    | 1261 |
| 295  | 2168   | 965     | 18         | 1318    | 1322 |
| 292  | 2333   | 318     | 3          | 8009    | 8009 |
| 298  | 2399   | 303     | 10         | 2471    | 2473 |

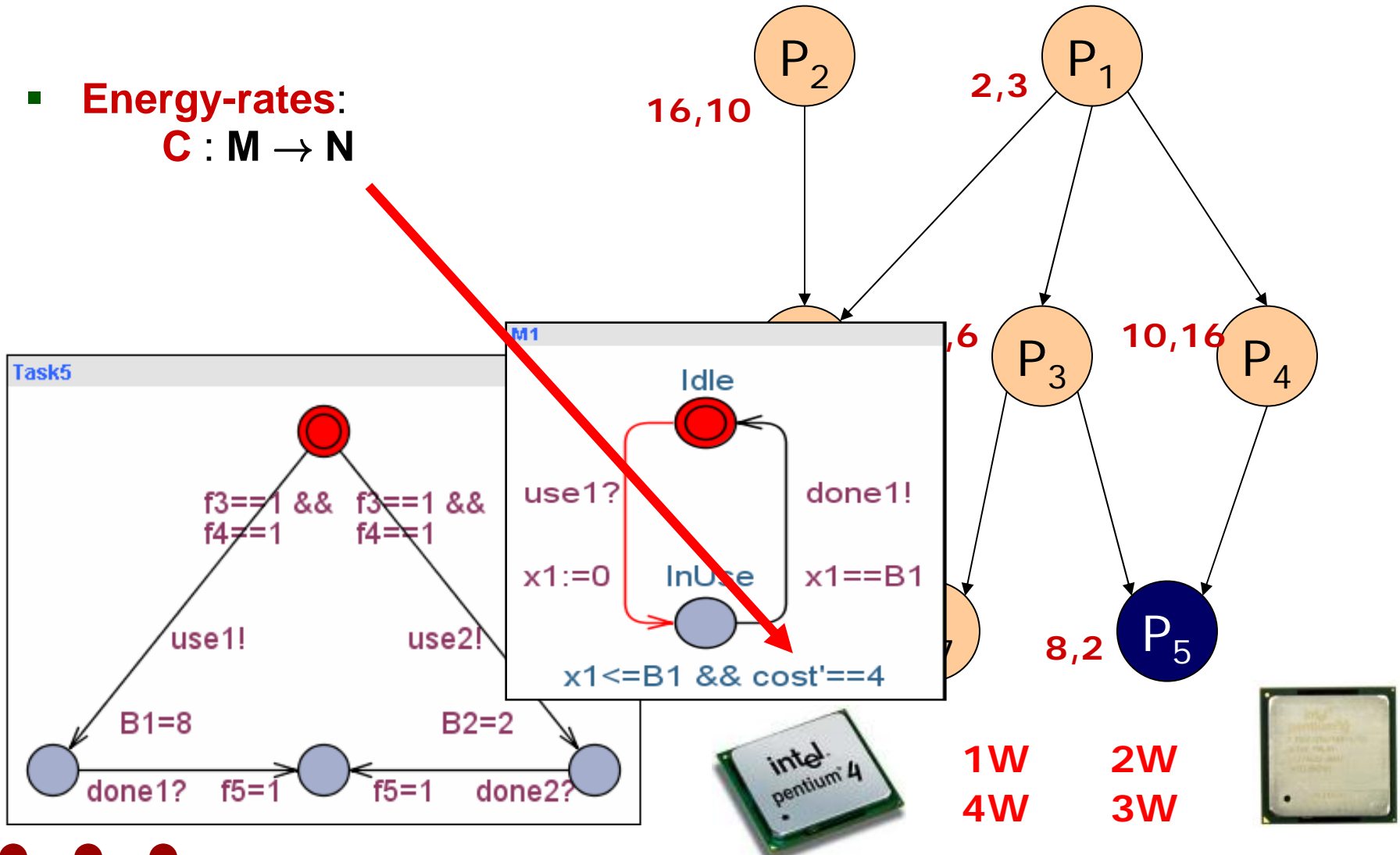
Abdeddaïm, Kerbaa, Maler

# Optimal Task Graph Scheduling

Power-Optimality



- Energy-rates:  
 $C : M \rightarrow N$



# Dynamic Voltage Scaling



DaNES



CENTER FOR INDLJEKREDE SOFTWARE SYSTEMER

# Task Scheduling

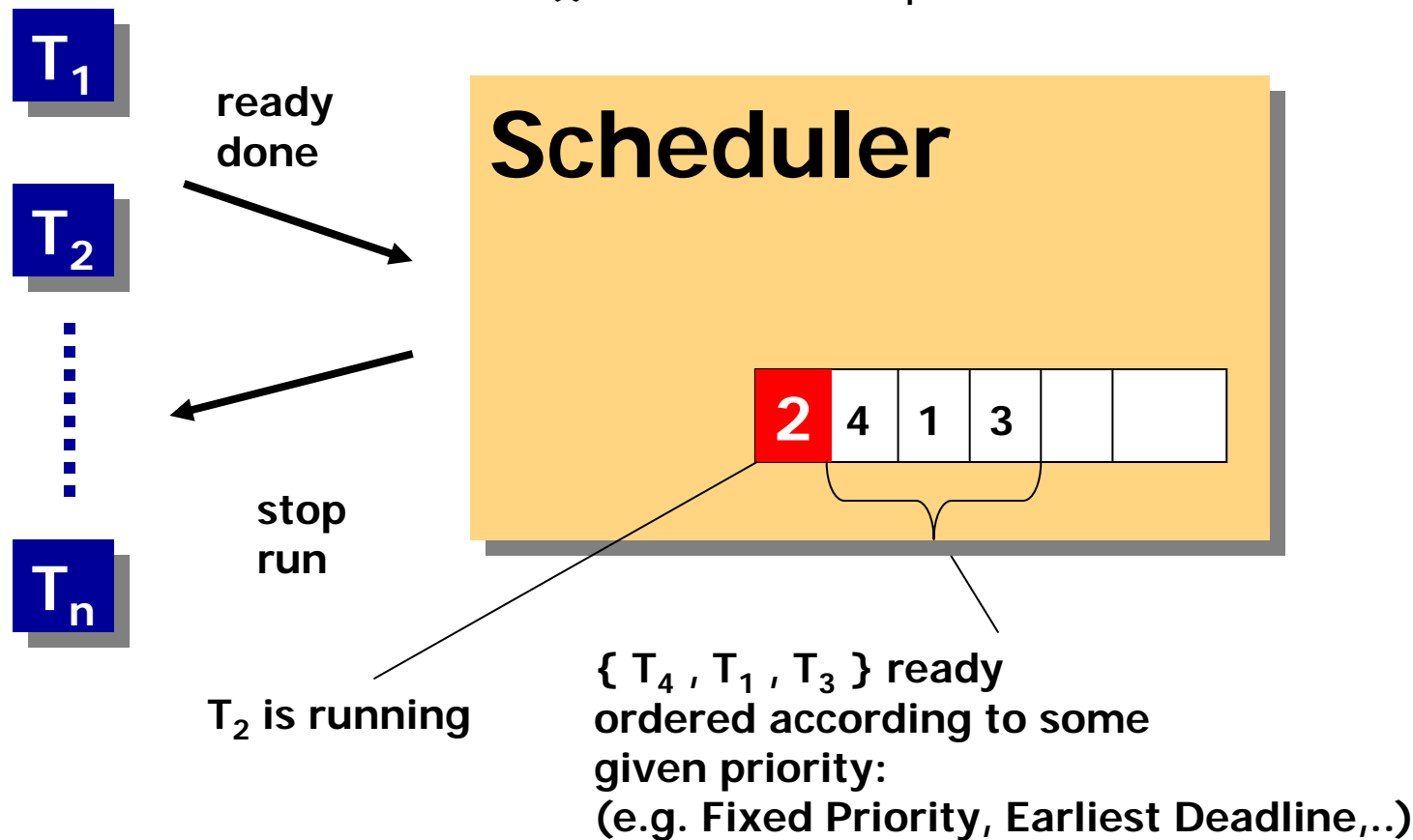
*utilization of CPU*



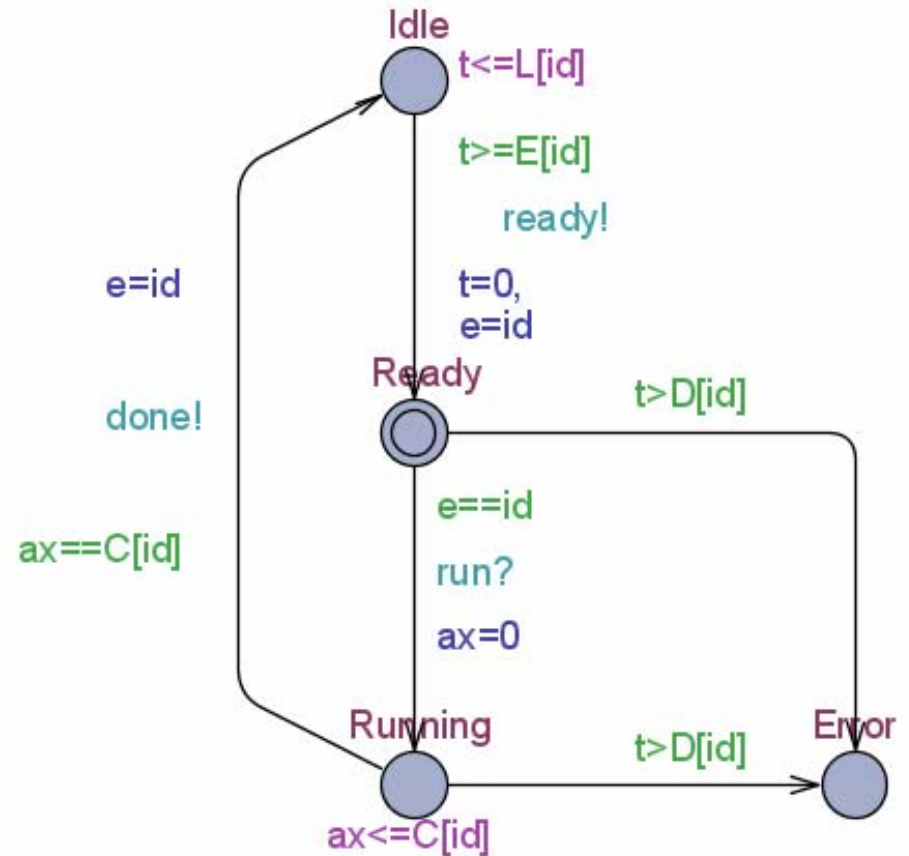
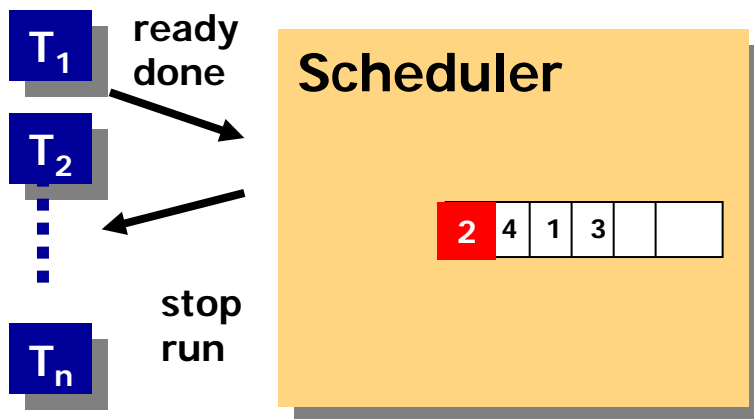
$P(i)$ ,  $[E(i), L(i)]$ , .. : period or  
earliest/latest arrival or .. for  $T_i$

$C(i)$ : execution time for  $T_i$

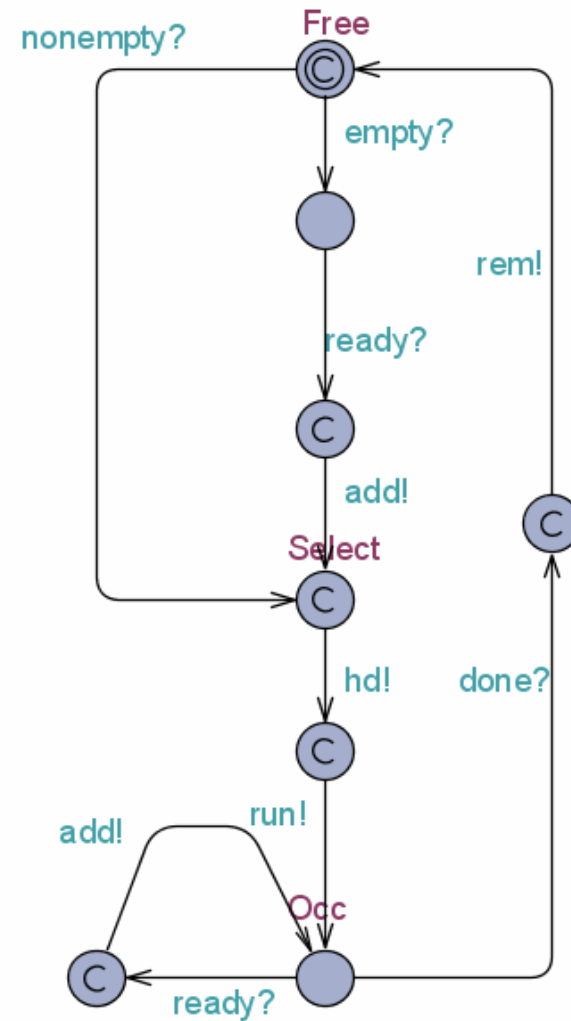
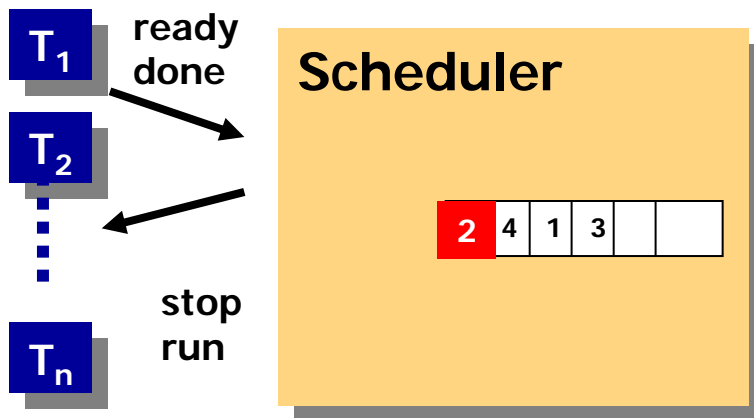
$D(i)$ : deadline for  $T_i$



# Modeling Task



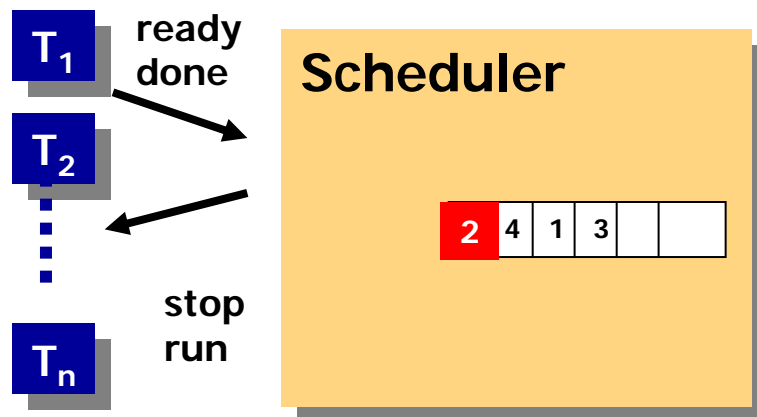
# Modeling Scheduler





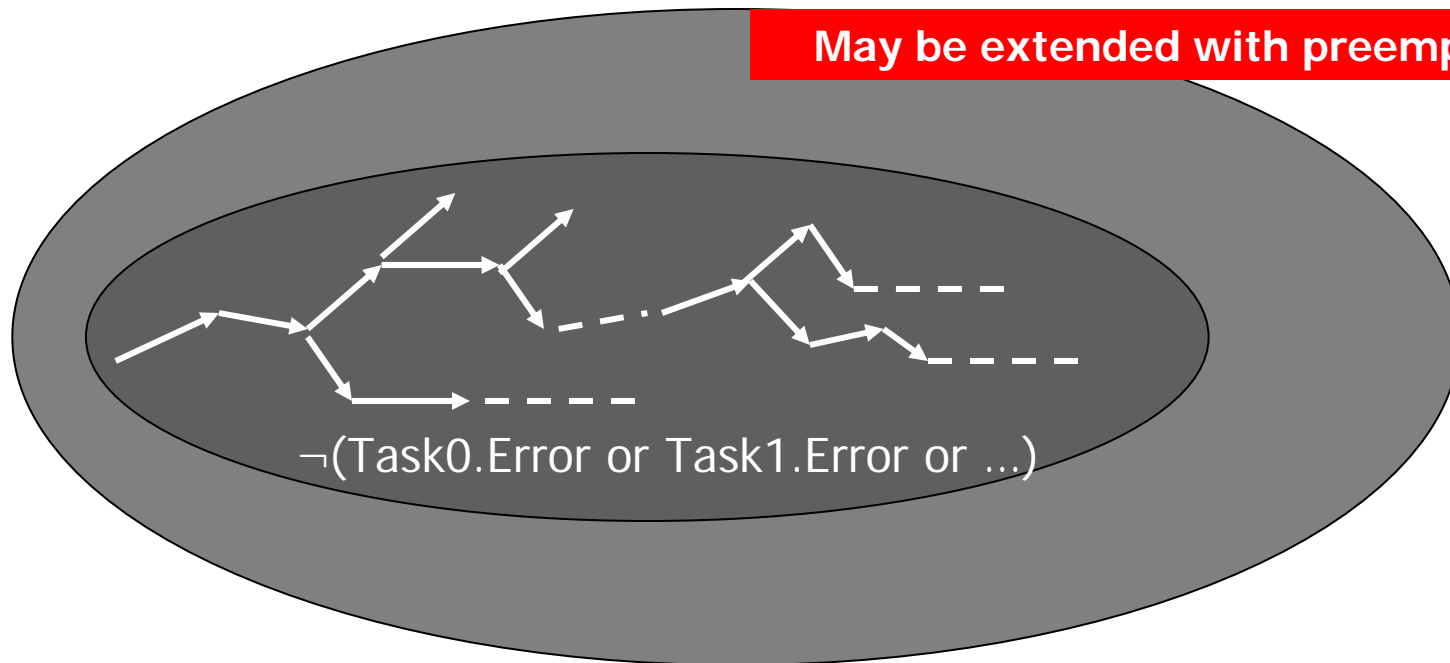
# Modeling Queue

In UPPAAL 4.0  
User Defined Function



```
void add(id_t element)
{
  int i=len;
  int temp=0;
  if(len==0)
  {
    list[len]=e;
    len=1;
  }
  else
  {
    list[len]=e;
    i=len;
    len=len+1;
    while (i>1 && P[list[i]]> P[list[i-1]])
    {
      temp=list[i-1];
      list[i-1]=list[i];
      list[i]=temp;
      i=i-1;
    }
  }
}
```

# Schedulability = Safety Property



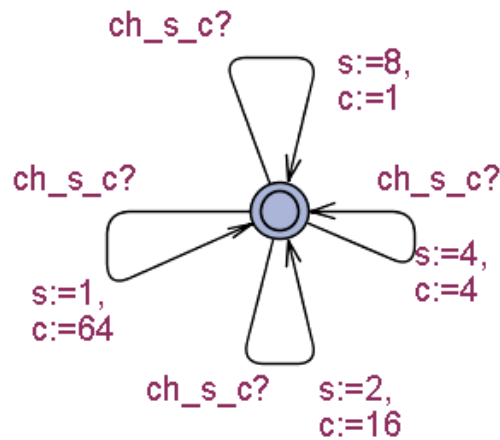
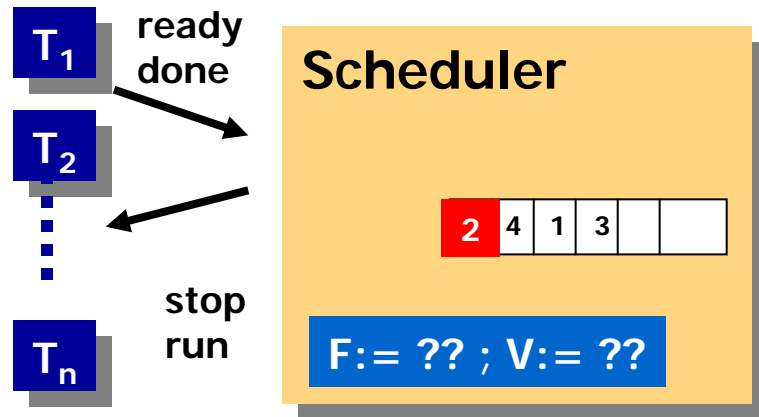
$A \square \neg(\text{Task0.Error or Task1.Error or ...})$



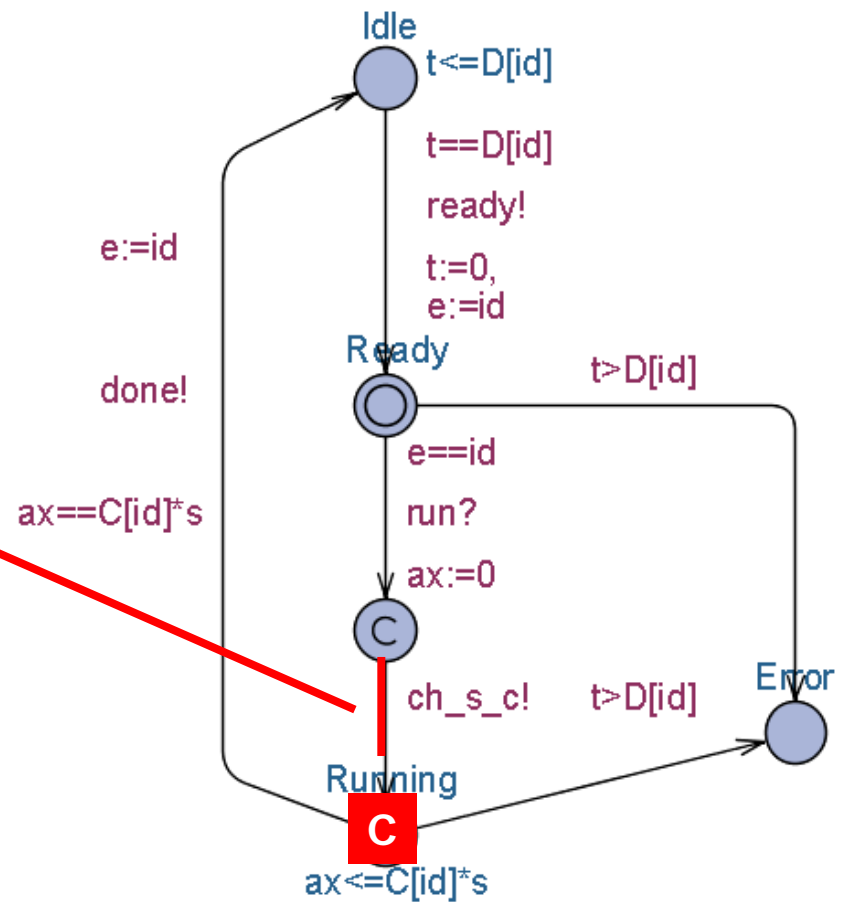
# Energy Optimal Scheduling



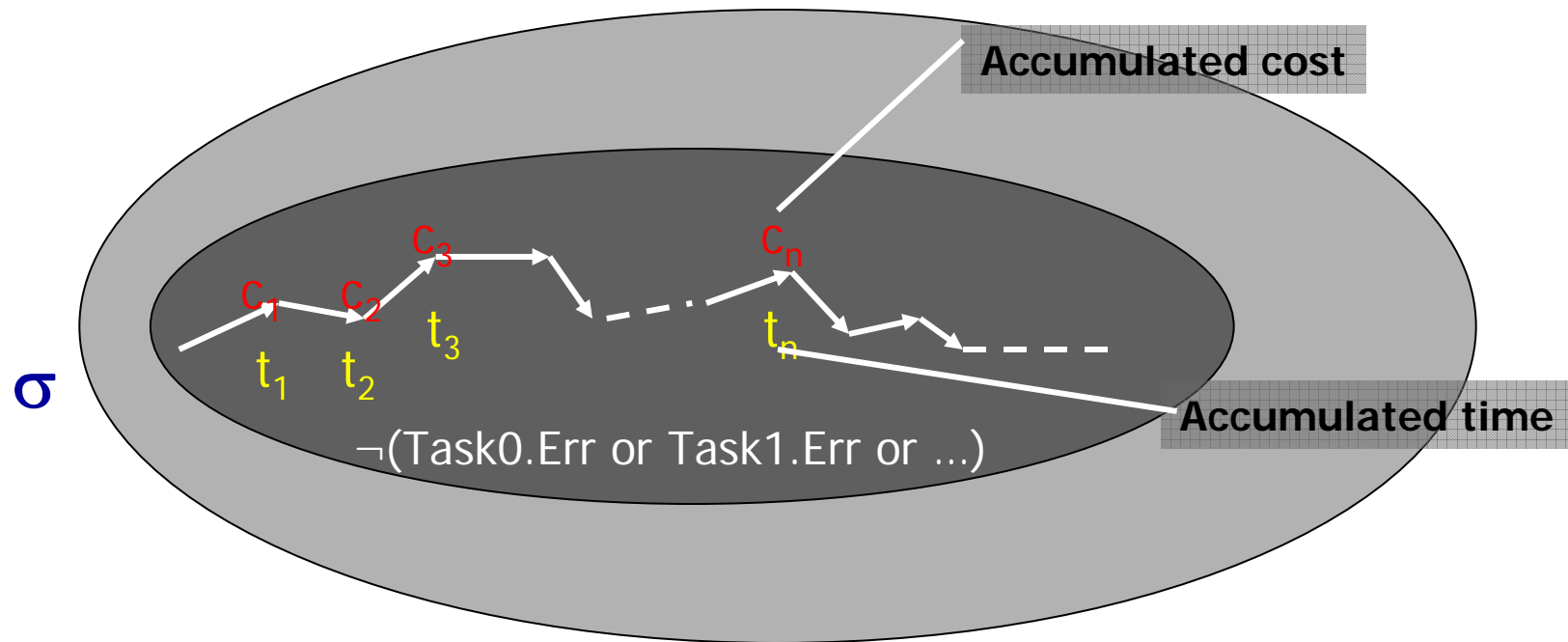
Using Priced Timed Automata



"Choose" Scaling/Cost (Freq/Voltage)



# Cost **Optimal** Scheduling = *Optimal Infinite Path*

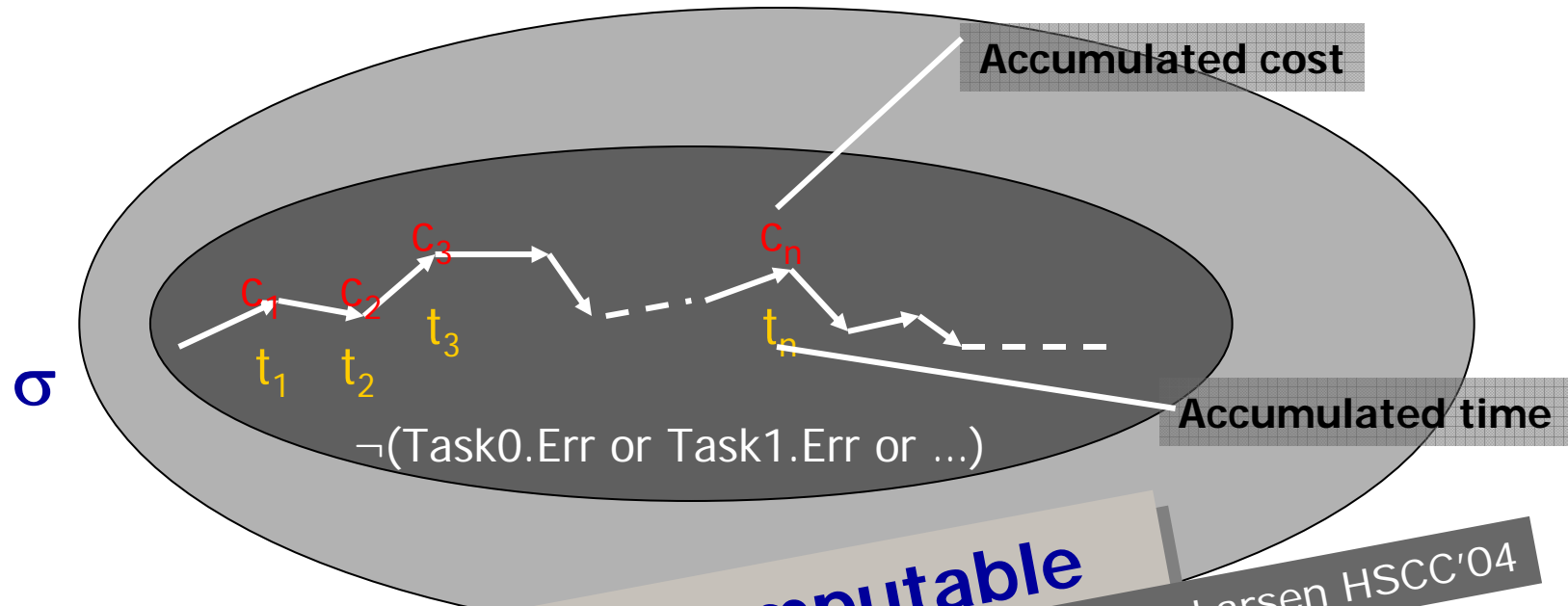


Value of path  $\sigma$ :  $\text{val}(\sigma) = \lim_{n \rightarrow \infty} C_n / t_n$

Optimal Schedule  $\sigma^*$ :  $\text{val}(\sigma^*) = \inf_{\sigma} \text{val}(\sigma)$



# Cost Optimal Scheduling = Optimal Infinite Path



**THEOREM:  $\sigma^*$  is computable**

Bouyer, Brinksma, Larsen HSCC'04

For path  $\sigma$ :  $\text{val}(\sigma) = \lim_{n \rightarrow \infty} c_n / t_n$

Optimal Schedule  $\sigma^*$ :  $\text{val}(\sigma^*) = \inf_{\sigma} \text{val}(\sigma)$



# Contact: [www.uppaal.com](http://www.uppaal.com)



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## UPPAAL

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UPPAAL is an integrated tool environment for modeling, validation and verification of real-time systems modeled as networks of timed automata, extended with data types (bounded integers, arrays, etc.).

The tool is developed in collaboration between the [Department of Information Technology](#) at Uppsala University, Sweden and the [Department of Computer Science](#) at Aalborg University in Denmark.

### Download

**News:** We are proud to officially release UPPAAL 4.0.2 (Aug 7, 2006), available from the [Download](#) page. The 4.0 release is the result of over 2.5 years of development, and many new features and improvements are introduced (see also this [release note](#) and the web help section [new features](#)). To support models created in previous versions of UPPAAL, version 4.0 can convert most old models directly from the GUI (alternatively it can be run in 3.4 compatibility mode by defining the environment variable UPPAAL\_OLD\_SYNTAX, see also item 2 of the [FAQ](#)).

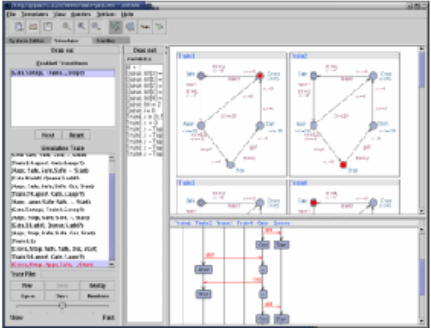


Figure 1: UPPAAL on screen.


### License

The UPPAAL tool is **free** for non-profit applications. For information about commercial licenses, please email [sales\(at\)uppaal\(dot\)com](mailto:sales(at)uppaal(dot)com).


To find out more about UPPAAL, read this short [introduction](#). Further information may be found at this web site in the pages [About](#), [Documentation](#), [Download](#), and [Examples](#).

### Mailing Lists

UPPAAL has an open [discussion forum](#) group at Yahoo!Groups intended for users of the tool. To join or post to the forum, please refer to the information at the [discussion forum](#) page. Bugs should be reported using the [bug tracking system](#). To email the development team directly, please use [uppaal\(at\)list\(dot\)it\(dot\)uu\(dot\)se](mailto:uppaal(at)list(dot)it(dot)uu(dot)se).



UPPSALA  
UNIVERSITET



AALBORG UNIVERSITY

# Formalizing the ARTS MPSoC Model in UPPAAL

Jan Madsen and Michael R. Hansen

Embedded Systems Engineering Group

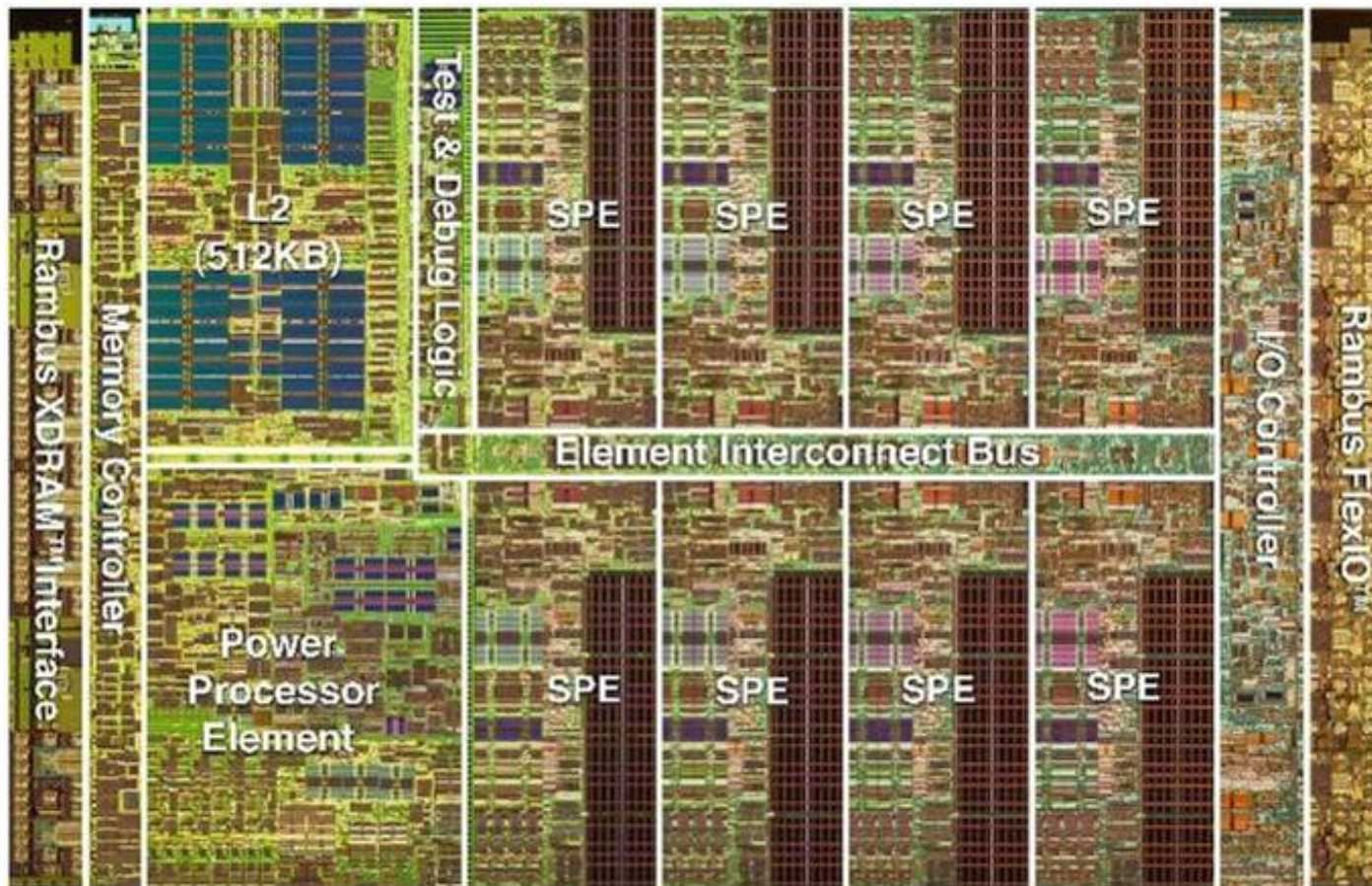
Informatics and Mathematical Modeling  
Technical University of Denmark



# Motivation

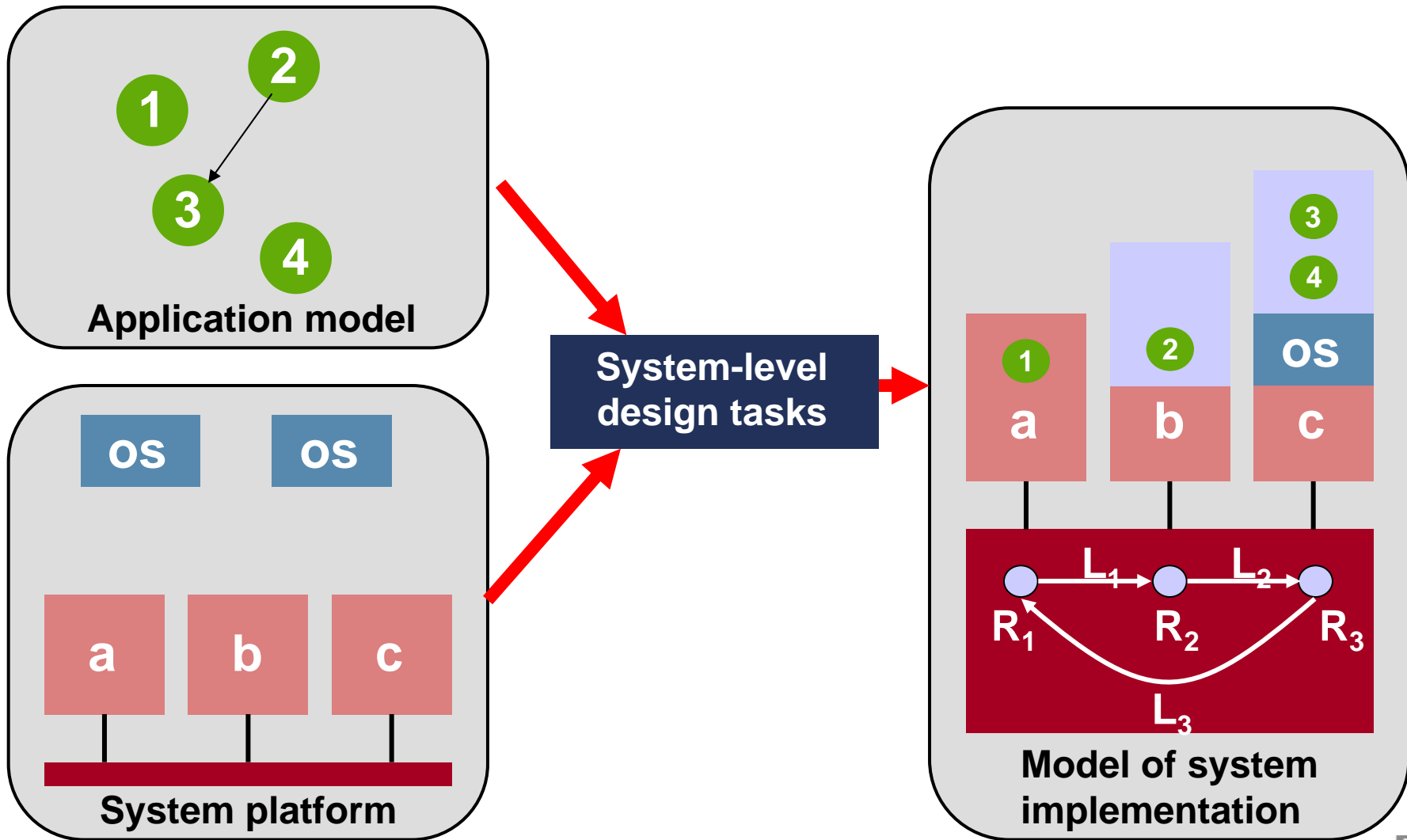


## CELL processor





# Motivation

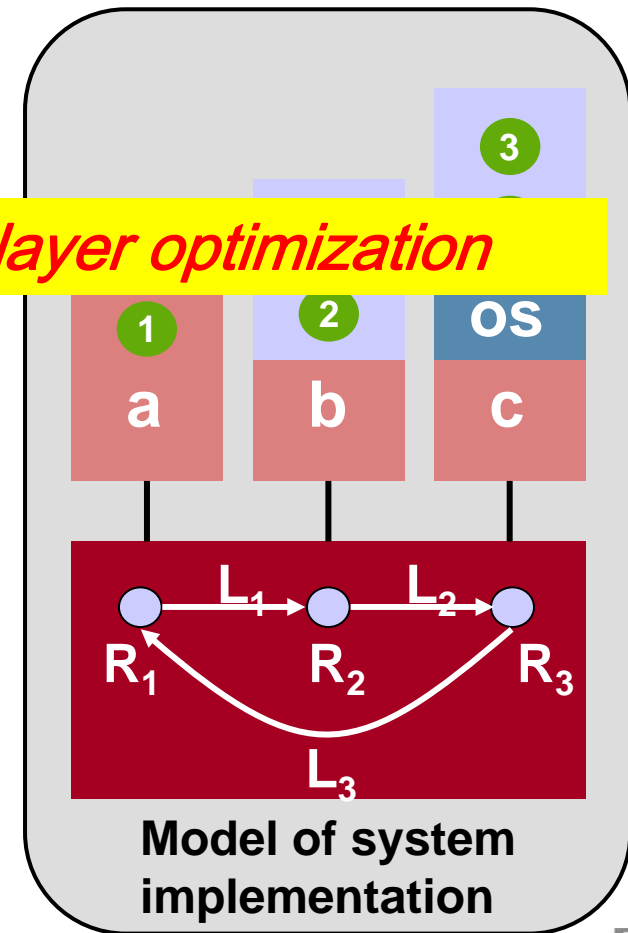


# ARTS objectives

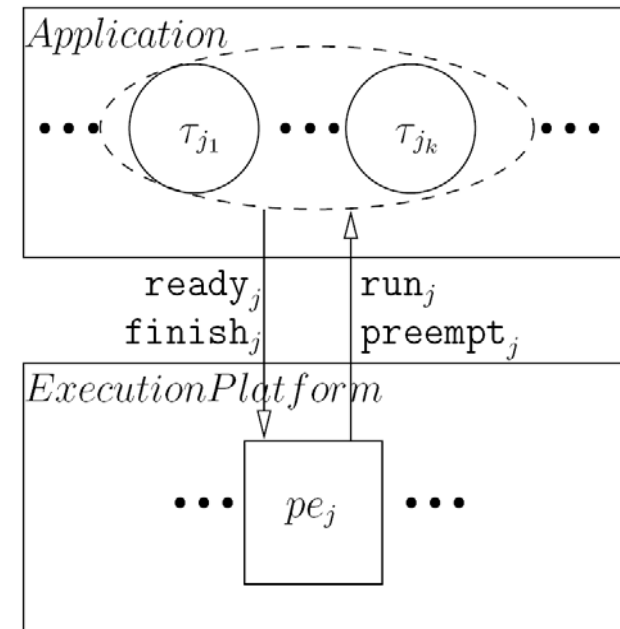
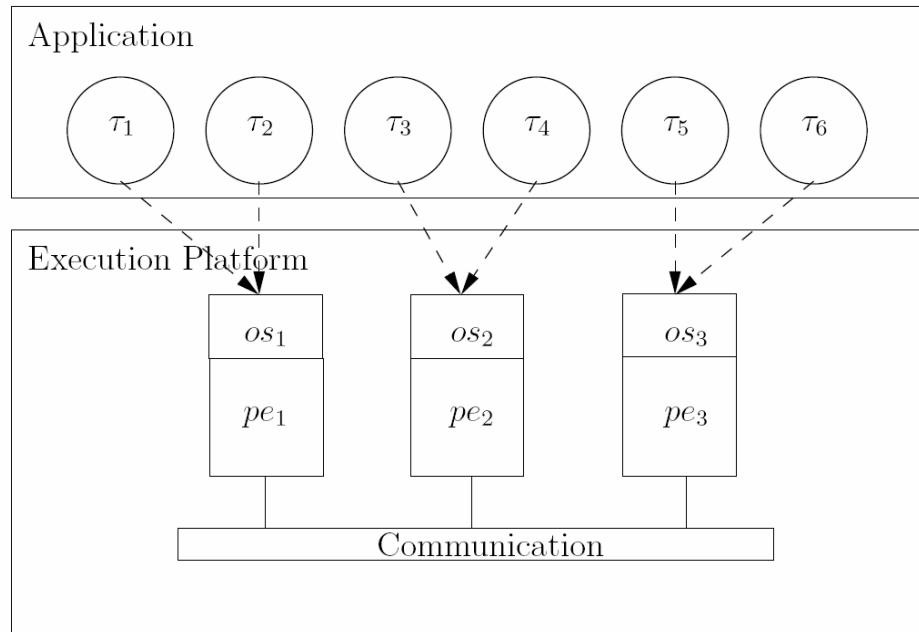


- System-level modeling framework
- Bridging,
  - Application
  - RTOS
  - Execution platform
    - Processing elements
    - NoC
- Supporting
  - System-level analysis
  - Early design space exploration

*Cross-layer optimization*



# Formalizing ARTS



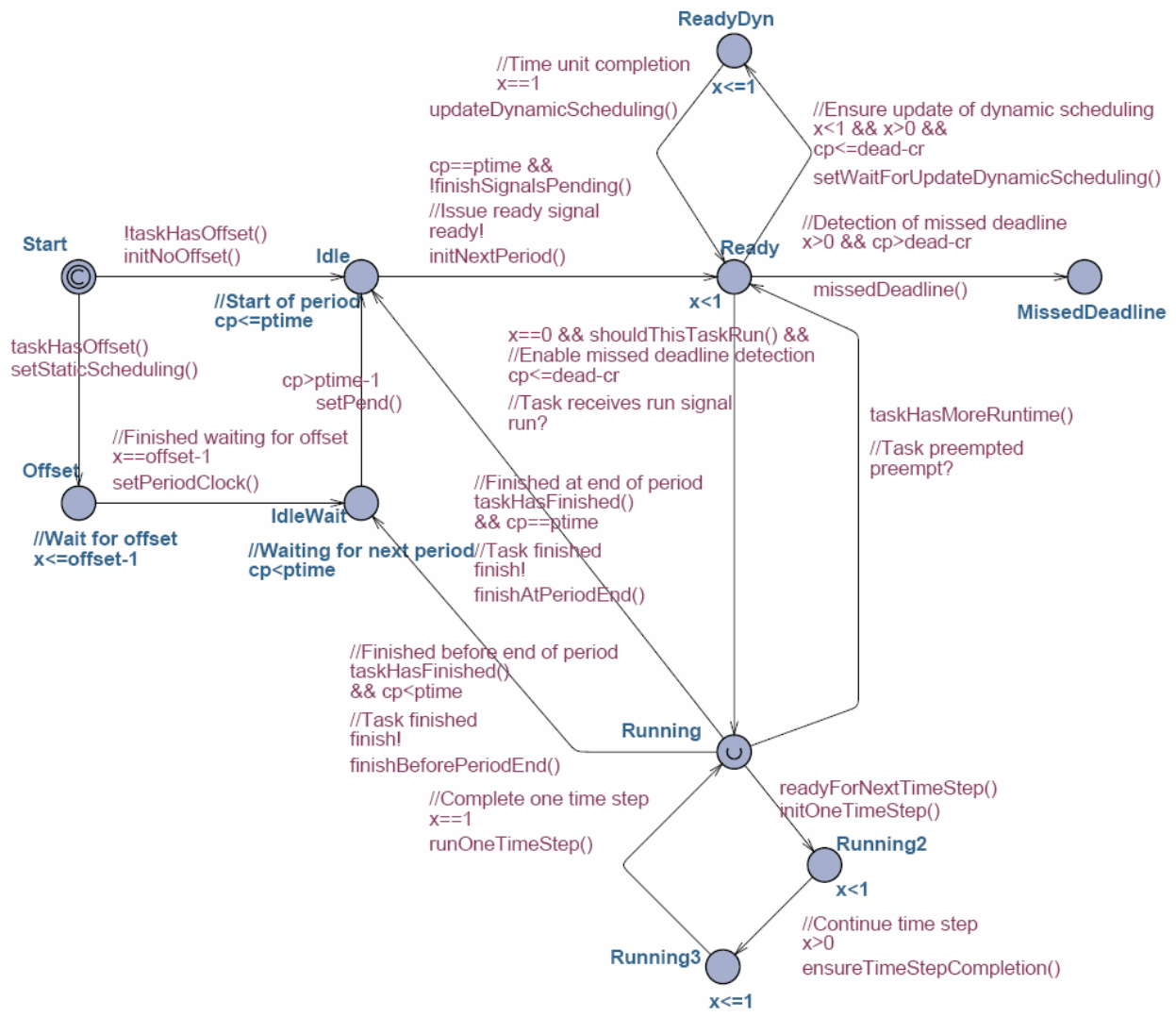
$$System = Application \parallel ExecutionPlatform$$

$$Application = \parallel_{i=1}^n \tau_i$$

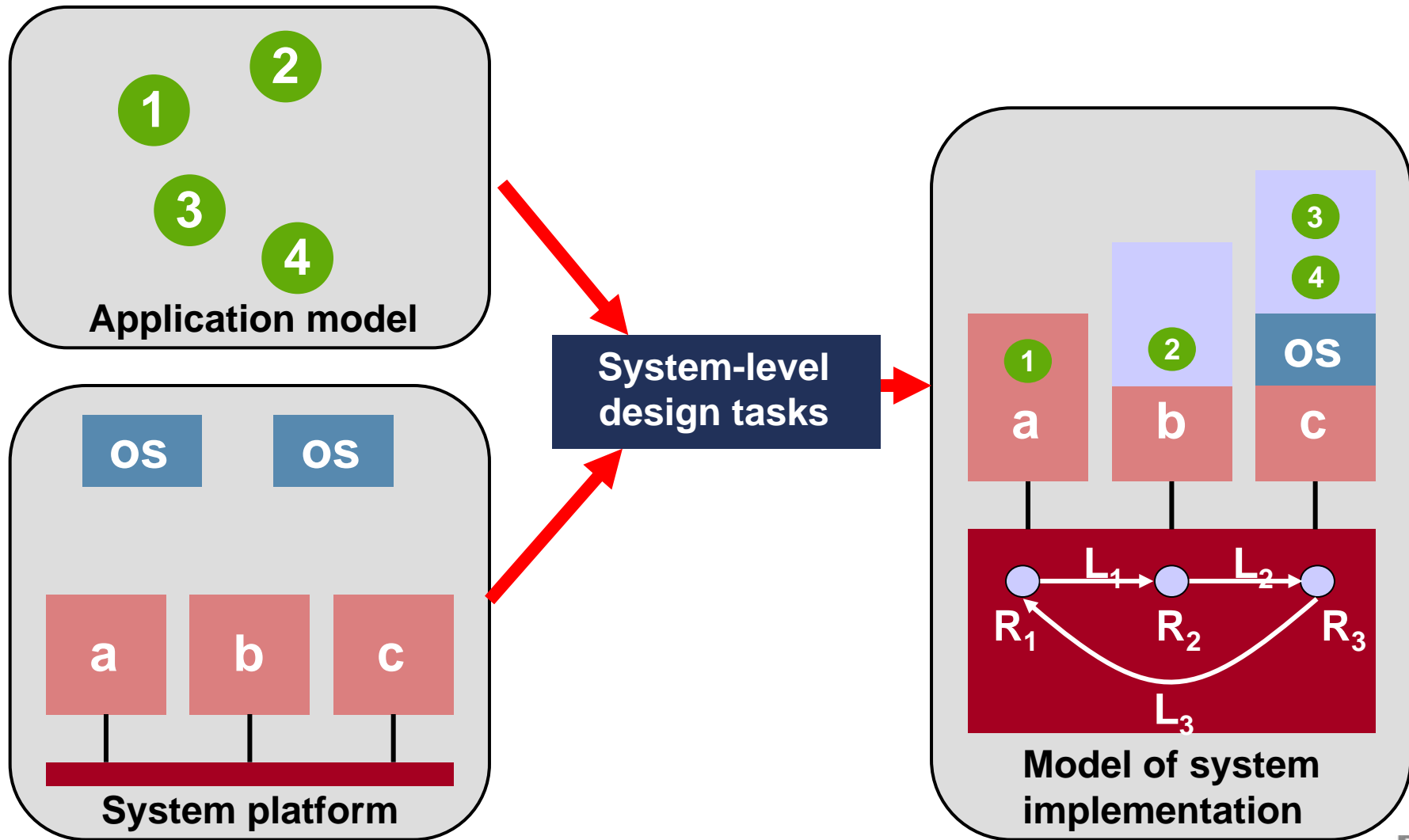
$$ExecutionPlatform = \parallel_{j=1}^m pe_j$$



# Timed Automata for a task



# MOVES: Hiding UPPAAL!



# MOVES



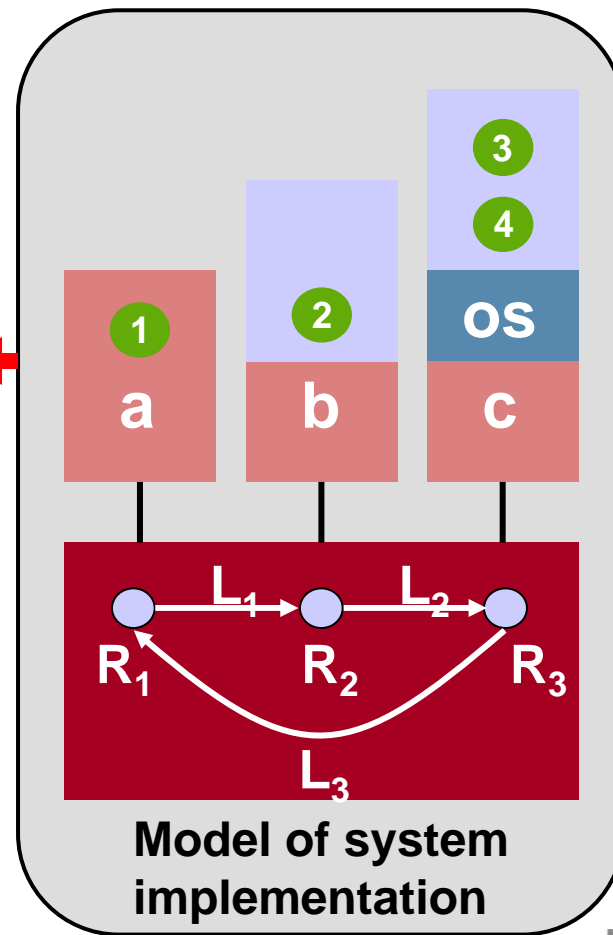
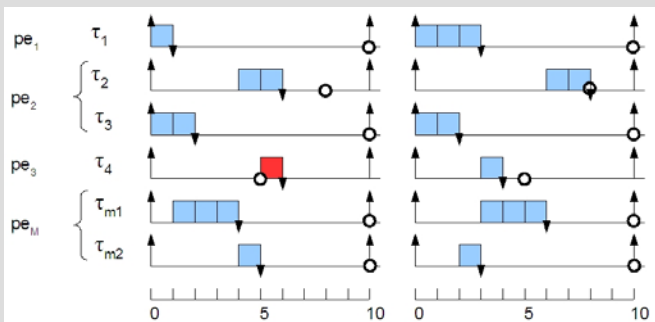
$E \langle \rangle \text{missedDeadline}$

$E \langle \rangle \text{totalCostUsed (Memory)} \geq 23$

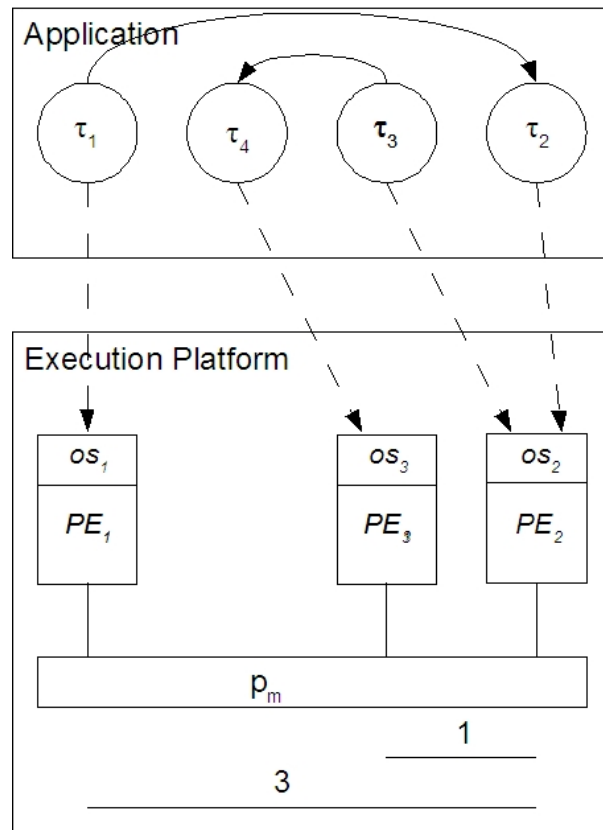
$E \langle \rangle \text{totalCostUsed (Energy)} \geq 15$

**Required specification**

**Model checking**



# Example: MPSoC specification



| Task     | $\pi$ | $\delta$ | $\omega$ |
|----------|-------|----------|----------|
| $\tau_1$ | 10    | 10       | 0        |
| $\tau_2$ | 10    | 8        | 0        |
| $\tau_3$ | 10    | 10       | 0        |
| $\tau_4$ | 10    | 5        | 0        |

PE<sub>i</sub> f = 1 MHz, os = RM

| Task     | bcet | wcet | sm | dm | pw |
|----------|------|------|----|----|----|
| $\tau_1$ | 1    | 3    | 1  | 3  | 5  |
| $\tau_2$ | 2    | 2    | 1  | 7  | 5  |
| $\tau_3$ | 2    | 2    | 1  | 6  | 10 |
| $\tau_4$ | 1    | 1    | 2  | 9  | 10 |

$\pi$  : period [s]  
 $\delta$  : deadline [s]  
 $\omega$  : offset [s]  
 bcet : best case execution time [cycles]  
 wcet : worst case execution time [cycles]  
 sm : static memory [Byte]  
 dm : dynamic memory [Byte]  
 pw : power [mW]  
 f : frequency [Hz]  
 os: operating system[ $\{FP, RM, DM, EDF\}$ ]



# Specifying the application



```
Task t1 = new Task(1, 3, 10, 10, 0, 1);
Task t2 = new Task(2, 2, 8, 10, 0, 2);
Task t3 = new Task(2, 2, 10, 10, 0, 3);
Task t4 = new Task(1, 1, 5, 10, 0, 4);
```

| Task     | $\pi$ | $\delta$ | $o$ |
|----------|-------|----------|-----|
| $\tau_1$ | 10    | 10       | 0   |
| $\tau_2$ | 10    | 8        | 0   |
| $\tau_3$ | 10    | 10       | 0   |
| $\tau_4$ | 10    | 5        | 0   |

PE<sub>i</sub>, f = 1 MHz, os = RM

| Task     | <i>bcet</i> | <i>wcet</i> | <i>sm</i> | <i>dm</i> | <i>pw</i> |
|----------|-------------|-------------|-----------|-----------|-----------|
| $\tau_1$ | 1           | 3           | 1         | 3         | 5         |
| $\tau_2$ | 2           | 2           | 1         | 7         | 5         |
| $\tau_3$ | 2           | 2           | 1         | 6         | 10        |
| $\tau_4$ | 1           | 1           | 2         | 9         | 10        |



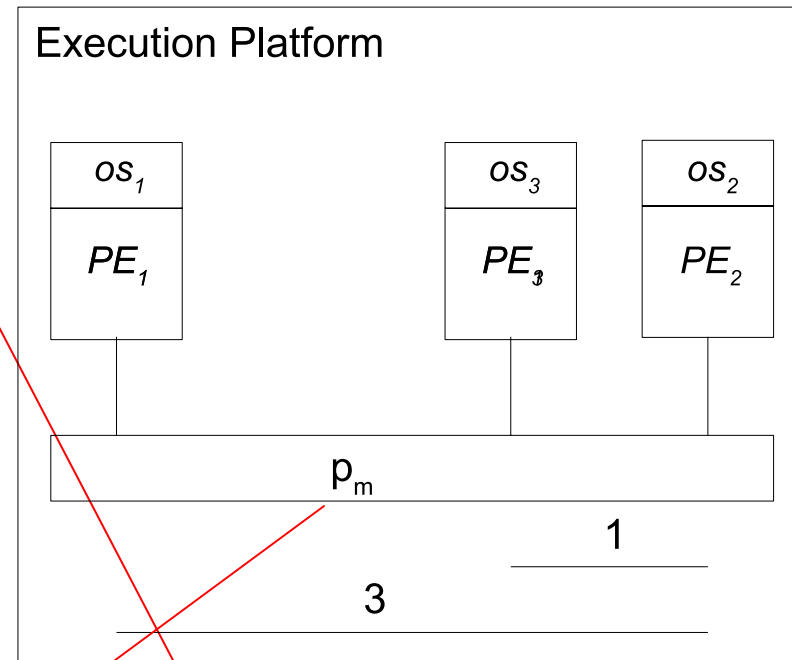


# Execution platform



$PE_1, f = 1 \text{ MHz}, os = RM$

| Task     | <i>bcet</i> | <i>wcet</i> | <i>sm</i> | <i>dm</i> | <i>pw</i> |
|----------|-------------|-------------|-----------|-----------|-----------|
| $\tau_1$ | 1           | 3           | 1         | 3         | 5         |
| $\tau_2$ | 2           | 2           | 1         | 7         | 5         |
| $\tau_3$ | 2           | 2           | 1         | 6         | 10        |
| $\tau_4$ | 1           | 1           | 2         | 9         | 10        |



```

Processor p1 = new Processor(1, Processor.RM);
Processor p2 = new Processor(1, Processor.RM);
Processor p3 = new Processor(1, Processor.RM);
Processor pm = new Processor(1, Processor.RM);
Resource r1 = new Resource();
    
```



# Mapping application onto platform



```
Task[][] tasks =  
    {{t1},{t2,t3},{t4},{tm1,tm2}};
```

```
Task tm1 = new Task(3, 3, 10, 5);
```

```
Task tm2 = new Task(1, 1, 10, 6);
```

```
apps.useResource(tm1,r1);
```

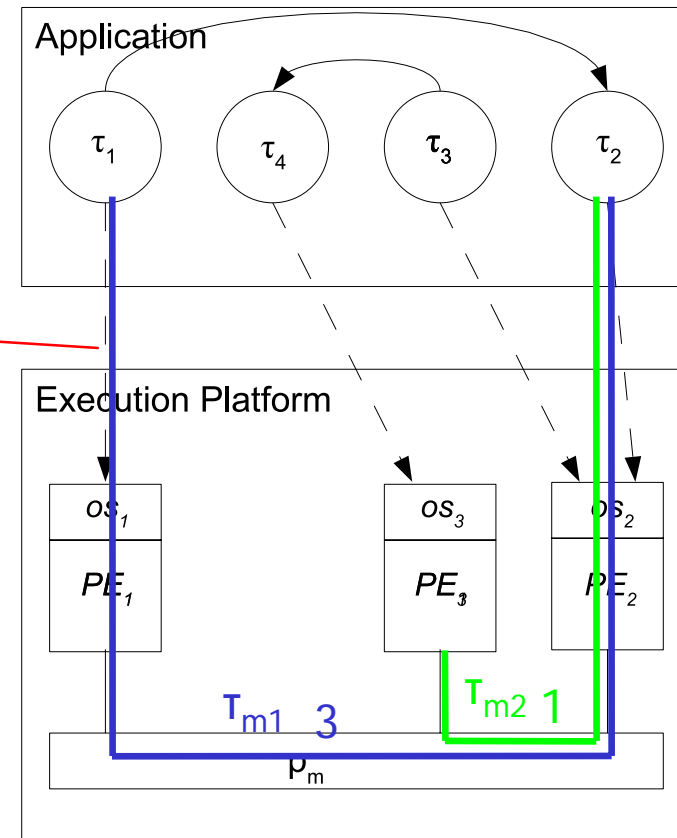
```
apps.useResource(tm2,r1);
```

```
apps.addDep(t1,tm1);
```

```
apps.addDep(tm1,t2);
```

```
apps.addDep(t3,tm2);
```

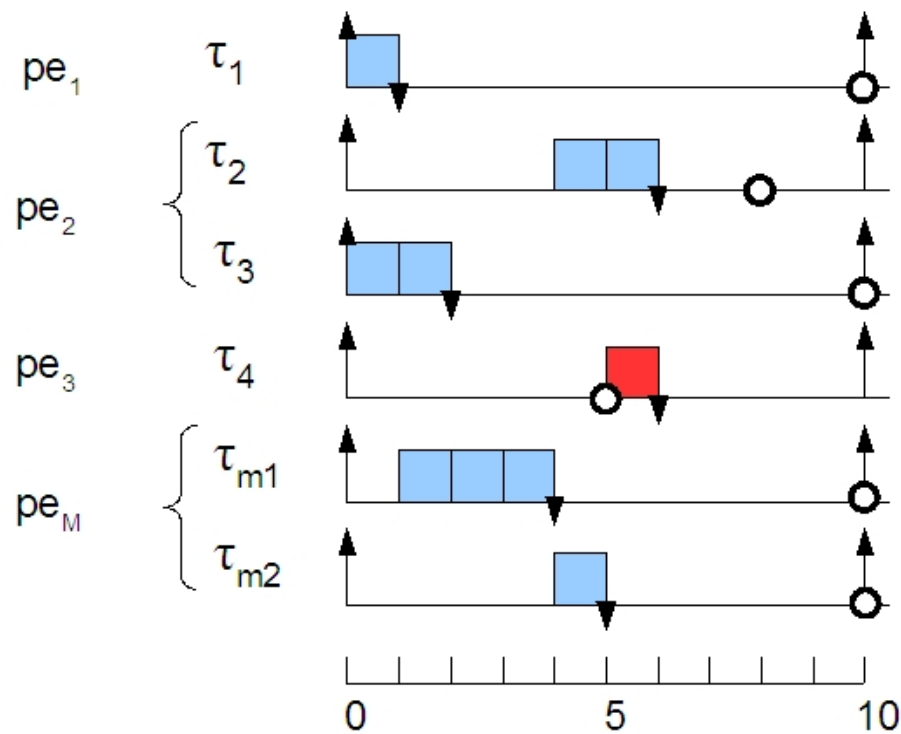
```
apps.addDep(tm2,t4);
```



# Traces



$$e(\tau_1) = [1:3]$$



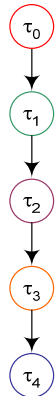
# Handling realistic applications?



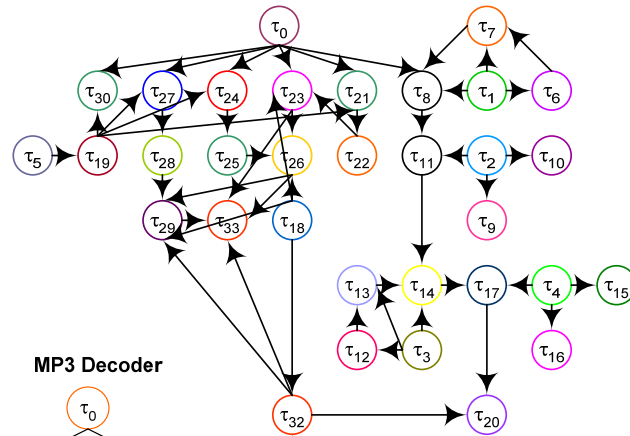
## Smart phone:



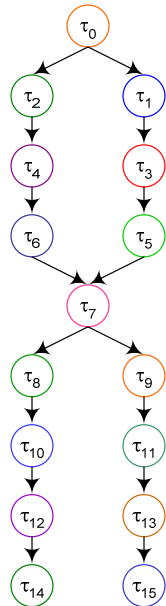
JPEG Encoder



GSM Decoder



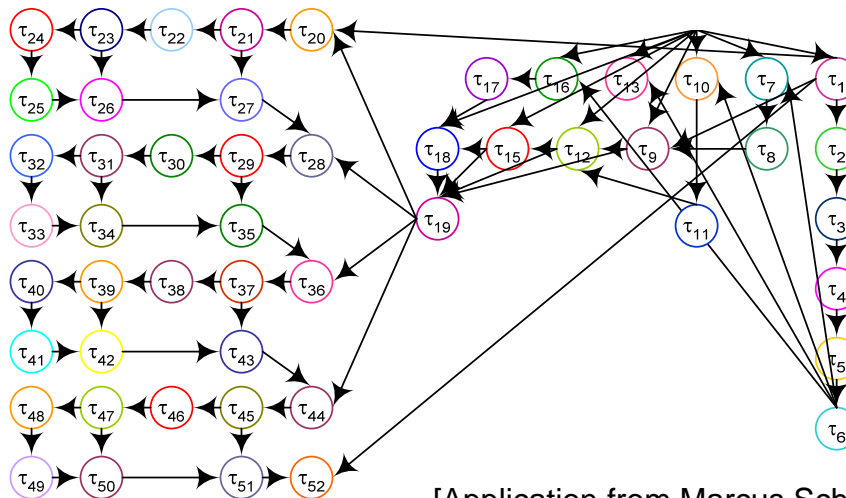
MP3 Decoder



JPEG Decoder



GSM Encoder



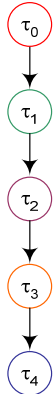
[Application from Marcus Schmitz, TU Linkoping]



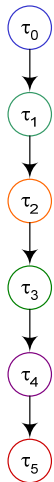
# Smart phone



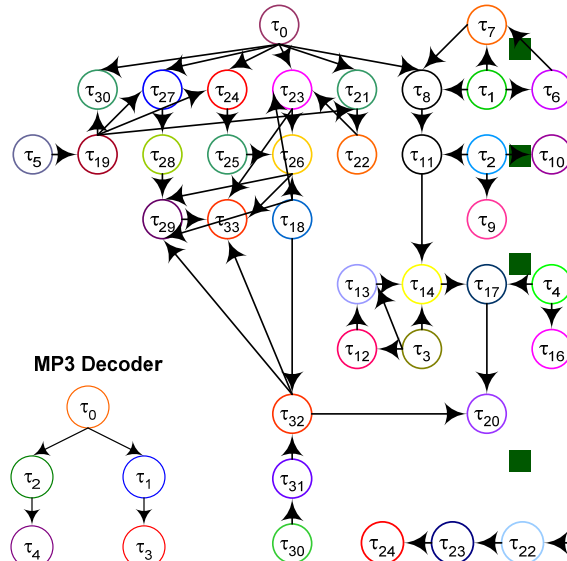
JPEG Encoder



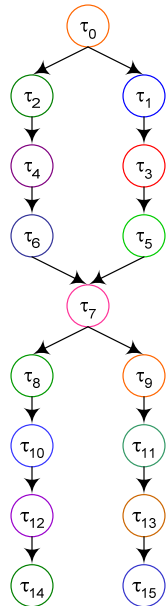
JPEG Decoder



GSM Decoder



MP3 Decoder



Tasks: 114

Deadlines: [0.02: 0.5] sec

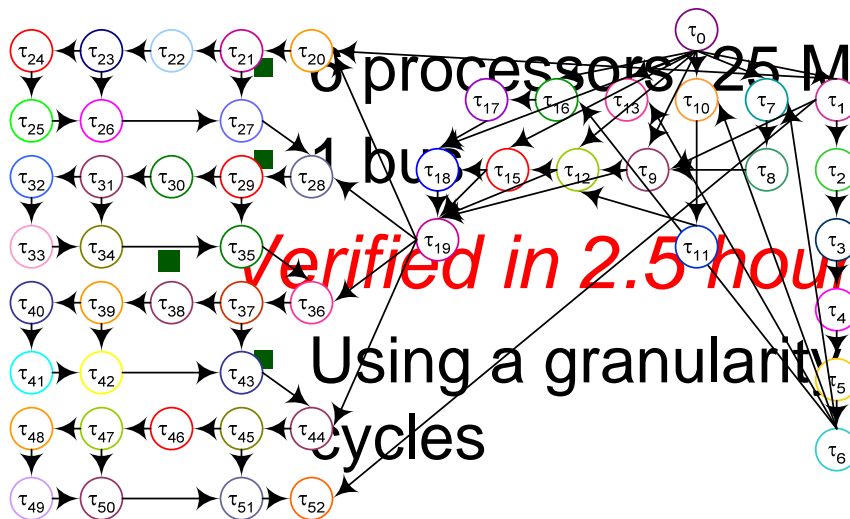
Execution: [52 : 266.687] cycles

Platform:

2 processors, 25 MHz  
1 bus

*Verified in 2.5 hours!*

Using a granularity of 400 cycles



# Acknowledgements



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## ARTS

- Shankar Mahadevan
- Kehuai Wu
- Kashif Virk
- Michael Storgaard
- Mercury Gonzalez



# Discussion Points



- **Accuracy** versus **scalability**
  - UPPAAL & SymTA/S (Network Calculus)
- **Verification** versus **simulation**
  - UPPAAL & ARTS (System C)
  - UPPAAL & Ptolemy
  - UPPAAL & TrueTime
- Efficient verification methods for **optimal infinite scheduling** for PTA.
  - Negative rates
  - Discounting



# Collaborators



## @UPPsala



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- Pavel Krcal
- Leonid Mokrushin
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