Network of Excellence

IST-004527 ARTIST2:
Embedded Systems Design

Activity Progress Report for Year 1

JPRA-Cluster Integration:

Design for Low Power

Cluster:

Execution Platforms

Activity Leader:

Luca Benini (University of Bologna)

Power dissipation is rapidly becoming one of the most serious obstacles in the evolution of electronic systems. Technology development leads to an increased active-state and stand-by power consumption. mainstream architectural design is moving towards energy-hungry architectures, e.g. programmability. It is the objective of this activity to develop, promote and integrate methods that address issues across several layers of abstraction.

Table of Contents

1. Introduction

1.1 Activity Leader

Luca Benini (University of Bologna)

Areas of his team's expertise: Low power design, System-on-chip design.

1.2 Policy Objective

Power dissipation is rapidly becoming one of the most serious obstacles in the evolution of electronic systems. Technology development leads to an increased active-state and stand-by power consumption. mainstream architectural design is moving towards energy-hungry architectures, e.g. programmability. It is the objective of this activity to develop, promote and integrate methods that address issues across several layers of abstraction.

1.3 Industrial Sectors

Low power design impact a large number of industrial sectors.

Consumer electronics: power consumption is a major contributor to system cost, both in terms of design, development, manifacturing and in terms of cost of ownership (batteries, lifetime). Moreover, low power consumption makes it possible to reduce battery weight and size, thereby enabling smaller form factors and better usability.

Communication: mobile communication terminials (handsets) are one of the largest markets for the electronics industry. Low power design is a clearly a strategic area for this market, since lower power execution platforms contribute to longer battery lifetime and make it possible to miniaturize the devices. Even if hanset miniaturization is reaching usability limits, reducing the power consumed for executing a particular function (i.e., increasing energy efficiency) makes it possible to support an increased number of features without increasing size or decreasing lifetime.

Even though consumer and communication electronics have traditionally been the sectors of key impact of low power design, the picture is rapidly changing and more industrial sectors now strategically need low power design. The computer industry is now facing significant challenges posed by the excessive power density of high-performance microprocessors, and a number of low power design techniques are pioneered in an effort to improve the energy efficiency of microprocessors. Looking forward, the maturing low-power wireless sensor network technology is likely to become a key differentiator for a large number of products and services in health monitoring, industrial monitoring, surveillance and protection of people and assets.

2. Overview of the Activity

2.1 Artist Participants and roles

Team leader: Petru Eles (University Linköping)

Areas of his team's expertise: dynamic and leakage power optimisation for real-time system, accurate system-level power modelling for communication.

Team Leader: Luca Benini (University of Bologna)

Areas of his team's expertise: power aware operating systems, low power system-on-chip architectures.

Team Leader: Jan Madsen, Jens Sparsoe (Technical University of Denmark)

Areas of his team's expertise: asynchronous low power design.

2.2 Affiliated partners and Roles

Team Leader: Luciano Lavagno (Politecnico di Torino)

Areas of his team's expertise: low power circuits.

Team Leader: Geert Deconinck (K.U. Leuven)

Areas of his team's expertise: low power architectures.

Team Leader: Roberto Zafalon (STMicroelectronics)

Areas of his team's expertise: low power single-chip multiprocessors.

2.3 Starting date, and expected ending date

Starting date: September 1st, 2004.

Ending date: the activity will span the duration of the project, since all current trends indicate that low power design will increasingly become a top priority for a number of industrial sectors

2.4 Baseline

The group of Luca Benini at the University of Bologna (UoB) is one of the leading centres in low power design, focusing on system level power management both from the architectural and from the software viewpoint. In this area, the group has produced a large number of contributions on OS-Based-dynamic power management, memory and communication architecture optimisation for low power consumption, low power circuit design, battery-driven

power management. One of the baselines contributions of UoB to the project is a complete power modelling infrastructure both for all components of current MPSoC Platforms and for future Network-on-Chip-based platform.

The group of Jan Madsen at DTU aims at low-power techniques for wireless sensor networks, and it brings significant experience on low-power asynchronous circuit design, as well as analytic and stochastic modelling of power consumption and battery usage.

The group of Petru Eles at Linkoeping University has given important contributions on high-level system modelling of both power and reliability, and on optimisation techniques for energy efficient mapping of applications on execution platforms.

2.5 Technical Description

The project aims at investigating comprehensive hardware-software power optimisation solutions for single and multi-processor embedded systems. A software power manager will be implemented within the kernel of the system support software. The power management software will closely interact with power-manageable hardware through a streamlined hardware-sofware interface. In this way, the different levels of abstraction participating in low power design will be integrated.

3. Activity Progress Report

3.1 Work achieved in the first 6 months

Università di Bologna has focused in the first six months on interconnect optimisation techniques for low power. Several schemes have been developed to instantiate application (platform) specific interconnect architectures for minimum energy consumption. An algorithm for automatic instantiation of multi-hop busses which includes topology generation and bus frequency assignment has been developed in collaboration with Penn State University.

Additionally several extensions to the power modelling infrastructure in the MPARM virtual platform simulators have been developed, including the model for variable frequency and variable voltage cores, as well as a prototype model for estimating the power consumption of IOs and external memories (this work has been performed in cooperation with associate partner STMicroelectronics)

Linkoeping University has developed a technique for static routing on NoC, with guaranteed delays and arrival probabilities in the presence of transient faults. The approach is based on schedulability analysis of tasks and messages with priority based arbitration. For fault-tolerance, a combination of spatial and temporal redundancy is considered. Reduced communication energy is one of the goals. More recently the the analysis of the worst-case buffer space needed has been performed. Based on this analysis, it is possible to develop an approach to buffer space minimization in the context described above.

Technical University of denmark has started the development of a generic sensor network platform (Hogthrob project) which allows to tradeoff hardware and software implementations of the various components of the platform. So far, the focus has been on: (1) Processor design: Low-power design techniques have been investigated, included low-power synthesis (e.g., clock-gating), power modes and de-synchronizing in the context of the OpenCores AVR core (using Synopsys) (2) Power modeling: Simulation-based power modeling and estimation techniques have been investigated. This involves analytic and stochastic modeling of batteries and investigation into the macromodeling of various hardware components.

3.2 Work achieved in months 6-12

Bologna university has started a research effort on energy aware mapping of multi-task applications on multi-processor SoC execution platforms. The approach is based on variable-voltage processors where execution speed and voltage supply can be independently adapted to the processor's workload. The first result of this effort has been a design space exploration technique that automatically finds pareto points in the power vs. throughput design space. The technique has been tested on streaming-like signal processing applications.

Linkoeping University's most recent efforts are aiming at a more accurate modelling of actual communication and memory techniques used in MP SoC. Such an accurate modeling is needed in order for a system level analysis and optimization to produce useful results. Thus, work is concentrating on: (1) Capturing the background communication due to cache misses in system level models. (2) Capturing the bus load due to system-wide synchronization. Once this modeling issues are solved, different optimization techniques can be used for e.g. task mapping and scheduling, as well as voltage selection. Results can be validated using accurate and fast simulation in the environment developed at Bologna. Another issue which is currently addressed is that of efficient optimization techniques based on advanced constraint solving

and mathematical programming techniques. This work is performed in cooperation with the group at University of Bologna.

In the framework of the research on low power wireless sensor networks (Hogthrob Project), the focus of the Technical University of Denmark has been on: (1) Processor design: DTU is currently investigating architectures for bit compression and bit-serial computation in the context of the BitSNAP core. (2) Power modelling: development of a sensor network power model within the UppAal model checking environment which allows for a formal analysis of power consumption within the network. (3) Empirical power estimation: Based on the prototype sensor network platform developed within Hogthrob, various testbench programs have been run on an AVR core synthesized on the FPGA and a number of physical measurements have been conducted. Finally, DTU has started investigating how the power modeling and the sensor network modeling can be captured within the multiprocessor simulation environment, ARTS, developed at DTU.

3.3 Difficulties Encountered

None

3.4 Recommendations

None

3.5 Milestones

Università di Bologna: (1) started an industrial contract with Freescale semiconductor on the development of an advanced OS-based power management solution targeting next-generation silicon platforms for handsets; (2) established a working cooperation with Linkoeping University on system-level power modelling and optimization

Linkoeping University: (1) established a cooperation with bologna: One PhD student from Linkoping has visited the Bologna group for on month in April 2005; Prof. Luca Benini has visited Linkoping for 3 days in December 2004; (2) Achieved important tesults in the development of reliability and energy aware system-level scheduling techniques and communication scheduling

Technical University of Denmark (1) Development of a Wireless sensor network hardware prototype and analysis of power consumption under a number of different operating conditions. (2) Development of an abstract simulation environment for estimating power consumption in sensor networks

3.6 Main Funding

Bologna University: STMicroelectronics industrial grant, Freescale semiconductor industrial grant

Linkoeping University: Swedish Foundation for Strategic Research (SSF)

Technical University of Denmark: national funded research project, Hogthrob

3.7 Indicators for Integration

Consistent progress has been reported with respect to the integration indicators. An active and productive cooperation between two of the partners has been setup and will be further developed.

From the technical viewopoint several new problems have been identified, and will be jointly researched by the partners. The research approach strongly leverages synergies between the partners, by integrating different levels of system abstraction (from scheduling via operating systems to system design).

3.8 Evolution

The work will evolve in several directions:

1. Further development of integration activities: the work of Bologna and Linkoeping will continue focusing on the development of accurate high-level optimization algorithms for task allocation and scheduling, as well as voltage assignment, which account for non-ideality of silicon platforms
2. Bologna will develop a software infrastrcture in a multi-processor operating system aiming at run-time management of voltage and frequency of multiple cores
3. Linkoeping will continue research on the interplay between fault tolerance and reliability and power consumption at the system level
4. DTU will carry on prototyping activity on sensor nodes and further refine the abstract stochastic model of sensor networks

Long term objectives are a tighter integration and the development of a software optimization framework that targets both multi-processor systems on chip for high-end multimedia applications and ultra-low power, reduced functionality wireless sensor nodes.

4. Detailed Technical View

4.1 Brief State of the Art

Even though power is now considered as the most critical issue in the design of advanced platforms for embedded applications, the state-of-the-art of research and industrial development is still at a highly instable and incomplete stage. As a result, comprehensive power analysis and management solutions for single and multi-processor embedded systems are still missing. First, we consider system-level power modelling methods and abstractions.

Currently, there exist component models that describe power dissipation of system components in various ways, such as abstract finite-state models (Power FSMs), stochastic modelling (Markovian, generalized semi-Markov processes) for power manageable components. In addition, there are many different QOS metrics related to power such as average power, peak power and battery lifetime, the joint power performance metrics energy and energy-delay, joint power-reliability metrics and power performance metrics for distributed systems. The state of the art in power modelling is therefore quite unstructured, and it can be summarized as follows:

- **Model power in computational units**. We distinguish between core processor and dedicated functional units. For the first class of units, the instruction-level power model is the most commonly adopted. In this model, a value of power consumption is associated to each instruction (or instruction pair, for increased accuracy and for taking state effects into consideration). Even though this model provides good accuracy for simple cores (single pipeline), it has serious limitations for more complex cores. Component-based power models represent a different approach, where a core is represented as an abstract composition of elements (e.g. instruction fetch unit, execution units). Each component is characterized by a power consumption, which depends on some execution-dependent parameter, which can be sampled an instruction-set simulation. This model is more accurate than the instruction-level power model in case of cores with high parallelism and multiple parallel sub-units (e.g. DSPs and superscalar processors). However, it requires some knowledge of the internal micro-architecture.
- **Special-purpose units**, which do not correspond to the template of an instruction-set processor are modelled using finite state (power-) state machines, where power values are associated to states and state transitions are associated to functional events (e.g. transition between read, execute, write modes).
- **Storage units**. The simplest model, used for simple single memory banks, associates to each memory operation a power cost (e.g. read power, write power, idle power). This is a simple table-based model, which provides sufficient accuracy for the basic memory macros. Complex memory blocks, such as DRAM chips, are similar to special purpose computational units and are modelled with power state machines, ad described above. Data dependency is generally neglected.
- **Communication blocks**. Dedicated wires implement the simplest communication function. In this case, a model based on switching activity and capacitive load is used to estimate power. In most cases, however, communication resources are not simple wires, but they contain significant logic resources (e.g. a bus arbiter, multiplexers, decoders). In this case, models are usually utilization-based. Power is correlated to the transactions that are carried through the interconnect (e.g. power for a write transaction, a read transaction, etc). In this case, dependency on switching activity is

reduced, but it can be considered via scaling factors linked to the number of bus lines switching.

One important missing point in the power estimation strategy at the system level is the integration of the model of multiple resources in a single modelling environment. Furthermore, the models are often obtained on speculative technology information, and they are often non-homogeneous in terms of power data (because they are based on different technology assumption).

From the point of view of power management, the focus of the state of the art is primarily on power control of a single system component, with significant emphasis on processors. The approaches relevant for ARTIST are software-centric. With the growing software content in most embedded systems, and the diffusion of programmability and flexibility, software has a very high degree of control on resource utilization. State-of-the-art processors provide the control of clock speed, supply delivery and supply voltage, device thresholds, The tuning of these parameters can be performed both at compile time (statically) and at run-time (dynamically), but the most significant results can be achieved only by a comprehensive approach that combines the advantages of static and dynamic techniques. Clearly, in this scenario, a tight integration between the software layers must be achieved. There is a need programming abstractions to expose power control and resource management options to the application programmer, to the compiler expert and to the operating system developer.

Several solutions have been proposed to manage processor frequency, voltage and shutdown at run time. The solutions are based on different assumptions on processor workload. Real-time power management formulations assume the knowledge of worst-case execution times; deadlines and they also assume well-characterized inter-task interactions. Non-real-time approaches rely on prediction and estimation of processor workload and employ online heuristics to minimize idle time (both by frequency and voltage scaling, and by shutdown), while controlling performance penalty (i.e. reducing idle time, but without driving the system into saturation).

It must be noted, however, comprehensive power management solutions for single and multi-processor embedded systems are still missing. They should be implemented within the kernel of the system support software and tightly coupled to process management. This way, the different levels of abstraction participating in low power design could be integrated. Moreover, a comprehensive power manager should consider tradeoffs between different system components.

4.2 Industrial Needs and Experience

Low power design has a deep impact on a large number of industrial sectors.

- **Communications**: Mobile communication terminals are one of the largest markets for the electronics industry. Low power design is an obviously a key strategic area for this market, since lower power execution platforms contribute to longer battery lifetime and make it possible to miniaturize the devices. Even if portable appliance miniaturization is reaching usability limits, reducing the power consumed for executing a particular function (i.e., increasing energy efficiency) makes it possible to support an increased number of features without increasing size or decreasing lifetime.
- **Consumer electronics**. Power consumption is a major contributor to system cost, both in terms of design, development, manufacturing and in terms of cost of ownership (batteries, lifetime). Moreover, low power consumption makes it possible to reduce battery weight and size, thereby enabling smaller form factors and better usability.

Even though consumer and communication electronics have traditionally been the sectors of key impact of low power design, the picture is rapidly changing and more industrial sectors now strategically need low power design. The computer industry is now facing significant challenges posed by the excessive power density of high-performance microprocessors, and a number of low power design techniques are pioneered in an effort to improve the energy efficiency of microprocessors. Looking forward, the maturing low-power wireless sensor network technology is likely to become a key differentiator for a large number of products and services in health monitoring, industrial monitoring, surveillance and protection of people and assets.

4.3 Ongoing Work in the Partner Institutions

The cluster integration activities leverage the multi-year research experience of all participating institutions. More specifically, the group at the university of Bologna (UNIBO) has traditionally focused on power management at the system level, as well as on high-level power characterization and modelling. The group at the technical university of Denmark (DTU) has experience in energy-efficient design of asynchronous hardware platforms, as well as in analytic and stochastic modelling of power consumption and battery usage. The group at Linkoeping University (LIU) has worked extensively on issues related to energy efficient real-time systems.

Based on the above-summarized research background, the participating partners have set up, within the cluster integration framework, a number of synergistic efforts, aiming at building a common infrastructure. Even though the infrastructure-building efforts have been developed by each individual partner in an autonomous way, with limited technical interactions with the other partners, these efforts are required as a preparatory action for the follow-up integration activities described in the next section of this document.

UNIBO has contributed to the common ARTIST2 research infrastructure in two main ways:

1. Extending MPARM, the pre-existing Multi-processor System-on-Chip (MPSoC) power modelling and analysis environment to better support research integration with the cluster partners. More in detail, Several schemes have been developed to instantiate application (platform) specific interconnect architectures for minimum energy consumption. This is a critical enabling feature for cluster integration, because exploration of energy-efficient hardware platforms critically relies the ability of modelling a wide variety of complex-multi hop interconnect architectures (as opposed to, for instance a simple, non-scalable, single-bus architecture)

2. Additionally, several extensions to the power modelling capabilities in MPARM have been developed, including the model for variable frequency and variable voltage cores, as well as a prototype model for estimating the power consumption of IOs and external memories. This work has been performed in cooperation with associate partner STMicroelectronics, which has provided the required technology-dependent information, from a state-of-the-art CMOS technology. The contribution of associate partner STM demonstrates strong industrial interest in the exploitation of the research results obtained by the cluster.

The main contribution of LIU to the clusters common research infrastructure has been in developing:

1. Energy efficient scheduling of tasks on multiprocessor systems with variable voltage/frequency levels.
2. Energy efficient, fault -tolerant communication on NOCs, for applications with hard time constraints.

With respect to the second theme, Linkoeping University has developed in the first 6 months of the project a technique for static routing on NoC, with guaranteed delays and arrival probabilities in the presence of transient faults. The approach is based on schedulability analysis of tasks and messages with priority-based arbitration. For fault-tolerance, a combination of spatial and temporal redundancy is considered. Reduced communication energy is one of the goals. Furthermore, analysis of the worst-case buffer space needed has been performed. Based on this analysis, it is possible to develop an approach to buffer space minimization in the context described above.

The contribution of DTU to the research infrastructure of the cluster has been in the area of distributed embedded systems. DTU has started in the first six months the development of a generic sensor network platform (Hogthrob project), which allows to trade off hardware and software implementations of the various components of the platform. The focus has been on: (1) Processor design: Low-power design techniques have been investigated, included low-power synthesis (e.g., clock-gating), power modes and de-synchronizing in the context of the OpenCores AVR core (using Synopsys) (2) Power modelling: Simulation-based power modelling and estimation techniques have been investigated. This involves analytic and stochastic modelling of batteries and investigation into the macromodeling of various hardware components.

4.4 Interaction, Building Excellence Between Partners

The infrastructure-building initiatives taken by the cluster partners have established the common ground for interaction, and building excellence activities that will be detailed next. The interaction between the involved groups has been very active and productive. The complementary expertise of the groups has led to several synergies.

UNIBO and LIU have started a joint research effort on energy aware mapping of multi-task applications on multi-processor SoC execution platforms. Power optimization for multi-core systems is a key problem in current execution platforms, and the interaction initiative initiated by the cluster aims at exploiting the complementary expertise in the cluster partners. The expertise of the LIU group is mainly in the area of Real-time embedded systems modeling and design based on formal methods . The group of UNIBO has a very strong expertise in the areas of SoC architectures and power management (Prof. Luca Benini), as well as a strong background in the field of optimisation by constraint solving (Prof. Michela Milano). In this context, unique opportunity of cooperation has been provided in the context of the ARTIST2 network. A visit of two PhD students from Linkoeping to Bologna, as well as the visit of professor Luca Benini at Linkoeping have laid the foundation of a cooperation which would have not been possible without the ARTIST2 network.
The following issues have been approached in common and have also opened the perspective of continuation in the second period of the project :

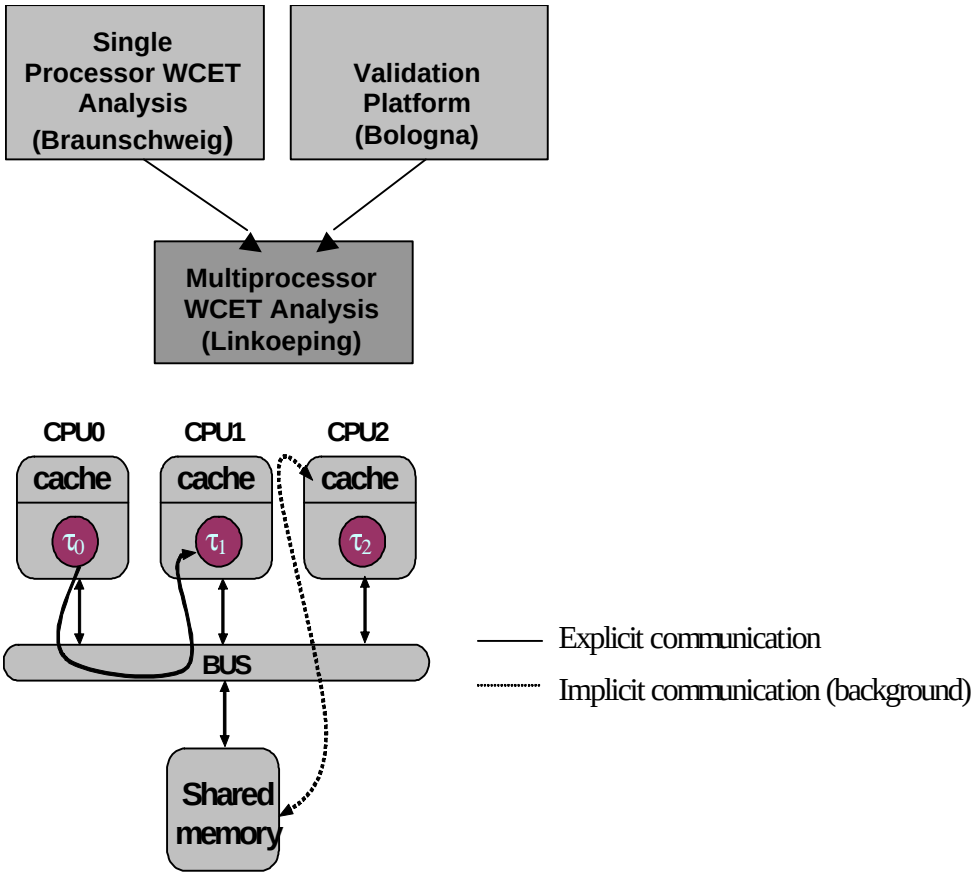
1. Accurate system (in particular communication) modeling for predictability and energy optimisation in multiprocessor architectures.
2. Optimisation of energy constrained real-time systems using mathematical programming and constraint solving techniques.

Thanks to the analysis of results using cycle accurate functional and power simulation (based on MPARM), the need has emerged for an accurate modelling of actual communication and memory allocation techniques used in MP SoC. Accurate modelling is needed in order for a system level analysis and optimization to produce useful results. Thus, work is concentrating on: (1) Capturing the background communication due to cache misses in system level models. (2) Capturing the bus load due to system-wide synchronization.

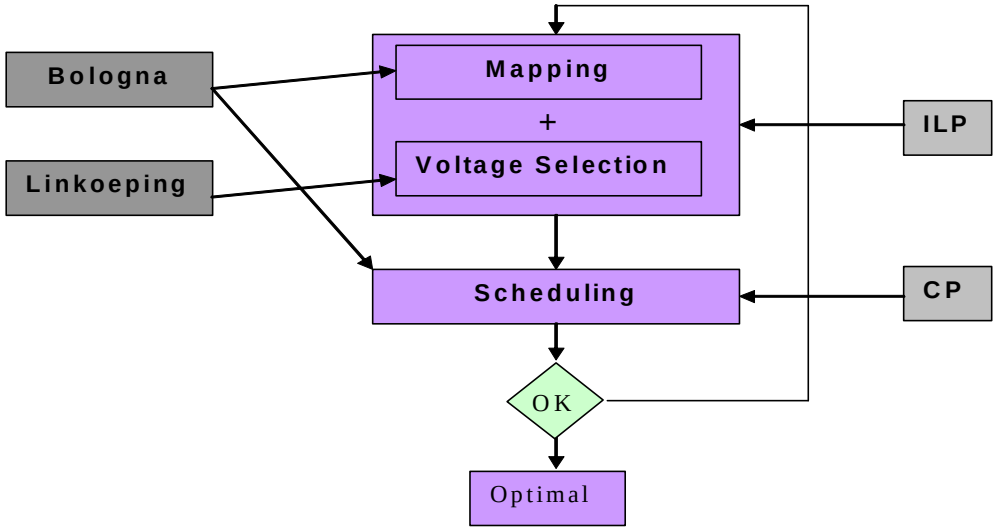
Worst-case execution time analysis is a well established research area. Existing tools (e.g. Symta/P from Braunschweig University) are able to compute the worst-case execution time of

applications running on single processors, in the presence of instruction and data caches. However, there are no existing tools that are capable to compute the worst-case execution time for applications running on multiprocessor systems with caches. An example of such a platform is in the figure below.

For every cache miss, the shared memory is read. This generates additional traffic on the bus (implicit communication) that potentially collides with the explicitly modelled interprocessor communication. Thus, as opposed to a single processor platform, where a cache miss is served in constant time, in a multiprocessor environment, the cache misses take a variable amount of time, depending on the bus contention. The goal is to propose an approach that deals with this problem and is able to compute the worst-case execution time for applications running on multiprocessor platforms. As starting point we consider an existing single processor tool (Symta/P), developed at TU Braunschweig. The result will be validated on the multiprocessor ARM platform (MPARM) developed at UNIBO.



Multiprocessor platform with cache



Benders Decomposition for Mapping, Scheduling and Voltage Selection

Once these modelling issues are solved, different optimization techniques can be used for e.g. task mapping and scheduling, as well as voltage selection. Results can be validated using accurate and fast simulation in MPARM.
In particular, as a result of UNIBO and LIU cooperation, an issue that we currently address is an efficient optimization technique based on advanced constraint solving and mathematical programming techniques. We solve the general problem of mapping, scheduling and voltage scaling of real-time applications with the objective of energy minimization. We use the Benders decomposition to separate the mapping and voltage selection (implemented using integer linear programming) from scheduling (implemented using constraint programming). The algorithm flow is depicted in Fig. 4. The ILP formulation for mapping and voltage selection computes for each task the mapping and speed that could provide the minimum energy. In the next phase, constraint programming checks the timing feasibility of the current mapping and voltage assignment. If the scheduling finds a valid schedule, the optimization stops and that is the optimal system configuration. In case a valid solution could not be found, constraint programming generates a NO-GOOD solution that is fed back to the ILP.
The development of highly-tuned optimization approaches that overcome the computational limitations of general-purpose optimization tools is one of the expected outcomes of the integration work within the cluster. Preliminary results in the first year of activities demonstrate that signficant power savings can be achieved at an acceptable computational cost.

DTU has contributed to the interaction by sponsoring several visit of a PhD student to UNIBO, for joint work on the MPARM platform. The main purpose of the visit was to *develop a coherent interface for modeling complex systems (both on-chip and distributed) using combined formal and simulation approaches*. Both functional and power modeling has been addressed. This work is very relevant for modeling complex distributed system like sensor networks.

In this area DTU has contributed a high-level sensor network power model within the UppAal model checking environment, which allows for a formal analysis of power consumption within the network. The UppAal framework from Upsala and Aalborg (both ARTIST2 partners), builds upon the theory of timed automata but has been extended to support features required by the real-time system and protocol verification community. This allows protocol designers to formally reason about safety and liveness properties of a new protocol. Similarly, liveness properties such as guaranteeing that a system always will try to send a message, can be verified. Also, designers of real-time systems have successfully used UPPALL to formally verify different scheduling policies. The UPPAAL framework is therefore an extremely versatile tool

that has already proven successful for large corporate organizations, but it still has much potential left to explore.

The UPPAAL framework can be exploited to analyze Power Consumption in wireless sensor networks. This has been accomplished by developing an UPPAAL model of a sensor network, and then exploring the possibilities of formal reachability analysis. This has resulted in detailed worst-case analysis of both total power consumption and power patterns in wireless sensor networks. Wireless sensor networks are powered by small batteries. Therefore, it is critical to optimize the sensor nodes and the programs running on the nodes in order to minimize energy consumption. The code size and execution time are also limited by the memory size and the real-time constraints. The sensor node itself may be designed and implemented as a heterogeneous multiprocessor system, i.e. a complicated System-on-Chip.

The aim of the research has been to examine the possibilities of using formal analysis to verify energy properties of wireless sensor networks. In particular, to reason about the energy consumption of the entire system. Formal analysis requires the use of models, trusted to behave like a real system. It is therefore critical to find the correct abstraction layer for the models and to verify the models. When good models exist, the formal analysis of the systems can be performed; this will give the system designers a new way of analyzing their systems. The traditional way to obtain power or energy figures, is by simulation of a typical sequence of events (maybe also a few extreme cases to cover worst case scenarios). However, although simulation may be a very useful tool, exhaustive search for the worst case scenario is often impossible. There are two corner cases regarding energy consumption which can be checked through this way of modelling, the lowest possible energy consumption and the highest possible energy consumption within a given interval.

The formal approach pursued by DTU has addressed these corner cases and demonstrated that it is feasible to use UPPAAL to formally reason about energy consumptions. This approach is synergistic and complementary to simulation-based power estimation (as supported by the UNIBO MPARM framework), and therefore an integrated approach can provide significant added value to the field of system level power modeling

Additionally, DTU has also focused on empirical power estimation: based on the prototype sensor network platform developed within the Hogthrob project, various test-bench programs have been run on an AVR core synthesized on the FPGA and a number of physical measurements have been conducted. DTU has also started investigating, during the visit of the PhD student in UNIBO, on how the power modelling and the sensor network modelling can be captured within a single multiprocessor simulation environment, which will merge the ARTS framework developed in DTU with the MPARM framework developed in UNIBO :

In summary, the significant amount of joint research and building excellence activities clearly shows that the partners are cooperatively working toward two key strategic objectives:

1. *Building a common set of methods and tools for system-level power estimation, applicable to a large number of embedded computing systems, including chips, systems-on-chip and distributed systems.* The main cornerstones of this efforts are the simulation-based platform maintained by UNIBO, and the formal models developed by DTU and LIU. All partners have contributed to the simulation platform (as users and developers of extensions and benchmarks) and to the refinement, validation and evolution of the formal models (leveraging simulation results).
2. *Joining abstract models of performance and power consumption, to be used in system-level mapping and optimisation, with a lower level power and performance analysis infrastructure, aiming at the validation of optimisation results*. Preliminary results obtained in this area are extremely promising, in that they show: (i) good matching of optimization results obtained on abstract models and simulation-based validation, (ii)

significant speedups in optimization time thanks to advanced optimization technologies (such as hybrid IP-CP techniques). These achievements have the potential to significantly bring forward the state of the art and to increase the adoption of optimization-based design methodology in the industrial system-level design practice.

4.5 Spreading Excellence

The partners involved in the project have been very active in publicly spreading the results of the building excellence activities.

Senior representatives of all the partners have given several invited presentations in conferences and symposia on joint research topics and results of building excellence activities:

Petru Eles LIU, (as an IEEE CAS Distinguished lecturer):

- IEEE Andian Region Conference ANDESCON 2004, Bogota Columbia "Energy-aware design of real time embedded systems"
- IEEE NSW Section, Sydney, Australia, 2005 "Analysis and optimisation of distributed real-time embedded systems"
- University of NSW, Sydney, Australia, 2005 "Energy-aware design of real-time embedded systems"

Paul Pop LIU

- International Conference on Integration of AI and OR Techniques in Constraint Programming for Combinatorial Optimization Problems, Prague, Czech Republic "Embedded Systems Design: Optimizations Challenges"

Luca Benini UNIBO

- IEEE VLSI Design Conference, Kolkata, India 2005 “Energy efficient networked embedded systems”
- First International Workshop on advanced Sensors and Interfaces Bari, Italy 2005, “Wireless sensor networks – Enabling technology for Ambient Intelligence”
- IEEE Symposium on Integrated Circuits and Systems Design, Florianopolis, Brazil 2005, “Advanced Power management of SoC Platforms”

Talks, Davide Bertozzi UNIBO

- Intel High-level design and verification Symposium, “Communication-centric Low Power Architectures for Multiprocessor Systems on Chip”

In all the above-mentioned presentations, the cluster members have disseminated the technical achievements obtained through the ARTIST2 building excellence activities within the cluster. The presentations have had an average attendance of approximately 100 people. Hence, several hundreds of researchers and engineers from academia, research institutes and industry around the world have been informed in details on the low-power cluster joint research results.

The partners have also organized various in depth spreading excellence initiatives focusing on low power.

- The LIU group is part of the excellence center STRINGENT (Strategic Integrated Electronic Systems Research). This is the Swedish excellence center for Microelectronic Systems research, financed by the Foundation for Strategic Research of Sweden. In the context of this center, several contacts, meetings, and information/technology exchange is carried out with international companies such as Ericsson, Infineon, Philips, Samsung.
- Jan Madsen (DTU) has been a key initiator in setting up and running a Danish industrial network for wireless sensor networks which among others focus on low power aspects and energy harvesting. The network covers around 20 companies and 56 universities and research institutions. The network meets 2-3 times a year for a half day seminar on a selected topic. Presentations are given by members as well as external invited speakers (such as Dr. Ralph Kling, Intel research, and Christian Enz, EPFL).
- Luca Benini (UNIBO) has organized together with Christian Probst (University of California, Irvine) and Ulrich Kremer (Rutgers University) the Dagstuhl Seminar On Power-Aware Computing Systems, held from April 3rd to April 8th 2005 at Schloss Dagstuhl, Germany. The program of the seminar featured presentations of about 35 participating researchers and practitioners from all over the world. They were chosen to represent major areas in targeting the energy consumption of a computing system---Applications, Compilers, Virtual-execution Environments, Operating Systems, and Hardware.
- All the partners have participated to the ARTIST2 Cluster meeting, held in ETHZ, Zurich 10-11/2/2005. During the meeting, the cluster representatives (one senior and one student representative for each cluster) have given presentation summarizing the building excellence activities. The meeting has been instrumental to the organization of the research cooperation in the following months.

A significant fraction of the spreading excellence efforts of the cluster participants have focused on dissemination to industry:

UNIBO has given presentations on low power design of embedded systems to the following companies: Freescale Semiconductors, Aylesbury, UK (on Dynamic Power Management for embedded processors), Philips Research Eindhoven NL (on Advanced Power Management of SoCs), STMicroelectronics, Agrate IT (on Low-Power SoC design), Samsung, Seoul KR (on design of low-power interconnects). Furthermore, UNIBO, LIU and DTU are involved in several industrially sponsored projects on low power design further emphasizes the dissemination effort in this activity

The activities of the low-power cluster have also produced several publications in the proceedings of the main international conferences in design automation. These contributions have also been presented orally at the conference. We list here the most relevant conference proceedings publications:

- Quasi-static voltage scaling for energy minimization with time constraints Andrei, A.; Schmitz, M.T.; Eles, P.; Peng, Z.; Al Hashimi, B.M.; Design, Automation and Test in Europe, 2005.

- Quasi-static assignment of voltages and optional cycles for maximizing rewards in real-time systems with energy constraints Cortes, L.; Eles, P.; Peng, Z.; Design Automation Conference, 2005.

- ARTS: A System-Level Framework for Modeling MPSoC Components and Analysis of their Causality Mahadevan, S.; Storgaard, M.; Madsen, J.; Virk, K.; Modeling, Analysis, and Simulation of Computer and Telecommunication Systems, 2005.

- Architectural, system level and protocol level techniques for power optimization for networked embedded systems Benini, L.; Shukla SK; Gupta, R.K.; IEEE International Conference on VLSI Design, 2005.

- Application-Specific Power-Aware Workload Allocation for Voltage Scalable MPSoC Platforms Ruggiero, M.; Acquaviva, A.; Bertozzi, D.; Benini, L.; IEEE International Conference on Computer Design, 2005.

- Allocation and cheduling for MPSoCs via decomposition and no-good generation" Benini, L.; Bertozzi, D.; Guerri, A.; Milano, M.; International Conference on Principles and Practice of Constraint Programming 2005.