ARTIST 2

Network of Excellence

IST-004527 ARTIST2:
Embedded Systems Design

Periodic Activity Report for Year 1

Executive Summary

Joseph Sifakis – Artist2 Scientific Coordinator

Bruno Bouyssounouse – Artist2 Technical Coordinator

Artist2 Consortium

Artist2's main objective is to set up a scientific community in the area of embedded systems. Our approach consists in gathering together clusters, which are teams, on essential topics in embedded systems design. The integration effort consists of to strengthening coherency within the clusters (cluster integration activities), and integration between clusters (NoE Integration activities).

Intra-cluster and inter-cluster integration is driven by work around cutting-edge research activities, technical platforms, and dissemination / spreading excellence.

We aim to create a lasting structure that will continue to benefit the research community and industry well beyond the lifespan of the NoE financing.

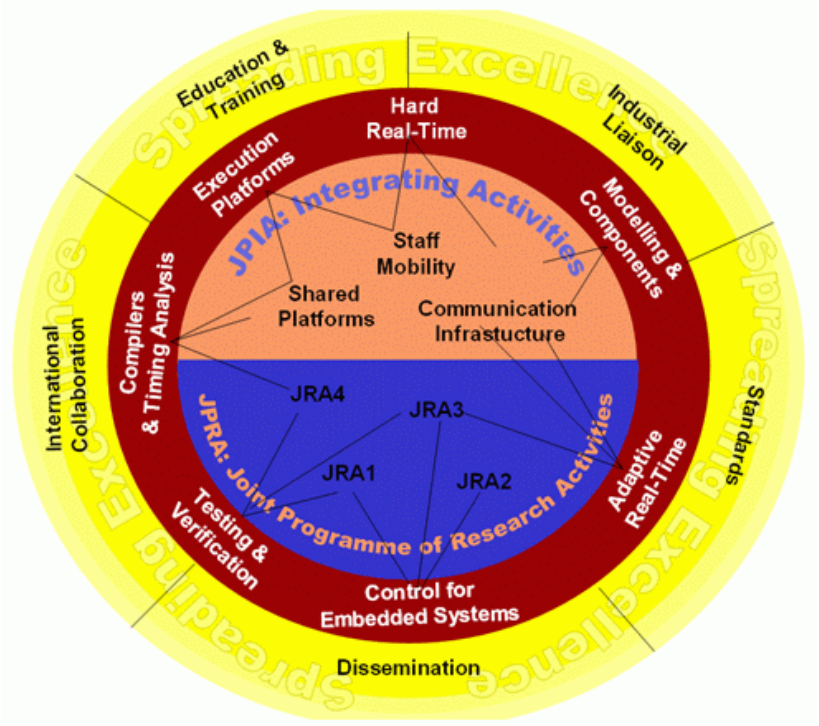
1. Executive Summary

1.1 Project Objectives

The strategic objective of the ARTIST2 Network of Excellence is to strengthen European research in Embedded Systems Design, and promote the emergence of this new multi-disciplinary area. We gather together the best European teams from the composing disciplines, and will work to forge a scientific community. Integration will be achieved around a Joint Programme of Activities, aiming to create critical mass from the selected European teams.

The ARTIST2 Network of Excellence on Embedded Systems Design implements an international and interdisciplinary fusion of effort to create a unique European virtual centre of excellence on Embedded Systems Design. This interdisciplinary effort in research is mandatory to establish Embedded Systems Design as a discipline, combining competencies from electrical engineering, computer science, applied mathematics, and control theory. The ambition is to compete on the same level as equivalent centres in the USA (Berkeley, Stanford, MIT, Carnegie Mellon), for both the production and transfer of knowledge and competencies, and for the impact on industrial innovation.

ARTIST2 has a double core, consisting of leading-edge research in embedded systems design issues (described later in this document) in the Joint Programme of Research Activities (JPRA), and complementary activities around shared platforms and staff mobility in the Joint Programme of Integration Activities (JPIA).



Building the embedded systems design scientific community is an ambitious programme. To succeed, ARTIST2 builds on the achievements and experience from the ARTIST1 FP5

Accompanying Measure (http://www.artist-embedded.org/) on Advanced Real-Time Systems. ARTIST1 provided the opportunity to test the concept of a two-level integration (within and between clusters) – four clusters in ARTIST2 originated as "actions" in ARTIST1. Building the ARTIST2 consortium and associated structure is the culmination of discussions and ambitions elaborated within ARTIST1.

ARTIST2 addresses the full range of challenges related to Embedded Systems Design, covering all aspects, ranging from theory through to applications.

1.2 Joint Programme of Activities

The Joint Programme of Activities is composed of 4 main branches:

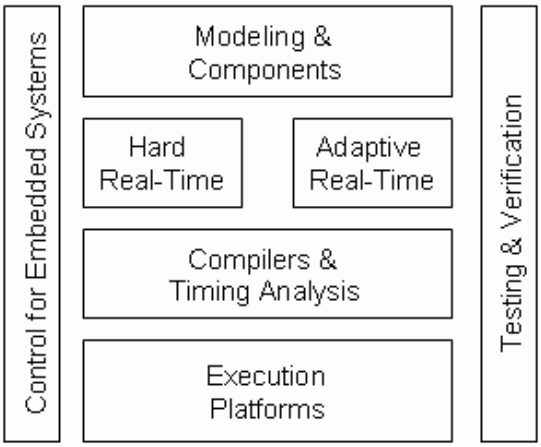
1.2.1 Joint Programme of Research Activities (JPRA)

The JPRA is composed of intra and inter-cluster research activities on cutting-edge topics in embedded systems design. While the main bulk of financing for these activities is taken up by outside programmes (Integrated Projects, National Programmes, Industrial Contracts, etc), the Artist2 NoE finances the extra burden due derived from integrating these into a single coherent research programme.

Thus, the essential ingredient within Artist2 is the JPRA, which motivates the participating research teams far more than the actual financing, which is tiny in comparison with the overall research aims. It is completed by the Joint Programme of Integrating Activities (JPIA), and the Joint Programme of Activities for Spreading Excellence (JPASE), and overseen by the Joint Programme of Management Activities (JPMA).

The structure of the research activities used in Year 1 reflects the following decomposition of the embedded systems design flow.

This design flow is composed of the following cooperating activities, starting with requirements capture and leading to implementation. These activities must be well coordinated, and supported by tools and methods to ensure satisfactory levels of productivity and quality. Accordingly, we have structured the area of embedded systems design into the following topics.



Modelling and Components: To express and validate system requirements, an abstract model of the system, representing the services provided, as well as system interaction with

its environment, needs to be built. Given the complexity of the systems to be modelled, a methodology and its accompanying technology are required allowing reuse of existing components.

Hard Real-time: This is one of the two main approaches to embedded systems design. It is applied to systems where temporal constraints are critical. This includes applications, which are often safety-critical, such as applications in space, automobile, rail transport, air traffic control, production control, etc. This is the oldest and most mature approach, and has led to significant research results in Europe, such as synchronous languages, fixed-priority scheduling, the time-triggered architectures, and these have been significantly transferred and developed in industry (for example, SCADE and Esterel to Airbus, and TTA to automotive).

Adaptive Real-time: This is a more recent approach to embedded systems design, where temporal constraints can be relaxed, which allows optimized use of resources. This includes applications – where managing the Quality of Service (QoS) is essential, such as telecommunication systems, multi-media, and wide-area networked applications. In this relatively new area, there is a recognized lack of design theory and tools.

Compilers and Timing Analysis: Once the application software has been developed, using the above, the system must be implemented on a given target platform. Compilation tools and their associated technologies play a fundamental role for automating this process. For the implementation of embedded systems, we need tools capable of combining platform independent software and a description of the target platform, to generate an executable code having the desired properties related to use of such resources as memory, power, energy, network bandwidth, and computation time). Resource-aware compilation requires the use of Timing Analysis tools to estimate the execution times of embedded software on a given platform.

Execution Platforms: This topic is strongly linked to the compilation and implementation of embedded systems. For a given application, it is important to have the technology, methods and tools to make rational choices about the platform and the design used, before proceeding to final implementation. Research in Execution Platforms targets the development of the theoretical and practical tools for modelling the dynamic behaviour of application software for a given platform. This is a new area of research, which will allow greater flexibility in designing optimal embedded systems.

Testing and Verification: This is transversal topic, which interacts with all the other topics in embedded systems design. It aims to ensure that the different design steps meet given properties, as well as the overall correctness of the implementation. This is a very active research topic, with results at different levels of the design process. The current challenge is in achieving on overall approach for testing and verification, focussing on two important aspects.

First is the Verification and Testing of real-time properties, to ensure that hard real-time constraints or quality of service constraints are met. Second is for Verification of Security Properties, where identification of gaps in security is desired.

Control for Embedded Systems: Embedded systems are deployed in the real world, and are often reactive to it. This interaction with the environment is intrinsic to the service provided. A large proportion of embedded systems can be considered to be controllers. On the other hand, most automated control applications will be implemented as embedded components. Thus, it is essential that work on joining control theory and embedded systems be included in the ARTIST2 NoE.

An overview of each intra-cluster ("Cluster Integration") and inter-cluster ("NoE Integration") research activity is provided in this document, and each platform has provided a deliverable that provides the detailed information.

1.2.2 Joint Programme of Integration Activities (JPIA)

The Joint Programme of Integrating Activities contains the technical but non-research activities that participate in the overall effort. As with the JPRA, the main financing for these technical activities is derived from other sources, and is small in comparison with the overall objectives.

The JPIA is composed of Platform Activities (roughly one for each cluster), and Mobility actions between partners – both core and affiliated partners.

Integration between research teams work to achieve critical mass in 2 important dimensions:

- Strong integration within selected topics by assembling the best European teams, to advance the state of the art in the topic.
- Integration between topics to achieve the multi-disciplinary excellence and skills required for the development of future embedded technologies.

Both types of integration are achieved through JPIA activities involving:

- Sharing Research Platforms, Tools, and Facilities
  State of the art research platforms, composed of competencies, resources, and tools targeting specific technical and scientific objectives around a chosen topic. These are made available to the R&D community for experimentation, demonstration, evaluation, and teaching.

  The ARTIST2 platforms integrate the results of long-term efforts, and are meant to be durable, evolving with the state of the art. The partners are committed to durability, and have invested significant resources into their development. The construction of ARTIST2 has provided the opportunity to assemble existing pieces into a rationally-structured set of platforms, covering the area of embedded systems design.

  Some of the ARTIST2 platforms have international visibility, and the ambition is for these to serve as world-wide references in their respective topics.

  - Staff Mobility and Exchanges
    Within Year 1, 40 different staff mobility actions have taken place between Artist2 partners (see section 6.1 of the "Spreading Excellence" deliverable).

    This is an essential activity for integration within the NoE, including mobility of students and/or researchers, between core teams, or between core teams and affiliated teams. To encourage exchange between core teams and affiliated industrial teams, specific scholarships co-funded with industry have been initiated in Year 1 and will be increased in Year 2:
  - Joint scholarships co-funded with industry.
  - Exchange of students and personnel within the consortium.
  - ARTIST2 Distinguished Lecturer Programme.
  - Support for relocating staff and teams (according to needs).

An overview of each platform is provided in this document, and each platform has provided a deliverable that provides the detailed information.

1.2.3 Joint Programme of Activities for Spreading Excellence (JPASE)

The achievements and results from the Joint Programme of Activities for Spreading Excellence (JPASE) is contained in a separate deliverable, entitled: “Spreading Excellence”.

1.3 Contact Details and Contractors Involved

1.3.1 Core Partners

For a complete description including web links, see:
http://www.artist-embedded.org/FP6/Partners/CorePartners/

Scientific Coordinator:	Technical Coordinator:
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Mailing address: Verimag Laboratory - Centre Equation - 2, ave de Vignate - 38610 Gières - France	

Partic N°	Participant name	Country
1	Caisse des Dépots et Consignations	France
2	University Joseph Fourrier / Verimag	France
3	RWTH Aachen	Germany
4	BRICS – Aalborg University	Denmark
5	AbsInt Angewandte Informatik GmbH	Germany
6	University of Aveiro	Portugal
7	Universidad de Cantabria	Spain
8	Commissariat à l'Énergie Atomique – Laboratoire LIST	France
9	Centre Fédéré en Vérification, Université de Liège	Belgium
10	Czech Technical University	Czech Republic
11	Dortmund University	Germany
12	Technical University of Denmark	Denmark
13	Swiss Federal Institute of Technology – Zurich	Switzerland
14	France Telecom R&D	France
15	Institut National de Recherche en Informatique et Automatique	France
16	Royal Institute of Technology	Sweden
17	Linköping University	Sweden
18	Centre National de la Recherche Scientifique / Laboratoire LSV	France
19	Lund University (Sweden)	Sweden
20	University of Mälardalen	Sweden
21	Kuratorium OFFIS e. V.	Germany
22	PARADES EEIG	Italy
23	University of Pavia	Italy
24	Universidad Politecnica de Madrid	Spain
25	Saarland University	Germany
26	ST Microelectronics – Central R&D	France
27	Technical University of Eindhoven	Netherlands
28	Technical University of Vienna	Austria
29	Technical University Braunschweig	Germany
30	University of Twente	Netherlands
31	University of Bologna	Italy
32	Uppsala University	Sweden
33	Universidad Polytecnica de Valencia	Spain
34	University of York	UK
35	Polytechnic Institute of Porto	Portugal

1.3.2 Affiliated Partners

Affiliated partners play a very strong role in the Spreading Excellence from the core partners to the research and industrial communities at large.

Affiliated partners generally play an active role in the research activities, either participating directly in research, or transferring the results directly to industry.

Each of the JPRA and JPIA activities' deliverables provides the list of the corresponding affiliated partners and roles.

Affiliated Industrial Partners

Christer Norström Göran Arinder	ABB	Peter Mårtensson	NOKIA Connecting People
Thomas Thurner Matthias Grochtmann	DaimlerChrysler	Sven Holme Sørensen	SIEMENS
Alain Ourghanlian	EDF Electricité de France	Roberto Zafalon	ST
Johan Eker	Ericsson	Dominique Potier	THALES
Philippe Baufreton	Hispano-Suiza Groupe SAFRAN	Fabian Wolf	VW
Vladimir Havlena	Honeywell	Magnus Hellring	VOLVO
Dr. Michael Winokur	IAI Israel Aircraft Industries	Jakob Axelsson	VOLVO for life

Affiliated SME Partners

Hans van Someren	ACE	Paolo Gai	Evidence
Alan Moore	ARTiSAN SOFTWARE	Carl von Platen	IAR SYSTEMS
Dr. Monica Donno	BullDAST Design Automation Services and Tools	António Garrido	LIFTECH LIFT TECHNOLOGIES
Joachim Stroop	dSPACE	Fernando Santos	Micro I/O www.microio.pt
Jan Lindblad	ENEA	Niklas Holsti	*Tidorum Ltd*
Bernard Dion	ESTEREL Technologies	Jean-Luc Lambert	VALIOSYS

Affiliated Academic Partners

RWTH Aachen
Prof. Stefan Kowalewski

University of the Balearic Islands
Julián Proenza

Humboldt University Berlin
Prof. Dr. Miroslaw Malek

Masaryk University Brno
Prof. Lubos Brim

Universidad Carlos III de Madrid
Prof. Dr. Marisol Garcia Valls

Universitat Politècnica de Catalunyaμ
Dr. Pau Martí Colom

University of Catania
Prof. Lucia Lo Bello

TU Darmstadt
Prof. Neeraj Suri

ENST

Royal Institute of Technology (KTH)
Prof. Axel Jantsch

Leiden University
Prof. Dr. Ed Deprettere

LIAFA - Université Paris 7 & CNRS
Prof. Ahmed Bouajjani

Politecnico di Milano
Prof. Donatella Sciuto

TU München
Prof. Dr. Dr. h.c. Manfred Broy

University of Nijmegen
Dr.ir. G.J. Tretmans

University of Salzburg
Prof., Head of the Computatonal Sciences Group
Christoph Kirsch

Democritus University of Thrace :
Laboratory of Electrical and Electronic

Laurent Pautet

University of Florence
Prof. Andrea Bondavalli

IMEC
Dr. Francky Catthoor

IRISA / INRIA
Dr. Isabelle Puaut

Katholieke Universiteit Leuven
Prof. Pierre Verbaeten,
Prof. Geert Deconinck

Materials Technology
Ass. Prof. Dimitrios Soudris

Timisoara - Institute e-Austria Timisoara
Dr. Marius Minea

Politecnico di Torino
Prof. Luciano Lavagno

Affiliated International Collaboration Partners

University of California at Berkeley
DARPA MoBIES, CHESS
Prof Ed Lee
Prof. Shankar Sastry

University of Michigan
Prof. Kang Shin

University of Notre Dame
Prof. Sharon Hu

University of Illinois at Urbana–Champaign
Prof. Lui Sha

Stanford University
Prof. Giovanni De Micheli

Tata Research Development & Design
Centre (TRDDC)
Mathai Joseph

National University of Singapore
Prof. P.S. Thiagarajan

UNU-IIST (United Nations University -
Institute for Software Technology)
Zhiming Liu

Vanderbilt University
Prof. Janos Sztipanovits

University of Virginia
Prof. John Stankovic
Prof. Tarek Abdelzaher

1.4 Vision and Work Performed

Artist2 finances durable integration between teams and not the concrete elements of the JPA which most often belong to other projects. These specific technical objectives may or may not be attained (this is the essence of research as opposed to development), but we feel that the main product of Artist2 is the emergence of a lasting European research community, that has a significantly enhanced capacity for preparing Europe's future.

The research is completed by work on the JPIA Platforms, which aim to transform research results in tangible tools and components.

We believe that the topics chosen provide a good coverage of the area, for embedded software and systems.

There are two other NoE's in the area: HiPEAC and Hycon, which are more focused on specific topics, and with which there is some overlap: the Control cluster with Hycon, and the Compilers and Timing Analysis cluster with HiPEAC. These NoEs do not have as broad integration aims as has Artist2.

Over the course of Year 1, we have not had the opportunity for significant interaction with these other NoEs, but this is something that we aim to develop starting in Year 2.

Our assessment of Artist2 progress on integration over Year 1 is very positive. Integration within some clusters that already existed in Artist FP5, such as Modelling and Components, and Hard Real Time, has achieved a significant degree of maturity. To pursue further integration, we propose the merger of these two clusters, into a single larger one, to be called "Real-Time Components"'. This new cluster inherits some activities from the previous ones, and also launches new ones.

Cluster-level integration in Execution Platforms cluster has also reached a high level of maturity, and plays an important role in pulling the NoE forward. It has a significant level of NoE-level integration with the Compilers and Timing Analysis cluster, as well as with the new Real-Time Components cluster. The Control for Embedded Systems cluster also plays an important role within the NoE, and has strong links with the Adaptive Real Time, and Real-Time Components clusters.

Cluster-level integration needs to mature for the Compilers and Timing Analysis, Testing and Verification, and the Adaptive Real-Time clusters. These clusters are doing excellent work, and there is attested collaboration between cluster members, but there is not a sufficiently strong overall vision for each. This situation can be explained by to the broadness of the overall scope of these clusters. For example, Compilers and Timing Analysis gathers together two distinct communities, that we feel should interact to a higher degree. Testing and Verification covers both real-time verification aspects and security. Adaptive Real-Time spans real-time programming languages, networks, scheduling, and quality of service. We propose to take another year to assess the degree of cluster-level integration that can be achieved.

The ARTIST2 NoE is a complex construction assembled from world-leading communities, teams, and individuals. This is certainly an asset, but also a source of complexity in management. Each team has two essential characteristics: world-class excellence and strong interaction with top industrial players. Artist2 partners play a leading role in the different communities in embedded systems design, and they advance the state of the art in each of these.

Over the course of the Year 1, Artist2 has been extremely active in submitting new proposals

It is difficult to abstract out a global synthesis of the overall technical achievements. This is due to the diversity and the low granularity of the actions to be covered (meetings, publications, attendance at workshops, visits, platforms). We should probably define a way for the partners to report more efficiently.

The following is a certainly non-exhaustive assessment of the work in the Joint Programme of Activities.

In the Joint Programme of Research Activities (JPRA), there has been significant progress in:

- Understanding timing and QoS aspects for components and component-based construction – through interaction in the Modelling and Components, Hard Real-Time, and Execution Platforms clusters. The results have been incorporated into proposals for standards, such as MARTES.
- Fundamental studies for the definition of a unifying framework encompassing heterogeneous execution, through interaction between Hard Real-Time, and Modelling and Components. The results have been extensively published in international conferences. They place Artist2 partners at the leading edge of the state of the art. They constitute the basis for new tool development and new projects such as the SPEEDS Integrated Project on Rich Components, recently accepted. It should be noted that INRIA, Verimag, PARADES and OFFIS are the driving partners in this project.
- Setting up an activity on diagnosis for embedded systems, which has major importance for industry. This work has been done in tight collaboration with industrial partners from automotive, and in particular the core members of the DECOS Integrated Project.
- Development of top world-class results on timing analysis, combining program flow analysis and architecture analysis. Integration of these results into the Timing Analysis Platform. We believe that we clearly have the strongest team world-wide in this area, in terms of both theory and application.
- Significant progress on the Compilers Platform, which integrates the commercially-available CoSy compiler, and leading-edge results on architecture-aware compilation.
- Breakthrough research on the trade-offs between predictability and efficiency in embedded systems. This has led to joint publications between the Compilers activities and Execution Platforms. The results propose methods for determining optimal design choices regarding predictability and efficiency. This work has also led to new project proposals, currently under evaluation.
- Breakthrough research on performance and evaluation of communication-centric systems, based on analytical approaches (network calculus, and max-plus algebra). Implementation of the results in tools by Braunschweig and ETHZ.
  The Execution Platforms cluster has a world-leading expertise in platform modelling, evaluation, analysis and optimisation. Their platform combines tools based on analytic models (SymTA/S, Real-Time Calculus) and executable models (SystemC components developed by the Denmark Technical University and the University of Bologna).
- Breakthrough research in low-power engineering. The University of Bologna is one of the leading centres in the area.

- The Control for Embedded Systems cluster has done excellent work in transferring results to be taken up in Adaptive Real Time and Modelling and Components. There has been very strong interaction with the Adaptive Real Time cluster on the application of control-based techniques in adaptive scheduling.
- Adapting to embedded systems and pushing to the limits available testing and verification technology (UPPAAL). The focus is on industrial application-driven work around the platform, and carried out in tight collaboration with industrial partners.

In the Joint Programme of Integration Activities (JPIA) Platforms, there has been progress in the following areas:

- Setting up a state of the art common software infrastructure for embedded systems, consisting of the SHaRK kernel, open for experimentation to Artist2 partners.
- In the Modelling and Components Platform, we have defined a common architecture for the platform and tools to be integrated. A first integration will be achieved in the course of the next 18 months.
- For the two Compilers and Timing Analysis platforms, there has been significant progress in integrating innovative research results. The strong involvement of Ace and Tidorum shows the relevance of the work.
- There has been a very significant integration of world-class tools in the Execution Platform cluster's System Modelling Infrastructure. We note the strong integration between the event-stream analysis which is at the basis for SymTA/S and the real-time calculus by ETHZ. There is also a strong integration with the work on SystemC-based clock-accurate simulation.
- The main progress in the T&V Platform has been the improvements made to the UPAAL tool, to support probabilistic analysis and optimal scheduling and planning problems.
- In the Control platform, there has been significant developments on individual tools, and an overall plan for integration has been defined.

In the Joint Programme of Activities for Spreading Excellence (JPASE), there has been progress in the following areas:

- The NoE has actively associated to its technical work approximately 50 affiliated partners, from academia, industry and SMEs. This cooperation extends to joint projects, and events.
- The NoE has sponsored the main scientific events in the area, including the Embedded Systems Week, organised in New Jersey, in October of this year. It also plays a leading role in their organization of conferences such as DATE, EmSoft and CODES/ISS, and actively promotes structuring the scientific events' landscape.
  Our sponsoring policy aims specifically at enforcing integration of existing scientific events in the area. This is sought in particular through the creation of Embedded Systems Week, in which we have played a crucial role. The ambition is that Embedded Systems Week federates an increasingly large number of existing scientific events within a single week.
- The NoE has been very successful in organizing high-level events for International Collaboration, in close interaction with the NSF. This is recognized through the

funding by the NSF of specific collaborative actions between Artist partners and NSF projects.

- The NoE participants have an impressive publication record. Furthermore, as a result of the integration achieved via the NoE, over 50 joint papers have been published in international conferences as well as 7 books. These are listed in section 10.1 of the deliverable on “Spreading Excellence”.
- The NoE has a strong impact for structuring R&D in Europe, through its actions for launching Integrated Projects, such as DECOS, ASSERT and more recently SPEEDS, as well as through its contribution to the definition of the Strategic Research Agenda of the ARTEMIS platform.
- The NoE sets up or participates in the main leading events in the area (see the deliverable on Spreading Excellence). The materials presented in these events are regularly made available to the public through the Artist web site. Furthermore, in Year2 we will set up a repository for courseware, also made available to the public.

The NoE still needs to define and implement a knowledge dissemination strategy through the web. This is in progress.

In the Joint Programme of Management Activities (JPMA), we have defined an effective and readable governance structure. All the bodies have proven to be effective. Nevertheless, the interaction with the Industrial Advisory Board needs refinement.

Within the consortium, we should refine the reporting procedures, and strengthen monitoring.

The NoE is moving forward with plans for setting up a sustainable structure for continuing interaction between research and industry, after the end of the NoE contract.

1.5 End Results

At the end of the NoE, we expect to achieve a more integrated community, in which the fragmentation by topics and communities will fade. This will be implemented through the disappearance of the currently existing clusters. This will take time, to create convergence of interests, and allow the emergence of recognized leaders. This will also require progressive changes to the consortium, by including new members and removing others.

We are currently promoting the emergence of Centres of Excellence in the area. For this, we are actively monitoring the evolution at national and European level, and positioning the NoE so as to be in line with this evolution.

A complete list of the detailed expected end results is provided in the Project Timetable / Milestones available in the overall Periodic Activity Report.

Network of Excellence

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2. Periodic Activity Report

2.1 Project Objectives and Major Achievements

A detailed description of objectives, and particularly the main aims for integration, is provided for each cluster in the sections labelled « State of Integration in Europe ».

2.1.1 Historical Perspective

Before setting up the Artist2 NoE, a subset of the current consortium implemented an FP5 Accompanying Measure, whose objectives were to:

- Coordinate the R&D effort in the area of Advanced Real-time Systems
- Improve awareness of academics and industry in the area
- Define innovative and relevant work directions

This was achieved through work along 3 axes:

- Roadmaps for selected actions: (Hard Real Time, Component-based Design, Adaptive Real Time, Execution Platforms)
- International Collaboration
- Education

Information about these results is publicly available:

http://www.artist-embedded.org/Roadmaps/

2.1.2 Current Relation to the State of the Art

The NoE's current relation to the State of the Art is provided in the deliverables for this review:

- This document:
  sections "Description of the Area", for each Artist2 cluster.
- Each of the sections called "Brief Description of the State of the Art", provided within each of the 24 activity deliverables.

2.2 Workpackage progress of the period

Given the size of this NoE, and the structuring by clusters, this information is provided in detail in sections 3-10 of this document.

2.3 Deliverables for the Reporting Period

The due date for all the Year1 deliverables was August 31st, 2005.
The delivery dates are provided per deliverable below.

ref	Title	Cluster		Partner
Management				
1-1	Deliv-JPMA-Y1 Year 1 Periodic Management Report *November 15th, 2005,* *Revised December 16th, 2005*	JPMA		1 CDC
1-2	Deliv-JPMA-Y1-b Year 1 Activity Report *October 3rd, 2005,* *revised January 18th, 2006*	JPMA / JPIA		2 UJF/verimag
4	Deliv-JPASE-Y1 Report on Spreading Excellence Deliv-JPIA-b-Y1 (fused) Report on Staff Mobility and Exchange *October 3rd, 2005* *revised January 18th, 2006*	JPASE		2 UJF/ VERIMAG
Components & Modelling				
2-1	Deliv-JPIA-a-Components-Y1 Report on Components Platform for Component Modelling and Verification *Sept 26th, 2005* *revised January 19th, 2006*	JPIA - Platform	Components & Modelling	2 UJF/ VERIMAG
10	Deliv-JPRA-Cluster Integration – Modelling and Components – a - Y1 Report on Component Modelling and Composition *Sept 26th, 2005* *revised January 19th, 2006*	JPRA - Cluster Integration	Components & Modelling	32 Uppsala
11	Deliv-JPRA-Cluster Integration – Modelling and Components – b - Y1 Report on Development of UML for Real-time Embedded Systems *Sept 26th, 2005*	JPRA - Cluster Integration	Components & Modelling	8 CEA
Hard Real-Time				
5	Deliv-JPRA-NoE Integration-a-Y1 Report on Semantic Framework for Hard Real-Time Design Flow *Sept 28th, 2005* *Revised December 15th, 2005*	JPRA - NoE Integration	**Hard Real-Time** Adaptive Real-Time Control for Embedded Systems	15 INRIA

6	Deliv-JPRA-NoE Integration-b-Y1 Report on Merging the Event-triggered and Time-triggered Paradigms *Sept 28th, 2005* *Revised December 15th, 2005* Annex 1 - June 27-28 2005 meeting minutes Annex 2 - January 12-14 2005 meeting minutes	JPRA - NoE Integration	**Hard Real-Time** Adaptive Real-time Execution Platforms	1 VERIMAG
12	Deliv-JPRA-Cluster Integration – Hard Real Time - Y1 Report on Diagnosis in Distributed Hard Real-Time Systems *Sept 28th, 2005* *Revised December 15th, 2005* Annex 1 - Dec 20-21 2004 meeting minutes Annex 2 - May 2-3 2005 meeting minutes	JPRA - Cluster Integration	Hard Real Time	28 TU Vienna

Adaptive Real Time

2-2	Deliv-JPIA-a-ART-Y1 Report on ART Platform: A Common Infrastructure for Adaptive Real-time Systems *Sept 26th, 2005* *Revised December 15th, 2005* Annex 1: Report on the SHARK Workshop	JPIA - Platform	Adaptive Real Time	2 UJF/ VERIMAG
8	Deliv-JPRA-NoE Integration-d-Y1 Report on QoS aware Components *Sept 28th, 2005*	JPRA - NoE Integration	**Adaptive Real-Time** Modelling and Components	24 UP Madrid
13	Deliv-JPRA-Cluster Integration – Adaptive Real Time – a – Y1 Report on Flexible Scheduling Technologies *Sept 26th, 2005* *Revised December 15th, 2005*	JPRA - Cluster Integration	Adaptive Real Time	23 Pavia
14	Deliv-JPRA-Cluster Integration – Adaptive Real Time – b – Y1 Report on Adaptive Resource Management for Consumer Electronics *Sept 28th, 2005* *Revised December 15th, 2005*	JPRA - Cluster Integration	Adaptive Real Time	20 Mälardalen

Compilers & Timing Analysis

2-3	Deliv-JPIA-a3-Y1 Report on Timing Analysis Platform *Sept 26th, 2005* *Revised January 18th, 2005*	JPIA - Platform	Compilers & Timing Analysis	2 UJF/ VERIMAG
2-4	Deliv-JPIA-a4-Y1 Report on Compilers Platform *Sept 28th, 2005* *Revised December 15th, 2005*	JPIA - Platform	Compilers & Timing Analysis	2 UJF/ VERIMAG
15	Deliv-JPRA-Cluster Integration – Compilers and Timing Analysis – Y1 Report on Architecture-aware compilation *Sept 28th, 2005* *Revised December 15th, 2005*	JPRA - Cluster Integration	Compilers and Timing Analysis	3 RWTH Aachen

Execution Platforms

2-5	Deliv-JPIA-a-EP-Y1 Report on EP Platform: System Modelling Infrastructure *Sept 26th, 2005*	JPIA - Platform	Execution Platforms	2 UJF/ VERIMAG
9	Deliv-JPRA-NoE Integration-e-Y1 Report on Resource-aware Design *Sept 26th, 2005* *Revised December 15th, 2005*	JPRA - NoE Integration	**Execution Platforms** Compilers and Timing Analysis	31 Bologna
16	Deliv-JPRA-Cluster Integration – Execution Platforms – a – Y1 Communication-centric systems *Sept 26th, 2005*	JPRA - Cluster Integration	Execution Platforms	29 TUBS
17	Deliv-JPRA-Cluster Integration – Execution Platforms –b – Y1 Design for low power *Sept 26th, 2005* *Revised December 15th, 2005*	JPRA - Cluster Integration	Execution Platforms	31 Bologna

Testing and Verification

2-7	Deliv-JPIA-a-TV-Y1 Report on T&V Platform for Embedded Systems *Sept 30th, 2005* *Revised December 15th, 2005*	JPIA - Platform	Testing and Verification	2 UJF/ VERIMAG
20	Deliv-JPRA-Cluster Integration – Testing and Verification – a – Y1 Quantitative Testing and Verification	JPRA - Cluster Integration	Testing and Verification	30 Twente

	Sept 26th, 2005 *Revised December 15th, 2005*			
21	Deliv-JPRA-Cluster Integration – Testing and Verification – b – Y1 Verification of Security Properties *Sept 26th, 2005* *Revised January 18th, 2006* *Revised December 15th, 2005*	JPRA - Cluster Integration	Testing and Verification	1 UJF/VERIMAG
Control for Embedded Systems				
2-6	Deliv-JPIA-a-Control-Y1 Report on Control Platform: Design Tools for Embedded Control *Sept 26th, 2005*	JPIA - Platform	Control for Embedded Systems	2 UJF/ VERIMAG
7	Deliv-JPRA-NoE Integration-c-Y1 Report on Adaptive Real-time, HRT and Control *Sept 26th, 2005*	JPRA - NoE Integration	**Control for Embedded Systems** Hard Real-Time Adaptive Real-Time	19 Lund
18	Deliv-JPRA-Cluster Integration – Control for Embedded – a – Y1 Control in real-time computing *Sept 26th, 2005* Annex 1: Roadmap on Control of Real-Time Computing Systems Annex 2: Strategic Research Agenda on Control for Computing Systems	JPRA - Cluster Integration	Control for Embedded Systems	19 Lund
19	Deliv-JPRA-Cluster Integration – Control for Embedded – b – Y1 Real-time techniques in control system implementations *Sept 26th, 2005* Annex 1: Roadmap on Real-Time Techniques in Control System Implementation Annex 2: Report on the Valencia Graduate Course on Embedded Control	JPRA - Cluster Integration	Control for Embedded Systems	33 UPVLC

2.4 Consortium Management

2.4.1 Governance Structure

Scientific Coordinator:	Technical Coordinator:
Joseph Sifakis	Bruno Bouyssounouse
Tel: +33 4 56 52 03 51	Tel: +33 4 56 52 03 68
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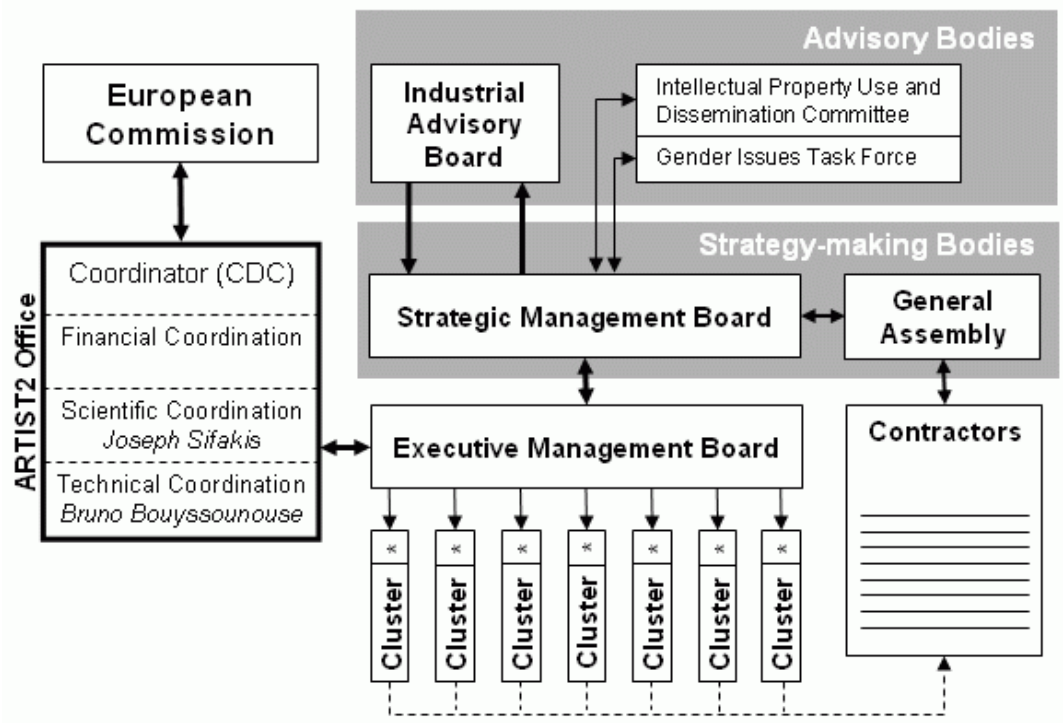
The methodology adopted for achieving the JPA objectives follows the same lines as for managing a laboratory. The activities, their objectives, their technical description, the partners involved, their roles, and the resources available have been clearly defined in the initial Description of Work, and updated in the deliverables. This will be monitored and guided by a tight and rigorous management, as defined in the diagram below:



The main governance bodies are:

The **General Assembly** is composed of one representative per core partner. It is convened at the beginning of the project and meets once per year. It is chaired by the Scientific Manager.

The **Strategic Management Board** is initially composed of the NoE cluster leaders, and a representative of the Coordinator – who attends, with no voting rights. It is chaired by the Scientific Manager, assisted by the Technical Manager. It meets at least once per year –

close to the General Assembly meeting. Its members are elected by the General Assembly every two years, according to modalities to be determined in the Consortium Agreement.

The **Cluster Leaders** (who compose the Executive Management Board) are responsible for the overall coordination of the activities led by their cluster. A cluster functions as a virtual team – with a degree of autonomy for defining its internal meetings and day to day management.

2.4.2 Partners Involved

This is provided in the publishable Executive Summary, in the first part of this document.

2.4.3 Consortium Management Tasks

Consortium management tasks and their achievement; problems which have occurred and how they were solved

2.4.4 Contractors

At the end of Year 1, we have made the following changes to the consortium:

- Merged the clusters “Modelling and Components” with “Hard Real-Time”, to form the new cluster “Real-Time Components”, led by Albert Benveniste (INRIA), who previously led the “Hard Real-Time” cluster.
- Added 3 new partners, who were already active in the JPRA and JPIA as affiliated partners:
    - EPFL (Tom Henzinger), active in:
        - Cluster: “Real Time Components”
          Activity: “NoE Integration - Forums with specific industrial sectors”
          Activity: “NoE Integration - Seeding New Work Directions”
        - Cluster: “Execution Platforms” cluster
          Activity: “NoE Integration Resource-aware Design”
        - Cluster: “Testing and Verification”
          Activity: “NoE Integration - Quantitative Testing and Verification”
    - In the Compilers and Timing Analysis cluster, two affiliated partners are joining as full core partners: Tidorum, an SME, and Ace, a software tool vendor.
    - For 2 partners, the main Artist2 researcher transferred to a different university. For this reason, we are replacing partner Malardalen with Kaiserslautern, and Pavia with Scuola Sant’Anna in Pisa. Malardalen will stay on as a core partner but with limited resources, and Pavia will continue as an affiliated partner.

2.4.5 Project Timetable

The JPA is organized into activities. The activities should not be considered as tasks of a workprogramme, with begin/end and synchronisation dependencies. Of course, the detailed description of an activity could be decomposed into sub-tasks and intermediate milestones, but this would imply a granularity that is too fine for research activities.

The inter-dependencies between activities are complex and rich, and will evolve dynamically. The work plan for the activities is provided in the 18 month workpackage descriptions.

The major milestones per activity are described below, updated at the start of Year 2:

Cluster: Real-Time Components

Albert Benveniste (INRIA)

This is a new cluster led by Albert Benveniste (INRIA), which takes up some of the activities previously in the clusters halted at the end of Year 1: "Hard Real Time" and "Modelling and Components".

The following activities from the two previous clusters will continue in the new cluster:

- WP1: Platform for Component Modelling and Verification
- WP4 Cluster Integration: Development of UML for Real-time Embedded Systems

The following activities are new starting in Year 2, taking up many of the essential elements of the activities "Semantic Framework for Hard Real-Time Design Flow" and "Merging the Event-triggered and Time-triggered Paradigms", and "Diagnosis in Distributed Hard Real-time Systems".

- WP4 NoE Integration: Forums with Specific Industrial Sectors
- WP4 NoE Integration: Forums with Specific Industrial Sectors

The following activities are halted at the end of Year 1:

- WP4 Cluster Integration: Component Modelling and Composition
- WP3 NoE Integration: Semantic Framework for Hard Real-Time Design Flow (see the new activities above)
- WP3 NoE Integration: Merging the Event-triggered and Time-triggered Paradigms (see the new activities above)
- WP5 Cluster Integration: Diagnosis in Distributed Hard Real-time Systems (see the new activities above)

The milestones for the activities in Year 2 are as follows:

- **WP1: Platform for Component Modelling and Verification**
  Previously in "Modelling and Components".
  Susanne Graf (Verimag)
  - (achieved) Year1: Initial definitions of modules to assemble in the platform
  - Year2: Version 1 of the platform: integrate and unify the existing partners' UML extensions for real time, as well as the definition of a kernel target language, suitable for analyzing semantic issues.
  - Year4: Final integration of the results of the related Joint Research Activities.
- **WP4 Cluster Integration: Development of UML for Real-time Embedded Systems**
  Previously in "Modelling and Components"
  Francois Terrier (CEA)

- Annual Y1-3 milestones: Continued work with the OMG for advancing the UML standard, for real-time systems, leading to the year4 milestone.
- Year4: Work should promote convergence of different views on how UML should be defined and be used for real-time system development, which will induce greater interaction between tool providers, developers, and researchers in the area.

- **WP4 NoE Integration: Forums with Specific Industrial Sectors**
  New activity started in Year 2.
  Albert Benveniste (INRIA)
  - Year2: organize a forum with AUTOSAR industrial actors on the topic of design methods and tools for heterogeneous large embedded systems; draw resulting issues and research questions. Co-organizers Werner Damm (OFFIS) and Albert Benveniste (INRIA)
  - Year3: organize a forum with aeronautics sector; draw resulting issues and research questions on the topic of design methods and tools for heterogeneous large embedded systems; plan a third forum with another sector, not fixed yet.
  - Year4: organize the third forum; draw resulting industrial issues and research questions on the topic of design methods and tools for heterogeneous large embedded systems; deliver a summary of findings and recommendations for research on the topic of design methods and tools for heterogeneous large embedded systems.
- **WP4 NoE Integration: Seeding New Work Directions**
  New activity started in Year 2.
  Albert Benveniste (INRIA) and Alberto Sangiovanni (PARADES)
  - Year2: organize a *research seeding* meeting on the topic “Classification and study of Models of Computation and Communication (MoCC), and resulting Conceptual Model for Embedded Systems”. Co-organizers Paul Caspi (Verimag) and Hermann Kopetz (TU Vienna)
  - Year3: organize a *seeding research* meeting on a topic not fixed yet, but related to design methods and tools for heterogeneous large embedded systems.
  - Year4: organize a *seeding research* meeting on a topic not fixed yet, but related to design methods and tools for heterogeneous large embedded systems. Write concluding report on the findings of this JPRA.

Cluster: Adaptive Real-Time
Giorgio Buttazzo (Pisa)

- **WP1 Platform: A common infrastructure for adaptive Real-time Systems**
  Giorgio Buttazzo (Univ. of Pavia)
  - (achieved) Year1: Initial definition of the operating system and network features
  - Year2: Deploy a working platform for experimental RTOS and network development
  - Year3: Participate in the evolution of RTOS and networking standards, by developing new concepts.

- **WP3 NoE Integration: QoS aware Components**
  Alejandro Alonso (UP Madrid)
    - Year2: Definition of notations for describing QoS properties of component interfaces and precise techniques for composing them.
    - Year4: Development of holistic frameworks and models for QoS management that show how to combine features of component models, component frameworks, middleware infrastructure, OS and Kernel support, and networking.
- **WP6 Cluster Integration: Flexible Scheduling Technologies**
  Giorgio Buttazzo (Pavia)
    - (achieved) Year1: Preliminary work on the integration of diverse scheduling schemes
    - Year2: Demonstrate the combination of specific scheduling schemes applied both to CPU as well as to the network, to suit diverse application requirements in the same system
    - Year4: Provide a framework providing for the seamless integration of flexible scheduling schemes, allowing the choice of appropriate scheduling methods for individual activities in a system or messages on the network.
- **WP6 Cluster Integration: Adaptive Resource Management for Consumer Electronics**
  Gerhard Fohler (Mälardalen University)
    - (achieved) Year1: Identify case studies, perform preliminary assessment
    - Year2: Define a set of case studies and from them deduce the QoS requirements and their mapping into operational parameters of the computing and communication infrastructures.
    - Year3: Expend these into a meaningful set of requirements of dynamic application domains (for instance, multimedia) that allow the creation of global mechanisms for resource management.
    - Year4: Integration of the application adaptation processes into a general QoS resource management structure.

Cluster: Compilers and Timing Analysis
Reinhard Wilhelm (Saarland)

- **WP1: Timing - Analysis Platform**
  Reinhard Wilhelm (Saarland University)
    - Year2: Standard tool architecture and interfaces
    - Year3: Initial integration of existing components
    - Year4: Version 2 integration of existing components
- **WP1: Compilers Platform**
  Rainer Leupers (RWTH Aachen)
    - (achieved) Year1: Initial definition of the year1 compiler platform and synthesis tools
    - Year2: Initial implementation of the platform
    - Year4: Version 2 of the platform

- **WP7 Cluster Integration: Architecture-aware compilation**
  Rainer Leupers (RWTH Aachen)
    - (achieved) Year1: Loop-splitting algorithms of Dortmund University will be integrated into the IMEC tool flow.
    - Year2: Integrate the Program-Analyzer Generator (PAG) into the Compilers Platform
    - Year3 Integrate further innovative functionalities into the Compilers Platform
    - Year4: Released version of the Compilers Platform

Cluster: Execution Platforms
Lothar Thiele (ETHZ)

- **WP1 Platform: System Modelling Infrastructure**
  Jan Madsen (Technical University of Denmark)
    - Year2: Initial definition of the modelling platform
    - Year3: Version 1 of the system modelling platform implementation
- **WP3 NoE Integration: Resource-aware Design**
  Luca Benini (University of Bologna) and Peter Marwedel (University Dortmund)
    - Year2: A set of tools that can interact and work together and demonstrate the achievable optimizations on a particular hardware platform
    - Year4: A methodology for the design of predictable embedded systems
- **WP8 Cluster Integration: Communication-centric systems**
  Rolf Ernst (TU Braunschweig)
    - (achieved) Year1: Assess the state-of-the-art in models that take into consideration the particularities of various quasi-standard communication protocols during system analysis and scheduling
    - Year2: New best-case/worst-case models for hard real-time systems and at combined statistical and interval models for QoS applications in multi-media. These models may combine communication and computation, different models of computation, event models and scheduling policies
    - Year3: Analytic methods to estimate system properties
    - Year4: Refinement and dissemination of these methods
- **WP8 Cluster Integration: Design for low power**
  Luca Benini (University of Bologna)
    - Year2: Component models will be investigated that model power dissipation of system components
    - Year4: Integration of the different levels of abstraction - from scheduling via operating systems to system design - participating in low power design

Cluster: Control for Embedded Systems
Karl-Erik Arzen (Lund)

- **WP1 Platform: Design Tools for Embedded Control**
  Karl-Erik Årzén (Lund University)

- (achieved) Year1: Generate a survey of existing co-design tools for control, computing and communication
- Year2: Identification of which of the existing tools that will be included in the platform, and specification of their interfaces
- Year3: Develop the necessary interfaces that allow the individual tools to be used together
- Year4: Usage of the tools in new co-design based research activities, adoption in industrial case studies.

- **WP3 NoE Integration: Adaptive Real-time, HRT and Control**
  Karl-Erik Årzén (Lund University)
  - (achieved) Year1: Setting the technical background and assess the needs
  - Year2: Demonstrate that applications of diverse type can be specified in terms of resource-aware tasks
  - Year3: Demonstrate that scheduling algorithms can be made adaptive by means of control schemes
  - Year4: Recommendations for new computational models and methods based on well established control theory for resource-constrained real-time applications.
- **WP9 Cluster Integration: Control in real-time computing**
  Karl-Erik Årzén (Lund University)
  - (achieved) Year1: Roadmap describing the current state-of-the-art and the important research issues
  - Year2-4: Progress made on the fundamental underlying issues: decreased requirements on prior knowledge about resource utilization, increased possibilities to use COTS implementation platforms, and enhanced robustness towards load variations
- **WP9 Cluster Integration: Real-time techniques in control system implementations**
  Alfons Crespo (UPVLC)
  - (achieved) Year1: Roadmap describing the current state-of-the-art and the important research issues
  - Year2: A common framework of the control parameters that can be influenced by an embedded control system implementation and the real time operating systems criteria that can be adjusted to increase the robustness of the control system.
  - Year3-4: A common framework model in order to facilitate the control and computing co-design

Cluster: Testing and Verification
Kim Larsen (Aalborg)

- **WP1 Platform: Testing and Verification Platform for Embedded Systems**
  Kim G. Larsen (BRICS/Aalborg)
    - Year2: A server on which the main testing and verification tools developed and used by the participants will be installed and configured.
      Design of a coordination layer for parallel and distributed model checking,
      Design of a GRID infrastructure, links to mature model checking tools via the Yahoda homepage.
    - Year4: Integration of results from the related Joint Research Activities
- **WP10 Cluster Integration: Quantitative Testing and Verification**
  Ed Brinksma (University of Twente)
    - (achieved) Year1: Initial results for testing and verification with emphasis on quantitative aspects
    - Year2: Develop theory, methods and tools for testing and verification of embedded systems with emphasis on quantitative aspects (e.g. real-time and stochastic phenomena) that are of particular importance for the correctness of embedded systems.
      Further work on robustness, metrics and abstraction. Also repository and classification of major case studies.
    - Year3: Existing verification tools and test generation tools are more strongly connected, including stronger links between academic and industrial tools
    - Year4: Emergence of a range of new powerful debugging and analysis based on various combinations of testing and verification techniques.
- **WP10 Cluster Integration: Verification of Security Properties**
  Yassine Lakhnech (Verimag)
    - (achieved) Year1: Define a reference model for security protocols
    - Year2: prototypes capable of performing automatic analysis of security protocols
    - Year4: Contributions to standards for security protocols

Non-cluster Activities

JPIA-Staff Mobility and Exchanges (WP1)

- **WP1: Staff Mobility and Exchanges**
  All partners
    - Each year, we expect to have a significant number of students and staff members exchanged between the partners, on the topics in the Joint Programme of Research Activities

JPASE-Education (WP2)

- **WP2: Courseware**
  At the end of Year 1, we feel that it is not feasible to provide a satisfactory response to this objective. This would mean providing a complete and structured single viewpoint for education in the area. We have overestimated the maturity and readiness of the main academic players for adopting a

common view and set of priorities in education.

Instead, we propose to provide course materials (slides, references, links to websites) through our web pages.

- **WP2: Support for Summer Schools**
  Bruno Bouyssounouse (Verimag)
  - Each year, we plan to either provide support to, or organise at least one International School focusing on selected topics in Embedded Systems Design

JPASE – Dissemination and Communication (WP2)

- **WP2: Conferences, workshops, seminars, publication in journals**
  Bruno Bouyssounouse (Verimag)
  - Each year, we will organise, participate in, and provide support to a number of conferences, workshops and seminars. The ARTIST2 researchers will publish research results widely.

JPASE – Industrial Liaison (WP2)

- **WP2: Industrial Liaison**
  Bruno Bouyssounouse (Verimag)
  - Year1-4: Actions for structuring industrial relations between ARTIST2 and European R&D, through involvement in Integrated Projects and in the governance of the ARTEMIS European Technology Platform.

JPASE – International Collaboration (WP2)

- **WP2: International Collaboration**
  Bruno Bouyssounouse (Verimag)
  Annual International Collaboration events, continuing and expanding on the annual events organised by the ARTIST FP5 Accompanying Measure. The annual events are each focused on a specific topic, and include presentations from leading figures in Europe, the USA, and Asia.

2.4.6 Comments and Information on Coordination Activities

After 1 year, we can identify a problem with reporting and monitoring. We still need to define the procedures to allow efficient reporting and monitoring.

As coordinators, we will continue to propose and implement changes in the structure of the consortium, to accompany and guide advancing integration.

2.4.7 Other Issues

None

2.4.8 Plan for using and disseminating the knowledge

This is described in detail within the “Spreading Excellence” deliverable, in section: “1.2.5 Spreading Excellence Actions Planned for Year 2”.

3. Cluster: Modelling and Components

Contributor: Prof. Bengt Jonsson - Uppsala

3.1 Description of the Area

Component-Based Software Development (CBSD) is expected to increase software productivity, by reducing the amount of effort needed to develop, update, and maintain systems. It gives structure to system design and system development, and allows reuse of development effort by allowing components to be re-used across products and in the longer term by paving the way for a market for software components. CBSD has become widespread in general program development. Adoption for embedded real-time systems is significantly slower. Major reasons are that

- real-time systems must satisfy requirements of timeliness, quality-of-service, predictability, that they are often safety-critical, and that they must obey stringent constraints on resource usage (memory, processing power, communication). Existing wide-spread component technologies do not in general address these desiderata.
- There is a lack of widely adopted standards for component technology. A complicating factor is that different industrial sectors have different priorities concerning the main characteristics offered by such a standard.

3.1.1 Main Research Trends

Major research directions address the applicability of CBSD for embedded systems

- **Specification and Determination of extra-functional properties** of components, in particular timing, performance, QoS, memory, power and other resource consumption. Particular problems include to capture the dependency on the characteristics of the underlying platform in a modular way, and to specify many different extra-functional properties simultaneously in a both modular and consistent manner.
- **Handling interference between components.** Components have individual requirements that can be violated when composed and deployed with other components. Techniques are needed that ensure that component features do not interfere with those of other components. Such interferences can be very subtle. An important specific scenario where unexpected interferences may occur is when several components, each implementing a piece of functionality, are mapped onto one small hardware unit.
- **Handling heterogeneous system descriptions.** The interaction between components of an embedded system is typically much more extensive than between components in the business processing domain, where, e.g., interaction via method calls can suffice. Components can execute and communicate synchronously or asynchronously, sometimes using different timing models. It is not well understood how to understand systems whose components execute and communicate using different paradigms.
- **Tool support** for different development activities, including tools to model systems, and to analyse and predict system properties.
- **Standards** and **implementations of component frameworks** must be developed that suit different embedded systems application domains. A single technology will not suit all the various domains, and in fact domain specific standardization efforts are underway in several industrial sectors. A standard should preferably be independent of a particular platform or vendor, to avoid future dominance by a single platform provider.

3.1.2 Industrial Applications

CBSD technology is an important driver in all sectors of embedded systems industry. As an example, the automotive industry is working hard to develop standards for component composition mechanisms, component and system modelling, and software architectures, e.g., in the AUTOSAR project. Analogous efforts are underway in other sectors.

3.2 State of Integration in Europe

3.2.1 European Research Teams

Modelling Component based systems in general software engineering is a vast discipline with many European teams having made important contributions, e.g., the team by Bertrand Meyer, ETHZ. For embedded systems, where focus is also placed on non-functional aspects of systems, European teams work along several different directions. One community are developing techniques and implemented software tools to model, specify, and reason about timing and QoS properties. Teams that work on precise approaches for handling timing properties include ARTIST2 teams at Aalborg, EPFL, INRIA, Munich, OFFIS, Twente, Timisoara, Uppsala, VERIMAG, and others (it is not possible to include a complete list). Another direction of work concerns the integration of techniques for handling non-functional properties into existing general software engineering paradigms, based, e.g., on UML, to support a model driven development process. Topics studies include the development of notations that are compatible with UML, to develop techniques for monitoring contracts, and handling violations of guaranteed QoS properties. ARTIST2 teams prominent in these topics include CEA, MdH, OFFIS; TU/E, IRISA, VERIMAG (again, a complete list is not possible to pursue).

In general, there are a number of existing approaches and tools developed by different teams in all of the above aspects. Also, the problem of specifying and reasoning about QoS properties of embedded systems recur in many contexts in embedded system design, e.g., in solving scheduling problems, hardware modelling, etc. It is therefore of interest to avoid duplication of work and distil essential principles for the treatment of timing and other QoS properties in component-based systems.

Another grand challenge for embedded system design is the development of theories and tools for design of heterogeneous systems. There are some tool-based approaches, e.g., by PARADES, and as well proposals for encompassing theories, by INRIA, PARADES, VERIMAG and others.

3.2.2 Interaction of the Cluster with other Communities

Interaction with the OMG Standardization community through the work on standardization of RTES aspects in the context of UML.

Interaction with the Verification and analysis community, in order to connect modelling tools to analysis tools.

Interaction with the RTOS community, in order to adapt support from middleware layers to adaptive handling of QoS properties.

Interaction with other clusters in ARTIST2, for which compositional handling of timing properties is a central problem such is the Adaptive time and the Hard Real-time cluster

3.2.3 Main Aims for Integration through Artist2

To develop and disseminate a more coherent view on handling timing and QoS properties in component-based systems for RTES,

To contribute such a view in UML standardization of RTES aspects.

To synchronize European efforts on modelling and development tools.

3.3 Overall Assessment and Vision for the Cluster

3.3.1 Assessment

Here is a preliminary assessment for the different work directions.

Handling of timing and QoS for RTES. A result of ARTIST2 meetings, it has been recognized that this topic is central in many different aspects of RTES development. Several connections between different communities have been established. Some examples include:

- The work in Execution Platforms has been influenced by the concept of Assumed and Guaranteed properties of the Components cluster, and resulted in very interesting research work. This line of work will continue, and has a potential to merge several different technical directions in the area.
- A catalogue of different QoS properties is being compiled.
- The relationship between existing approaches to design of heterogeneous component-based systems has been clarified in seminars, and the generated understanding will impact research work of attendants.

It is very important to continue this line of effort to work on central problems in component-based design, and establish bridges with different communities.

Platform for Modelling and Components. The work on bridging tools has progressed by collaboration within several other projects. Within ARTIST2, more progress can be achieved by collaboration with other communities (clusters). It may be a good idea to bring this activity in more explicit contact with other tool building activities of ARTIST2.

Standardization. Standardization is an important form of dissemination of the work in ARTIST2. The work on standardization of the MARTES profile in OMG is progressing according to the time plan in OMG. It is important that in the future, to integrate views from the cluster as a whole, in order to include a broad spectrum of perspectives in the work.

3.3.2 Vision and Long-Term Goals

All the above three work directions are obviously of central importance to industry in Europe. The cluster has a clear role in working on issues which are central to many aspects of RTES development, partly in establishing contacts between different groups, and partly in synthesizing and performing new work which is of general interest to several communities. Alongside with this work, there is an important mission in harmonizing, to the extent possible, tool platforms for development, modelling, analysis of real time embedded systems. This also suggests the importance of standardization of central concepts for modelling and specification of Real Time Embedded Systems.

3.3.3 Recommendations

In view of the above assessment, it could be discussed to bring some of the activities in more explicit contact with other activities within ARTIST2

3.4 Meetings Held

3.4.1 Meeting: Workshop on Specification and Validation of UML models for Real Time and Embedded Systems, SVERTS 2004

Dates	October, 11, 2004
Venue	Lisbon, Portugal -- hold in conjunction with Seventh International Conference On UML, UML 2004
Main Organiser	Susanne Graf (Verimag, Ileana Ober (Verimag), Bran Selic (IBM), Oystein Haugen (U. of Oslo)
Web link	http://www-verimag.imag.fr/EVENTS/2004/SVERTS/
Objectives	Today's applications have often strong constraints with respect to time related aspects. Moreover, overall systems may be huge, and even if the embedded hard real-time components are relatively small, there is some global interdependence and the existence of a global model in a uniform framework is an important issue. The Unified Modelling Language UML can play this role, even if the real-time aspects are not really integrated today. The definition of UML has been motivated by the need for a standard notation for modelling system architectures and behaviours at functional and implementation level. UML aims at providing an integrated modelling framework encompassing architecture descriptions and behaviour descriptions. A first step to the integration of extra functional characteristics into the modelling framework has been achieved by the "UML profile for schedulability, Time and Performance"; It provides the basic concepts and a first attempt for a common syntax. Nevertheless, in order to be able to exchange models and to build validation tools, it is important to have also a common understanding of the semantics of the given notations. Other important issues in the domain of real-time is methodology and modelling paradigms allowing to break down the complexity, and tools which are able to verify well designed systems. This workshop should bring together researchers to discuss different time related issues in the context of modelling, design and validation of real-time systems, such as • notations for expressing time and related requirements • semantic issues and tools • modelling paradigms for real-time systems The workshop aims to gather people from academia and industry to discuss the needs and possible solutions for handling *time, scheduling and architecture* related issues which should help to define a work programme in this field.

Overview of the Agenda	Programme: **Session I: Modelling of real-time systems with UML** *Comparing two UML profiles for non-functional requirement annotations: the SPT and QoS profiles* Bernardi Simona, Dorina Petriu paper *A Formal Framework for UML Modelling with Timed Constraints: Application to Railway Control Systems* Rafael Marcano, Samuel Colin and Georges Mariano *Real-Time Requirements in Formalized Use Cases: Specification and Validation* Risto Pitkänen and Tommi Mikkonen *Incremental Design and Formal Verification with UML/RT in the FUJABA Real-Time Tool Suite* Sven Burmester, Holger Giese, Martin Hirsch, and Daniela Schilling **Discussion of presentations in session** **Session II: Tools for model based timing analysis** *An Analysis Tool for UML SPT Models* John Häkansson, Leonid Mokrushin, and Paul Pettersson *Worst-Case Execution Time Analysis from UML-based RT/E Applications* Chokri Mraidha, Sébastien Gérard, François Terrier, David Lugato *Validating UML models of Embedded Systems by Coupling Tools* J. Hooman, Nataliya Mulyar, Ladislau Posta **Discussion of presentations in session II** **PANEL: How useful can be UML in the context of real-time systems ?** **Participants:** Susanne Graf (Verimag), Oystein Haugen (U. of Oslo), Jozef Hooman (Embedded System Inst Eindhoven), Robert Pettit (Aerospace Corporation, USA)
Conclusions	The presentations in this workshop lead to interesting discussions. An overview on the presentations has been published in an LNCS volume common to all workshops associated with UML 2005, and is available at the workshop website. As for the outcome, With respect to the expression of time constraints there are two opposed trends: 1. There are those frameworks based on a small set of relatively low level but expressive concepts as they are handled in validation tools, 2. And those providing the user mainly with a set of relatively rigid patterns for the expression of time constraints. The contribution [BP04] show that even closely related profiles define redundant concepts which are even incompatible at the syntactic level. Some effort is clearly still to be done concerning this issue. Concerning validation of timing constraints an important issue is to provide methodologies allowing the application of compositional methods also in a non distributed setting.
Next meetings	In 2005, the SVERTS workshop and the SIVOES workshop have merged to the Workshop MARTES to be hold jointly with the successor

planned	conference of the UML conference, MoDELS 2005.

3.4.2 Meeting: Cluster Meeting

Dates	Oct. 12-13 2004
Venue	VERIMAG laboratory, Grenoble, France
Main Organiser	Susanne Graf, VERIMAG
Web link	http://user.it.uu.se/~bengt/Artist2
Objectives	Inventory of partners work and intentions
Overview of the Agenda	Component Modelling and Composition Platform for Modelling and Composition UML for RTES
Conclusions	• The work on Specification of timing should be discussed with other clusters, and a transversal meeting should be organized. • It should be investigated how the IF toolset can be connected with tools based on model transformation • The OMG plans for standardization f. RTES were presented,
Next meetings planned	See below

3.4.3 Meeting: Symposium on Formal Methods for Components and Objects (FMCO 2004)

Dates	November 2, 2004, November 5, 2004
Venue	Lorentz Center, Leiden University, Leiden, the Netherlands
Main Organiser	Frank de Boer (CWI), Marcello Bonsangue (LIACS), Susanne Graf (Verimag) and Wilem-Paul de Roever (U. Kiel)
Web link	http://fmco.liacs.nl/fmco04.html
Objectives	The objective of this symposium is to bring together researchers and practioners in the areas of software engineering and formal methods to discuss the concepts of reusability and modifiability in component-based and object-oriented software systems. Presentations are on invitation. The is to get together the most interesting people on different topics.
Overview of the Agenda	The programme included the following talks November, 2, 2004 • Keynote: Robin Milner (Cambridge University, UK), *Bigraphs and*

their mathematics

- Rocco de Nicola (University of Firenze, IT), *Open Nets, Contexts and their Properties*
- Eugenio Moggi (Genova University, IT), *Program Generation and Components*
- Keynote: Kim Bruce (Williams College, USA), *Fixing the meaning of object-oriented languages*
- Julian Rathke (Sussex University, UK), *A fully abstract trace semantics for a core Java language*
- Martin Steffen (Kiel University, DE), *Observability, classes, and object connectivity*
- Marcello Bonsangue (LIACS, NL), *Roles, ports and components*

November 3, 2004

- Keynote: Tom Henzinger (University of California, Berkeley, USA) *Games with Secure Equilibria: A Theory for Component Behavior*
- Wolfgang Weck (Software Architect, CH), *Three stories from Component Hell*
- Wang Yi (Uppsala University, SE), *Generation of real-time software with predictable timing behaviour*
- Keynote: Thomas Ball (Microsoft Research at Redmond, USA), *A Theory of Predicate-Complete Test Coverage and Generation*
- Frits Vaandrager (Nijmegen University, NL), *Switched Probabilistic I/O Automata*
- Susanne Graf (Verimag, FR), *Specification of systems with UML and verification with timed automata in the IF environment*

November 3, 2004

- Keynote: Kim Larsen (Aalborg University, DK), *Priced Timed Automata: Decidability Results, Algorithms and Applications*
- Ed Brinksma (University of Twente, NL), *Hybrid Systems and Composition: a Process Algebraic Approach*
- Andreas Podelski (Max Plank Institute for Informatics, DE), *Transition Invariants and Transition Predicate Abstraction*
- Keynote: Chris Hankin (Imperial College, UK), *Probabilistic Coordination Languages*
- David Naumann (Stevens Institute of Technology, USA), *Assertion-based encapsulation and refinement of classes*
- Tobias Nipkow (Munchen University, DE), *A Machine-Checked Model for a Java-Like Language, Virtual Machine and Compiler*
- Liu Zhiming (UNU-IIST, Macao), *A Model of Refinement for Component and Object Systems*

November 5, 2004

- Keynote: Samson Abramsky (Oxford University, UK), *Game*

	Semantics, Open Systems and Components • Luca de Alfaro (UC Santa Cruz, USA), *Types for real-time components* • Luis Barbosa (Minho University, PT), *A Perspective on Component Refinement* • Keynote: Reinhard Wilhelm (Saarland University, DE), *Timing Analysis of Hard Real-Time Systems* • Olaf Owe (University of Oslo, NO), *CREOL: A formal language for open, distributed and object-oriented systems* • Pierre Cointe (Ecole des Mines de Nantes, FR), *From objects to aspects*
Conclusions	This was a very interesting meeting with many stimulating discussions and over 50 participants, including many Artist participants and speakers. Post conference contributions of the speakers at FMCO 2004 will be published in the series "Revised Lectures of Lecture Notes in Computer Science" by Springer-Verlag. A special issue of the Elsevier journal Theoretical Computer Science dedicated to FMCO 2004 is planned.
Next meetings planned	The next issue of FMCO is planned in November 2005 in Amsterdam. Contrary, to the previous issues, this time there will not be exclusively invited talks, but half of the programs will consist of submitted contributions selected by the programme committee.

3.4.4 Meeting: Extended Cluster meeting

Dates	Jan 24-25, 2005
Venue	CEA main headquarters, Paris, France
Main Organiser	Hubert Dubois, CEA
Web link	http://user.it.uu.se/~bengt/Artist2
Objectives	Reviewing the concrete work directions for the cluster.
Overview of the Agenda	Presentations (several invited) on specification of timing for component-based systems Detailed presentation of the planned MARTES work in OMG
Conclusions	The work on "modelling and composition" will be organized in two action lines: • Formalisms for compositional timing specifications • Fundamentals of component composition The two other activities continue as before.

Next meetings planned	See below

3.4.5 Meeting: Inter cluster meeting “components” and “hard real time”

Dates	June 28-30
Venue	IRISA, Rennes, FRANCE
Main Organiser	Noel Plouzou, IRISA
Web link	http://user.it.uu.se/~bengt/Artist2
Objectives	Review progress in action lines
Overview of the Agenda	Presentations pertaining to different action lines in different sections.
Conclusions	See web-link.
Next meetings planned	January 2006, Meeting on standardization OFFIS,

3.4.6 Meeting: Modelling of Real-Time and Embedded Systems, MARTES 2005

Dates	October 4, 2005
Venue	Montego Bay Jamaica, in association with the Int. MoDELS/UML conference
Main Organiser	Sébastien Gerard (CEA), Susanne Graf (Verimag), Øystein Haugen (Univ. of Oslo), Iulian Ober (Verimag), Bran Selic (IBM, Canada)
Web link	http://www.martes.org/
Objectives	The OMG initiative, called MDA -- for "Model Driven Architecture" puts forward the idea that future process development will be centred around models, thus keeping application development and underlying platform technology as separate as possible. The aspects influenced by the underlying platform technology concern mainly non functional aspects and communication primitives. The first significant result of the MDA paradigm for engineers is the possibility for them to build application models that can be conveniently ported to new, emerging technologies - implementation languages, middleware, etc.- with minimal effort and risk in one hand, but also that can be analyzed either directly or through a model transformation toward a specific formal technological space in order to validate or/and verify real-time properties such as for example schedulability.

	In the area of DRES (distributed, Real-time and Embedded Systems), this model-oriented trend is also very active and promising. But DRES are different from general-purpose systems. The purpose of this workshop is to serve as an opportunity to gather researchers and industrials in order to survey some existing experiments related to modelling and model-based analysis of DRES.
	Moreover in order to be able to exchange models with the aim to apply formal validation tools and to achieve interoperability, it is important to have also a common understanding of the semantics of the given notations. Other important issues in the domain of real-time are methodology and modelling paradigms allowing breaking down the complexity, and tools which are able to verify well designed systems.
	This workshop seeks contributions from researchers and practitioners interested in all aspects of the representation, analysis and implementation of DRES models, on the following principal topics:
	• Modelling RT/E using UML
	  ○ How to specify real-time requirements and characteristics in UML
	  ○ How to enhance UML to capture real time, embedded and distributed aspects in a convenient manner
	  ○ Declarative versus operational real-time specifications
	  ○ Notations for defining the architecture of heterogeneous systems
	  ○ Behaviour Modelling
	  ○ RT/E platforms modelling, integration of scheduling aspects
	• Semantic aspects of real-time in UML
	  ○ Formal semantics, in particular, semantic integration of heterogeneous systems
	  ○ Interpretations of annotations
	  ○ Executability of models
	• Methods and tools for analysis of RT systems and components
	  ○ Ensure consistency of timing constraints throughout the system
	  ○ Validation of time and scheduling related properties
	  ○ Validation of functional properties of time dependent systems
	The workshop aims to gather people from academia and industry to discuss the needs and possible solutions for handling *Modelling, semantic and validation* related issues which should help to define a work programme in the context of model based Development.

Overview of the Agenda	**Programme** **Session I : UML Profiles** *Modelling and Analysis of Concurrent and Real-Time Object-Oriented Designs*, Robert G. Pettit IV, Hassan Gomaa

	Introducing Control in the Gaspard2 Data-Parallel Metamodel: Synchronous Approach, Ouassila Labbani, Jean-Luc Dekeyser, Pierre Boulet and Éric Rutten *Some Requirements for Quantitative Annotations of Software Designs*, Dorina C. Petriu, Murray Woodside *A General Structure for the Analysis Framework of the UML MARTE Profile*, Huáscar Espinoza, Hubert Dubois, Sébastien Gérard, Julio Medina **Discussion of presentations in session I** **Session II : Quantitative analysis** *A Unified Approach for Predictability Analysis of Real-Time Systems using UML-based Control Flow Information*, Vahid Garousi *Modular Verification of Safe Online-Reconfiguration for Proactive Components in Mechatronic UML*, Holger Giese, Martin Hirsch *Timing analysis and validation of the embedded MARS bus manager* Iulian Ober, Susanne Graf, Yuri Yushtein *Validating temporal properties of a deployed application with an MDD approach*, Jean-Louis Houberdon, Pierre Combes, Jean-Philippe Babau, Isabelle Auge-Blum **Discussion of presentations in session II**
Conclusions	Meeting not yet hold
Next meetings planned	Not yet defined

3.5 Cluster Participants

3.5.1 Core Partners

Institution	Researcher
Uppsala University **Focus:** **Verification, Testing, Scheduler analysis, component models, compositionality**	**Team Leader: Bengt Jonsson,** Main areas of research: Verification**,** Testing, Scheduler analysis, component models, compositionality Other projects involved in: SAVE, ASTEC, National projects, Artist2 activities and role: Coordinator of Modeling and Components Cluster, Component modelling and composition: activity leade, and compositional modelling Platform for Component Modeling and Verification: Connection fo modelling and verification tools
CEA **Focus:** **MDE, UML, Standardization, Test generation**	**Francois Terrier,** **Sebastien Gerard** Main areas of research: Test case generation, UML modelling notation, Model transformation, Standardization Other projects involved in: STACS, COMTESSE, CARROLL Initiative, Artist2 activities and role: Component modelling and composition: testing component modeling Platform for Component Modeling and Verification: definition of UML modelling notation Development of UML for Real-time Embedded Systems: Activity leader, and standadization of UML notations for Real Time systems

FTR&D **Focus:**	**Pierre Combes** Main areas of research: Other projects involved in: STACS, COMTESSE, CARROLL Initiative, Artist2 activities and role: Component modelling and composition: testing component modeling Platform for Component Modeling and Verification: definition of UML modelling notation Development of UML for Real-time Embedded Systems: Activity leader, and standadization of UML notations for Real Time systems
INRIA **Focus:** **MDE,** **UML** **Contracts**	**Jean-Marc Jezequel,** **Noel Plouzeau** Main areas of research: Model Driven Engineering, UML, Contracts Other projects involved in: TRISKELL; QCCS, CARROLL Initiative Artist2 activities and role: Component modelling and composition: extra-functional properties specification and testing Platform for Component Modeling and Verification: UML-based transformation technology Development of UML for Real-time Embedded Systems:

VERIMAG Focus: Component Models, DevelopmentTools, Tool integration, Semantics, Verification	**Susanne Graf,** **Joseph Sifakis** Main areas of research: Modeling notation, semantics, verification, tool integration, Other projects involved in: OMEGA, EDEN, PERSIFORME Artist2 activities and role: Component modelling and composition: Composition of timed systems Platform for Component Modeling and Verification: Activity leader, development of Kernel notation, Connection fo semantic kernerl modelling notation. Development of UML for Real-time Embedded Systems: modelling of real-time components

3.5.2 Affiliated Industrial Partners

Company	Researcher
ABB	**Christer Norström** Main areas of research: development of large embedded systems Other projects involved in: ASTEC Artist2 activities and role: Component modelling and composition: handling non-functional properties in large embedded systems Platform for Component Modeling and Verification: case study from industrial automation
ARTiSAn Software	**Alan Moore** Main areas of research: UML based development tools Other projects involved in: Artist2 activities and role: Development of UML for Real-time Embedded Systems: Activity leader, and standadization of UML notations for Real Time systems

Thales Research and Technology	**Dominique Potier** Main areas of research: Standardization, case studies, Other projects involved in: Artist2 activities and role: Platform for Component Modeling and Verification: case study from aerospace industry Development of UML for Real-time Embedded Systems: standardization, case studies

3.5.3 Affiliated Academic Partners

Institution	Researcher
EPFL	**Tom Henzinger** Artist2 activities and role: Component modelling and composition: Modelling and interfaces for real time systems
Timisoara	**Marius Minea** Artist2 activities and role: Component modelling and composition: extraction and absraction of timed interfaces
Mälardalen	**Ivica Crnkovic** Artist2 activities and role: Component modelling and composition: component models for real time systems
Aalborg:	**Anders Ravn** Artist2 activities and role: Component modelling and composition: specification of QoS properties Development of UML for Real time embedded systems: Case study

OFFIS	**Bernhard Josko** Artist2 activities and role: Development of UML for Real time embedded systems:language development
Dortmund	**Bernhard Steffen** Artist2 activities and role: Component modelling and composition: extraction of functional and timing properties for components Platform for Component Modeling and Verification: Electronic tool integration
U. of Cantabria	**Julio Medina** Artist2 activities and role: Component modelling and composition: modelling for schedulability analysis Development of UML for Real time embedded systems: notation for schedulability analysis

3.6 Research and Platform Activities

3.6.1 Joint Programme of Research Activities: Cluster Integration

3.6.1.1 **JPRA-Cluster Integration**: *Component Modelling and Composition*

Leader	Bengt Jonsson (Uppsala: compositional modelling)
Policy Objective	The development of a general framework for component-based engineering of complex heterogeneous systems is one of the grand challenges in information sciences and technologies. This JPRA will combine the efforts and skills of world-leading researchers in Europe to address this challenge.

3.6.1.2 **JPRA-Cluster Integration**: *Development of UML for Real-time Embedded Systems*

Leader	Francois Terrier (CEA: Standardization of UML notations for Real time systems)
Policy Objective	A framework for handling central aspects of Real time Systems in UML-based notations, and in UML-based system development. This will influence standardization and allow European UML-based tool providers to have a larger impact.

3.6.2 Joint Programme of Research Activities: NoE Integration

The cluster “Modelling and Components” is involved in the NoE Integration activity: “QoS-aware Components”, described in section 2.3.7.

3.6.3 Platform

3.6.3.1 JPIA-Platform*: Platform for Component Modelling and Verification*

Leader	Susanne Graf (Verimag: Development of kernel modelling notation, Connection to semantic kernel modelling notation, coordinator of the IST OMEGA project on real-time UML)
Policy Objective	To integrate European research on modelling and analysis of component-based real-time systems, by providing modelling notations and semantics based on UML standards. This platform builds on work on UML modelling by INRIA, CEA, KU Leuven, and UPM, and the work on semantics by VERIMAG, Uppsala. This platform will support translations to semantic kernel languages to leverage associated powerful analysis tools, in particular those from the “Testing and Verification” cluster.

4. Cluster: Hard Real Time

Contributor: Prof. Albert Benveniste - INRIA

4.1 Description of the Area

4.1.1 Main Research Trends

Cluster HRT focuses on

1. *design processes,* and
2. *architectures,*

for Real-Time embedded systems. Actually, research is not restricted to “hard” real-time, strictly speaking. What characterizes HRT cluster as compared to other clusters is its main focus on design processes and related fundamental issues. More specifically, the following topics are considered central:

- Dealing with heterogeneity in design flows; this includes mixing different styles of scheduling policies (Event-Triggered and Time-Triggered, fixed and adaptive) as well as mixing different Models of Computation and Communication (MoCC), *e.g.,* synchronous and asynchronous. Main results obtained by the HRT teams include:
  i. Mixing ET with TT while preserving functional and scheduling semantics;
  ii. Relating schedulability and existence of deadlock freedom, for timed systems models;
  iii. Formally sound techniques for correct-by-construction deployment.
- Addressing functional and non-functional aspects, jointly. Main results obtained by the HRT teams include:
  i. A comprehensive theory of heterogeneous reactive systems.
- Paving the foundations for design space exploration and platform-based design, for embedded electronics and software systems.

In addition, HRT cluster has focused on the particular topic of embedded systems *diagnosis* with its combined aspects of analog devices, computer hardware, and uncertainties arising from software. The main outcome of this investigation has been the discovery of possible cross-fertilizations between different research communities (dependability, control, and statistics).

4.1.2 Industrial Applications

This area of research is mainly driven by two sectors:

- *Aeronautics.* This sector is faced with the challenge of Integrated Modular Avionics (IMA), which drastically changes the OEM/supplier relations. Integration will occur at the level of functions, not any more at the level of packaged hardware modules and devices. Therefore, constructors are faced with the need of mastering system integration at all levels of the design process (from requirements to hardware). This move will drastically impact how certification will be performed in the future.
- *Automobile.* The move is similar to that in aeronautics, the changes being in fact much more rapid and drastic – within a few years, the OEM/supplier chain will be entirely reconfigurated. Added value, for constructors, will move to completely different components of the car, namely those mostly contributing to building the "concept" and "personality" of each different car. Sharing platforms with competitors is now the trend, as shown by the *Autosar* initiative.

In any case, the major challenge for research is this need for ***mastering system integration at all levels of the design process***. This central challenge motivated the research directions listed above.

Now, it should be clear that the research issues addressed will be also essential to other sectors such as transportation in general, power, military, consumer electronics and medical equipment, as they will be faced with the same trend regarding their business model.

4.2 State of Integration in Europe

4.2.1 Interaction of the Cluster with other Communities

The HRT cluster, seen as a body, has been mainly interacting with the following other clusters from ARTIST2:

- Components (Bengt Jonsson)
- Execution Platform (Lothar Thiele)

Interactions have been motivated by the need to share views regarding the central notion of *component,* for embedded systems. Clearly, our three clusters contribute to this notion – my opinion is that the notion of component is also contributed to by other ARTIST2 clusters as well, in particular regarding RTOS and verification&testing; but no synchronization with these clusters has occurred so far.

On the other hand, HRT has regular contacts with some participants from the CHESS project in the US, both via the Berkeley group (with Ed Lee and the dual participation of Alberto Sangiovanni-Vincentelli) and the Vanderbilt University (Janos Sztipanovits).

Next, the teams constituting HRT are involved in major activities involving other communities:

- TU Vienna is highly active in RT architectures (TTA) and dependability, as represented in EU par the DECOS project;
- OFFIS is a key actor in Verification engines for embedded systems, and has special ties with the automotive industry (BMW, DC) and the Autosar initiative;
- Verimag is a central actor in research for embedded systems in all its aspect regarding software (synchronous languages, components for RT, hybrid systems, verification tools), and has special ties with Airbus and Esterel technologies.
- PARADES has a deep experience in advance research contracts for industry in both sectors of digital circuits and automobile, and has special links with Cadence and UC Berkeley;
- INRIA is a recognized actor in synchronous languages and reactive systems.

4.2.2 Main Aims for Integration through Artist2

Integration through ARTIST2 is motivated by the following:

- Collecting the best teams in embedded systems area in EU will per se result in cross-fertilization between ideas and approaches;
- It provides the required fertilizer for a consensus to emerge on what the central issues in embedded systems research are, for the 10 years ahead;
- It offers arenas for people to meet, who otherwise would remain scattered among their respective communities and conferences and never talk to each other;
- Integration through ARTIST2 is both open to industry's challenges and open toward offering novel ideas to industry;
- Integration through ARTIST2 provides the due critical mass for efficient exchanges with US and other international teams.

4.3 Overall Assessment and Vision for the Cluster

4.3.1 Assessment

Assessment of the activities and results of HRT cluster should in principle not be considered in isolation from other cluster's activity. Still, I shall try to formulate such an assessment by properly acknowledging others clusters whenever needed.

In providing such an assessment, I shall structure the activities of HRT into two main directions:

- Embedded systems diagnosis;
- Fundamental studies related to design process and architectures.

The second direction has concentrated the major part of the cluster's work force so far.

4.3.1.1 Embedded systems diagnosis

The original goal of this activity was twofold:

- Setting an activity in an area where research is required by industry and lacking in academia;
- Providing additional inputs for this subject to the ongoing DECOS project.

Accordingly, the activity group was a small group of teams composed of core members of DECOS (core members or affilate-members of ARTIST2: TU Vienna, Humboldt University of Berlin, TU Darmstadt, University of Firenze) and other teams not participating to DECOS and not active in the dependability community (DECOS' scientific community regarding this topic), these were INRIA, VERIMAG, and PARADES.

Regarding the skills and background collected, these were dependability, architectures, formal methods and verification techniques, statistics, and control. This was a very interesting panel offering rich promises and possibilities.

Indeed, the following findings were formulated as results of the two meetings held for this activity:

- The problem of stating *"out-of-norm assertions*" (a concept proposed by TU Vienna) is indeed tightly related to logics for real-time (Verimag, Parades). Cheking whether such assertions can actually be assessed for possible violation in a system can be seen as a diagnosability issue, for timed automata (Verimag). Relating these up to now separated areas is therefore worth the effort and should be pursued.
- Detecting and properly assessing *intermittent faults* in embedded systems is now recognized as a major issue. The ultimate question is when and how to properly decide on putting a component out of the fault-tolerant architecture. So-called "threshold-based" policies have been developed in the dependability community to detect such faults, taking their random nature into account. In the two seminars, it was found that these methods are indeed tightly related to *sequential stopping rules* from statistics, as known from the HRT participants having control background. This finding indeed provides a systematic approach to developing detection methods for various situations, and better ways to take probabilistic prior knowledge into account.
- In the second meeting, it was found that the timed automata approach could be indeed lifted to handling statistical aspects related to intermittent faults. This opened new possibilities for research.

At this point, the results of this group are extremely positive. Yet it is unclear that this activity can continue, due to administrative difficulties.

The question of proper, regular, funding was raised at the 1st meeting by the three affiliate partners of the group. These affiliates were not satisfied with being supported on a per-travel basis, by payment through INRIA (the leading institution of HRT). No simple agreement could be found to settle this problem between the 1st and 2nd meetings. Consequently, I decided to move the meeting originally planed at Berlin, to Grenoble, to have it organized by a core partner. Affiliates decided to leave the group, which impairs activities listed in the second bullet. Since, on the other hand, the researcher in charge of the topic at TU Vienna will leave by end of this year, it is suggested that *the surviving part this activity (with Verimag, PARADES, and possibly INRIA) will be shifted to the cluster on Verification and Testing*.

To avoid losing all results regarding statistical methods, I offered TU Vienna to give presentations related to the above results at some forthcoming DECOS meeting. This is still open.

4.3.1.2 Fundamental studies related to design process and architectures

This activity went very smoothly, with impressive results indeed. Two meetings were held, where a number of research issues were debated and as a consequence were much better identified. Regarding the nature of the exchanges, the following points must be observed:

- It is not obvious to get top class engineers from industry participating to our seminars, since the return that ARTIST2 can offer is quite diffuse and on a long time scale. In addition, such engineers are typically overloaded. Still, this group was happy enough having an outstanding participation from three engineers from General Motors and BMW – thanks are due to Alberto Sangiovanni-Vincentelli for these invitations. This participation indeed drove our 1st meeting and was very fruitful as shown by the minutes of this Rome meeting.
- Again, gathering people from different communities proved being a major strength of these ARTIST2 meetings. For this group, people originated from “formal methods and models”, “scheduling”, “architectures and hardware”. This mix is indeed instrumental in addressing overall systems design process, with its functional and non-functional aspects.

Major findings were:

- It was agreed that studies on *embedded systems architecture* should be a central research topic for embedded systems community. This term covers a number of issues, however:
    - Architectural languages *e.g.,* AADL…
    - Architectural paradigms, *e.g.,* TTA; these consist in a systematic and coherent set of architectural design choices with certain objectives (for TTA: fault-tolerance, subsystems compartmentalization, determinism, composability).
    - Modelling and semantics aspects, with supporting mathematics; the point is to offer a mathematical machinery that is rich and flexible enough, and still tractable, to formally model systems architectures in their joint functional and non-functional aspects and rich heterogeneity; it should provide support for reasoning on open systems, interfaces, black/grey-box models, and the like.
- Main concern in automobile industry is systems architecture, with design process coming only second; this is in contrast with aeronautics industry, where the two topics are seen more or less of equal importance.

4.4 Research and Platform Activities

4.4.1 *JPRA-Cluster Integration*: Diagnosis in Distributed Hard Real-time Systems

Leader	Hermann Kopetz and Philipp Peti (TU Vienna: expertise in fault-tolerant systems architecture)
Policy Objective	The objective is to provide an integrated approach to diagnosis of distributed real-time systems, in particular with respect to transient anomalies. This topic will be tightly connected with the proposed DECOS Integrated Project.

4.4.2 *JPRA-NoE Integration*: Participation in activities led in other clusters

Beyond the NoE-Integration activities described here, the cluster “Hard Real Time” is also involved in the NoE Integration activity: “Adaptive Real-time, HRT and Control”, described in section 2.6. 7.

4.4.3 *JPRA-NoE Integration*: Semantic Framework for Hard Real-Time Design Flow

Leader	Albert Benveniste (INRIA: synchronous languages and models of computation) Alberto Sangiovanni-Vincentelli (PARADES: design methodology in automotive and hardware industries, models of computation, embedded and hybrid systems, design automation)
Clusters	Hard Real-Time Adaptive Real-Time Control for Embedded Systems
Policy Objective	Joint work within the “Hard Real-Time” cluster, with participation from the “Adaptive Real-Time”, and “Control for Embedded Systems” clusters.

4.4.4 *JPRA-NoE Integration*: Merging the Event-triggered and Time-triggered Paradigms

Leaders	Paul Caspi and Nicolas Halbwachs (Verimag, synchronous languages, strong collaboration with Airbus Industries)
Clusters	Hard Real-time Adaptive Real-time Execution Platforms
Policy Objective	Fundamental work on merging two of the main paradigms in real-time systems design. The expected results are important from both a theoretical point of view, and also for industry (distributed embedded systems and network on chip applications). Two approaches for designing and implementing synchronous hard real-

	time systems have been developed: event triggered and time-triggered. These have been applied separately to large-scale embedded systems in Europe. This activity will investigate how to integrate these approaches in a semantically sound and efficient design flow, preferably platform-based. It will require in particular research on mathematical modelling and simulation of both time-triggered and event-triggered architectures, research on RTOS execution mechanisms and research on performance evaluation and optimisation.

4.4.5 Platform

There is no platform for the Hard Real Time Cluster, since this is replaced by a large number of JPRA-NoE Integration activities.

5. Cluster: Adaptive Real Time

Contributor: Prof. Giorgio Buttazzo – University of Pavia

5.1 Description of the Area

5.1.1 Main Research Trends

Most of today's embedded systems are required to work in dynamic environments, where the characteristics of the computational load cannot always be predicted in advance. Still timely responses to events have to be provided within precise timing constrains in order to guarantee a desired level of performance. The combination of real-time features in dynamic environments, together with cost and resource constraints, creates new problems to be addressed in the design of such systems, at different architecture levels.

To cope with dynamic environments, a system must be adaptive; that is, it must be able to adjust its internal strategies in response to a change in the environment, to keep the system performance at a desired level. Implementing adaptive embedded systems requires specific support at different levels of the software architecture. The most important component affecting adaptiveness is the kernel; however, flexibility can also be introduced above the operating system, in a software layer denoted as a middleware, and also in the programming language used to develop the application. Some embedded systems are large and distributed among several computing nodes. In these cases, special network methodologies are needed to achieve adaptive behavior and predictable response. Often such a support cannot be found in today's commercial software.

5.1.2 Industrial Applications

The most important industrial fields that can benefit from adaptive real-time technology include Consumer Electronics, Industrial Automation, and Telecommunications.

Consumer Electronics (CE) products range from miniature cameras and MP3 players to advanced media servers and large displays. Mainly driven by Moore's law, the evolution in the CE industry is very fast. The software content, measured in ROM size, grows one order of magnitude every 6 to 7 years. To keep up with this speed, the industry moves to families of products based on retargetable platforms: systems on chip that allow media streaming and featurization.

In the area of Industrial Automation there is a trend to search distributed solutions and to prepare hardware and software for connecting the general plant actuators, sensors and the controllers. Distributed solutions give a natural automation condition to common industrial needs as usually such plants are physically and topologically distributed. At the same time, there is an increase of demands for new options and improvements in the automation results, fetching more control of plant secondary data. This imposes a continuous increment in processing power and memory capacity that requires adaptivity at different levels of system operation.

Embedded systems for telecommunications applications are mainly targeted to the interfaces between communication technologies and to coding/decoding operations. They may be considered real-time as they have timeliness requirements for some of the critical operations they must perform. The referred systems are microprocessor based platforms, often integrating a second processor (e.g., a DSP) devoted to specific functions, like MPEG coding. Depending on the system, a proprietary kernel can be used or a real-time operating

system, (e.g. iRMX). Currently Linux starts to become the adopted operating system. The verification of real-time behavior is made by the experimental inspection of the timeliness requirements at the development phase and at the operation phase by in-situ monitoring.

5.2 State of Integration in Europe

5.2.1 European Research Teams

The most relavant research conducted in Europe on adaptive real-time systems is carried out by the following research groups:

- University of Pavia (Prof. Giorgio Buttazzo) with expertize on real-time scheduling, robotic systems and interfacing.
- Scuola Superiore S. Anna (Prof. Giuseppe Lipari), with expertize on flexible scheduling and real-time kernel technology.
- University of Aveiro (Prof. Luis Almeida) with expertize on networking platforms and distributed applications.
- University of Cantabria (Prof. Michael Gonzalez Harbour) with expertize on real-time langages, distributed systems and operating system standards.
- University of York (Prof. Alan Burns), with expertize on fixed priority scheduling and real-time languages.
- Mälardalen University (Prof. Gerhard Fohler) with expertize on video streaming and distributed scheduling with complex constraints.
- Polytechnical University of Madrid (Prof. Juan Antonio De la Puente), with expertize on Quality of Service management architecture and tools.
- Polytechnic Institute of Porto (Prof Eduardo Tovar), with expertize on distributed applications and QoS over heterogeneous networks.
- University Carlos III of Madrid (Prof. Carlos Delgado Kloos), with expertize on middleware and Quality of Service management.
- University of Catania (Prof. Lucia Lo Bello), with expertize on communication protocols and stochastic scheduling.
- Universitat Politècnica de Catalunya (Prof. Josep Fuertes) with expertize on adaptive real-time control methodologies.
- Evidence s.r.l. (Dr. Paolo Gai) with expertize on kernels and design tools for real-time embedded systems.

5.2.2 Interaction of the Cluster with other Communities

The ART cluster had several interactions with the communities:

- University of Illinois at Urbana Champagne (reference persons: Prof. Lui Sha and Prof. Marco Cacciamo) on wireless communication protocols for real-time distributed emebedded systems.
- University of Virginia (reference persons: John Stankovic and Tarek Abdelzaher) on adaptive real-time systems for sensor networks.
- University of Lund (reference persons: Karl-Erik Arzen and Anton Cervin) on feedback control tecniques for adaptive real-time systems.
- University of California at Berkeley (reference person: Alberto Sangiovanni Vincentelli) on the design of component-based operating systems.

- ARTIST2 cluster on Modelling and Components, for modelling, composition, and verification of timing properties.
- Philips Research Eindhoven (reference persons: Dr. Liesbeth Steffens and Dr. Sjir van Loo) on resource management for consumer electronics.

5.2.3 Main Aims for Integration through Artist2

Achieving adaptivity in embedded real-time systems is a complex task that requires expertize from several disciplines, including operating systems and kernels, scheduling theory, distributed systems, network communication, control theory, quality of service management, and programming languages. Combining the results achieved in such different domains and orchestrating the various groups active in these fields is only possible by a tight interaction among the cluster participants. Hence, the aim of the integration through Artist2 is to facilitate communication among cluster members in order to:

- Improve understanding of the key problems from different perspectives;
- Clarify the terminology to provide a common language for exchanging information;
- Build a common platform to perform experiments and develop tools that can be shared by the differnet gruops;
- Identify new research directions aimed at overcoming the problems encountered during the integration phase.
- Interact with industries to understand their problems and identify possible solutions;
- Form new consortia and make concrete project proposals to address specific reseasrch problems or develop critical applications of industrial interest.

5.3 Overall Assessment and Vision for the Cluster

5.3.1 Assessment

Adaptive real-time is a new discipline that developed to provide support to emerging applications (e.g., consumer electronics, multimedia systems, telecommunications) characterized by reactive behaviors in highly dynamic environments. In Europe, some of the leading research groups, traditionally involved in hard real-time computing, started investigating how to extend the notion of predictability to provide more flexibility in computer control systems.

Thanks to the ARTIST FP5 project, these groups had the opportunity to collaborate for exchanging ideas, discussing key issues, and coordinated for a joint effort in such an emerging research discipline. The ARTIST roadmap for adaptive real-time systems for quality of service management, published by Springer in 2005, represents the result of such a joint effort. It established the guidelines for future research directions to overcome the limitations of the present software technology and address the problems identified by industry.

The ARTIST2 network of excellence gave the opportunity to strengthen such collaborations, also actracting new research groups and institutions that provided complementary expertize in the field of adaptive real-time systems.

In the first year of activity, the ART cluster worked with the main objective of creating a common software infrastructure, consisting of a shared operating system platform, the Shark kernel, to be used as a tool for carring out experiments, test new algorithms, and experiment novel programming interfaces. All the core and affiliated partners actively contributed to this activity, either by providing the necessary expertize for dissemination or by sending students to Pisa (where the lectures have been organized) for learning the kernel internals.

This preliminary step represents an important milestone for building excellence in the new research field of adaptive real-time systems. It allows to build a critical mass of people that work with the same tools and perform extensive experiments on a shared platform, whose results can be compared to evaluate the effectiveness of novel software methodologies.

5.3.2 Vision and Long-Term Goals

The long term goal of the ART cluster is to build the fundamental bases of a new real-time software technology that can provide a more efficient and predictable support to the development of future embedded systems. In particular, the new software technology should

- support scalability to facilitate the porting of control applications to different platforms;
- simplify the management of resources to control the growing complexity of embedded systems;
- increase programming flexibility, for specifying functional and performance requirements that simplify test and verification;
- increase system adaptivity to react to environmental changes, still providing a sufficient level of performance;
- be robust to tolerate transient and permanent overloads conditions due to wrong design assumptions or unpredictable changes.

Using such a novel software technology would be of paramount importance for European industry, because it would allow to have a better control of complexity, so reducing the time to market, and would improve software realiability and testabilty, so reducing the time spent in debugging and

Also research would benefit from such an evolutionary change, because new tools, algorithms and kernel mechanisms will be necessary to support industry in such a transient period. In this respect, the ART cluster will play an essential role for suggesting the appropriate research directions, acting as a bridge between the academic and the industrial world.

5.3.3 Recommendations

To achieve the objectives of the ART cluster, the partners should continue to work as a team in the areas identified in the project, organizing meetings and workshops to facilitate direct collaboration. Summer schools and special courses are also of crucial value for spreading excellence among the partenrs and speed up the development of a common infrastructure for developing adaptive real-time embedded systems.

The activities planned in the proposal are still valid and the structure of the cluster does not need to be changed.

5.4 Meetings Held

5.4.1 Meeting: Towards a Common Infrastructure for Adaptive Real-Time Systems

Dates	December 7, 2004
Venue	SANA Lisboa Park Hotel Lisbon Portugal
Main Organiser	Giorgio Buttazzo University of Pavia
Web link	
Objectives	To define a concrete plan for achieving a common infrastructure for adaptive real-time systems.
Overview of the Agenda	The main issue to be discussed has been the organization of a tutorial to introduce each partner to the use of the Shark real-time kernel. Each partner invloved in the activity was assigned a specific responsibility, consisiting of implementing a component for the Shark kernel or in developing a real-time control application.
Conclusions	The definition of the activities carried out by each partner to create a common infrastructure for adaptive real-time systems.
Next meetings planned	The first Shark workshop Feb. 28 to March 4 2005 organised by: Giorgio Buttazzo and Giuseppe Lipari

5.4.2 Meeting: First Shark Workshop

Dates	Feb. 28, 2005 - March 4, 2005
Venue	Polo Sant'Anna Valdera Pontedera (Pisa) Italy
Main Organiser	Giuseppe Lipari – Scuola S. Anna of Pisa Giorgio Buttazzo – University of Pavia
Web link	
Objectives	To define a common operating system platform for adaptive real-time systems
Overview of the Agenda	The workshop was structured as a short course with lectures and laboratory exercises. The goal of the lectures was to provide a detailed presentation of the Shark operating system, explaining how to write a real-time application, new scheduling modules, resource protocols, and drivers.

	The goal of the lab exercises was to help people in using Shark, both at the application level and at the kernel internal level.
Conclusions	All the participants were trained in the use of the Shark kernel and each group identified a real-time application to be developed under Shark as a test case for their experiments.
Next meetings planned	Workshop on Operating Systems Platforms for Embedded Real-Time applications (OSPERT) July 5, 2005 organised by: Giuseppe Lipari (Pisa)

5.4.3 Meeting: Flexible Scheduling Technologies

Dates	June 16, 2005
Venue	University of Cantabria Santander Spain
Main Organiser	Michael Gonzalez Harbour University of Cantabria
Objectives	A brainstorming session to discuss the main objectives and develop a work plan for writing a research project proposal on contract-based scheduling.
Overview of the Agenda	Presentation Objectives of the project Partner contributions Workpackages Workplan Name of the project
Conclusions	As a result of the meeting, a consortium of 9 core members was established with the goal of preparing a proposal for an IST STREP project in Embedded systems, woth focus on advanced scheduling techniques through the use of a contract-model. Participation of other members would be souugh after the meeting. The objectives of the research project were settled down, and an initial workplan was sketched, with division into workpackages and assignment or workpackage leaders.
Next meetings planned	Preparation of the proposal on contract-based scheduling July 6, 2005 organised by: Guillem Bernat, Univ. of York

5.4.4 Meeting: OSPERT: Workshop on Operating Systems Platforms for Embedded Real-Time applications

Dates	July 5, 2005

Venue	University of Palma de Mallorca Palma de Mallorca Spain
Main Organiser	Giuseppe Lipari Scuola Superiore S. Anna, Pisa (Italy)
Web link	http://feanor.sssup.it/~lipari/OSPERT.html
Objectives	This workshop was intended as a forum for researchers and practitioners of RTOS to discuss the recent advances in RTOS technology and the challenges that lie ahead. Research on innovative RTOS architectures and services is a hot topic. Developers of Real-Time Operating Systems (RTOS) are faced with many challenges arising from two opposite needs: extreme optimization of resource usage (processor, energy, network bandwidth, etc.) vs. dynamic configuration and upgrading, flexible scheduling, component-based development and deployment, etc. While real-time systems continue to be used in many small embedded applications, real-time services are being introduced and used in general-purpose operating systems. Notable examples are the various flavors Linux that provide support to time-sensitive applications.
Overview of the Agenda	The workshop was organized into 4 sessions. The “Session 1: Kernel Architectures for Embedded Systems.” included the presentation of 3 papers, and was followed by an open discussion on novel kernel architectures that deal with dynamically reconfigurable hardware architectures. In “Session 2: RTOS Architectures and APIs – I.”, 4 papers were presented on and novel APIs that support flexible scheduling, the need for flexible scheduling in commercial RTOSs and applications, a nanokernel for making many RTOS cohexist on the same processor, and an architecture and API for power management. In “Session 3: Real-Time in general purpose OS”, the presenter discussed the introduction of real-time support on general purpose operating systems, and in particular on the Linux kernel. In “Session 4: RTOS Architectures and APIs – II”, other issues on RTOS were discussed like a presentation of the OCERA kernel, a new Ravenscar profile, porting a open source kernel on a DSP, and using power measurement as a basis for power management.
Conclusions	Participation to the workshop was large (about 30 attendants), and this confirms the interest in the academia and in the industry on real-time operating systems. The topics addressed by the presentations raised many questions and a lot of discussion. In particular, Session 1 was the most attended and raised the largest interest, showing the importance of pursuing further research in the field of reconfigurable architectures.

5.4.5 Meeting: Real-time wireless networks for mobile robots

Dates	July 7, 2005
Venue	Gran Hotel, Fundació “La caixa” Palma de Mallorca Spain
Main Organiser	Luis Almeida University of Aveiro
Objectives	To coordinate a joint research on mobile wireless networks and identify the key issues to be solved in order to develop a distributed application in which a team of autonomous robots cooperate to accomplish a coomon goal.
Overview of the Agenda	Introduction by Luis Almeida to present the various research aspects of the problem. Open discussion to identify significant research issues to be investigated by the members of the ART cluster. Identification of significant applications that would benefit from a coordinated team of mobile robots. Planning for a possibile research project on the topic.
Conclusions	The key research issues identifyed by the partners include real-time communication protocols for wireless networks, robot localization, navigation, topology management, energy-aware strategies, dynamic message routing, adaptive data streaming over wireless networks. Significant applications have been identified in environmental monitoring, surveillance of restricted areas, object searching in large fields, and supprt in rescuing operations. A tentative consortium has been identified for a STREP project proposal.

5.4.6 Meeting: Flexible Scheduling Technologies

Dates	July 6, 2005
Venue	Gran Hotel, Fundació “La caixa” Palma de Mallorca Spain
Main Organiser	Guillem Bernat University of York
Objectives	Preparation of a EU research project proposal on contract-based scheduling
Overview of the Agenda	Name of project Partners Responsibilities for workpackages and tasks Deadlines

	Talking to the commission IP issues
Conclusions	The name of the project was decided to be FRESCOR. The consortium was settled with 11 partners. Workpackages were broken into tasks, and responsible people were assigned. A work plan was established for the proposal writing. Intellectual property issues were discussed and a plan was sketched for the proposal.

5.4.7 Meeting: Resource Management for Consumer Electronics

Dates	July 8, 2005
Venue	Gran Hotel, Fundació “La caixa” Palma de Mallorca, Spain
Main Organiser	Gerhard Fohler Mälardalen University
Objectives	The objective of the meeting was to identify concrete and specific research issues in adaptive resource management for consumer electronics, led by MDH in cooperation with Philips research.
Overview of the Agenda	Academic research issues in resource management with respect to cache and multi-resource scheduling; Industrial issues with research results on the topics.
Conclusions	The meeting was useful to identify relevant academic issues, in particular resource management, with respect to cache and multi-resource scheduling as interesting topics.
Next meetings planned	Resource Management for Consumer Electronics August 17, 2005 Organized by Gerhard Fohler, Mälardalen University

5.4.8 Meeting: Resource Management for Consumer Electronics

Dates	August 17, 2005
Venue	Philips Research Eindhoven
Main Organiser	Gerhard Fohler Mälardalen University
Objectives	The objective of the meetings was to identify concrete and specific research issues in adaptive resource management for consumer electronics, led by MDH in cooperation with Philips research.
Overview of the Agenda	Academic research issues in resource management with respect to cache and multiresource scheduling; industrial issues with research results on topics.
Conclusions	The meeting was helpful for identifying the actual issues around scheduling, e.g., various granularities, resources, and overheads on existing plaforms as topics for a future encounter with industrial engineers.

	These topics were agreed to have the most discrepancy between industrial practice and academic research.
Next meetings planned	Encounter industrial engineers and academic researchers on specific research issues in resource management for consumer electronics Currently, the workshop is planned for October, dates are to be confirmed. organised by: Gerhard Fohler, MDH and Liesbeth Steffens, Philips Research.

5.4.9 Meeting: QoS aware components

Dates	May 30, 2005
Venue	ETSI Telecomunicación Madrid, Spain
Main Organiser	Alejandro Alonso Universidad Politécnica de Madrid
Objectives	The goal was to push forward the QoS aware components by stablishing a personal contact and identifying the topics of interest and work in progress in the different partners. The meeting should allow identifying potential integration activities and plan future work.
Overview of the Agenda	The agenda was partitioned in two parts. Initially, all the groups presented their research activity and interests with respect to the topic of the activity. Then, a discussion started with the goal of identifying and prioritazing the integration activities.
Conclusions	The key research issues identifyed by the partners include: UML QoS components, modeling and composing QoS components, extraction of QoS-information and transformation to alternative notations, integration of resource information, containers & configuration for components infrastructure, modeling QoS management API, components assemble and QoS Component frameworks.

5.5 Cluster Participants

5.5.1 Core Partners

Institution	Researcher
University of Pavia **Focus:** **real-time systems** **Team Leader :** **Giorgio Buttazzo, Prof.**	**Giorgio Buttazzo** Main areas of research: real-time scheduling, QoS management, control applications Other projects involved in: EU projects: OCERA, FIRST, ARTIST-5FP; 1 national project on open source software for distributed embedded systems; 1 national project on distributed mobile sensing for surveillance applications; Artist2 activities and role: JPIA Platforms: A common infrastructure for adaptive real-time systems – Coordination activity for platform distribution. JPRA NoE: Adaptive real-time, HRT and Control – Adaptive real-time scheduling techniques. JPRA Cluster: Flexible Scheduling Technologies – Aperiodic server mechanisms for event-driven scheduling. JPRA Cluster: Adaptive Resource Management for Consumer Electronics – Scheduling mechanisms for temporal isolation.
	Tullio Facchinetti Main areas of research: wireless communication protocols, distributed systems Other projects involved in: EU projects: ARTIST-5FP; 1 national project on open source software for distributed embedded systems; 1 national project on distributed mobile sensing for surveillance applications; Artist2 activities and role: JPIA Platforms: A common infrastructure for adaptive real-time systems – support for teaching and maintaining the shared platform.

Mauro Marinoni

Main areas of research:
power management and energy-aware scheduling.

Other projects involved in:

EU projects: ARTIST-5FP;

1 national project on open source software for distributed embedded systems;

1 national project on distributed mobile sensing for surveillance applications;

Artist2 activities and role:

JPIA Platforms: A common infrastructure for adaptive real-time systems – support for teaching and maintaining the shared platform.

Gianluca Franchino

Main areas of research:
wireless communication protocols, distributed systems

Other projects involved in:

1 national project on open source software for distributed embedded systems;

1 national project on distributed mobile sensing for surveillance applications;

Artist2 activities and role:

JPIA Platforms: A common infrastructure for adaptive real-time systems – support for teaching and maintaining the shared platform.

Institution	Researcher
University of Aveiro **Focus:** **real-time networks** **Team Leader :** **Luis Almeida, Prof.**	**Luis Almeida** Main areas of research: real-time networks, distributed systems, robot applications. Other projects involved in: ARTIST-5FP; 1 national project on development of cooperative autonomous mobile robots; 1 national project on science education through mobile robotics and embedded systems Artist2 activities and role: JPIA Platforms: A common infrastructure for adaptive real-time systems – Support for real-time network protocols. JPRA NoE: Adaptive real-time, HRT and Control – adaptation of control parameters based on communication load. JPRA Cluster: Flexible Scheduling Technologies – Scheduling algorithms in industrial networks. JPRA Cluster: Adaptive Resource Management for Consumer Electronics – Bandwidth adaptation in wireless networks.
	Paulo Pedreiras Main areas of research: network communication protocols, distributed systems Other projects involved in: EU projects: ARTIST-5FP; 1 national project on development of cooperative autonomous mobile robots; Artist2 activities and role: JPIA Platforms: A common infrastructure for adaptive real-time systems – technical support for network communication and distributed applications. JPRA NoE: Adaptive real-time, HRT and Control – adaptation of control parameters based on communication load. JPRA Cluster: Flexible Scheduling Technologies – Scheduling algorithms in industrial networks. JPRA Cluster: Adaptive Resource Management for Consumer Electronics – Bandwidth adaptation in Ethernet networks for video streaming

Jose Alberto Fonseca

Main areas of research:
embedded networks and network interfacing.

Other projects involved in:

EU projects: ARTIST-5FP;

Artist2 activities and role:

JPIA Platforms: A common infrastructure for adaptive real-time systems – support for teaching and developing distributed applications.

JPRA NoE: Adaptive real-time, HRT and Control – adaptation of control parameters based on communication load.

Ricardo Marau

Main areas of research:
embedded networks and network interfacing.

Other projects involved in:

1 national project on development of cooperative autonomous mobile robots;

Artist2 activities and role:

JPIA Platforms: A common infrastructure for adaptive real-time systems – Development of the FTT-Ethernet protocol based on Shark.

JPRA Cluster: Flexible Scheduling Technologies – Scheduling algorithms in industrial networks.

JPRA Cluster: Adaptive Resource Management for Consumer Electronics – Bandwidth adaptation in Ethernet networks for video streaming

Francisco Borges

Main areas of research:
embedded networks and network interfacing.

Other projects involved in:

EU projects: ARTIST-5FP;

Artist2 activities and role:

JPIA Platforms: A common infrastructure for adaptive real-time systems – development of setups for embedded real-time Ethernet

	Frederico Santos Main areas of research: wireless networks, robot architectures. Other projects involved in: 1 national project on development of cooperative autonomous mobile robots; Artist2 activities and role: JPIA Platforms: A common infrastructure for adaptive real-time systems – development of wireless communication protocols for robot cooperation
	Ana Antunes Main areas of research: distributed embedded control systems Other projects involved in: None Artist2 activities and role: JPRA NoE: Adaptive real-time, HRT and Control – adaptation of control parameters based on communication load.
	Alexandre Mota Main areas of research: distributed embedded control systems Other projects involved in: None Artist2 activities and role: JPRA NoE: Adaptive real-time, HRT and Control – adaptation of control parameters based on communication load.

Institution	Researcher

Mälardalen University **Focus:** **real-time systems and media processing** **Team Leader :** **Gerhard Fohler, Prof.**	**Gerhard Fohler** Main areas of research: real-time systems and networks, video streaming, media prcoessing Other projects involved in: ARTIST-5FP; FABRIC, BETSY Artist2 activities and role: JPIA Platforms: A common infrastructure for adaptive real-time systems – Support for real-time network protocols. JPRA NoE: Adaptive real-time, HRT and Control – Feedback control on communication. JPRA Cluster: Flexible Scheduling Technologies – Scheduling algorithms in industrial networks. JPRA Cluster: Adaptive Resource Management for Consumer Electronics – Bandwidth adaptation in wireless networks.
	Damir Isovic Main areas of research: real-time mediaprocessing Other projects involved in: EU projects: ARTIST-5FP; BETSY Artist2 activities and role: JPRA Cluster: Adaptive Resource Management for Consumer Electronics – Bandwidth adaptation in wireless networks.

Institution	Researcher
Universidad Politecnica de Madrid **Focus:** **real-time systems** **Team Leader :** **Juan A. de la Puente, Prof.**	**Juan A. de la Puente** Main areas of research: real-time scheduling, control applications Other projects involved in: EU projects: ASSERT, MODELWARE, ARTIST-5FP; 1 national project on support for distributed real-time systems and QoS resource management Artist2 activities and role: JPRA NoE: Adaptive real-time, HRT and Control – Application of real-time scheduling techniques to control systems. JPIA Platforms: A common infrastructure for adaptive real-time systems – real-time operating systems and distributed real-time systems
	Alejandro Alonso Main areas of research: QoS and resource management, consumer electronics, software engineering. Other projects involved in: EU projects: HIJA, Space4U, MODELWARE, ARTIST-5FP; 1 national project on support for distributed real-time systems and QoS resource management Artist2 activities and role: JPRA Cluster: QoS aware components – Activity coordinator. QoS specification in components, QoS characteristics composition, component frameworks. JPRA Cluster: Adaptive Resource Management for Consumer Electronics – Resource management of CPU, power and networks. QoS support.

Juan Zamorano

Main areas of research:

real-time operating systems, distributed real-time systems.

Other projects involved in:

EU projects: ASSERT, MODELWARE, ARTIST-5FP;

1 national project on support for distributed real-time systems and QoS resource management

Artist2 activities and role:

JPIA Platforms: A common infrastructure for adaptive real-time systems – adding QoS to the the shared platform.

Miguel A. de Miguel

Main areas of research:

Model Driven Architecture, QoS specification and composition

Other projects involved in:

EU projects: MODELWARE, HIJA, ARTIST-5FP;

1 national project on support for distributed real-time systems and QoS resource management

Artist2 activities and role:

JPRA Cluster: QoS aware components – QoS specification with UML profiles. Extraction of QoS characteristics.

5.5.2 Affiliated Industrial Partners

Company	Researcher
EVIDENCE s.r.l. **Focus:** **real-time kernels and developing tools for embedded systems** **Team Leader :** **Paolo Gai, PhD**	**Paolo Gai** Main areas of research: real-time operating systems Other projects involved in: EU projects: OCERA, FIRST, ARTIST-5FP; Artist2 activities and role: JPIA Platforms: A common infrastructure for adaptive real-time systems - Support for kernel maintenance JPRA Cluster: Flexible Scheduling Technologies – Modular design of kernel mechanisms

5.5.3 Affiliated Academic Partners

Institution	Researcher
Scuola Superiore di Studi Universitari e di Perfezionamento Sant' Anna **Focus:** **real-time embedded systems** **Team Leader :** **Giuseppe Lipari, Prof.**	**Giuseppe Lipari** Main areas of research: real-time systems, operating systems, developing tools Other projects involved in: EU projects: OCERA, FIRST, ARTIST-5FP; Artist2 activities and role: JPIA Platforms: A common infrastructure for adaptive real-time systems – Support for teaching and distributing the shared platform. JPRA Cluster: Flexible Scheduling Technologies – Resource reservation methods for overrun handling. JPRA Cluster: Adaptive Resource Management for Consumer Electronics – Bandwidth reservation techniques.

	Paolo Valente Main areas of research: network and disk scheduling methodologies Other projects involved in: Artist2 activities and role: JPRA Cluster: Flexible Scheduling Technologies – Flexible network scheduling. JPRA Cluster: Adaptive Resource Management for Consumer Electronics – Disk scheduling in multimedia applications.
	Enrico Bini Main areas of research: Schedulability analysis and energy-aware computing Other projects involved in: Artist2 activities and role: JPRA Cluster: Flexible Scheduling Technologies – Analysis of hierarchical scheduling schemes.

Institution	Researcher
University of Catania **Focus:** **real-time networks and distributed systems** **Team Leader :** **Lucia Lo Bello, Prof.**	**Lucia Lo Bello** Main areas of research: real-time networks and distributed systems. Other projects involved in: 1 national project on distributed mobile sensing for surveillance applications; Artist2 activities and role: JPIA Platforms: A common infrastructure for adaptive real-time systems – Support for networks protocols and distributed applications. JPRA Cluster: Flexible Scheduling Technologies – Stochastic scheduling and distributed systems.

	Orazio Mirabella Main areas of research: networks and distributed systems Other projects involved in: 1 national project on distributed mobile sensing for surveillance applications; Artist2 activities and role: JPIA Platforms: A common infrastructure for adaptive real-time systems – Support for teaching and distributed applications. JPRA Cluster: Flexible Scheduling Technologies – Stochastic scheduling and distributed systems.

Institution	Researcher
Universidad Carlos III de Madrid **Focus:** **Real-time middleware, distributed systems, QoS management** **Team Leader :** **Marisol García-Valls, Prof.**	**Marisol Garcia-Valls** Main areas of research: Real-time support in middleware and distributed systems, QoS management, Java networked embedded applications Other projects involved in: EU projects: ARTIST-5FP; MUSE ARTIST2 activities and role: JPRA: Cluster Integration: Adaptive resource management for consumer electronics - QoS management JPIA Platforms: A common infrastructure for adaptive real-time systems - QoS management architectures in middleware JPRA NoE Integration: QoS Aware components - QoS component infrastructures

Carlos Delgado-Kloos

Main areas of research:

Synchronous languages, formal methods, real-time languages, applications for educational platforms

Other projects involved in:

EU projects: ARTIST-5FP; GENIUS; E-LANE

ARTIST2 activities and role:

JPIA Platforms: A common infrastructure for adaptive real-time systems - QoS management architectures in middleware

JPRA NoE Integration: QoS Aware components - QoS component infrastructures

5.6 Research and Platform Activities

5.6.1 *JPRA-Cluster Integration:* Flexible Scheduling Technologies

Leader	Giorgio Buttazzo (Pavia: dynamic scheduling and overload management techniques)
Policy Objective	Many applications domains (including robotics, automotive and multimedia systems) require the execution of many concurrent activities with different criticality and timing constraints (e.g., periodic, aperiodic, time driven, event driven tasks) for which a single scheduling policy is not sufficient to satisfy the different requirements of the application. Hence, the objective of the research is to exploit the excellence of the different teams for developing a real-time scheduling framework capable of handling various types of tasks with different real-time requirements in the same system. The challenge is to develop an efficient resource manager that can be adopted in next generation kernels to perform adaptive QoS control of time sensitive applications with dynamic characteristics..

5.6.2 *JPRA-Cluster Integration:* Adaptive Resource Management for Consumer Electronics

Leader	Gerhard Fohler (Mälardalen University: handheld devices)
Policy Objective	Leveraging on the critical mass afforded by ARTIST2, tackle adaptive QoS techniques that can be applied to a diversity of applications fields, from consumer electronics to embedded control equipment. Analysis of resource usage tradeoffs - processing, communication, etc – to provide support for adaptive QoS techniques and achieve higher resource efficiency. This means either adding more functionality without increased CPU power or network bandwidth, or assigning the available resources dynamically in a way that maximizes the QoS delivered to the application

5.6.3 *JPRA-NoE Integration*: Participation in activities led in other clusters

Beyond the NoE-Integration activities described here, the cluster “Adaptive Real Time” is also involved in the NoE Integration activities: “Semantic Framework for Hard Real-Time Design Flow ”, “Merging the Event-triggered and Time-triggered Paradigms”, and “Adaptive Real-time, HRT and Control”.

5.6.3.1 **JPRA-NoE Integration***: QoS aware Components*

Leader	Alejandro Alonso (UP Madrid: QoS component infrastructures)
Clusters	Adaptive Real-Time Modelling and Components
Policy Objective	QoS management is one of the most important concerns in design of real-time systems. We will bring together competencies in component-based design for hard and adaptive real-time systems, to produce advances that would be difficult to achieve without all three. To achieve its aims, this activity requires competency in component models, middleware, networking infrastructures.

5.6.4 *JPIA-Platform*: A common infrastructure for adaptive Real-time Systems

Leader	Giorgio Buttazzo (Univ. of Pavia: real-time scheduling, robotic systems and interfacing)
Policy Objective	The objective is to show how current operating systems and network protocols have to be extended to support emerging real-time applications that exhibit a high degree of complexity and operate in dynamic environments. The impact on operating system standards (like RT-POSIX and OSEK) as well as network protocols will also be taken into account.

6. Cluster: Compilers&TA – Timing Analysis

Contributor: Prof. Reinhard Wilhelm – Saarland University

6.1 Description of the Area

Run-time guarantees play an important role in the area of embedded systems and especially hard real-time systems. These systems are typically subject to stringent timing constraints which often result from the interaction with the surrounding physical environment. It is essential that the computations are completed within their associated time bounds; otherwise severe damages may result. Therefore, a schedulability analysis has to be performed which guarantees that all timing constraints will be met (also called timing validation). All existing techniques for schedulability analysis require the worst case execution time (WCET) of each task in the system to be known before the task is executed. Since in general, the problem of computing WCETs is not decidable, estimations of the WCET have to be calculated. These estimations have to be safe, i.e., they may never underestimate the real execution time. Furthermore, they should be tight, i.e., the overestimation should be as small as possible.

In modern microprocessor architectures caches and pipelines are key features for improving performance. Unfortunately, they make the analysis of the execution behaviour of instructions very difficult since this behaviour now depends on the execution history. Therefore, the classical approaches to worst case execution time prediction are not directly applicable or lead to results exceeding the real execution time by orders of magnitude. This may influence the degree of success of timing validations or may lead to a waste of hardware resources and more expensive hardware. For products which are manufactured in high quantity, e.g., in the automobile or telecommunications markets this possibly results in high expenses.

6.1.1 Main Research Trends

A standard tool architecture for WCET analysis has evolved. In a first phase, which may itself consist of several subphases, the software is analyzed to determine invariants about the sets of execution states at each instruction. Abstract interpretation is mostly used for this phase.The invariants allow the prediction of conservative execution times for individual instructions and for basic blocks. A second phase determines a worst-case path through the program. This is often done by implicit path enumeration; the control flow is translated into an integer linear program and then solved.

/* suggestion from Peter Puschner: add some mention of control-flow analysis */

The results are more precise if a strong analysis of the control flow is performed. The compiler that has translated the source program into the executable often has valuable information about the control flow. Making this information available is a promising avenue.

The construction of timing-analysis tools is difficult, tedious, and error-prone. Research is on the way to develop computer support for this task.

For non-hard real time tasks, measurement-based methods are being evaluated and tested.

6.1.2 Industrial Applications

Timing-Analysis tools have recently entered industrial practice and are in routine use in the aeronautics and automotive industry. Precision of the results is good, efficiency is tolerable, and usability needs improvement.

6.2 State of Integration in Europe

6.2.1 European Research Teams

Saarland University, Germany: compilers and timing analysis tools, design for predictability.
AbsInt, Germany: compilers and timing analysis, tool provider.
Tidorum, Finland, Timing-Analysis, tool provider.
University of York, UK, measurement-based Timing-Analysis Tools, schedulability.
Mälardalen University, Timing-Analysis Tools, in particular Flow Analysis.
IRISA, measurement-based Timing-Analysis Tools.
TU Vienna, Timing-Analysis Tools and temporally predictable HW-SW architectures.

6.2.2 Interaction of the Cluster with other Communities

Close cooperation has started with the Execution-Platform cluster, in particular with Lothar Thiele and Luca Benini.

6.2.3 Main Aims for Integration through Artist2

Agreement on a platform architecture and on tool interfaces.

6.3 Overall Assessment and Vision for the Cluster

6.3.1 Assessment

- The timing-analysis work in the cluster partly suffers from the success of previous research. This research has solved several central problems, in particular the prediction of the architectural behaviour for single tasks on uniprocessors. This problem can be regarded as being essentially solved. However, the development of the corresponding tools is tedious and error-prone. Research to support tool development is still needed. This research, however, is concentrated in Saarbrücken only.
- Program-flow analysis needs to be integrated with path analysis. This is planned for the later phase of the project.
- Several partners consider measurement-based methods and tools. While these can not give guarantees they may give a feel for the distance between predictions and reality and are of interest for applications where QoS is of importance, e.g. multimedia applications.
- Europe is still leading the field. Only light competition exists in the US and in Singapore.
- USaar has started cooperation about design for predictability with partners in the Execution-Platform cluster, ETHZ, Bologna, and Dortmund.
- Mälardalen will componentize its flow-analysis methods.
- Mälardalen and Vienna have been working on programming-support strategies for writing code with good timing predictability.
- Vienna has developed concepts to maintain the control-flow information needed for WCET analysis during the code transformations of optimizing compilers.
- Critical Mass is definitely present in the cluster. Two measurement-based partners and 4 analytical partners are enough to develop synergies.

6.3.2 Vision and Long-Term Goals

The cooperation will strengthen the position of European toolmakers in industry. Usability of the tools and precision of the results will be further improved.

The next step is the integration of the single-task-on-uniprocessor methods and tools into tools considering distributed and communication-centric systems. These approaches are represented in the Cluster Execution Platforms.

6.3.3 Recommendations

- Tidorum should become a full-fledged partner, as it contributes heavily to the work in the cluster.
- A new activity is the integration of a compiler with a timing-analysis tool to obtain more information about program flow.
- Mälardalen together with York will establish a benchmark for time-critical programs to evaluate timing-analysis tools.

- USaar will implement a way to store the instruction-set semantics into CRL2 as needed by Tidorum and Mälardalen.
- York and Vienna will further develop measurement-based/hybrid timing-analysis strategies.

6.4 Meetings Held

6.4.1 Meeting: Kick-off Meeting

Dates	September, 6 – 7, 2004
Venue	International Conference and Research Center for Informatics, Schloss Dagstuhl, Germany
Main Organiser	Reinhard Wilhelm Saarland Unversity
Web link	<Once this is on the web, provide the link here.>
Objectives	Resuming the state of the art of the participating groups. Discussing ways of cooperation and goals for the platform activity.
Overview of the Agenda	1. Presentation of existing tools by the partners 2. Discussion of interface formats 3. Presentation of CRL2 as one potential interface format.
Conclusions	**Subgroup** Interfaces established Analysis by Mälardalen, Tidorum Ltd., U Saarland, AbsInt, TU Vienna, U Rennes. Goal: Design document incl. interfaces, annotation language, file formats Contributions by U York, TU Vienna: measurement-based evidence • Work on the Timing-Analysis platform ○ Definition of architecture and interfaces: Defining document Feb. 2005 (Interface subgroup) ○ Supporting and documenting the interfaces: Implementation August 2005 (AbsInt) ○ Demonstrator Feb. 2006 ○ Compiler integration of flow facts (U Mälardalen, TU Vienna) Prototype Feb. 2006 ○ Rights, Exploitation, Licensing • Interfaces are published ○ Components are owned by the partner who implemented them ○ Cooperation between tool vendors and academia: *tool evaluation in industry projects, research licenses* ○ Work on increasing Timing Predictability

	jointly with the *Execution-Platforms* cluster,
	will integrate Computation and Communication
	• Timing-Analysis Framework
	  ○ Design interface language for communication between components
	  ○ Adapt existing components to new language
	  ○ First experiments with component integration

Next meetings planned	CRL2 Meeting <date> organised by: Guillem Bernat (York University), Henrik Theiling (AbsInt) <title> November 2004 organised by: Guillem Bernat

6.4.2 Meeting: CRL2 Meeting

Dates	November 2004
Venue	Fundacio la Caixa Palma de Mallorca Spain
Main Organiser	Henrik Theiling, AbsInt
Web link	<Once this is on the web, provide the link here.>
Objectives	Clarify whether CRL2 would be a good starting point for exchange format
Overview of the Agenda	Presentations: Isabelle Puaut: Heptane, Andreas Ermedahl: NIC, Jan Lisper: Annotations; Discussion

Conclusions	CRL2 seems to suite all party's requirements, but for final evaluation, we need to:
	• Publish list of Annotations (AbsInt),
	• Before march:
	  ○ is syntax tree needed
	  ○ what annotations are needed
	  ○ how does NIC integrate (or does it at all)
	• clarify CRL2 license issues
	• how to link CRL2 library against ADA (Tidorum)

Next meetings planned	March 10, Reinhard Wilhelm

6.4.3 Meeting: Interface Language

Dates	March 10, 2005
Venue	Ludwig Maximilian Universität München München Germany
Main Organiser	Reinhard Wilhelm Saarland Unversity
Web link	<Once this is on the web, provide the link here.>
Objectives	Overview of industrial experience with WCET tools Define strategy towards the Common Interchange Format for the ARTIST2 Timing-Analysis Platform
Overview of the Agenda	• Report about activities (RW) • Deliverable: Specification of Interchange Format • Discussion about strategy • A challenge to CRL2 (NH) • Reports about Industrial Experience • Editing of ARTIST WCET Tool Survey
Conclusions	Definition of test cases for the interface language: • Transfer NEC V850E binary reader of aiT to Mälardalen and Basic-Block Timing-Analysis from Mälardalen to aiT • Transfer annotated CRL2 between Bound-T and aiT or • Transfer path lengths between Mälardalen longest-path search tool and aiT • Integrating Mälardalen's Flow Analysis with aiT's processor-behavior prediction (long term)
Next meetings planned	Interface and Compiler Meeting July 4, 2005 organised byReinhard Wilhelm

6.4.4 Meeting: Interface and Compiler Meeting

Dates	July 4, 2005
Venue	Hotel Saratoga Palma de Mallorca Spain
Main Organiser	Reinhard Wilhelm Saarland Unversity
Web link	<Once this is on the web, provide the link here.>
Objectives	Discussing progress and additional requirements as to CRL2 and integration issues between Compilers and Timing Analysis
Overview of the Agenda	• Compiler + Timing Analysis Intergration • Representation of Semantics in CRL2

Conclusions	• Compiler + Timing Analysis integration based on LANCE
	  ○ Björn Lisper, Uni Dortmund
	  ○ AbsInt
	  ○ Possibly Tidorium
	• Representation of Semantics in CRL2
	  ○ Format to be fixed (“NIC - - “?)
	  ○ Exchange examples for semantics specification (ANDF, TDL, …)

Next meetings planned	<title> November 8 organised by: Reinhard Wilhelm <title> <date> organised by: <main organiser>

6.5 Cluster Participants

6.5.1 Core Partners

Institution	Researcher
Saarland University **Focus:** **Timing Analysis and Compilation** **Team Leader :** **Reinhard Wilhelm, Professor**	**Reinhard Wilhelm, Prof.** Main areas of research: Timing Analysis Other projects involved in: AVACS Artist2 activities and role: Timing-Analysis Platform Cluster Director
	Oleg Parshin Main areas of research: Timing Predictability Other projects involved in: ARTIST Artist2 activities and role: Resource-aware design Core partner project member
	Stephan Thesing Main areas of research: Timing Analysis Other projects involved in: AVACS Artist2 activities and role: Timing Analysis Platform Core partner project member
	<Name> Main areas of research: <areas> Other projects involved in: <projects> Artist2 activities and role: <activity name (please use the exact name)> <role in year 1>
Institution	Researcher

Institution	Researcher
Dept. of Computer Science and Electronics, Mälardalen University, Sweden. **Focus:** **Static WCET analysis** **Team Leader :** **Björn Lisper, Prof.**	**Björn Lisper, Prof.** Main areas of research: Static WCET analysis, programming languages Other projects involved in: none Artist2 activities and role: Timing-Analysis Platform core partner project leader
	Andreas Ermedahl, Dr. Main areas of research: Static WCET analysis Other projects involved in: none Artist2 activities and role: Timing-Analysis Platform core partner project member
	Jan Gustafsson, Dr. Main areas of research: Static WCET analysis Other projects involved in: none Artist2 activities and role: Timing-Analysis Platform core partner project member
	Christer Sandberg, PhD student Main areas of research: Static WCET analysis Other projects involved in: none Artist2 activities and role: Timing-Analysis Platform core partner project member

Vienna University of Technology **Focus:** **Timing Analysis, Hybrid WCET Analysis, Temporally Predictable HW-SW Architectures** **Team Leader :** **Peter Puschner, Professor**	**Peter Puschner** Main areas of research: Temporally Predictable HW-SW Architectures, Timing Analysis Other projects involved in: MoDECS, DECOS, Te-DES Artist2 activities and role: Timing-Analysis Platform leader of WCET activities in Vienna
	Raimund Kirner Main areas of research: Timing Analysis, Compilers and Timing Analysis, Hybrid WCET Analysis Other projects involved in: MoDECS, Te-DES Artist2 activities and role: Timing-Analysis Platform researcher
	Ingomar Wenzel Main areas of research: Hybrid WCET Analysis Other projects involved in: MoDECS, Te-DES Artist2 activities and role: Timing-Analysis Platform researcher

6.5.2 Affiliated Academic Partners

Institution	Researcher
IRISA **Focus:** **Timing analysis** **Team Leader :** **Isabelle Puaut, Professor**	**Isabelle Puaut** Main areas of research: Worst-Case Execution Time Analysis Artist2 activities and role: Timing Analysis Platform

6.6 Research and Platform Activities

6.6.1 ***JPRA-Cluster Integration**:* Architecture-aware compilation

Leaders	Reinhard Wilhelm (Saarland University: co-leader, program analysis tools) Rainer Leupers (RWTH Aachen: co- leader, code optimization, retargetable compilation)
Policy Objective	The objective of this activity is to exploit the world-leading position and expertise of academic and industrial cluster partners in order to integrate and further develop the technology currently available with the partners, so as to provide a unified architecture-aware code-synthesis and compiler methodology to a variety of users, also beyond ARTIST.

6.6.2 ***JPRA-NoE Integration***: Participation in activities led in other clusters

The cluster "Compilers and Timing Analysis" is involved in the NoE Integration activities: "Resource-aware Design".

6.6.3 *JPIA-Platform*: Timing - Analysis Platform

Leader	Reinhard Wilhelm (Saarland University: Timing Analysis, Coordinator)
Policy Objective	Combine the best components of existing European Timing-Analysis tools and prototypes in a standard tool architecture with well-defined textual interfaces. Our objective is to integrate European efforts on the Timing Analysis of Real-Time Systems, to preserve the existing lead of European Research and Industry in this important sector. The resulting platform will be used in teaching the technology all over Europe.

6.6.4 *JPIA-Platform*: Compilers Platform

Leader	Rainer Leupers (RWTH Aachen: co-leader, compilers)
Policy Objective	The objective is to provide world-class code-synthesis and compiler tools for the generation of efficient machine code. Goals of the cluster include the integration of existing compiler-generation approaches allowing compilers for new architectures to be built quickly, efficiently and reliably. One goal of the compilers sub-cluster is to achieve a tighter integration of European R&D activities by building on a carefully chosen industrial re-targetable compiler development platform that ensures interoperability. The CoSy compiler platform provided by ACE is a state-of-the-art software system on which the common activities will build. This will reinforce Europe's leading position in the area of compilers for embedded processors. Also, the partners aim at making existing advanced optimization algorithms

	available to designers of embedded systems. Finally, advanced high-level source-to-source transformations will be made available to users.

7. Cluster: Compilers&TA - Compilers

Contributor: Rainer Leupers – RWTH Aachen

7.1 Description of the Area

7.1.1 Main Research Trends

Embedded system software –if compared to hardware- usually involves a significant overhead in terms of energy consumption and execution time. However, for flexibility reasons, hardware cannot be used in applications with changing requirements. In order to make a software implementation feasible, efficiency of embedded software is a must. Various approaches for achieving this efficiency have been explored.

Due to the efficiency requirements, using power-hungry, high-performance off-the-shelf processors from desktop computers is infeasible for many applications. Therefore, the use of customized processors is becoming more common. These processors are optimized for a certain application domain or a specific application. As a consequence, hundreds of diffeent domain or even application specific programmable processors (ASIPs) have appeared in the semiconductor market, and this trend is expected to continue. Prominent examples include low-cost/low-energy microcontrollers (e.g. for wireless sensor networks), number-crunching digital signal processors (e.g. for audio and video codecs), as well as network processors (e.g. for internet traffic management). While assembly language used to be predominant in embedded processor programming for quite some time, the increasing complexity of embedded application code now makes the use of high-level languages like C and C++ just as inevitable as in desktop application programming. Therefore all these devices demand for their own programming environment, obviously including a high-level language (mostly ANSI C) compiler. This requires the capability of quickly designing compilers for new processors, or variations of existing ones, without the need to start from scratch each time. While compiler design traditionally has been considered a very tedious and man-power intensive task, contemporary retargetable compiler technology makes it possible to build operational (not heavily optimizing) C compilers within a few weeks and more decent ones approximately within a single man-year. Therefore retargetable compilers have been recognized as key tools for several years. Naturally, the exact effort heavily depends on the complexity of the target processor, the required code optimization and robustness level, and the engineering skills. However, compiler construction for new embedded processors is now certainly much more feasible than a decade ago. This permits to employ compilers not only for application code development, but also for optimizing an embedded processor architecture itself, leading to a true "compiler/architecture codesign" technology that helps to avoid hardware-software mismatches long before silicon fabrication.

Source-to-source level transformations are another approach for improving the efficiency of embedded software. These transformations are applied before any compiler is started. To some extent, these transformations are independent of the final processor architecture. Therefore, the advantage of this approach is that it can be used with almost any compiler. It can also be used in combination with retargetable compilation.

A third approach is the use of sophisticated optimizations within a compiler. Optimizations tuned towards embedded systems have been designed by a number of members of the ARTIST compiler cluster.

Due to the increasing importance of the memory interface, various optimizations have been designed that help to maximize the efficiency of the memory interface. These optimizations can be either integration into compilers or used as source-to-source level optimizations.

7.1.2 Industrial Applications

Retargetable compilers, as part of ASIP architecture exploration platforms, are now widely accepted industrial tools. There is a general trend in the industry to replace non programmable hardware accelerators (NPAs) with flexible reconfigurable cores, which have specialized resources and instructions dedicated to a class of applications. This reconfigurable cores create real new challenges for embedded development tools and more especially for the compiler and new challenge for architecture investigation tools for the end user. Examples of such cores are Xtensa from Tensilica, ARC600 and700 from ARC, CorXtend from MIPS.

An example of flexible development tools is the Coware/LISATek processor and compiler designer based on CoSy Express, or the toolsets proposed by Tensilica and ARC for their core extension development. Example applications of ASIPs include: audio processing, video processing and data streaming applications in the TV, Set Top box, DVD player and recorder, mobile, base stations, printer and disk drive markets.

7.2 State of Integration in Europe

7.2.1 European Research Teams

- Within the ARTIST2 project, RWTH Aachen focuses on retargetable compilers and code optimization for embedded processors. RWTH Aachen closely cooperates with ACE and CoWare Inc. on the LISATek Compiler Designer product, based on the CoSy compiler system that is also used as the primary compiler platform within ARTIST2.
- Dortmund University: memory-aware code optimization, source-level code optimization
- STMicroelectronics: embedded processor design, tools adaptation
- Absint: compiler and timing analysis tools
- IMEC: SoC design tools, source-level code optimization
- ACE: compiler platform provider
- TU Vienna: program analysis and optimization

7.2.2 Interaction of the Cluster with other Communities

A close cooperation exists with the ARTIST2 Execution Platforms cluster, in particular between Dortmund, Aachen, and Bologna University. RWTH Aachen participates to the HiPEAC network of excellence and is starting up new cooperations related to code optimization, e.g. with Edinburgh University. Furthermore, Aachen maintains tight industry cooperations, e.g. with CoWare, ACE, Infineon, Texas Instruments, and Samsung. TU Vienna maintains a close interaction with the Lawrence Livermore National Laboratory, CA, USA, in optimizing high-level abstractions.

7.2.3 Main Aims for Integration through Artist2

One goal is the combination of areas of excellence of the different partners by defining and implementing interfaces between their design flows and tools in order to achieve compilation platforms applicable to a wider problem scope. In the compiler cluster, this is implemented by the formation of several topic-specific “mini-clusters”, partially based on a common compiler platform (Cosy). This form of integration works well and will be intensified in the future.

7.3 Overall Assessment and Vision for the Cluster

7.3.1 Assessment

The compilers cluster partially suffers from the presence of relatively fragmented research topics and tool environments. Different partners have different research interests and design tools. Coupling of completely separated tools within one single platform requires huge manpower, which not all partners are willing to invest. This issue has been resolved by the formation of several topic-specific “mini-clusters”, each typically comprising 2-3 partners. Thanks to this fine grained structure, a number of successful new cooperations have been established, and previously existing cooperations have been extended. The cluster participants believe that by the mini-cluster formation a sufficient critical mass has been achieved for day-to-day research activities. Still, global coordination of the compilers cluster takes place via regular cluster-wide meetings.

7.3.2 Vision and Long-Term Goals

The cooperation will strengthen the position of European toolmakers in industry. Usability of the tools and precision of the results will be further improved. The compilers cluster emphasizes this vision by active participation of key industrial players such as STM and ACE. The cooperations begun in ARTIST2 year one will be intensified, and new upcoming research challenges will be taken up together by the participants in order to exploit synergy effects right from the start. The long-term goal is a stable, self-sustained cluster structure, naturally open to new research teams with excellence in specific new areas.

7.3.3 Recommendations

Integration and research activities are generally running well and already led to first results in terms of demonstrators, joint publications etc. The division of the compilers cluster into loosely coupled mini-clusters turned out to be the right choice in this area. It is highly recommended to retain this structure. Simultaneously, the cluster will look out for new partners (e.g. TH Karlsruhe, Univ. of Erlangen) to complete the research and integration scope. Specifically, it is recommended to promote ACE into a core member of the cluster, due to their key role in providing the compiler platform infrastructure.

7.4 Meetings Held

7.4.1 Meeting: compiler kickoff meeting

Dates	20.9.2004
Venue	RWTH Aachen, Germany
Main Organiser	Rainer Leupers RWTH Aachen
Web link	
Objectives	Presentation of partners´ research activities and identification of cooperation areas
Overview of the Agenda	Presentations by cluster members Discussion of technical challenges Planning
Conclusions	Tentative mini-cluster structure formed. Specific partnerships include: ACE/STM/Absint, Aachen/ACE, Dortmund/Aachen, Dortmund/Absint, IMEC/Dortmund
Next meetings planned	Compiler cluster meeting at DATE 2005 in Munich.

7.4.2 Meeting: PAG-Cosy Integartion

Dates	21.1.2005
Venue	ACE Associated Compiler Experts bv Amsterdam The Netherlands
Main Organiser	Christian Ferdinand AbsInt Angewandte Informatik GmbH
Web link	<Once this is on the web, provide the link here.>
Objectives	Study the technical challenges of a tight integrationand assess the integration effort
Overview of the Agenda	Presentation of CoSy wrt. PAG Presentation of PAG wrt. CoSy Discussion technical challenges Planning
Conclusions	The integration is feasible. The effort is currently not covered by other sources of funding. The integration will be part of a new project proposal. All concrete work depends on the funding situation.

7.4.3 Meeting: compiler cluster meeting

Dates	9.3.2005
Venue	LMU Munich, Germany (next to DATE 2005 conference)
Main Organiser	Rainer Leupers, Reinhard Wilhelm RWTH Aachen
Web link	
Objectives	Update of partners´ research activities and status of cooperation areas
Overview of the Agenda	Presentations by cluster members Discussion of technical challenges Planning
Conclusions	Mini-cluster structure refined, refocusing of common research and integration activities via definition of appropriate interfaces. Necessary software will be exchanged. Coarse milestones have been defined.
Next meetings planned	compiler cluster meeting 8.11.2005 organised by: ACE

7.4.4 Meeting: WCET-Aware Compiler

Dates	18.3.2005
Venue	Absint Angewandte Informatik GmbH Saarbrücken Germany
Main Organiser	Heiko Falk Universität Doermund
Web link	<Once this is on the web, provide the link here.>
Objectives	Discuss and define common infrastructure, access to IR and analysis results
Overview of the Agenda	Selection of target, CRL2, generation and access to IR and analysis results, compilation infrastructure, compatible compiler versions
Conclusions	Target is Infineon TriCore (1.3), exchange via CRL2, Uni Dortmund gets necessary software

7.5 Cluster Participants

7.5.1 Core Partners

Institution	Researcher
RWTH Aachen **Focus:** **Retargetable compilers** **Team Leader :** **Rainer Leupers**	**Rainer Leupers** Main areas of research: Other projects involved in: several EU, DFG, and industrial projects Artist2 activities and role: compiler cluster leader
	Gerd Ascheid Main areas of research: embedded system implementation Other projects involved in: several EU, DFG, and industrial projects
	Heinrich Meyr Main areas of research: wireless communication systems Other projects involved in: several EU, DFG, and industrial projects

7.5.2 Core Partners

Institution	Researcher
Saarland University **Focus:** **<(keywords)>** **Team Leader :** **<name>, <title(s)>**	**Reinhard Wilhelm** Main areas of research: Compiler Construction, Static Program Analysis, Timing Analysis Other projects involved in: Transregional Collaborative Research Centre AVACS of DFG Artist2 activities and role: Timing Analysis Platform

	Coordinator Resource-aware compilation partner
	Stephan Thesing Timing Analysis participant Other projects involved in: Transregional Collaborative Research Centre AVACS of DFG Artist2 activities and role: Timing Analysis Platform participant
	Oleg Parshin Main areas of research: Timing Analysis Other projects involved in: <projects> Artist2 activities and role: Resource aware compilation participant

7.5.3 Core Partners

Institution	Researcher
AbsInt Angewandte Informatik GmbH **Focus:** **Timing Analysis and Compilation** **Team Leader :** **Christian Ferdinand, Dr.-Ing.**	**Christian Ferdinand** Main areas of research: Timing Analysis and Compilation Other projects involved in: Verisoft, Embounded, ASTEC Artist2 activities and role: Timing-Analysis Platform Participant
	Reinhold Heckmann Main areas of research: Timing Analysis Other projects involved in: Verisoft, Embounded

	Artist2 activities and role: Timing-Analysis Platform Participant
	Daniel Kästner Main areas of research: Compilation and Optimization Other projects involved in: Embounded Artist2 activities and role: Compilers Platform Participant
	Henrik Theiling Main areas of research: Timing Analysis Other projects involved in: Verisoft Artist2 activities and role: Timing-Analysis Platform Participant

7.5.4 Core Partners

Institution	Researcher
STMicroelectronics **Focus:** **SoC integration** **Team Leader :** **Dr. Christian Bertin**	**Christian Bertin** Main areas of research: Dr Christian Bertin is the director of the ST/HPC Compilation Expertise Center. Home, Personal and Communication sector (HPC) is the most important group of ST, which develops all the consumer business of the company. HPC centralises the design, implementation, optimisation and integration into SOCs of all processors used by ST and its customers for embedded applications. Created in 1996, the compiler expertise center is now composed of 30 expert engineers in the area of highly optimized compilers for embedded applications. The strategy of the group is to focus on embedded compiler features, automatic flows from architecture definition to tools generation, and on optimizations that bring the best added value for ST processors (code size, speed and application portability). The compiler technologies used in the group are mostly open source (GNU C, Open64) or rely on 3rd licensed compiler technology (Codemist, Archelon, ACE, LISATek).

	The group cooperates with several french research laboratories on register allocation and I-cache optimisation (ENS Lyon/Compsys), on fast floating point arithmetic (ENS Lyon/Arenaire), optimal scheduling (IMAG/ID), automatic generation of controlled software (VERIMAG, IRISA Rennes). Further collaboration on machine description and instruction semantics with RWTH/Aachen is expected in 2005. Recently, new processors designed by ST to replace non programmable accelerators have challenged compielr technologies to support highly reconfigurable and extensible compiler and tools.

7.5.5 Core Partners

Institution	Researcher
Dortmund University **Focus:** **Memory aware compilation** **Team Leader :** **Prof. Dr. P. Marwedel**	**Prof. Dr. Peter Marwedel** Main areas of research: Prof. Dr. Peter Marwedel is the head of the embedded systems group at the University of Dortmund. The embedded systems group within the department of computer science was established in 1989. Initially, the focus was on the generation of electronic design automation (EDA) tools, with emphasis on high-level synthesis, microcode generation and processor self-test. This work was later extended to general code generation techniques for embedded systems. The efficiency of embedded software, in particular energy efficiency, became a key objective. The memory is expected to become more and more a bottleneck as the speed of processors is increasing at a faster rate than the speed of the memory. The group's research work addresses this "memory wall" and shows that a suitable combination of compiler and architecture design techniques can lead to fast, energy-efficient and timing-predictable memory interfaces. In 2003, Dr. Marwedel published a very influential text book on embedded system design which is setting standards worldwide. In the same year, he received the teaching award of his University. He is also heading the local technology transfer centre ICD. ICD is in charge of transforming research results into industrial products. ICD has designed several simulators, compilers and debuggers for industrial customers.

7.5.6 Affiliated Industrial Partners

Company	Researcher

ACE **Focus:** **compiler framework** **Team Leader :** **Hans van Someren**	**Hans van Someren** Main areas of research: Compilation and Optimization, Standardization

7.5.7 Affiliated Academic Partners

Institution	Researcher
IMEC **Focus:** **embedded system design (DESICS division)** **Team Leader :** **Prof. Rudy Lauwereins**	**Francky Catthoor** Main areas of research: Other projects involved in: Several EU and bilateral industrial projects Artist2 activities and role: Compiler Cluster participant <role in year 1>

7.5.8 Affiliated Academic Partners

(remove this section if there are none)

Institution	Researcher
TU Vienna **Focus:** **Compilers** **Team Leader :** **Andreas Krall, ao. Univ. Prof. Dipl.-Ing. Dr.**	Andreas Krall Main areas of research: compilers, just-in-time compilers, architectures Other projects involved in: Christian-Doppler Lab Compilation Techniques for Embedded Processors Artist2 activities and role: compilers platform participant
	Markus Schordan Main areas of research: program analysis, source-to-source transformation, library aware optimization Other projects involved in: ROSE (Lawrence Livermore National Laboratory,USA) Artist2 activities and role: compilers platform participant

8. Cluster: Execution Platforms

Contributor: Prof. Lothar Thiele - ETHZ

8.1 Description of the Area

8.1.1 Main Research Trends

Embedded systems are computer systems embedded into a technical environment. Therefore, they consist of hardware and software components. As the boundaries between the two domains are getting more blurred (dynamically re-configurable hardware, adaptable embedded systems, breakthrough in power consumption and performance) and challenging questions are at the border (trade-offs in mapping applications to hardware and software components, re-configurable hardware, WCET, performance of distributed computer and communication systems), it is necessary to have both aspects represented in a NoE on embedded systems.

There is a link to the topic of Networks on Chip. But it is useful to establish a connection between both communities and to explore the boundaries. This can be seen for example in the fact that at classical design automation conferences there are 'embedded system days' and many sessions related to scheduling, OS and compiler design. The topic does not represent the whole area of SoC but only those aspects that are closely related to RTOS, control, compilers and timing analysis.

In platform-based design, one tries to establish a methodology that is composable in various aspects. In particular, components of a system should cooperate not only in terms of hardware protocols and software layers but also with respect to the design methods applied such as models of computation for specification and formal verification, design space exploration, simulation, global timing analysis and performance analysis. One of the most critical issues to be faced in the research on execution platform is their rapidly growing complexity. Complexity increase is pushed by Moore's law, and by the ever-increasing demand for high performance computing. In order to increase the impact and effectiveness of research in the area of computing platform we cannot simply rely on prototype of existing hardware, which give an outdated snapshot of state-of-the (and obviously, near-future) integration and complexity potentials. A key research and research integration enabler is a scalable and realistic modeling platform which is abstract enough to provide complete system representations and some form of functional models even for billion-transistor future systems, while at the same time providing the needed flexibility for modelling a number of different embodiments (e.g. multi-processors, homogeneous and heterogeneous, reconfigurable, etc.).

The integration of heterogeneous systems consisting of various sorts of components (memory, various sorts of computation units, communication networks) and various models of computation (packet oriented, stream oriented, event vs. time triggered) in terms of the design methods is a major challenge. In terms of communication centric systems, it is of major importance to consider performance, memory and delay models for embedded systems that contain heterogeneous computing and communication resources, support different event models and are communication-centric. The research challenge is to integrate the different approaches used so far. There is the need for formal analysis of complex embedded systems for reliable integration and early architecture exploration. In addition, sensitivity analysis and flexibility optimization for reducing the design risk of critical components will be necessary to cope with the increasing complexity of embedded systems.

The importance of ressource awareness in embedded systems is growing very rapidly. For example, power minimization under performance (more generally, quality of service) constraints are a key objective for current and future research effort. With the growing software content in embbedded systems, and the diffusion of highly programmable and re-configurable platform, software is given an unprecedented degree of control on resource utilization. Technology advances are enabling the control of clock speed, supply delivery and supply voltage, device thresholds, dynamically and independently for multiple modules of a system (even an integrated system-on-chip). The tuning of these ressource-related parameters can be performed both at compile time (statically) and at run-time (dynamically), but the most aggressive optimizations can be achieved only by a sinergistic approach that combines the advantages of static and dynamic techniques. Clearly, in such an aggressive optimization scenario, a tight integration between the software layers must be achieved. We therefore need programming abstractions to expose ressource issues to the application programmer, to the compiler expert and to the operating system developer. We also need a modeling and simulation infrastructure which can deal with large-scale, complex (e.g. multiprocessing) systems, and provide power modeling capability together with performance models and functional accuracy.

In terms of low power design, comprehensive power management solutions for single and multi-processor embedded systems are still missing. They should be implemented within the kernel of the system support software and tightly coupled to process management. This way, the different levels of abstraction participating in low power design could be integrated.

Currently, there exist component models that describe power dissipation of system components in various ways, such as abstract finite-state models (Power FSMs), stochastic modelling (Markovian, generalized semi-Markov processes) for power manageable components. In addition, there are many different QOS metrics related to power such as average power, peak power and battery lifetime, the joint power performance metrics energy and energy-delay, joint power-reliability metrics and power performance metrics for distributed systems. It is necessary to compare and possibly unify the approaches existing so far in order to be able to achieve future design constraints.

In relation to the ARTIST network, it is the overall goal of the topic on execution platforms to extend the current state in composability towards issues like modeling of non-functional constraints, power and energy, end-to-end real-time behavior, timing and performance analysis and heterogeneous models of computation.

8.1.2 Industrial Applications

Automotive electronic systems are increasingly implemented using distributed heterogeneous architectures composed of interconnected networks of processors. High-end vehicles currently have up to 100 microprocessors implementing and controlling various parts of their functionality. We see today the following trend: on the one hand, several functions are integrated into one hardware node, and on the other hand, functionality is distributed over several nodes.

There is large amount of research on scheduling and schedulability analysis, with results having been incorporated in analysis tools such as TimeWiz, RapidRMA, RTA-OSEK Planner, TTPBuild, Rubus Visual Studio. These tools only address the schedulability of a single ECU. As the applications become distributed, new tools are needed that can handle several scheduling policies and communication protocols. One notable exception is the Volcano Network Architect, which addresses the communication analysis of interconnected CAN and LIN networks.

State-of-the-art research tools, such as Aires at the University of Michigan in collaboration with General Motors, Metropolis developed at UC Berkeley in collaboration with BMW and SymTA/S developed at TU Braunschweig in collaboration with Volkswagen are addressing distributed applications. However, none of the existing tools offers a holistic analysis that can handle applications distributed across different types of networks (e.g., CAN, FlexRay, TTP) consisting of nodes that may use different scheduling policies (e.g., static cyclic scheduling, fixed-priority preemptive scheduling, earliest deadline first) and fault-tolerance techniques (e.g., replication, re-execution, checkpointing).

New analysis and optimization tools are needed for safety-critical automotive applications distributed over such heterogeneous fault-tolerant embedded systems. The analysis tools determine if an implementation meets its timing constraints, while the optimization tools support the designer in deriving the least-costly dependable implementation that satisfies the imposed requirements.

Affiliated partners, such as Volvo Technology AB, have identified the *dependability* attribute as being very important for automotive applications. Dependable automotive applications have to be designed such that they implement correctly the required functionality. Very important for the correct functioning of such applications are their timing constraints. The correctness of the functionality depends not only on the results of the computation, but also on the physical instant when the results are produced. In addition, dependable automotive applications should deliver the required functionality even in the presence of faults.

During the project, a lot of industrial contacts have contributed to an improved insight in the current state of the art in the engineering of mechatronics systems. These contacts include collaborations with companies on joint projects, but also feedback obtained during symposia, courses for continuing education of industrial engineers, and so-called knowledge circles where industrial partners exchange problems and solutions. Main issues have been multi-disciplinary system development, and problems related to three key quality attributes: performance, reliability and evolvability.

The development of mechatronic systems typically involves several disciplines, such as electrical engineering, mechanical engineering, and software engineering. Although these disciplines are tightly coupled in the considered embedded systems, their development is often a rather sequential, mono-disciplinary, process. Typically, first the mechanical part is designed, next the hardware infrastructure is fixed, and finally the embedded software is developed. This approach can create large problems, especially for the software engineers. For instance, choices about the placements of sensors (and implicitly the occurrence of interrupts), control rates, control delays, hardware, etc., have a strong influence on the complexity of the software. Moreover, usually many implicit assumptions are made, which first become visible at system integration. This easily leads to non-optimal solutions.

Within each discipline, a common solution is the frequent use of models to detect problems as early as possible. For instance, in the software domain a lot of effort is put on model driven development, based on UML models. Moreover, mono-disciplinary modeling is usually supported by tools that allow some form of execution or simulation. Lacking, however, is the possibility to combine tools of different disciplines and to investigate the mutual influence of modeling choices.

An additional problem which makes it difficult to design products with the required performance, is the strong interaction with other system qualities that have to be achieved, such as reliability, limited resources, robustness, cost limitations, energy consumption, and evolvability. Trade-offs between performance and other system qualities (e.g., product costs and energy consumption) are essential in many applications. A proper combination of all relevant system qualities is a key for achieving a successful product. Observe that in practice there are many relevant qualities and constraints, and it is not easy to select the most

important tensions. Moreover, at design time one has to deal with a large number of uncertainties, which make it very difficult to support well-founded trade-offs.

8.2 State of Integration in Europe

8.2.1 European Research Teams

The major research teams in execution platforms for embedded systems are participants of the cluster. The following table shows the list of key partners and their associated work direction and expected contributions within the cluster:

DTU–Jan Madsen: Hardware/Software Codesign: The research group is internationally recognized for its work on hardware/software codesign. The group has important contributions in the area of automated partitioning and co-processor optimization, with emphasis on taking communication overhead into account. Design space exploration: Several design space exploration approaches for embedded systems have been developed including methods for finding static schedules on heterogeneous multiprocessor platforms, optimizing memory and buffer usages while meeting real-time requirements. Real-time system modeling: System-level modelling of real-time embedded systems for performance analysis, bringing together models of the platform hardware, i.e. processors and interconnection infrastructure (in particular Network-on-Chip) and models of the application software with the use of models of the middleware, in partucular the RTOS layer. Network on Chip: The research group has started a number of activities within the new and emergin field of Network-on-Chip. Activities include on-chip network topology and protocol development, with emphasis on GALS (globally asynchronous, locally synchronous) protocols, and abstraction of the on-chip network for system-level modeling and analysis.

UoB–Luca Benini: Low power architectures and systems: the research group is a recognized center of eccellence in power optimization and power modeling at the system level. The results obtained by the group on memory system optimizations memory compression, bus encoding, are known and referenced worldwide. Some of the proposed techniques are in use in commercial designs. Dynamic Power Management: Prof. Benini is the author of a seminal text on dynamic power managment, and the group has produced a number of advanced in the field, among which we mention the first low-power embedded operating system, developed in cooperation with the hewlett-packard laboratories, Palo Alto, CA, USA. Network on chip: Prof. Benini is deeply involved in the research on the topic and he has co-authored one of the seminal papers on NoCs. His work focuses on NoC design and on developing the software infrastructure for energy efficient on chip communication.

ETHZ–Lothar Thiele: The research group is a center of excellence in multiobjective optimization. Results as well relate to the underlying theory as to providing algorithms and software which is currently used by many research groups worldwide. Performance Estimation: The group has been developing analytic methods based on max-+ algebra to analyze combined computation and communication systems. Packet Processing: The research groups has outstanding expertise in modelling and analysing packet flow communication and network processors and conditional task graphs. Based on these results, scheduling methods that guarantee QoS constraints in network processors have been obtained.

LiU–Petru Eles: Analysis and optimisation of distributed embedded systems: The group has important contributions regarding scheduling and schedulability analysis of complex, multi-protpocol, time-and event triggered distributed embedded systems. Several approaches to the optimisation of the communication infrastructure for such systems have been elaborated. Specific analysis methods have been developed targeting systems with stochastic task execution times. Design space exploration and mapping:Several design space exploration approaches have been developed including aspects like architecture selection, mapping of computation and communication tasks, partitioning into time-and event triggered domains, as well as global testability of the system. Low power system design: The expertise concerns optimisation of power constrained real-time systems. In particular, voltage scaling techniques as well as particular issues related to multi-mode systems has been studied. Hardware synthesis and hardware/software co-design: The group has important contributions in the area of high-level synthesis and that of hardware/software partitioning and co-synthesis.

TUBS–Rolf Ernst: The research team has extensive experience in embedded system design and in theoretical development and practical application of performance models. Theoretical work includes formal combination of heterogeneous models of computation (SPI project with ETH Zuerich), formal and coherent modeling of several types of hardware resource sharing strategies, formal timing and power analysis of individual HW and SW processes, HW/SW system generation from different models of computation, and HW/SW co-synthesis including performance estimation of HW and SW components and communication. Practical experience in leading edge embedded system design includes projects in professional video system design leading to the first flexible and reconfigurable HDTV mixer/switcher on the world market now extended in a follow-up project for on-line electronic film processing where formal methods shall be applied, analysis and formal software integration of automotive power-train control systems, analysis, verification, and design space exploration for automotive and aerospace embedded systems.

ESI–Jozef Hooman: The Embedded Systems Institute currently carries out several research projects related to embedded system design in mechatronics, reliability and performance analysis. For example, the Boderc project focuses on distributed, embedded, real-time control of heterogeneous systems. The target is an integral approach for a systematic architectural design, modeling, analysis, and validation methodology of such systems. The Tangram project focuses on a test methodology, supported with processes and tools, for complex, embedded systems. The target is a test approach that supports heterogeneity and multi-technology testing for early validation, model-based validation, and automatic test generation and diagnostics.

8.2.2 Interaction of the Cluster with other Communities

There have been interactions with several communities whose work is closely related to the activities in ‘Execution Platforms’. In particular, this concerns

- Hybrid Systems and Control (see also the conference HSCC 05 that has been organized on this subject). There needs to be a link between control algorithms/theory, appropriate models of computation/communication and a marching to the underlying hardware system. Whereas there is substantial effort under way to establish those in terms of computation (see e.g. Giotto), concepts for including communication are still missing.

- Real-Time Systems through the participation in common workshops organized by the partners (24th and 25th of January in Paris), the participation in a workshop on Worst Case Execution Time (WCET 05) that was organized by Reinhard Wilhelm at ECRTS 05. If going beyond time-triggered models of computation and communication, properties and constraints by the underlying infrastructure are important. Here, the topic on platforms can contribute and cooperate in several ways: Performance analysis across heterogeneous computing and communication components (different protocols such as time and event triggered, end-to-end timing analysis). This is a major challenge. Establishing global properties accross different models of computation.
- System-on-Chip and Networks-on-Chip through the research activities of partners at University of Bologna (Luca Benini) and Denmark Technical University (Jan Madsen). It is an open issue how and where to integrate low power into a system kernel. This concerns also a link to hardware layers and appropriate models (e.g. Markov models) and the partitioning between kernel, OS, middleware and application.
- Application areas such as automotive, mechatronics and multimedia/consumer electronics through the projects of the partners and the industrial affiliates. In addition, there are close relations to Ford Research Center Aachen and Bosch Research.

8.2.3 Main Aims for Integration through Artist2

Currently, the research in embedded systems is fragemented. This not only is true within a single subject but also between several subdisciplines. Examples are the parallel efforts in real-time scheduling and real-time analysis in the area of ‘Execution Platforms’, ‘Hard Real-Time Systems’ and ‘Software Components’. It is one of the major goals of the cluster on ‘Execution Platforms’ to establish closer links to the other communities and to take advantage of the scientific results and insights.

Cross-layer design is a key issue in embedded systems. The classical view of a strict layering according to chosen abstraction levels does not work any more because of the importance of non-functional constraints and limited resources. Therefore, completely new concepts are necessary that enable the integrated modelling and design under predictability AND efficiency constraints. It is expected that this move towards a resource-aware design trajectory involves all current layers and a breakthrough can be obtained by integration only.

8.3 Overall Assessment and Vision for the Cluster

8.3.1 Assessment

Integration of Research in Europe: It is already visible from the activities in the first year, that a major step towards integrating research in Europe has been possible through ARTIST. For example, the different methods for formal performance analysis and real-time systems have been related to each other. In addition, first attempts have been made to integrate all the efforts (simulation on different layers of abstraction AND formal analysis) into one system modelling infrastructure (see JPIA platform). As a result of these activities, common tools and publications with members of different research teams have been made possible. As the next step, a common set of benchmarks will be made available as a result of a workshop at the end of 2005 in Leiden, The Netherlands. There are many other examples of this integration, such as the common activities in terms of 'Predictability and Efficiency' with the cluster on 'Compilers and Timing Analysis' and the link between timed automata based approaches for performance analysis (cluster on 'Modelling and Components') with those based on Real-Time Calculus.

Building Excellence and Critical Mass: The major step forward achieved in the first year of ARTIST is the significant increase in mobility of PhD students. This way, excellence is built up significantly faster than usual among the participating research teams. All the participating research teams have a substantial number of PhD students and research projects funded by other sources than ARTIST. In addition, all major teams are present in ARTIST as well in the cluster on 'Execution Platforms' as in all the others. As a result, easy access to the broad range of knowledge and expertise in embedded systems is guaranteed and major steps towards cross-layer design and multi-disciplinary research are enabled.

8.3.2 Vision and Long-Term Goals

As a result of fast technological development and of an increasing demand for reliable embedded systems with highly complex functionality, new, more sophisticated architectures, consisting of a large number of interconnected programmable components and ASICs, are now widely used. These processors may be of different types, ranging from simple micro-controllers over general purpose processors (CPU's) to specialized digital signal processors (DSP's), programmable and re-configurable processors and dedicated hardware engines (ASIC's). Given the very high development cost and short time-to-market demands, these complex architectures will not be designed from scratch, but are likely to be heterogeneous multi-processor platforms which can be (re-)configured to fit a particular application. This will force ASIC and system companies to create and use domain specific platforms, i.e. platforms which can be (re-)configured to meet the constraints of a particular application within the domain.

There has been a lot of work in the area of real-time systems which traditionally have concentrated on issues like schedulability analysis, software engineering of real-time systems, modelling and verification. Such a limited view of the problem is insufficient in the context of the above mentioned developments in embedded real-time applications. They are characterized by a continuously increasing complexity and strong constraints on safety, performance, power consumption, and costs. To be able to design such systems, it is needed to (1) consider the hardware architecture and software components in their interaction, in order to produce a system which satisfies the requirements at low cost, (2) support the designer with tools for accurate estimation of certain design parameters (power,

performance) based on appropriate models for hardware and software components and (3) provide the designer with adequate support for design space exploration and optimisation.

These deficiencies have been identified by major European companies in the areas of automotive, mechatronics and consumer electronics. Many of them are either industrial affiliates to the cluster on 'Execution Platforms' or the participating research teams have close contact via other common projects.

For a given embedded system application, it is important to have the technology, methods and tools to make rational choices about the platform and the design used, before proceeding to final implementation. Research in Execution Platforms targets the development of the theoretical and practical tools for modelling the dynamic behaviour of application software running on an underlying platform. This is a new area of research, which will allow greater flexibility in designing optimal embedded systems.

8.3.3 Recommendations

As can be seen from the report, all of the planned acitivites are performing in an excellent way and are still very topical. Therefore, no new ones are planned and there are no activities to be skipped.

On the other hand, some of the academic affiliates are so far not active and one may try to find incentives to increase their participation in the ongoing integration work.

Finally, it appears that the overhead for the cluster head is significant in terms of organizing meetings, be present in meetings of other clusters of ARTIST and shaping the ongoing activities. In addition, he has to take care of accounting and has a major role in reporting. It is proposed to install a rotating scheme.

8.4 Meetings Held

8.4.1 Meeting: Predictability and Efficiency

Dates	22nd December 2004
Venue	Airport Frankfurt, Germany
Main Organiser	Reinhard Wilhelm, Peter Marwedel, Lothar Thiele University Saarland, University of Dortmund, ETH Zurich
Web link	
Objectives	It was the objective to understand the main issues involved in the trade-off between Predictability and Efficiency in Embedded System Design. Potential research objectives and cross-layer activities have been discussed.
Overview of the Agenda	
Conclusions	It was concluded that there is a large gap as well in industry as in academia in the area of predictability and efficiency. Despite the fact that there are several interesting approaches available today (e.g. in the area of compilers for scratch-pad memory, distributed operation, WCET analysis), there is the need for initiating a major research thread.
Next meetings planned	There have been several smaller meetings that continued this discussion, in particular during conferences and workshops (DATE, WCET 2005, ECRTS).

8.4.2 Meeting: Cluster Meeting Execution Platforms

Dates	10th February – 11th February 2005
Venue	Swisse Federal Insitute of Technology Zurich
Main Organiser	Prof. Lothar Thiele ETH Zurich
Web link	
Objectives	It was the objective of the meeting to review the progress in the different activities of the cluster. In addition, further activitiy threads should be defined.
Overview of the Agenda	**Thursday February 10:** 10.00 – 10.15 Lothar Thiele: General Remarks and Organizational Issues 10.15 – 12.30 A representative of each research group gives overview about recent relevant research related to ARTIST2 and results 12.30 – 13.30 Lunch 13.30 – 13.40 Jan Madsen: Introduction to System Modeling

	Infrastructure 13.40 – 14.00 Jan Madsen: Abstact System Simulation Model 14.00 – 14.20 Shankar Mahadevan: Merging MPARM and ARTS 14:20 - 14:40 Petru Eles: ARTS for Distributed Embedded Systems 14.40 – 15.30 Jan Madsen: Discussion and future plans in activity 16.00 – 17.00 Activities for NoE Integration (Resource-Aware Design / Merging ET and TT) **Friday February 11:** 9.30 – 9.40 Rolf Ernst: Introduction to Activity Communication-Centric Systems 9.40 – 10.10 Razvan Racu: Memory Access and Sensitivity Analysis 10.10 – 10.40 Paul Pop: Holistic Performance Analysis 10.40 – 11.10 Simon Kuenzli and Ernesto Wandeler: Combining Real-Time Calculus with SymTA/S; Real-Time Calculus and Performance Analysis 11.10 – 11.30 Rolf Ernst: Future plans in Activity 11.30 – 12.00 Luca Benini Introduction to Design for Low Power 12.00 – 12.30 Alexandru Andrei Dynamic Voltage Scaling and Leakage 12.30 – 13.30 Lunch 13.30 – 14.00 Jens Sparsoe: Low-Power activities at DTU 14.00 – 14.30 Luca Benini: Future plans in Activity 14.30 – 15.00 Discussion about future common research activities, concrete research questions; agreement on next steps
Conclusions	There has been considerable progress in all of the activities. Cooperation between partners has been intensified to a large extent. **Participants:** Embedded Systems Institute, Eindhoven, Netherlands: Jozef Hooman, Jozef.Hooman@embeddedsystems.nl Linkoeping University, Sweden: Petru Eles, petel@ida.liu.se, Paul Pop, aupo@ida.liu.se, Alexandru Andrei, alean@ida.liu.se Technical University of Denmark: Jan Madsen, jan@imm.dtu.dk, Jens Sparsoe, jsp@it.dtu.dk, Shankar Mahadevan, sm@imm.dtu.dk Universita di Bologna: Luca Benini, lbenini@deis.unibo.it, Davide Bertozzi, dbertozzi@deis.unibo.it Technical University Braunschweig: Rolf Ernst, r.ernst@tu-bs.de, Razvan Racu, razvan@ida.ing.tu-bs.de Swiss Federal Insitute of Technology: Lothar Thiele, thiele@tik.ee.ethz.ch, Jan Beutel, beutel@tik.ee.ethz.ch, Simon Kuenzli, kuenzli@tik.ee.ethz.ch, Ernesto Wandeler, wandeler@tik.ee.ethz.ch, Matthias Dyer, dyer@tik.ee.ethz.ch

	Affiliates and Members of Other Clusters: Fabrizio Ferrandi, ferrandi@elet.polimi.it, Reinhard Wilhelm, wilhelm@cs.uni-sb.de, Joseph Sifakis, Joseph.Sifakis@imag.fr, Bart Kienhuis, kienhuis@liacs.nl, Frank Slomka, slomka@informatik.uni-oldenburg.de, Gian Mario Maggio ST Microelectonics, maggio@ieee.org
Next meetings planned	Meeting on Distributed Embedded Systems and Benchmarking, Nov 21-24, Leiden University, The Netherlands, organized by Lothar Thiele and Ed Deprettere (affiliate member) Cluster Meeting, Spring 2006, University Bologna, organized by Luca Benini.

8.4.3 Meeting: Hybrid Systems and Control

Dates	9th March – 11th March 2005
Venue	ETH Zurich, Switzerland
Main Organiser	Prof. Manfred Morari, Prof. Lothar Thiele ETH Zurich, Switzerland
Web link	
Objectives	Linking computation and control in the area of hybrid systems.
Overview of the Agenda	Three days of invited talks and contributions from submitted papers. The topics have been identification, contriol, computation, analysis and applications.
Conclusions	The workshop has been very successful. In particular, the invited talk of ARTIST affiliate Edward Lee showed the increasing interest in and request of appropriate models of computations for hybrid systems.
Next meetings planned	The next meeting in this area will be held in Santa Barbara, CA.

8.5 Cluster Participants

8.5.1 Core Partners

Institution	Researcher
Swiss Federal Institute of Technology Zurich **Focus:** **Embedded Software and Systems** **Team Leader :** **Prof. Lother Thiele**	**Prof. Lothar Thiele** Main areas of research: Embedded Systems and Software Artist2 activities and role: Communication Centric Systems: Formal Performance Analysis, Linking Simulation and Verification, Design Space Exploration of Embedded Systems
	Simon Kuenzli Main areas of research: Design Space Exploration of Embedded Systems Artist2 activities and role: Communication Centric Systems: Formal Performance Analysis, Linking Simulation and Verification, Design Space Exploration of Embedded Systems
	Alexander Maxiaguine Main areas of research: Formal Perfromance Analysis Artist2 activities and role: Communication Centric Systems: Formal Performance Analysis
	Ernesto Wandeler Main areas of research: Formal Perfromance Analysis Artist2 activities and role: Communication Centric Systems: Formal Performance Analysis

Institution	Researcher
<Company or Institution full name> **Focus:** **<(keywords)>** **Team Leader :** **<name>, <title(s)>**	**Jozef Hooman** Main areas of research: Development of Embedded Systems, Performance and Reliability of Software Artist2 activities and role: Performance Analysis in the System Design Process

	Jeroen Voeten Main areas of research: System-level Design Methodology, Performance Modeling Artist2 activities and role: Performance Analysis in the System Design Process
	Marcel Verhoef Main areas of research: Peformance Analysis Artist2 activities and role: Performance Analysis in the System Design Process
	Oana Florescu Main areas of research: Performance Analysis Artist2 activities and role: Performance Analysis in the System Design Process

Institution	Researcher
Linköping University **Focus:** **Embedded syst.** **Communication centric systems** **Low power** **Team Leader :** **Prof. Petru Eles**	**Petru Eles** Main areas of research: Embedded Systems Artist2 activities and role: Communication Centric Systems: analysis, optimisation. Low Power: modeling, optimisation, power management. System modeling infrastructure: modelling and simulation of distributed embedded systems.
	Zebo Peng Main areas of research: Embedded Systems Artist2 activities and role: Communication Centric Systems: analysis, optimisation. Low Power: optimisation, power management.
	Paul Pop Main areas of research: Embedded Systems Artist2 activities and role: Communication Centric Systems: analysis, optimisation.

	Traian Pop Main areas of research: Real-Time Systems Artist2 activities and role: Communication Centric Systems: analysis and optimisation of heterogeneous real-time systems.
	Alexandru Andrei Main areas of research: Low power Artist2 activities and role: Low Power: optimisation, power management.
	Soheil Samii Main areas of research: Modeling, Simulation Artist2 activities and role: System modeling infrastructure: modelling and simulation of distributed embedded systems.

Institution	Researcher
Università di Bologna **Focus:** **Low power execution platforms, Communication-centric architectues** **Team Leader :** **Luca Benini, Professor**	**Luca Benini** Main areas of research: Execution platforms Other projects involved in: low power design, communication-centric architectures Artist2 activities and role: JPRA Communication centric Systems (coordinator) JPRA Design for Low Power (coordinator) JPRA Resource-aware design (co-coordinator)
	MICHELA MILANO Main areas of research: constaint programming Other projects involved in: combinatorial optimization Artist2 activities and role: JPRA Resource-aware design (research planner)
	Francesco Poletti Main areas of research: design for low power Other projects involved in: communication centric systems Artist2 activities and roleArtist2 activities and role: JPRA Design for Low Power (technical contributor):

	Federico Angiolini<Name> Main areas of research: communication centric system Other projects involved in: Network-on-chip design Artist2 activities and role: JPRA communication centric Systems (technical contributor)
	Christine Nardini Main areas of research: Design of energy efficient algorithms Other projects involved in: Design of micro-array data mining algorithms Artist2 activities and role: JPRA Design for Low Power (technical contributor)
	Alessio Guerri Main areas of research: Design of optimization-based mapping algorithms Other projects involved in: Constraint programming techniques Artist2 activities and role: JPRA Resource-Aware Design (technical contributor)

Institution	Researcher
Technical University of Denmark **Focus:** **Embedded Systems Modeling, System-on-Chip, Network-on-Chip** **Team Leader :** **Prof. Jan Madsen**	**Prof. Jan Madsen** Main areas of research: Embedded Systems Design and Modeling Artist2 activities and role: System Modelling Infrastructure, Communication-Centric, Systems, Design for Low-Power
	Assoc. Prof. Jens Sparsø Main areas of research: Asynchronous Circuit Design, Network-on-Chip Artist2 activities and role: Communication-Centric Systems, Design for Low-Power

	Shankar Mahadevan Main areas of research: System-Level Modelling of MPSoC Platforms Artist2 activities and role: System Modelling Infrastructure, Communication-Centric Systems
	Kashif Virk Main areas of research: System-Level Modelling of Wireless Sensor Networks Artist2 activities and role: System Modelling Infrastructure, Design for Low-Power
	Tobias Bjerregaard Main areas of research: Network-on-Chip Artist2 activities and role: Communication-Centric Systems
	Kehuai Wu Main areas of research: Adaptable Computing Arcitectures Artist2 activities and role: Communication-Centric Systems

Institution	Researcher
Institute of Computer and Communication Network Engineering **Focus:** **Embedded systems** **Team Leader :** **Prof. Rolf Ernst**	**Prof. Rolf Ernst** Main areas of research: Embedded Systems Artist2 activities and role: Communication Centric Systems: Formal Performance Analysis, Design Space Exploration of Embedded Systems, Sensitivity Analysis of Embedded Systems. System modelling infrastructure: Flexibility Optimization of Embedded Systems.

	Arne Hamann Main areas of research: Design Space Exploration and Optimization of Embedded Systems Artist2 activities and role: Communication Centric Systems: Formal Performance Analysis, Design Space Exploration of Embedded Systems. System modelling infrastructure: Flexibility Optimization of Embedded Systems.
	Razvan Racu Main areas of research: Sensitivity Analysis of Embedded Systems Artist2 activities and role: Communication Centric Systems: Formal Performance Analysis, Sensitivity Analysis of Embedded Systems. System modelling infrastructure: Flexibility Optimization of Embedded Systems.
	Simon Schliecker Main areas of research: Memory Access Modeling and Analysis Artist2 activities and role: 8.5.2 System modelling infrastructure: Formal Performance Analysis, Modelling and Analysis of Complex Memory Access Patterns
	Rafik Henia Main areas of research: Context Sensitive Formal Performance Analysis Artist2 activities and role: Communication Centric Systems: Formal Performance Analysis, Modelling and Exploitation of Context Informations
	Matthias Ivers Main areas of research: Network Processor Architectures Artist2 activities and role: Communication Centric Systems: Design and Formal Performance Analysis of Complex Network Processor Architectures

8.5.3 Affiliated Industrial Partners

Institution	Researcher
Volvo Technology Corporation **Focus:** **Automotive** **Team Leader :** **Magnus Hellring**	**Magnus Hellring** **Manager Systems and Architecture** Main areas of research: Archtiecture and Design of Automotive Embedded Systems Artist2 activities and role: none

Institution	Researcher
STM, Advanced System Technology – Research and Innovation **Focus:** **Low Power Design** **Team Leader :** **Roberto Zafalon**	**Roberto Zafalon** **Manager Low Power Systems Design** Main areas of research: Low Power System Design Artist2 activities and role: JPRA design for low power, JPRA Resource-aware design

Institution	Researcher
BullDast Corp. **Focus:** **Low Power EDA Tools** **Team Leader :** **Monica Donno**	**Maria Cristina Avalle** Main areas of research: Tools and Methods for Low Power Design Artist2 activities and role: JPRA Design for Low Power

Institution	Researcher
Volkswage AG **Focus:** **Automotive** **Team Leader :** **Dr. Fabian Wolf**	**Dr. Fabian Wolf** Main areas of research: Software and Hardware for Embedded Systems in Automotive Applications Artist2 activities and role: none

Institution	Researcher
SymTAVision GmbH **Focus:** **Automotive** **Team Leader :** **Dr. Kai Richter**	**Dr. Kai Richter** Main areas of research: Formal Performance Analysis and Optimization of Embedded Systems, Reliable System Integration, Early Architecture Exploration Artist2 activities and role: none

Institution	Researcher
Robert Bosch AG **Focus:** **Automotive** **Team Leader :** **Dr. Dirk Ziegenbein**	**Dr. Dirk Ziegenbein** Main areas of research: Automotive Software Architectures Artist2 activities and role: none

Institution	Researcher
Nokia Denmark A/S **Focus:** **Mobile terminals** **Team Leader :** **Peter Mårtensson**	**Peter Mårtensson** Main areas of research: Platform architectures for mobile terminals Artist2 activities and role: none

8.5.4 Affiliated Academic Partners

Institution	Researcher
Royal Institute of Technology Stockholm **Focus:** **Design Methodology** **Team Leader :** **Prof. Axel Jantsch**	**Prof. Axel Jantsch** Main areas of research: Design Methodology for Embedded Systems Artist2 activities and role: none

Institution	Researcher
EPFL **Focus:** **Embedded Systems Architectures, Low Power Design** **Team Leader :** **Prof. Giovanni De Micheli**	**Prof. Giovanni De Micheli** Main areas of research: Design Methodology for Embedded Systems, Low Power Design Artist2 activities and role: JPRA communication centric design

Institution	Researcher

Politechnico Di Milano **Focus:** **Embedded Systems Architectures, Low Power Design** **Team Leader :** **Prof. Donatella Sciuto**	**Prof. Donatella Sciuto** Main areas of research: Design Methodology for Embedded Systems, Low Power Design Artist2 activities and role: none

Institution	Researcher
University Leiden, The Netherlands **Focus:** **Design Methodology** **Team Leader :** **Prof. Ed Deprettere**	**Prof. Ed Deprettere** Main areas of research: Design Methodology for Embedded Systems, Signal and Image Processing, Algorithm Design and Mapping Artist2 activities and role: Preparation of ARTIST2 Workhsop on Embedded Systems in Leiden, The Netherlands; Visists to Zurich in order to discuss on JPRA “Communication Centric Systems”.

Institution	Researcher
Universidad de Cantabria **Focus:** **Design and Verification of Embedded H/S Systems** **Team Leader :** **Prof. Eugenio Villar**	**Prof. Eugenio Villar** Main areas of research: Design and Implementation of Embedded H/S Systems Artist2 activities and role: none **Prof. Pablo Pedro Sanchez** Main areas of research: Design and Implementation of Embedded H/S Systems Artist2 activities and role: none

Institution	Researcher
Katholieke Universiteit Leuven **Focus:** **Design Methods** **Team Leader :** **Prof. Geert Deconinck**	**Prof. Geert Deconinck** Main areas of research: Dependability, embedded systems, control & automation, real-time, robust communication, interdependencies, critical information infrastructure protection Artist2 activities and role: none

Institution	Researcher

Politecnico Di Turion, Italy **Focus:** **Asynchronous Circuit Design and Testing** **Team Leader :** **Prof. Luciano Lavagno**	**Prof. Luciano Lavagno** Main areas of research: Asynchronous Circuit Design and Testing, H/S Codesign Artist2 activities and role: none

Institution	Researcher
Royal Institute of Technology Stockholm **Focus:** **Design Methodology** **Team Leader :** **Prof. Axel Jantsch**	**Prof. Pablo Sanchez** Main areas of research: Design Methodology for Embedded Systems Artist2 activities and role: none

Institution	Researcher
University of Notre Dame **Focus:** **Design for Low Power** **Team Leader :** **Prof. Sharon Hu**	**Prof. Sharon Hu** Main areas of research: Design for Low Power Artist2 activities and role: none

8.6 Research and Platform Activities

8.6.1 *JPRA-Cluster Integration*: Communication-centric systems

Leader	Rolf Ernst (TU Braunschweig: formal performance models for networks-on-chip)
Policy Objective	The work aims at new best-case/worst-case models for hard real-time systems and at combined statistical and interval models for QoS applications in multi-media. These models will combine communication and computation, different models of computation, event models and scheduling policies. In addition, appropriate tool support will be made available to industry and being used.

8.6.2 *JPRA-Cluster Integration*: Design for Low Power

Leader	Luca Benini (University of Bologna)
Policy Objective	Power dissipation is rapidly becoming one of the most serious obstacles in the evolution of electronic systems. Technology development leads to an increased active-state and stand-by power consumption. mainstream architectural design is moving towards energy-hungry architectures, e.g. programmability. It is the objective of this activity to develop, promote and integrate methods that address issues across several layers of abstraction.

8.6.3 *JPRA-NoE Integration*: Resource-aware Design

Leader	University of Bologna (Luca Benini) and University Dortmund (Peter Marwedel)
Clusters	Execution Platforms Compilers and Timing Analysis
Policy Objective	Provide, through the integration of research activities of many participants a viable path for resource-aware software and hardware development. The final objective is to achieve integration of research activities in concrete deliverables: • A set of tools that can interact and work together and demonstrate the achievable optimizations on a particular hardware platform. A methodology that enables the design of predictable embedded systems with a special focus on issues that cut several layers of abstraction, such as hardware and compiler design.

8.6.3.1 JPIA-Platform: *System modelling infrastructure*

Leader	Jan Madsen (Technical University of Denmark: abstract RTOS and NoC models for multiprocessor system simulation)

Policy Objective	Integrate ongoing research efforts on infrastructure modelling. This would replace prototyping hardware to reduce the cost and time required for designing embedded systems. This activity is strategic for providing one angle in tackling the growing complexity of embedded systems.

9. Cluster: Control for Embedded Systems

Contributor: Prof. Karl-Erik Arzen – Lund University

9.1 Description of the Area

The focus of the research in the Control for Embedded Systems cluster is implementation-related real-time issues for networked embedded control systems and control of real-time computing and communications systems.

9.1.1 Main Research Trends

Controllers are in most cases based on periodic sampling and assume a negligible or constant latency between input and output (sampling and actuation). This is something that in many cases can be difficult or costly to achieve. Time-triggered solutions based on static scheduling are one solution, but are sometimes too inflexible or are incompatible with the rest of the system software. In event-based solutions, pre-emption, blocking, execution time variations and non-deterministic kernels generate sampling jitter and latency jitter. The same holds for event-based network protocols. The problem can be approached in different ways. Robust design can be applied to guarantee a certain level of temporal robustness. Techniques can be used to compensate for the timing variations, either passively based on off-line information about the characteristics of the variations, or actively using measurements. The interaction between control and real-time computing becomes extra important in situations where the computing and communication resources are severely limited, e.g., in embedded control system applications, where separation of concerns-based design principles, with strict interfaces between control and computing, may be unfeasible. Instead it is necessary to take both computing and control aspects into account simultaneously. This requires theory and tools that support codesign. From a pure real-time systems approach it is also desirable to provide more flexible ways of allocating computing resources to different applications or tasks. The area of adaptive or feedback-based resource scheduling is one example of this.

Taking implementation issues and limited resources into account in the control design is covered by the terms *resource-aware control* and *implementation-aware control*. The development in this area needs to be matched with the similar developments within the real-time field. It is necessary to create models of computation and scheduling, and system software and hardware, which are tailored to the true needs of control applications. This is covered under the terms of *control-aware computing and networking.*

A new area is control of computer software systems, e.g., large eCommerce servers. These servers are complex dynamic systems with high levels of uncertainty. The need for control arises at several levels, e.g., admission control, delay control, and utilization control. Several new challenges apply. Since the servers are engineering artefacts, first principles do not apply, at least not on the macroscopic level. Several competing modeling formalisms needs to be combined, e.g., continuous-time flow models, queuing models, and various types of event-based models. System stability has an unclear meaning, and the whole issue of how to write controllable and observable software system is still largely unexplored.

9.1.2 Industrial Applications

Embedded control systems are vital in most industrial application areas, e.g., automotive, avionics, manufacturing, and automation. The use of feedback-based (adaptive) resource management is of particular interest for soft real-time applications, e.g., multimedia applications within consumer electronics systems. The main applications of control of computer systems can be found at companies like IBM or HP. However, also large users of server technology such as Amazon have in-house application development within this area.

9.2 State of Integration in Europe

9.2.1 European Research Teams

The main European research teams within the fields of interests of this cluster are the following for the different subfields:

Control of Web server systems: This field is strongly dominated by US groups, e.g., Univ of Virginia (Abdelzaher (associated with the cluster)), University of Illinois (Lui Sha (associated with the cluster)), University of Michigan (Tilbury) and IBM (Hellerstein). The only European group active in this area is LUND (Robertsson).

Control-based resource allocation: This is a field where Europe has several strong groups. Scuola Superiore S. Anna and Univ of Pavia (Buttazzo and Lipari) are strong in adaptive resource management. The same hold for Mälardalens högskola (Fohler) and Philips (Steffens). University of Linköping (Hansson) is strong in control-based approaches for database servers. LUND (Årzén/Cervin), UPVLC (Crespo/Albertos) and KTH (Törngren) are strong in feedback scheduling of control systems and QoS approaches in control.

Control of Communications Network: Also here Europe has several strong groups. For example, KTH (Johansson), Univ of Patras (Lygeros), and Univ of L'Aquila (Santucci).

Real-Time Control Systems: Here LUND (Årzén/Cervin) is working in implementation-aware real-time control. The same holds for KTH (Törngren), UPVLC (Albertos), CTU (Hanzalek), UPC (Marti), INRIA (Simon), and Univ of Pisa (Bicchi). Univ of York (Bate) is strong on scheduling of control systems.

Codesign Tools: Several groups are working tools for codesign of control and computing issues. These include LUND (Årzén), KTH (Törngren), Univ of Pisa (Lipari), PARADES (Sangiovanni-Vincentelli).

Hybrid Control: Hybrid control is an area with strong relationships to this cluster. The good European groups are all gathered in the HYCON NoE. These include ETH (Morari), Siena (Bemporad), PARADES (Belluchi), Verimag (Maler), LUND (Rantzer) and KTH (Johansson).

9.2.2 Interaction of the Cluster with other Communities

During the first 12 months the priority of the cluster has been the inter-cluster activities, with a strong focus on the development of two roadmaps which will de delivered at M12. This and the limited resources has somewhat hampered the intra-cluster activities. The cluster has the potential to have strong relationships with almost all clusters in ARTIST2. The cluster is the leader of the networking activity on Adaptive Real-Time, Hard Real-Time and Control. Within this area the interaction has mainly been with the Adaptive RT cluster where joint activities have been started involving LUND, Mälardalen, UPC, CTU, SSSA, UPVLC, Aveiro and Ericsson. The cluster has also been represented at a workshop on diagnosis in embedded systems organized by the HRT cluster. The Euromicro session on Model based development was arranged by invitation from and in cooperation with Ivica Crncvic from the Modeling and Components.

In June 13-16 the cluster arranged an International ARTIST2 Workshop on Control for Embedded Systems in Lund, to which the affiliated partners Lui Sha and Tarek Abdelzaher were invited. The workshop was also attended by a representative from Caltech and by two members of the ART cluster (Buttazzo and Fohler). All clusters were invited to participate in the meeting.

9.2.3 Main Aims for Integration through Artist2

The main aims for the integration through Artist2 are the following. The first aim is to unite the best European groups in the field and create a strong European research network on control for embedded systems. The second aim is to integrate this network with the other Artist2 clusters, thereby increasing the awareness within the embedded system community of the true computing and communication requirements of networked embedded control applications and of how control techniques can be used in the design of embedded systems to achieve increased robustness and flexibility.

9.3 Overall Assessment and Vision for the Cluster

9.3.1 Assessment

The work within the cluster has progressed nicely during the first year. The focus has been the development of two roadmaps (Control of real-time computing systems and Real-time techniques in control system implementation) and one survey of codesign tools. The quality of the roadmaps as they will be delivered at M12 is good, but needs to be improved if they should be developed into book chapters, similarly to what was done with the Artist roadmaps. In addition to these, a separate Artist2 Strategic Research Agenda on Control for Embedded Systems has been developed. The latter is the outcome on the Lund Workshop on Control for Embedded Systems organized by the cluster in Lund, June 13-16.

In addition to these joint Artist2 publications a number of quality publications have been produced by the members of the cluster during the year. For example, both Årzen and Cervin are co-authors of the RTSS 25 year anniversary article “Real-Time Scheduling: A Historical Perspective” (has appeared in the Real-Time Systems journal). Several of the cluster members are also authors of chapters in the recently published “Handbook of Networked and Embedded Control Systems” (Birkhäuser), with Årzén in the editorial board.

The cluster has also been involved in several activities for spreading of excellence. A major event was the Valencia Graduate Course on Embedded Control Systems in April where the cluster members lectured and the course material was developed jointly. Other activities that we have organized includes a Real-Time Control workshop in association with ECRTS 05 at Mallorca, a special session on model-driven engineering at Euromicro, and one invited session, one half-day tutorial, and one summer school in connection with the IFAC World Congress in Prague. The cluster has been successful in exposing its activities both to the real-time computing community and to the control community.

The cluster consists of five partners: LUND, KTH, UPVLC, CTU and ETH. The KTH node consists of three subgroups, representing different departments. Similarly, the UPVLC node consists of members from two departments. Due to limited resources ETH (Manfred Morari) decided to not be active in Artist2 during the first year. With only four nodes the cluster is on the limit of having under-critical mass. It is, however, our hope that ETH will rejoin the activities during the second year. The cluster has also been approached by several others who are interested in joining in some way or another. This includes both those who formally are part of other Artist2 clusters, e.g., Ian Bate from York, Daniel Simon from INRIA and Pau Marti from UPC, and those who are not currently part of Artist2 at all, e.g., Jan Broenink from University of Twente. However, without an increased Artist2 funding for the cluster any increase of the number of partners would have negative effects.

9.3.2 Vision and Long-Term Goals

The technical long-term goals of the cluster consists of two parts: The first is the creation of methods and theory that allow faster and more efficient development of networked embedded control systems that are safer, more flexible, more predictable, have higher degree of resource utilization, and better performance than what is possible today. The way to achieve this is increased understanding for the interactions between the control and the computing subsystems, development of tools that allow us to analyze these interactions, codesign approaches, and the use of control-theoretic approaches in the design and implementation of these systems. The second goal is to advance the state of the art in applying control methods for providing flexibility and robustness and manage uncertainty in general embedded computing and communication systems.

Without the participation of this cluster within Artist2 the link to the control community would be lost. The result would be incorrect or overly restrictive assumptions about the resource requirements of control applications and it would lead to ad hoc based application of control in the design of embedded systems rather than approaches that are firmly based in control theory. This would affect both academia and industry.

9.3.3 Recommendations

The current cluster activities (Real-Time Techniques in Control System Implementation and Control in Real-Time Computing) should both be continued. The network integration activity Adaptive Real-Time, Hard Real-time and Control should have a stronger focus than before, in particular should the HRT cluster be involved more. This is also possible now when the internal structure of the cluster has been established and the development of the roadmaps is completed. The JPIA activity on platforms and tools has with respect to the control cluster consisted of further development of the individual tools, development of course material for individual tools, and the writing of a survey on codesign tools. In the coming year, the interaction between this work and the work being performed within other clusters needs to be strengthened.

The existing Artist2 structure is very hierarchical. It has both advantages and disadvantages. One advantage is that it is organizationally simple. Another advantage is that it is easier to get joint work done when the number of partners and people involved is quite small. However, it can also lead to situations where clusters are isolated from the rest of the Artist2 activities. An alternative, more network-oriented, structure that would simplify for individual researchers, rather than entire teams, to be involved in several sub-communities (“clusters”) could be an alternative.

9.4 Meetings Held

Since most of the partners are involved in both the inter-cluster activities of this cluster, no separate inter-cluster meetings have been held. Instead both inter-cluster activities have been covered together on the cluster meetings.

9.4.1 Meeting: Cluster Kickoff Meeting

Dates	October 10, 2004
Venue	Hotell Mercur, Grenoble, France
Main Organiser	Karl-Erik Årzén, LUND
Web link	Not available
Objectives	Administrative kickoff meeting for the cluster
Overview of the Agenda	• Brief Partner Presentations • Development of common cluster presentation
Conclusions	Since Artist2 had just started the amount of questions was large concerning how the network and the cluster should function.
Next meetings planned	Technical cluster meeting December 5, Lisbon (RTSS) organised by: Karl-Erik Årzén

9.4.2 Meeting: Cluster Meeting

Dates	December 5, 2004
Venue	SANA Lisboa Park Hotel, Lisbon, Portugal
Main Organiser	Karl-Erik Årzén, LUND
Web link	Not available
Objectives	• Provide a technical overview of the work being done among the partners • Plan the work with the year one deliverables • Plan the contents of the Valencia Graduate Week on Embedded Control Systems • Decide on how to spend the mobility funding and which JPASE activities to have
Overview of the Agenda	Points corresponding to the objectives
Conclusions	The responsibilities and workplan for the roadmaps and the tools survey were decided upon. It was decided to use the mobility for longer research stays for PhD students and senior researchers and what is left after that for travels associated with JPASE activities.

Next meetings planned	Cluster meeting April 4-8 (in connection with the Valencia Graduate Week) organised by: Pedro Albertos

9.4.3 Meeting: Inter-cluster Meeting on Adaptive Real-time, HRT and Control

Dates	December 7, 2004
Venue	SANA Lisboa Park Hotel, Lisbon, Portugal
Main Organiser	Karl-Erik Årzén, LUND
Web link	Not available
Objectives	• Identify already existing connections / collaborations • Identify how we can work together
Overview of the Agenda	Individual brief position statements from the participating partners
Conclusions	The cluster activities Flexible Scheduling Technologies and Adaptive Resource Management for Consumer Electronics within ART match well the cluster activities in this cluster.
Next meetings planned	International Artist2 Workshop, Lund June 13-16 organised by: Karl-Erik Årzén

9.4.4 Meeting: Cluster Meeting

Dates	April 5-8, 2005 in connection with the Graduate Week
Venue	UPVLC, Valencia, Spain
Main Organiser	Pedro Albertos, UPVLC
Web link	http://www.artist2.upv.es/ (Weblink for the Graduate week)
Objectives	Update of the status on the work on roadmaps and survey.
Overview of the Agenda	• Report from the SMB meeting • Presentation of revised cluster budget • The IMT tool • Activity status
Conclusions	The work in the cluster activities proceeds nicely. The Graduate Week has been a great success.

Next meetings planned	Cluster meeting July 8 organised by: Zdenek Hanzalek, CTU

9.4.5 Meeting: International Meeting on Control for Embedded System

Dates	June 13-16
Venue	Biskopshuset, Lund, Sweden
Main Organiser	Karl-Erik Årzén, LUND
Web link	http://www.control.lth.se/~karlerik/LundWorkshop.html
Objectives	The aim of the workshop was to gather key researchers within the control and real-time computing fields to chart the research agenda for the next decade in control for embedded systems. The international affiliated partners Lui Sha and Tarek Abdelzaher were specially invited, together with representatives from Caltech. The meetings should also serve as a meeting point for the network integration activity on adaptive RT, hard RT and Control.
Overview of the Agenda	See the program together with the presentation at the home page
Conclusions	A 16 page Strategic Research Agenda was written as the result of the workshop. The agenda discusses objectives and research directions within the fields *Real-Time Implementation of Control Systems, Sensor/Actuator Networks (real-time and control issues), Control of Computer Systems*, and *Error Control of Software.* The control of computer system subject included three subtopics*: Control of Web Server Systems, Control of Communication Networks*, and *Control of CPU Resources*.
Next meetings planned	No meeting of this type planned.

9.4.6 Meeting: Cluster Meeting

Dates	July 8
Venue	CTU, Prague
Main Organiser	Zdenek Hanzalek
Web link	Not available
Objectives	Synchonize the remaining work on the M12 deliverables
Overview of the Agenda	Planning of the time up to September 10

Conclusions	Time plan generated
Next meetings planned	In connection with the Artist2 review in Grenoble, October 3-5, 2005

9.5 Cluster Participants

9.5.1 Core Partners

Institution	Researcher
Lund University, LUND **Focus:** **Integrated control and scheduling, embedded control systems, control of computer systems, codesign tools** **Team Leader :** **Karl-Erik Årzén** **Professor**	**Karl-Erik Årzén** Main areas of research: Integrated control and scheduling, embedded control systems, control of computer systems, codesign tools Other projects involved in: EU: RUNES National: FLEXCON, VR (multi-project grant) Artist2 activities and role: JPIA-Platform: Design Tools for Embedded Control Researcher JPRA-NoE Integration: Adaptive Real-Time. HRT and Control Leader JPRA-Cluster Integration: Control in real-time computing Researcher , Roadmap editor JPRA-Cluster Integration: Real-time techniques in control system implementation Researcher
	Anton Cervin Main areas of research: Integrated control and scheduling, embedded control systems, control of computer systems, codesign tools Other projects involved in: EU: RUNES National: FLEXCON, VR (multi-project grant) Artist2 activities and role: JPIA-Platform: Design Tools for Embedded Control Researcher JPRA-NoE Integration: Adaptive Real-Time. HRT and Control Researcher JPRA-Cluster Integration: Control in real-time computing Researcher JPRA-Cluster Integration: Real-time techniques in control system implementation Researcher
	Anders Robertsson

	Main areas of research: Control of computer systems, Mechatronics Other projects involved in: EU: SMErobot, EURON II National: FlexAA Artist2 activities and role: JPRA-Cluster Integration: Control in real-time computing Researcher
	Björn Wittenmark Main areas of research: Computer-controlled systems Other projects involved in: National: VR (Multi-project grant) Artist2 activities and role: JPRA-Cluster Integration: Control in real-time computing Researcher

Institution	Researcher
Royal Institute of Technology, KTH **Focus:** **Model based development of embedded control systems, model and tool integration, hybrid control systems, control of computer and communication systems systems** **Team Leader :** **Martin Törngren, Professor**	**Martin Törngren** Main areas of research: Model based development of embedded control systems, model and tool integration, embedded control systems, distributedsystems Other projects involved in: National projects CAS, SAVE, Flexcon, CODEX and ModComp Artist2 activities and role: JPIA-Platform: Design Tools for Embedded Control Responsible, tool survey editor JPRA-NoE Integration: Adaptive Real-Time. HRT and Control Researcher JPRA-Cluster Integration: Control in real-time computing Researcher (feedback scheduling of control systems) JPRA-Cluster Integration: Real-time techniques in control system implementation Researcher (embedded control systems
	Mikael Johansson Main areas of research: Control and communication networks, Hybrid control Other projects involved in:

EU: RUNES, HYCON, EuroNGI, Cellular
National: Winternet, AWSI, ProperNets, …

Artist2 activities and role:

JPRA-Cluster Integration: Control in real-time computing
Researcher (Control of Communication networks)

Karl-Henrik Johansson

Main areas of research:
Control and communication, Hybrid control

Other projects involved in:
EU: RUNES, HYCON, RECSYS, EuroNGI
National: NEC, network-aware control, Integrated control and coding, CAS, SRI, …

Artist2 activities and role:

JPRA-Cluster Integration: Control in real-time computing
Researcher (Control of Communication networks)

Ola Redell

Main areas of research:
Embedded & Distributed Control, Modelling and timing analysis

Other projects involved in:
National projects CAS, SAVE, Flexcon, CODEX and ModComp

Artist2 activities and role:

JPIA-Platform: Design Tools for Embedded Control
Researcher

JPRA-Cluster Integration: Real-time techniques in control system implementation
Researcher (embedded control systems)

Martin Sanfridson

Main areas of research:
Embedded & Distributed Control, Modelling and timing analysis, Feedback Scheduling

Other projects involved in:
National projects CAS, SAVE, Flexcon, CODEX and ModComp

Artist2 activities and role:

JPIA-Platform: Design Tools for Embedded Control
Researcher

JPRA-Cluster Integration: Real-time techniques in control system implementation
Researcher (embedded control systems)

JPRA-Cluster Integration: Control in real-time computing

	Researcher (feedback scheduling of control systems)
	Xiaoming Hu Main areas of research: Embedded control with distributed sensing and computing, hybrid control Other projects involved in: EU: RECSYS National: Control and sensing of nonlinear mobile systems, Embedded control with distributed sensing and computing, Hybrid control of autonomous systems, …. Artist2 activities and role: JPRA-Cluster Integration: Real-time techniques in control system implementation Researcher JPRA-Cluster Integration: Control in real-time computing Researcher
	Jan Wikander Main areas of research: Embedded & Distributed ControlOther projects involved in: National projects CAS Flexcon, CODEX and ModComp Artist2 activities and role: JPRA-Cluster Integration: Real-time techniques in control system implementation Researcher (embedded control systems)

Institution	Researcher
Universidad Politechnica de Valencia, UPVLC **Focus:** **Integrated control and scheduling, embedded real-time computing, multi-rate control, non-conventional sampling** **Team Leader :** **Alfons Crespo, Professor**	**Alfons Crespo** Main areas of research: Real-time and embedded computing systems, Embedded design tools Other projects involved in: EU: OCERA National: several Artist2 activities and role: JPIA-Platform: Design Tools for Embedded Control Researcher JPRA-NoE Integration: Adaptive Real-Time. HRT and Control Researcher JPRA-Cluster Integration: Control in real-time computing Researcher

	JPRA-Cluster Integration: Real-time techniques in control system Leader, researcher, roadmap editor
	Pedro Albertos Main areas of research: Computer-controlled systems, Integrated control and scheduling, multi-rate control, non-conventional sampling, handling of delays Other projects involved in: National: several Artist2 activities and role: JPIA-Platform: Design Tools for Embedded Control Researcher JPRA-NoE Integration: Adaptive Real-Time. HRT and Control Researcher JPRA-Cluster Integration: Real-time techniques in control system implementation Researcher
	Julian Salt Main areas of research: Real-time and embedded computing systems, Embedded design tools Other projects involved in: EU: OCERA National: several Artist2 activities and role: JPIA-Platform: Design Tools for Embedded Control Researcher JPRA-NoE Integration: Adaptive Real-Time. HRT and Control Researcher JPRA-Cluster Integration: Control in real-time computing Researcher JPRA-Cluster Integration: Real-time techniques in control system Researcher
	Joan Vila Main areas of research: Real-time and embedded computing systems, Distributed real-time systems Other projects involved in: EU: OCERA National: several Artist2 activities and role:

	JPRA-NoE Integration: Adaptive Real-Time. HRT and Control Researcher JPRA-Cluster Integration: Real-time techniques in control system Researcher

Institution	Researcher
Czech Technical University, CTU **Focus:** **Integrated control and scheduling, embedded real-time computing, multi-rate control, non-conventional sampling** **Team Leader :** **Vladimir Kucera, Professor**	**Vladimir Kucera** Main areas of research: Robust control, control systems design, process optimization and predictive control. Other projects involved in: National: numerous Artist2 activities and role: JPRA-Cluster Integration: Real-time techniques in control system Researcher
	Zdenek Hanzalek Main areas of research: Real-Time & embedded control, scheduling Other projects involved in: EU: OCERA, IFiBO National: numerous Artist2 activities and role: JPIA-Platform: Design Tools for Embedded Control Researcher JPRA-NoE Integration: Adaptive Real-Time. HRT and Control Researcher JPRA-Cluster Integration: Real-time techniques in control system implementation Researcher
	Michael Sebek Main areas of research: Robust control, control systems designOther projects involved in: EU: OCERA National: several Artist2 activities and role: JPRA-Cluster Integration: Real-time techniques in control system Researcher

Institution	Researcher

Swiss Federal Institute of technology, Zurich, ETHZ **Focus:** **Hybrid systems, predictive control** **Team Leader :** **Manfred Morari, Professor**	**Manfred Morari** Main areas of research: Hybrid systems and control, predictive control Other projects involved in: National: numerous Artist2 activities and role: Has not participated during M0-M12

9.5.2 Affiliated Industrial Partners

Company	Researcher
dSpace **Focus:** **Development of industrial tools for embedded control systems design** **Team Leader :** **Joachim Stroop**	**Joachim Stroop** Main areas of research: Development of industrial tools for embedded control systems design Other projects involved in: EU: EASIS Artist2 activities and role: JPIA-Platform: Design Tools for Embedded Control Provide input

Company	Researcher
ABB Automation Technology Products **Focus:** **Industrial Automation** **Team Leader :** **Göran Arinder**	**Göran Arinder** Main areas of research: Industrial automation Other projects involved in: Artist2 activities and role: JPRA-Cluster Integration: Real-time techniques in control system implementation Provide input
	Mikael Peterson Main areas of research: Industrial automation Other projects involved in:

	Artist2 activities and role: JPRA-Cluster Integration: Real-time techniques in control system implementation Provide input

Company	Researcher
Honeywell Prague Laboratory **Focus:** **Industrial Automation** **Team Leader :** **Vladimir Havlena**	**Vladimir Havlena** Main areas of research: Industrial automation Other projects involved in: Artist2 activities and role: JPRA-Cluster Integration: Real-time techniques in control system implementation Provide input

Company	Researcher
Volvor Car Corporation **Focus:** **Automotive systems** **Team Leader :** **Jakob Axelsson**	**Jakob Axelsson** Main areas of research: systems engineering, real-time systems, safety-critical systems, system architectures, and object-oriented development methods. Other projects involved in: Artist2 activities and role: JPRA-Cluster Integration: Real-time techniques in control system implementation Provide input

Company	Researcher
Volvo Technology Corporation **Focus:** **Automotive systems** **Team Leader :**	**Magnus Hellring** Main areas of research: systems engineering, real-time systems, safety-critical systems, system architectures, drive-by-X applications, and distributed systems. Other projects involved in:

Magnus Hellring	Artist2 activities and role: JPRA-Cluster Integration: Real-time techniques in control system implementation Provide input

Company	Researcher
Maquet Critical Care **Focus:** **Medical systems** **Team Leader :** **Klas Engwall**	**Klas Engwall** Main areas of research: Medical systems Other projects involved in: Artist2 activities and role: JPRA-Cluster Integration: Real-time techniques in control system implementation Provide input

9.5.3 Affiliated Academic Partners

Institution	Researcher
University of Illinois, Urbana-Champaigne **Focus:** **Embedded and real-time systems** **Team Leader :** **Lui Sha, Professor**	**Lui Sha** Main areas of research: Distributed real-time computing systems, dynamic real-time architecture, QoS driven resource management and security and fault tolerance in networked embedded systems Other projects involved in: Numerous US projects Artist2 activities and role: JPRA-Cluster Integration: Control in real-time computing Researcher, provide input

Institution	Researcher
University of Virginia **Focus:** **Embedded and real-time systems** **Team Leader :** **Tarek Abdelzaher, Professor**	**Tarek Abdelzaher** Main areas of research: middleware, OS, and networking solutions for providing performance-guaranteed services in distributed environments, both in embedded systems and on the Internet Other projects involved in: Numerous US projects Artist2 activities and role: JPRA-Cluster Integration: Control in real-time computing Researcher, provide input

9.6 Research and Platform Activities

9.6.1 *JPRA-Cluster Integration:* Control in real-time computing

Leader	Karl-Erik Årzén (Lund: feedback scheduling)
Policy Objective	Advance the state of the art in applying control methods for uncertainty handling and as a way to provide flexibility in embedded computing and communication systems.

9.6.2 *JPRA-Cluster Integration:* Real-time techniques in control system implementations

Leader	Alfons Crespo (UPVLC: embedded control)
Policy Objective	To advance the state of the art in applying real-time system methodology for embedded control system implementation.

9.6.3 *JPRA-NoE Integration*: Participation in activities led in other clusters

Beyond the NoE-Integration activities described here, the cluster “Control for Embedded Systems” is also involved in the NoE Integration activity: “Semantic Framework for Hard Real-Time Design Flow”.

9.6.4 *JPRA-NoE Integration*: Adaptive Real-time, HRT and Control

Leader	Karl-Erik Årzén (Lund University: real-time control/control in embedded computing)
Clusters	Control for Embedded Systems; Hard Real-Time; Adaptive Real-Time
Policy Objective	Integrate research among ARTIST2 control and real-time teams on different computational models for embedded control systems and the use of control techniques to provide flexibility in embedded systems.

9.6.5 *JPIA-Platform*: Design Tools for Embedded Control

Leader	Karl-Erik Årzén (Lund University: real-time control/control in embedded computing)
Policy Objective	Integrate ongoing research efforts on tools for co-design of resource-constrained embedded control systems This would provide an important interface between the control community and the embedded system community and contribute to the simplification of the design process for these systems.

10. Cluster: Testing and Verification

Contributor: Prof. Kim Larsen – BRICS - University of Aalborg

10.1 Description of the Area

10.1.1 Main Research Trends

Within the area of Testing and Verification the overall trend is that systems of increasing complexity with an increasing number of features taking into account may be dealt with.

A definite trend is also, that model-checking and testing techniques are being applied to software validation (in particular C and JAVA) with noticeable successes given by the SLAM, Blast , VeriSoft, Bandera and JAVA-Path-Finder projects. Here, the method of *abstraction-refinement* provides a combination of abstract interpretation with model-checking with success within given application domains (e.g. SLAM and Blast addresses debugging of device drivers).

Another trend within the research area of verification is the (re-)discovery of SAT-solving as a technique for performing so-called *bounded* model-checking. Advances made on SAT-solving during the last 5 years has made this approach competitive compared to other techniques including symbolic model-checking. Members of the T&V cluster are active in pursuing extensions of SAT-solving to extended logics with quantative aspces (difference constraints, liniear constraints) in order to make bounded model-checking applicable to models of embedded systems.

Yet another trend is that the features and properties supported by current technology goes beyond that of pure functional correctness to also include timed, stochastic and hybrid phenomenas. Within the Testing and Verification Cluster research on all of these quantitative extensions are pursued actively pursuing different techniques (bounded model checking, regular model checking, decision diagrams, automata for symbolic representation) are finding their way into powerfull tools (e.g UPPAAL, IF, CMC, MoDeST, EMTCC, FAST).

Advances in verification technology (in particular the development of symbolic datastructures) are finding their way into mature testing tools (e.g TGV, STG, ToRX). Substantial effort has been made by several parthers on model-based testing and monitoring of real-time systems with UPPAAL Tron and IF being some resulting tools. Also, related work on monitoring, controller synthesis, planning and scheduling, and schedulability analysis for real-time systems has been made resulting in tools such as TIMES and UPPAAL Cora and UPPAAL Tiga and several applications.

Model-driven development is highly appriated in software engineering particularly because of the possibility of automatic code-generation. However, for quantitative models the realization on real hardware raises several problems. Indeed, the quantitive models are theoretical frameworks, assuming infinitely fast hardware, infinitely precise clocks, etc. However, these characteristics are not fulfilled on real CPUs, that are digital and have a finite frequency. Current research within the cluster is addressing this problem in the setting of real-time and involves identification on when (and how) given timed automata models are implementable and to what extent properties proved by the model also may be guaranteed to hold of the final implementation.

Within verification of security properties work has been made on the semantic foundations and the verification of security protocols and web-services. A general verification method for secutiry protocols with possible unbounded sessions has been provided as well as a sound and complete inference systems for bounded-sesssions cryptographic protols. The work also include a classification and relation of different existing pecification methods (multiset rewriting and process algebra) for security protocols as well as the use of standard model-checkers for analysing various security protocols (e.g. use of muCRL, SPIN and CADP) and for addressing security treats based on real-time issues (using UPPAAL).

In the area of parallel and distributed model checking of embedded systems we are in close collaboration with other research teams in Europe (INRIA Rhtne-Alpes, CWI, Technical University Munich and Aachen Technical University) attempting to gather the European research communities working in the area on cluster and/or grids. Scientifically the work within the cluster has primarily focused on new algorithms for the enumerative distributed checking of reachability properties, and on extended the scope of *efficient* distributed algorithms to cover model checking of general CTL and LTL properties and of real-time models. The general environement DiVinE has been deployed and has also been extended by a Promela front-end for SPIN.

10.1.2 Industrial Applications

Several of the partners have in their portfolio a large collection ongoing industrial research projects on embedded systems engineering and several of these involve improving current practice with respect to testing and adoptation of verification of early design models. Often the researcher of the consortium meets industry on the topic of model-driven development, through the use of UML and UML-supporting tools such as Rhapsody and visualSTATE.

Sample case-studies carried out by partners of the cluster include:

France Telecom R&D (IRISA, duration 3 years)

> The goal of this project is to build a platform for the formal validation of France Telecom's vocal phone services. Vocal services are based on speech recognition and synthesis algorithms, and they include automatic connection to the callee's phone number by pronouncing her name, or automatic pronuncation of the callee's name whose phone number was dialed in by the user. Here, we are not interested in validation of the voice recognition/synthesis algorithms, but on the logic surrounding them. For example, the system may allow itself a certain number of attempts for recognizing a name, after which it switches to normal number-dialing mode, during which the user may choose to go back to voice-recognition mode by pronouncing a certain keyword. This logic may become quite intricate, and this complexity is multiplied by the number of clients that may be using the service at any given time. Its correctness has been identified by France Telecom as a key factor in the success of the deployment of voice-based systems. To validate them we are planning to apply a combination of formal verification and conformance testing techniques.

BMW (OFFIS R&D Division):

The central technology in the OFFIS R&D Division Safety Critical Systems is the formal verification of models with regard to safety-critical properties. To use this technology in an industrial environment, an optimised connection of the verification technologies to commercial software development tools is necessary. Here, OFFIS has performed the necessary integration work for various modelling tools, including the ASCET-SD tool from the company ETAS.

Accompanying the development of the verification environment for ASCET-SD, there was a project with BMW to test the efficiency of the formal verification techniques based on the active front steering (AFS) developed for the 5-Series BMW. In order to prevent uncontrolled intervention by the active steering, caused by faults in the sensors, the operator instrumentation, or the control unit, there must be very differentiated reactions to diagnosed faults so that the driver is always able to safely control the vehicle. The foundation for a suitable system reaction in case of a fault is fast fault recognition, or alternatively diagnostics of the system as well as error handling that is appropriate for the situation, and which the system is still able to handle.

Besides the actual control-related core functionality, active steering includes cut-off logic, which performs any controlled shutdown of the system depending on the evaluation of the sensor values, and which is outstandingly well suited to this formal verification due to its large logical content.

It has been possible to prove many central properties on this part of the system with the formal verification environment and consequently permanently justify the confidence in the software, which is already in use.

CEA (IRISA, duration 3 years):

The goal of the V3F project is to provide tools to support the verification and validation process of programs with floating-point numbers. More precisely, project V3F investigates techniques to check that a program satisfies the calculations hypothesis on the real numbers that have been done during the modelling step. The underlying technology is based on constraint programming. Constraints solving techniques have been successfully used during the last years for automatic test data generation, model-checking and static analysis. However in all these applications, the domains of the constraints were restricted either to finite subsets of the integers, rational numbers or intervals of real numbers. Hence, the investigation of solving techniques for constraint systems over floating-point numbers is an essential issue for handling problems over the floats.

Our contribution to this project is first to precisely formalize a conformance testing theory for programs with floating point with respect to their specifications, and second, to describe test generation algorithms in this framework. We currently investigate several possibiliies for the first point, where the conformance testing theory should take into account imprecisions due to floating point calculations.

Danfoss (CISS, Aalborg, duration 2 years):

This case-study documents the results of the Danfoss EKC trial project on model based development using IAR visualState. We present a formal state-model of a refrigeration controller based on a specification given by Danfoss. We report results on modeling, verification, simulation, and code-generation. It is found that the IAR visualState is a promising tool for this application domain, but that improvements must be done to code-generation and automatic test generation.

Terma (CISS, Aalborg, duration 3 years):

The company produces (among other things) radar systems mainly used for traffic control in ports and airports and for coastal surveillance. The real-time processing of radar signals includes integration of several received signals, requiring the signals to be stored temporarily in memory. This case-study consider the interface between the signal processing hardware and the memory consists of an arbiter and a collection of 9 FIFO buffersDuring processing the buffers are not allowed to become empty or overflow. The arbiter includes a scheduling algorithm deciding when to access the buffers. The aim of the case study is to verify that the behaviour of the scheduling algorithm is correct. A second step has been to synthesise a scheduler for a set of integrators and buffers. This is particular interesting for TERMA as the next generation of radar sensors will include similar memory interfaces, though with increased demands on access to the memory. The case-study has been fully analysed, an optimal (in terms of size of buffers) scheduler has been synthesized using the tool UPPAAL.

Ericsson Telebit (CISS, Aalborg, duration 3 years):

Ericsson Telebits core competence is to develop IP technologies for Product Units within the Ericsson organisation. ETAS' current main projects are focused on delivering software for the Realtime Router products as well as Ericsson's GSM and 3G mobile terminal platform. Ericsson is continuously engaged in several research projects to maintain their status as a leading provider in the IPv6 world. The goal of the collaboration is the development of a domain-specific methodology for off- and on-line test-case generation from so-called RFC (request for change documents) presented in the form of Live Sequence Charts.

10.2 State of Integration in Europe

10.2.1 European Research Teams

The Testing and Verification cluster includes the leading European research groups within the area and is well connected to other prominent research teams.

In the Netherlands partners are Twente University (core) and Nijmegen University (affiliated). At Twente University research is focucessed on testing and stochastic modelling – both with the desire of establishing theoretical foundations and providing tool support (TorX and MODEST). At Nijmegen University research is along two directions: modelling and analysis of real-time and embedded systems (largely with the use of model checkers SPIN and UPPAAL), and testing of data-intense systems. Other prominent research teams in The Netherlands not partners in the cluster include CWI, Technical University Eindhoven and the Embedded Systems Institute also in Eindhoven. The Dutch research teams are well-connected via national projects (PROGRESS), the teams at CWI and Technical University Eindhoven has just started a new Dutch project (VeriGEM) on distributed model checking which we intend to connect more closely to the activities on Testing and Verification within the cluster. The appointment of Ed Brinksma as scientific director of ESI ensures that the vast number of large industrial research projects on embedded systems carried out on routine basis by this center will be connected to the cluster.

In Germany OFFIS, Oldenburg, is partner of the cluster (core). OFFIS is a partner of the IST project EASIS (Electronic Architecture and System Engineering for Integrated Safety Systems, IST-507690) where the goal is to enable the realization of integrated safety systems by defining a powerful and highly dependable in-vehicle electronic architecture and an appropriate development support. EASIS integrates leading European car manufacturers, suppliers, tool vendors and research institutes to commonly achieve the project goals. Of particular relevance to the T&V cluster are AVACS and VERISOFT, two German top projects on verification and analysis of embedded systems, the DFG[1] funded long-term research project AVACS (Automatic Verification and Analysis of Complex Systems), a Transregional Collaborative Research Center (SFB/TR), and the BMBF[2] funded applied research project VERISOFT. Whereas AVACS´ research challenge is of foundational nature, developing novel verification algorithms covering the design space of complex embedded systems, VERISOFT´s challenge is to achieve fully verified components for industry-critical systems, employing state-of-art automatic and interactive verification tools.

[1] German Research Foundation

[2] The German Federal Ministry of Education and Research

From the Nordic countries participants of the cluster are CISS, Aalborg University and Uppsala University both doing research on testing and verification of real-time systems with emphasis on tool support. The widely distributed real-time verification tool UPPAAL is the most clear witness of a long-term collaboration between these two sites with emerging tools like UPPAAL Cora, UPPAAL Tron and TIMES sharing the fundamental engine of UPPAAL but targeting towards optimal scheduling and planning, real-time testing and schedulability analysis and code-generation, respectively. Prominent Nordic research teams not being prartners of the cluster are the group Chalmers, Gothenburgh Technical University (focussing on SAT-solving and hardware verification), Theoretical Computer Science at Helsinki Technical University, Finland, focussing on LTL model checking and bounded model checking, and Institute of Software Systems, Tampere University of Technology, Finland, with original contributions on reduction methods (stubborn set, partial order reduction, minimization) applied during explicit state-space exploration of concurrent systems.

From France the cluster has Verimag and LSV Cachan as (core) partners with ground-breaking contributions on the theoretical foundation of verification, monitoring and controller synthesis for real-time and hybrid systems. Also, the groups are working actively on providing tool support (IF, Taxys and CMC). IRISA is also (core) partner of the cluster with important research contributions on test generation for models of infinite state systems with control and data. Affiliated partner is LIAFA, University of Paris 7, focussing on verification of infinite-state systems. Other research groups in France relevant to the activities on testing and verification are IRCCyN, Nantex (verification and control of timed and hybrid systems) that is well connected to LSV and Verimag through French national projects CORTOS and CHRONO. Also the VASY research group at INRIA Rhone-Alpes are focusing on analysis of complex systems using LOTOS, with significant tool support CADP and contributions to the state-of-the-art of parallel and distributed model-checking.

In Belgium, The *Centre Fédéré en Vérification* is a working group financed since 2002 by the Belgian National Scientific Research Fund. All the research teams from the french part of Belgium that are interested in computer aided verification are present in the working group including University of Brussels, University of Namur, University of Liège and University of Mons.

From Schwitzerland, EPFL Lausanne is (affiliated) partner with a wide range of ground-breaking research contributions on real-time and hybrid systems, interface automata and games.

Other prominent research groups not being partner of the cluster include a number of teams from United Kingdom, in particular School of Computer Science, Birminghan (probabilistic model checking), Oxford University Computing Laboratory (real-time verification), Microsoft Research Laboratory at Cambridge and Royal Holloway, University of London (security).

From Italy important contributions come from the Automated Verification and Synthesis Group, Trento University (symbolic model-checking, SAT-solving, applications to planning) with support of the nuSMV tool.

Partners of the cluster have been the initiators, SC members and/or served as PC chairs of main conferences in the area such as CAV, TACAS, FORMATS, EMSOFT, CONCUR, ETPAS, PSTV/FORTE, PAPM, HSCC, ARTS, PDMC

10.2.2 Interaction of the Cluster with other Communities

Model-checking technology forms the basis for automatic verification and is utilized for test-case generation. However, model-checking is also increasingly applied successfully within and by other communities including control theory, planning and scheduling and performance evaluation. Members of the cluster has published and given invited talks at main conferences and in journals of these other communities (e.g. ICAPS, European Journal of Control, IFAC Annual Reviews in Control, ACM Performance Evaluation Review).

Also, the activities on parallel and distributed testing and verification are closely linked to the computational services provided to physicist, chemists and biologist via the Danish Center for Grid Computing (www.dcgc.dk) and NorduGrid.

10.2.3 Main for Integration through Artist2

Given the limited resources available within ARTIST2 it is paramount that substantial, additional European funding is obtained to support the man-power required to fully transform the research ideas and prototype tools into industrial testing and verification practice with a supporting collection of tools integrated with existing industrial tool chains.

Also, together with other prominent European research teams, INRIA Rhone-Alpes (France), Technical University Eindhoven and CWI (The Netherlands), the cluster investigates the possibility of pursuing the vision of a European Verification Grid with additional European funding supplementing the various national initiatives in the area.

10.3 Overall Assessment and Vision for the Cluster

10.3.1 Assessment

Each research activity within the cluster has demonstrated a high level of affinity in goals pursued boding for successful integration of the research carried out by the individual partners. The (very) extensive list of publications made by members of the cluster during the first year at leading scientific conferences and journals witnesses true excellence within the area.

The activities within Quantitative Testing and Verification and Verification of Security properties are largely carried out by disjoint groups of people (not research institutions) resulting in less interaction than first anticipated. The activities within Quantitative Testing and Verification and Testing and Verification Platform are tightly connected, but to achieve critical mass in pursuing the vision of a European Verification Grid it is felt necessary to involve other prominent research teams working actively on the topic of parallel and distributed model checking (INRIA Rhone-Alpes (France), Technical University Eindhoven and CWI (The Netherlands)).

Dissemination to research and industry has been done extensively during the first year period by partners individually and in concerted efforts: the participation at the German Verification Day, Oldenborg, March 4 2005, provided a unique opportunity for discussion and exchange of information on verification topics and cluster coordinator Kim G. Larsen gave an invited talk presenting the research of the cluster with emphasis on advances made within the verification tool UPPAAL; the ARTIST2 Summerschool on Modelling&Components, Testing&Verificaiton and Static Analysis, Nässlinge, September 29-October 1, features several participants of the testing and verification cluster as invited speakers (Ed Brinksma, Patricia Bouyer, Jean-Francois Raskin, Gerd Behrmann, Brian Nielsen, Thierry Jeron, Stavros Tripakis).

10.3.2 Vision and Long-Term Goals

As clearly observed by the many industrial contacts of the two national embedded systems centers, ESI (The Netherlands) and CISS (Denmark), testing is *by far* the most used and important validation technique applied by industry today. It is estimated that some *30-70% of the total development cost* for embedded systems is spent on testing at various stages. It is also a general observation that current testing practice is very ad-hoc often with manual construction and even execution of test-scripts. There is clearly a gap between current industrial practice and existing academic state-of-the art technology. It is important that the cluster continues its contribution to the bridging of this gap though collaborative projects attempting to make industry take-up existing state-of-the-art testing and verification techniques.

To focus on aspects such as performance, timeliness, and efficient resource-usage, the testing and verification techniques should be based on models with *quantitative information.* To provide a coherent testing and verification methodology with a well-integrated chain of tools applied in industrial practice is a long-term vision of the cluster.

10.3.3 Recommendations

It is overall important that the partners continue their effort on improving existing methods and their proprietary tools.

Given the limited resources available within ARTIST2 it is paramount that substantial, additional European funding is obtained to support the man-power required to fully transform the research ideas and prototype tools into an industrial testing and verification practice with a supporting collection of tools integrated with existing industrial tool chains.

Also, together with other prominent European research teams, INRIA Rhone-Alpes (France), Technical University Eindhoven and CWI (The Netherlands), the cluster investigate the possibility of pursuing the vision of a European Verification Grid with additional European funding supplementing the various national initiatives in the area.

10.4 Meetings Held

10.4.1 Meeting: Dissemination day on Software Testing – Trends and Visions

Dates	December 1st, 2004
Venue	Aalborg University Aalborg Denmark
Main Organiser	Kim G Larsen Aalborg Univeristy
Web link	
Objectives	Presentation of state-of-the-art and future trends on software testing
Overview of the Agenda	*Tom Ball, Microsoft Research: "SLAM and Static Driver Verifier: Technology Transfer of Formal Methods inside Microsoft"* Klaus Havelund, Kestrel Technology,NASA Ames Research Center: "Automated Runtime Verification" Ed Brinksma, Twente Universitet: "Testing Times: On Model-Based Functional Testing" Grabowski, University of Göttingen: "Modelbased Testing with UML applied to a Roaming Algorithm for Bluetooth Devices"
Conclusions	100 participants from the Danish industry and research community

10.4.2 Meeting: Business Meeting, Cluster on Testing and Verification

Dates	December 15, 2004
Venue	ULB Brussels Belgium
Main Organiser	Kim G Larsen Aalborg University
Web link	http://www.artist-embedded.org/FP6/intranet/ClusterPages/TV/PastMeeting-041215-T+V-Joint-Cluster-Meeting.php
Objectives	Introduction of partners. Planning of future work.
Overview of the Agenda	See web page

Conclusions	The partners obtained knowledge of each others work

10.4.3 Meeting: Business Meeting, Cluster on Testing and Verification

Dates	March 3, 2005
Venue	Oldenburg University Oldenburg Germany
Main Organiser	Kim G Larsen Aalborg University
Web link	http://www.artist-embedded.org/FP6/ARTIST2Events/SummerSchools/Artist05.html
Objectives	To go into details on the selected topics. To participate in the German Verification Day arranges by OFFIS/AVACS
Overview of the Agenda	See web page
Conclusions	Web pages for tools and case studies will be made. A summer school will be arranged on Testing & Verification, Components & Modelling and Statical Analysis in collaboration with two other clusters. See http://www.artist-embedded.org/FP6/ARTIST2Events/SummerSchools/Artist05.html
Next meetings planned	Business meeting September 2005 at Uppsala Summer School organised by: Kim G Larsen

10.4.4 Meeting: Workshop on the link between formal and computational models

Dates	June 23-24 2005
Venue	ENS, Paris, France
Main Organiser	Yassine Lachnech and others Verimag
Web link	http://www.loria.fr/~cortier/workshop.html
Objectives	Models for Protocol Verification
Overview of the Agenda	See web page
Conclusions	More than 70 international participants

10.4.5 Meeting: Embedded World 2005, Nürnberg

Dates	February 22-24, 2005
Venue	Nürnberg Messe, Nürnberg, Germany
Main Organiser	
Web link	http://www.embedded-world-2005.de/main/Page.html
Objectives	Aalborg participated in the National Danish exhibition at Embedded World 2005. The aim was to promote embedded software systems in general and two projects inparticular: The Uppaal tool and indoor climate contro
Overview of the Agenda	See web page
Conclusions	The stand was well visited and gave many contacts. More than 12.000 visitors to Embedded World 2005

10.5 Research and Platform Activities

10.5.1 ***JPRA-Cluster Integration**:* Quantitative Testing and Verification

Leader	Ed Brinksma (University of Twente: real-time testing and stochastic modelling and analysis)
Policy Objective	The objective is to combine the efforts and skills of the individual leading researchers in Europe into a world-class virtual team, for advancing the state-of-the-art in verification and testing methodologies. Achieving this objective requires development of theory, methods and tools for testing and verification of embedded systems with an emphasis on quantitative aspects (e.g. real-time and stochastic phenomena), that are of particular importance for the correctness of embedded systems. A particular effort will be made to transfer knowledge, methods and tools to industry, including integration of the techniques developed into existing tools.

10.5.2 ***JPRA-Cluster Integration**:* Verification of Security Properties

Leader	Yassine Lakhnech (Verimag: semantics and models for security protocols)
Policy Objective	Focus and align research in the area, with an emphasis on security for smart cards, e-commerce, and cell phones. Establish coherent links between research and industry. Develop the basic technology needed to certify security applications at levels EAL6, and EAL7, from the Common Criteria. Create the necessary critical mass for moving the state security technologies forward for embedded systems in Europe. This implies taking the next steps towards a ubiquitous, tight, and fluid security infrastructure for the area.

10.5.3 ***JPRA-NoE Integration***: Participation in activities led in other clusters

In Year 1, the cluster “Testing and Verification” has not been involved in any NoE Integration activities.

10.5.4 *JPIA-Platform*: Testing and Verification Platform for Embedded Systems

Leader	Kim G. Larsen (BRICS/Aalborg: verification and testing of real-time systems)
Policy Objective	Construction of powerful analysis tools by establishing a joint server platform providing extraordinary computational resources for conducting large-scale verification and testing efforts for embedded systems with

	respect to real-time requirements, quality-of-service guarantees as well as security properties. The platform will provide a uniform, open and secure access and to all testing and verification tools of the academic as well as industrial partners of the consortium. The platform builds on existing works from the various partners and will also make available new powerful analysis tools developed within the network, in particular those from the related Joint Research Activities ("Quantitative Testing and Verification" and "Verification of Security Properties").