ARTIST 2

Network of Excellence

IST-004527 ARTIST2:
Embedded Systems Design

18-month Workprogramme
September 2005 – February 2007

Scientific Coordinator: Joseph Sifakis
Technical Coordinator: Bruno Bouyssounouse

Based on input from the Cluster and Activity Leaders:

Albert Benveniste (INRIA)

Giorgio Buttazzo (Pavia)

Reinhard Wilhelm (Saarland University)

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Karl-Erik Arzen (Lund University)

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1. Joint Programme of Activities

1.1 Overview

The NoE is structured and will function as a distributed laboratory – composed of its virtual teams (clusters) which perform research activities. These JPRA activities can be internal to the clusters ("Cluster Integration"), or between clusters ("NoE Integration") to achieve the overall integration of the NoE. These are detailed in the diagram on the following page.
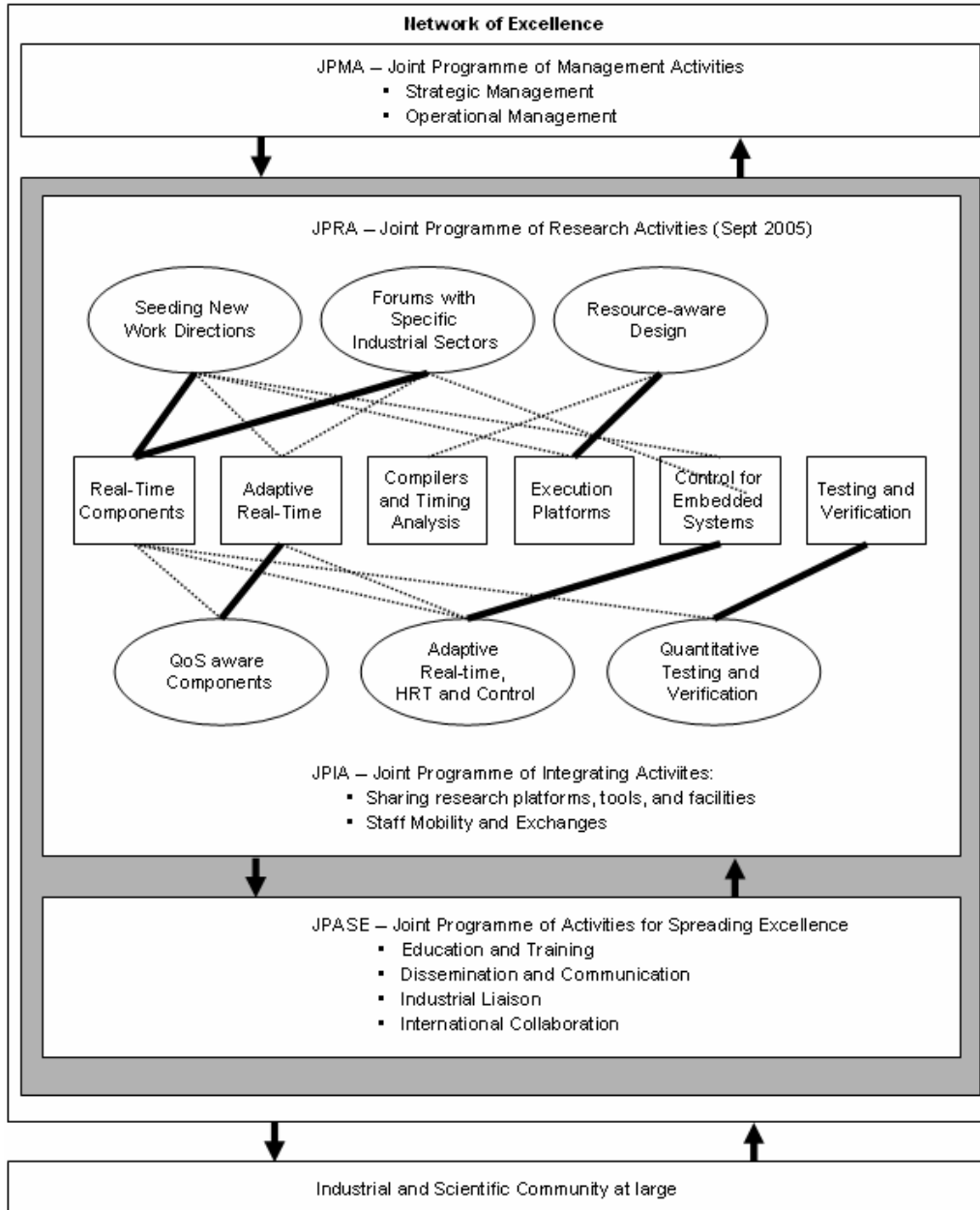
The "Cluster Integration" activities are managed within the cluster. For clarity they are not shown in the diagram, but are essential for integration at the cluster level. The "NoE Integration" activities - shown as ovals in the diagram – involve many clusters, and are driven by one cluster (identified by the thicker line).

The JPIA activities are transversal to the JPRA activities, and aim mainly to support their development through platforms, mobility, and infrastructure. They are strongly coordinated with the JPRA, and form the cement for the NoE's internal integration.

The JPASE activities serve as the interface between the NoE and the community at large.

## 1.2 Proposed Changes at End of Year 1

In the coming year, we propose to implement the following changes to the Artist2 structure:

- Merger of the Hard Real Time cluster with the "Modelling and Components" clusters into a single "Real Time Components" cluster. This new cluster will be managed by Albert Benveniste, assisted by Bengt Jonsson and Alberto Sangiovanni Vincentelli. The details regarding the activities are provided in the Milestones, in section 2 of this document.
  After this merger, the activity on Diagnosis in Distributed Hard Real Time Systems is halted. Nonetheless, the researchers who have participated in this activity are hosted in the Testing and Verification cluster.

- The activity leader for the "Verification of Security Properties" in the Testing and Verification cluster is now Sandro Etalle (Twente). We would have liked to implement Security in Embedded Systems as a full cluster, but for now there has been insufficient critical mass within the consortium.

- A new activity will probably be created over the course of Year 2, in the Adaptive Real Time cluster, called "Real-Time Languages", and led by the University of York. It would mainly focus on adding a real-time profile for Java.

- Reinforce collaboration within the Compilers and Timing Analysis cluster. This can be implemented by launching joint activities between the two communities.

- Two affiliated partners will now be full partners within the consortium: Tidorum is a small start-up company, and Ace is a tool provider for the CoSy compiler used in the Compilers and Timing Analysis cluster's platform.

- As planned initially, we have added the EPFL (Lausanne, Switzerland) as a core partner.

- Two leading researchers (Giorgio Buttazzo and Gerhard Fohler) have changed universities, and thus we will extend core membership to the Scuola Superiore Sant'Anna in Pisa and the University of Kaiserslautern. The University of Malardalen remains a core partner while the University of Pavia becomes an affiliated partner.

1.3 Governance

The governance structure is specified in the Consortium Agreement, and is reproduced below.

The methodology adopted for achieving the JPA objectives follows the same lines as for managing a laboratory. The activities, their objectives, their technical description, the partners involved, their roles, and the resources available have been clearly defined in the initial Description of Work, and updated in the deliverables. This will be monitored and guided by a tight and rigorous management, as defined in the diagram below:
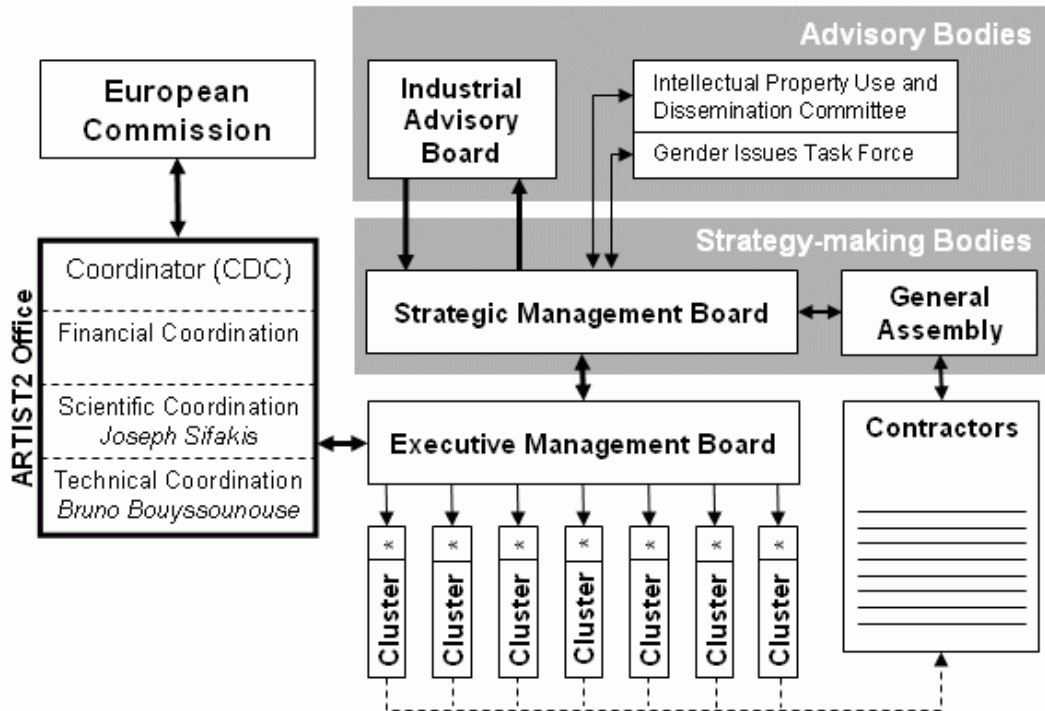
The main governance bodies are:

The **General Assembly** is composed of one representative per core partner. It is convened at the beginning of the project and meets once per year. It is chaired by the Scientific Manager.

The **Strategic Management Board** is initially composed of the NoE cluster leaders, and a representative of the Coordinator – who attends, with no voting rights. It is chaired by the Scientific Manager, assisted by the Technical Manager. It meets at least once per year – close to the General Assembly meeting. Its members are elected by the General Assembly every two years, according to modalities to be determined in the Consortium Agreement.

The **Cluster Leaders** (who compose the Executive Management Board) are responsible for the overall coordination of the activities led by their cluster. A cluster functions as a virtual team – with a degree of autonomy for defining its internal meetings and day to day management.

Over the course of the coming year, we do not intend to implement any changes to this management approach, but we do intend to reinforce, rationalize and insofar as is possible to automate the reporting. All the bodies have proven to be effective.

Nevertheless, the interaction with the Industrial Advisory Board has not been effective.

Within the consortium, we should improve the reporting procedures, and strengthen monitoring.

The NoE is moving forward with plans for setting up a sustainable structure for continuing interaction between research and industry, after the end of the NoE contract.

2. Project Timetable / Milestones

Given the size and complexity of the Artist2 NoE, it is preferable to use a detailed set of milestones to describe the JPA. This has the added advantage of presenting the past achievements and the expected evolution.

The JPA is organized into activities. The activities should not be considered as tasks of a workprogramme, with begin/end and synchronisation dependencies. Of course, the detailed description of an activity could be decomposed into sub-tasks and intermediate milestones, but this would imply a granularity that is too fine for research activities.

The inter-dependencies between activities are complex and rich, and will evolve dynamically. The work plan for the activities is provided in the 18 month workpackage descriptions.

The major milestones per activity are described below, updated at the start of Year 2:

2.1 Cluster: Real-Time Components

Albert Benveniste (INRIA)

This is a new cluster led by Albert Benveniste (INRIA), which takes up some of the activities previously in the clusters halted at the end of Year 1: "Hard Real Time" and "Modelling and Components".

The following activities from the two previous clusters will continue in the new cluster:

- WP1: Platform for Component Modelling and Verification
- WP4 Cluster Integration: Development of UML for Real-time Embedded Systems

The following activities are new starting in Year 2, taking up many of the essential elements of the activities "Semantic Framework for Hard Real-Time Design Flow" and "Merging the Event-triggered and Time-triggered Paradigms", and "Diagnosis in Distributed Hard Real-time Systems".

- WP4 NoE Integration: Forums with Specific Industrial Sectors
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The following activities are halted at the end of Year 1:

- WP4 Cluster Integration: Component Modelling and Composition
- WP3 NoE Integration: Semantic Framework for Hard Real-Time Design Flow
  (see the new activities above)
- WP3 NoE Integration: Merging the Event-triggered and Time-triggered Paradigms
  (see the new activities above)
- WP5 Cluster Integration: Diagnosis in Distributed Hard Real-time Systems
  (see the new activities above)

The milestones for the activities in Year 2 are as follows:

- **WP1: Platform for Component Modelling and Verification**
  Previously in "Modelling and Components".
  Susanne Graf (Verimag)

  - o (achieved) Year1: Initial definitions of modules to assemble in the platform

  - o Year2: Initial connections within a common framework of existing UML-based analysis and validation tools.

  - o Year3: Connect in a common framework several existing UML-based analysis and validation tools by means of mappings to a semantic framework shared by several tools.

  - o Year4: Final integration of the results of the related Joint Research Activities.

- **WP4 Cluster Integration: Development of UML for Real-time Embedded Systems**
  Previously in "Modelling and Components"
  Francois Terrier (CEA)

  - o Annual Y1-3 milestones: Continued work with the OMG for advancing the UML standard, for real-time systems, leading to the year4 milestone.

  - o Year4: Work should promote convergence of different views on how UML should be defined and be used for real-time system development, which will induce greater interaction between tool providers, developers, and researchers in the area.

- **WP4 NoE Integration: Forums with Specific Industrial Sectors**
  New activity started in Year 2.
  Albert Benveniste (INRIA)

  - o Year2: organize a forum with AUTOSAR industrial actors on the topic of design methods and tools for heterogeneous large embedded systems; draw resulting issues and research questions. Co-organizers Werner Damm (OFFIS) and Albert Benveniste (INRIA)

  - o Year3: organize a forum with aeronautics sector; draw resulting issues and research questions on the topic of design methods and tools for heterogeneous large embedded systems; plan a third forum with another sector, not fixed yet.

  - o Year4: organize the third forum; draw resulting industrial issues and research questions on the topic of design methods and tools for heterogeneous large embedded systems; deliver a summary of findings and recommendations for research on the topic of design methods and tools for heterogeneous large embedded systems.

- **WP4 NoE Integration: Seeding New Work Directions**
  New activity started in Year 2.
  Albert Benveniste (INRIA) and Alberto Sangiovanni (PARADES)

  - o Year2: organize a *research seeding* meeting on the topic "Classification and study of Models of Computation and Communication (MoCC), and resulting Conceptual Model for Embedded Systems". Co-organizers Paul Caspi (Verimag) and Hermann Kopetz (TU Vienna)

- o Year3: organize a *seeding research* meeting on a topic not fixed yet, but related to design methods and tools for heterogeneous large embedded systems.

- o Year4: organize a *seeding research* meeting on a topic not fixed yet, but related to design methods and tools for heterogeneous large embedded systems. Write concluding report on the findings of this JPRA.

2.2 Cluster: Adaptive Real-Time

Giorgio Buttazzo (Pisa)

- **WP1 Platform: A common infrastructure for adaptive Real-time Systems**
  Giorgio Buttazzo (Univ. of Pavia)

  - o (achieved) Year1: Initial definition of the operating system and network features

  - o Year2: Deploy a working platform for experimental RTOS and network development

  - o Year3: Participate in the evolution of RTOS and networking standards, by developing new concepts.

- **WP3 NoE Integration: QoS aware Components**
  Alejandro Alonso (UP Madrid)

  - o Year2: Definition of notations for describing QoS properties of component interfaces and precise techniques for composing them.

  - o Year4: Development of holistic frameworks and models for QoS management that show how to combine features of component models, component frameworks, middleware infrastructure, OS and Kernel support, and networking.

- **WP6 Cluster Integration: Flexible Scheduling Technologies**
  Giorgio Buttazzo (Pavia)

  - o (achieved) Year1: Preliminary work on the integration of diverse scheduling schemes

  - o Year2: Demonstrate the combination of specific scheduling schemes applied both to CPU as well as to the network, to suit diverse application requirements in the same system

  - o Year4: Provide a framework providing for the seamless integration of flexible scheduling schemes, allowing the choice of appropriate scheduling methods for individual activities in a system or messages on the network.

- **WP6 Cluster Integration: Adaptive Resource Management for Consumer Electronics**
  Gerhard Fohler (Mälardalen University)

  - o (achieved) Year1: Identify case studies, perform preliminary assessment

  - o Year2: Define a set of case studies and from them deduce the QoS requirements and their mapping into operational parameters of the computing and communication infrastructures.

- o Year3: Expend these into a meaningful set of requirements of dynamic application domains (for instance, multimedia) that allow the creation of global mechanisms for resource management.
- o Year4: Integration of the application adaptation processes into a general QoS resource management structure.

2.3 Cluster: Compilers and Timing Analysis

Reinhard Wilhelm (Saarland)

- **WP1: Timing - Analysis Platform**
  Reinhard Wilhelm (Saarland University)

  - o Year2: Standard tool architecture and interfaces

  - o Year3: Initial integration of existing components

  - o Year4: Version 2 integration of existing components

- **WP1: Compilers Platform**
  Rainer Leupers (RWTH Aachen)

  - o (achieved) Year1: Initial definition of the year1 compiler platform and synthesis tools

  - o Year2: Initial implementation of the platform

  - o Year4: Version 2 of the platform

- **WP7 Cluster Integration: Architecture-aware compilation**
  Rainer Leupers (RWTH Aachen)

  - o (achieved) Year1: Loop-splitting algorithms of Dortmund University will be integrated into the IMEC tool flow.

  - o Year2: Integrate the Program-Analyzer Generator (PAG) into the Compilers Platform

  - o Year3 Integrate further innovative functionalities into the Compilers Platform

  - o Year4: Released version of the Compilers Platform

2.4 Cluster: Execution Platforms

Lothar Thiele (ETHZ)

- **WP1 Platform: System Modelling Infrastructure**
  Jan Madsen (Technical University of Denmark)

    o Year2: Initial definition of the modelling platform

    o Year3: Version 1 of the system modelling platform implementation

- **WP3 NoE Integration: Resource-aware Design**
  Luca Benini (University of Bologna) and Peter Marwedel (University Dortmund)

    o Year2: A set of tools that can interact and work together and demonstrate the achievable optimizations on a particular hardware platform

    o Year4: A methodology for the design of predictable embedded systems

- **WP8 Cluster Integration: Communication-centric systems**
  Rolf Ernst (TU Braunschweig)

    o (achieved) Year1: Assess the state-of-the-art in models that take into consideration the particularities of various quasi-standard communication protocols during system analysis and scheduling

    o Year2: New best-case/worst-case models for hard real-time systems and at combined statistical and interval models for QoS applications in multi-media. These models may combine communication and computation, different models of computation, event models and scheduling policies

    o Year3: Analytic methods to estimate system properties

    o Year4: Refinement and dissemination of these methods

- **WP8 Cluster Integration: Design for low power**
  Luca Benini (University of Bologna)

    o Year2: Component models will be investigated that model power dissipation of system components

    o Year4: Integration of the different levels of abstraction - from scheduling via operating systems to system design - participating in low power design

2.5 Cluster: Control for Embedded Systems
Karl-Erik Arzen (Lund)

- **WP1 Platform: Design Tools for Embedded Control**
  Karl-Erik Årzén (Lund University)

  o (achieved) Year1: Generate a survey of existing co-design tools for control, computing and communication

  o Year2: Identification of which of the existing tools that will be included in the platform, and specification of their interfaces

  o Year3: Develop the necessary interfaces that allow the individual tools to be used together

  o Year4: Usage of the tools in new co-design based research activities, adoption in industrial case studies.

- **WP3 NoE Integration: Adaptive Real-time, HRT and Control**
  Karl-Erik Årzén (Lund University)

  o (achieved) Year1: Setting the technical background and assess the needs

  o Year2: Demonstrate that applications of diverse type can be specified in terms of resource-aware tasks

  o Year3: Demonstrate that scheduling algorithms can be made adaptive by means of control schemes

  o Year4: Recommendations for new computational models and methods based on well established control theory for resource-constrained real-time applications.

- **WP9 Cluster Integration: Control in real-time computing**
  Karl-Erik Årzén (Lund University)

  o (achieved) Year1: Roadmap describing the current state-of-the-art and the important research issues

  o Year2-4: Progress made on the fundamental underlying issues: decreased requirements on prior knowledge about resource utilization, increased possibilities to use COTS implementation platforms, and enhanced robustness towards load variations

- **WP9 Cluster Integration: Real-time techniques in control system implementations**
  Alfons Crespo (UPVLC)

  o (achieved) Year1: Roadmap describing the current state-of-the-art and the important research issues

  o Year2: A common framework of the control parameters that can be influenced by an embedded control system implementation and the real time operating systems criteria that can be adjusted to increase the robustness of the control system.

  o Year3-4: A common framework model in order to facilitate the control and computing co-design

2.6 Cluster: Testing and Verification

Kim Larsen (Aalborg)

- **WP1 Platform: Testing and Verification Platform for Embedded Systems**
  Kim G. Larsen (BRICS/Aalborg)

    - o Year2: A server on which the main testing and verification tools developed and used by the participants will be installed and configured.
      Design of a coordination layer for parallel and distributed model checking, Design of a GRID infrastructure, links to mature model checking tools via the Yahoda homepage.

    - o Year4: Integration of results from the related Joint Research Activities

- **WP10 Cluster Integration: Quantitative Testing and Verification**
  Ed Brinksma (University of Twente)

    - o (achieved) Year1: Initial results for testing and verification with emphasis on quantitative aspects

    - o Year2: Develop theory, methods and tools for testing and verification of embedded systems with emphasis on quantitative aspects (e.g. real-time and stochastic phenomena) that are of particular importance for the correctness of embedded systems.
      Further work on robustness, metrics and abstraction. Also collect and classify major case studies.

    - o Year3: Existing verification tools and test generation tools are more strongly connected, including stronger links between academic and industrial tools

    - o Year4: Emergence of a range of new powerful debugging and analysis based on various combinations of testing and verification techniques.

- **WP10 Cluster Integration: Verification of Security Properties**
  Yassine Lakhnech (Verimag)

    - o (achieved) Year1: Define a reference model for security protocols

    - o Year2: prototypes capable of performing automatic analysis of security protocols

    - o Year4: Contributions to standards for security protocols

2.7 Global NoE Activities

JPIA-Staff Mobility and Exchanges (WP1)

- **WP1: Staff Mobility and Exchanges**
  All partners
    - o Over the course of the next 18 months, we expect to have the same level of staff mobility as was the case for Year 1 (40 travels, detailed in section 6.1 of the Spreading Excellence deliverable). Currently, we have 30 travels already planned (see the detailed cluster descriptions in this document), although more will be defined over the course of the period.

JPASE-Education (WP2)

- **WP2: Courseware**
  At the end of Year 1, we feel that the best feasible solution is to collect and disseminate courseware from past and ongoing events, and provide pointers to existing external materials and repositories.

- **WP2: Support for Summer Schools**
  Bruno Bouyssounouse (Verimag)
    - o We will provide support to schools:
        - Summer school on communication centric systems (Summer 2006).
        - Adaptive real-time and control summer school (Summer 2006).
        - ARTIST2 / UNU-IIST Spring School in China on Models, Methods and Tools for Embedded Systems (April 3rd-15th, 2006, in Xi'an, China: http://www.artist-embedded.org/FP6/ARTIST2Events/Events/ChinaSchool/).
        - ARTIST2 Summer School in Sweden, summer 2006.

JPASE – Dissemination and Communication (WP2)

- **WP2: Organisation and Support for Conferences, Workshops, Seminars**
  Bruno Bouyssounouse (Verimag)
    - o Artist2 will organise the following workshops :
        - EmSoft within Embedded Systems Week (http://herkules.it.uu.se:8082/index.php?option=com_content&task=view&id=16&Itemid=30)
        - ARTIST2 Workshop: System Modelling for the Automotive Industry on AUTOSAR (Innsbruck, Austria - March 24th, 2006).
        - MARTES in October 2006 on Modelling and Analysis of Real Time Embedded Systems
        - Embedded electronics in automobile beyond AUTOSAR
        - Fundamental Challenges raised by Integrated Modular Avionics, in fall 2006 or winter 2007.

- Fundamental Challenges related to Real-Time Components raised by Consumer Electronics and Telecommunications, in fall 2006 or winter 2007.

- Conceptual Model for Distributed Embedded systems, and a taxonomy of MoCCs (Models of computation and Communication), in spring or fall 2006.

- Workshop on system modelling for communication centric systems, in the summer of 2006.

- Workshop on distributed embedded systems in Leiden (21.11.2005 – 24.11.2005).

- Workshop on Dynamics and Models of Computer Software Systems (June-August 2006)

- Control over networks (June 2006)

- Adaptive RT, HRT and Control Workshop 1 (late Spring 2006).

- Adaptive RT, HRT and Control Workshop 2 (late Fall 2006).

- Workshop on the link between formal and computational models (July 9-16, 2006, Venice, Italy)

- **WP2: Web Portal for Dissemination**
  Bruno Bouyssounouse (Verimag)

  o Over the course of the second year, we will spend considerable efforts for setting up the web portal as described in the Description of Work.
  The web portal will include the following elements relevant for Embedded Systems Design:

    - Access to main documents, including books, journals, position papers, documentation for standards, newsletters, and in particular, documents produced by Artist2.

    - Information about main events, including conferences, schools, seminars, high-level events, and in particular the events organised by Artist2.

    - Access to courseware collected by the Artist2 partners from education events, as well as links to other sites providing materials.

    - Management of a set of mailing lists, for selected themes (upcoming thesis presentations, open positions, calls for papers, etc).

JPASE – Industrial Liaison (WP2)

- **WP2: Links to Industry**
  Bruno Bouyssounouse (Verimag)

  o Year1-4: Actions for structuring industrial relations between ARTIST2 and European R&D, through involvement in Integrated Projects and in the governance of the ARTEMIS European Technology Platform.

- **WP2: Contributions to Standards**
  Bruno Bouyssounouse (Verimag)

  o Year1-4: In Year2, we will continue ongoing work on standards.

One top new priority for Year2 is the actions around the AutoSar standard for automotive applications. We have already planned a workshop on the standard that will take place in Innsbruck, March 23rd-25th.

JPASE – International Collaboration (WP2)

- **WP2: International Collaboration**
  Bruno Bouyssounouse (Verimag)
  Annual International Collaboration events, continuing and expanding on the annual events organised by the ARTIST FP5 Accompanying Measure. The annual events are each focused on a specific topic, and include presentations from leading figures in Europe, the USA, and Asia.

2.8 Provisional Budget: Sept 2005 – February 2007

| | 4 Year Total: 6 500 000 | 18 Month Total: 2 437 500 € | **18 month amounts:** |

JPMA	*WP0*	**Joint Programme of Management Activities**	**170 625 €**	
		Artist2 Office		170 625 €
JPIA	*WP1*	**Joint Programme of Integration Activities**		
		Sharing Research Platforms, Tools Facilities	**527 388 €**	
		Platform for Component Modelling and Verification		73 128 €
		A common infrastructure for adaptive Real-time Systems (Platform)		57 689 €
		Timing - Analysis Platform (Platform)		88 841 €
		Compilers Platform (Platform)		87 750 €
		System modelling infrastructure (Platform)		70 608 €
		Design Tools for Embedded Control (Platform)		65 004 €
		Testing and Verification Platform for Embedded Systems (Platform)		84 369 €
		Mobility	**268 704 €**	
		Mobility between partners' sites (core or not)		268 704 €
JPASE	*WP2*	**Joint Programme of Activities for Spreading Excellence**	**292 500 €**	
		Education (Summer & Graduate Schools)		48 750 €
		Dissemination and Communication (workshops, seminars, web portal)		73 125 €
		Industrial Liaison (direct interaction with leading companies)		73 125 €
		International Collaboration (High Level Events)		97 500 €
JPRA		**Joint Programme of Research Activities**		
	WP3	NoE Integration	**574 155 €**	
		Forums with specific industrial sectors (NoE Integration)		167 211 €
		Seeding New Work Directions (NoE Integration)		83 606 €
		QoS aware Components (NoE Integration)		42 377 €
		Resource-aware Design (NoE Integration)		119 435 €
		Adaptive Real-time, HRT and Control (NoE Integration)		82 122 €
		Quantitative Testing and Verification (NoE Integration)		79 406 €
	WP4	*Merged into WP5 (when Components and Modelling merged with HRT to form Real Time Components)*		
	WP5	Cluster Integration for cluster: "Real-Time Components"	**37 782 €**	
		Development of UML for Real-time Embedded Systems (Cluster Integration)		37 782 €
	WP6	Cluster Integration for cluster: "Adaptive Real-Time"	**176 240 €**	
		Flexible Scheduling Technologies (Cluster Integration)		63 590 €
		Adaptive Resource Management for Consumer Electronics (Cluster Integration)		59 049 €
		Real-Time Languages (Cluster Integration)		53 601 €
	WP7	Cluster Integration for cluster: "Compilers and Timing Analysis"	**55 575 €**	
		Architecture-aware compilation (Cluster Integration)		55 575 €
	WP8	Cluster Integration for cluster: "Execution Platforms"	**153 825 €**	
		Communication-centric systems (Cluster Integration)		80 694 €
		Design for low power (Cluster Integration)		73 131 €
	WP9	Cluster Integration for cluster: "Control for Embedded"	**122 504 €**	

Control in real-time computing (Cluster Integration)		52 502 €
Real-time techniques in control system implementations (Cluster Integration)		70 002 €
WP10 Cluster Integration for cluster: "Testing and Verification"	**58 203 €**	
Verification of Security Properties (Cluster Integration)		58 203 €

2.9 Indicative Efforts (Sept 2005 – February)

Figures are in man*months	JPMA WP0 Management	JPIA WP1 Platforms & Mobility	JPASE WP2 Spreading Excellence	JPRA WP3 NoE Integration	WP5 Real-Time Components	WP6 Adaptive Real-Time	WP7 Compilers and Timing Analysis	WP8 Execution Platforms	WP9 Control for Embedded	WP10 Testing and Verification	TOTALS
CDC	26										26
UJF/Verimag	26	6	4	12	2					3	53
Aachen		3	14	4			2				23
Aalborg		10	1							3	14
Absint		5	1				2				8
Aveiro		2	1	1		3					7
Cantabria		1	1			5					7
CEA		4	1	3	4						12
CFV		2	1							3	6
Czech		5	1	2					3		11
Dortmund		3	1	4			2				10
DTU		5	1	3				5			14
ETHZ		3	1					6			10
FTRD			1	2						2	5
INRIA		6	2	7	1					2	18
KTH		5	1	2					7		15
Linkoping		4	2	3				4			13
CNRS		2	1							3	6
Lund		5	2	2					7		16
Malardalen		3	6			1					10
OFFIS			1	5							6
PARADES			1	7						1	9
Pavia			2			1					3
Madrid		2	1	5		5					13
Saarland		5	2	4			2				13
ST		3	1				2				6
Eindhoven			1					6			7
Vienna		3	2	9			2				16
TUBS		5	1					5			11
Twente		2	1							5	8
Bologna		4	1	3				5			13
Uppsala		17	2	4						2	25
UPVLC		5	2	2					7		16
York		4	1			5					10
Porto		1	1			4					6
EPFL		2	1	12						2	17
Pisa		9	1	1		8					19
ACE		5	1								6
Tidorum		3	1								4
KaiserSlautern		2	1	1		4					8
TOTALS	52	146	68	98	7	36	12	31	24	26	500

2.10 List of Workpackages and Deliverables

The description of the Joint Programme of Activities for the first 18 months is composed of the following workpackages. Each workpackage consists of a set of activities.

> **Joint Programme of Activities**
> **(18 months period Sept 2005 – Feb 2007)**

All deliverables listed here are: of nature "R"=Report, Dissemination Level = "PU"=Public, and to be delivered at project month 24 (Sept 2006).

Person-months are a rough estimation, covering all partners (not just the lead contractor).

WP	Work package title		Lead contractor	Start month	End month	Deliverable ID
WP0	JPMA : Joint Programme of Management Activities	1	CDC	0	48	**D1-Mgt-Y2** **Year 2 Project Management Report**
		2	UJF/ VERIMAG	0	48	**D2-Mgt-Y2** **Year2 Project Activity Report**
WP1	JPIA : Joint Programme of Integrating Activities	2	UJF/ VERIMAG	0	48	**D4-RTC-Y2** **Component Modelling and Verification (Platform)**
		37	Scuola Sant'Ana	0	48	**D11-ART-Y2** **A common infrastructure for adaptive Real-time Systems (Platform)**
		25	Saarland	0	48	**D14-CTA-Y2** **Timing - Analysis (Platform)**
		3	Aachen	0	48	**D15-CTA-Y2** **Compilers (Platform)**
		12	DTU	0	48	**D19-EP-Y2** **System modelling infrastructure (Platform)**
		16	KTH	0	48	**D23-Control-Y2** **Design Tools for Embedded Control (Platform)**
		4	Aalborg	0	48	**D26-TV-Y2** **Testing and Verification Platform for Embedded Systems (Platform)**
WP2	JPASE : Spreading Excellence	2	UJF/ VERIMAG	0	48	**D3-Mgt-Y2** **Report on Spreading Excellence**
WP3	JPRA : NoE Integration - Research Activities	32	Uppsala	13	48	**D6-RTC-Y2** **Forums with specific industrial sectors (NoE Integration)**
		15	INRIA	13	48	**D7-RTC-Seeding New Work Directions (NoE Integration)**

		24	UP Madrid	0	48	**D8-ART-Y2** **QoS aware Components** **(NoE Integration)**
		31	Bologna	0	48	**D16-EP-Y2** **Resource-aware Design** **(NoE Integration)**
		19	Lund	0	48	**D20-Control-Y2** **Adaptive Real-time, HRT and** **Control (NoE Integration)**
		30	Twente	0	48	**D24-TV-Y2** **Quantitative Testing and** **Verification (NoE Integration)**
Please note that workpackages WP5-WP10 concern only Cluster integration (not NoE Integration), **and do not include the Platforms (which are in WP1).** **Workpackage 4 (Modelling and Components) was halted at the end of Year 1**						
WP5	JPRA : Real-Time Components	8	CEA	0	48	**D5-RTC-Y2** **Development of UML for Real-** **time Embedded Systems** **(Cluster Integration)**
WP6	JPRA : Adaptive Real-time	7	Cantabria	0	48	**D9-ART-Y2** **Flexible Scheduling** **Technologies** **(Cluster Integration)**
		40	Kaiserslauter	0	48	**D10-ART-Y2** **Adaptive Resource Management** **for Consumer Electronics** **(Cluster Integration)**
		34	York	18	48	**D12-ART-Y2** **Real-Time Languages** **(Cluster Integration)**
WP7	JPRA : Compilers and Timing Analysis	25	Saarland	0	48	**D13-CTA-Y2** **Architecture-aware compilation** **(Cluster Integration)**
WP8	JPRA : Execution Platforms	29	TUBS	0	48	**D17-EP-Y2** **Communication-centric systems** **(Cluster Integration)**
		31	Bologna	0	48	**D18-EP-Y2** **Design for low power** **(Cluster Integration)**
WP9	JPRA : Control for Embedded Systems	19	Lund	0	48	**D21-Control-Y2** **Control in real-time computing** **(Cluster Integration)**
		33	UPVLC	0	48	**D22-Control-Y2** **Real-time techniques in control** **system implementations** **(Cluster Integration)**
WP10	JPRA : Testing and Verification	30	Twente	0	48	**D25-TV-Y2** **Verification of Security** **Properties (Cluster Integration)**

3. Research Activities (JPRA) and Integrating Activities (JPIA): Detailed View

3.1 Cluster: Real-time Components

Cluster leader: Albert Benveniste (INRIA)

The following is a description of the activities and overall objectives for the period: September 2005 – February 2007. The next reporting period will cover September 2005 – August 2006.

This is a new cluster resulting from the merge of the former two clusters on Hard Real-Time and Components. This merge has been found quite natural, considering the convergence of the foci during the first period.

On the other hand, during the first period, we better learnt what we can gain from ARTIST2. Our original workplan was structured according to research topics. We found instead that ARTIST2 is better at acting as "seed support" for future research activities to be conducted elsewhere, very much like "seed capital" is needed to launch start-ups. As a consequence, we found that our previous structuring was not best adequate. While the organization of HRT around *diagnosis* proved appropriate, HRT quickly decided that the two topics of *semantic platform* and *merging ET&TT* should be considered jointly during group meetings and discussion forums.

This former mismatch in organization resulted in higher complexity when producing the progress report: we had to report on something else than what we actually did.

Therefore, we decided to deeply change the structuring of this new cluster:

- The structuring should reflect better what we actually want to do;

- The topics of the former JPRAs will define the *overall scientific scope* of the new activities.

Accordingly, the new organization for the RTC cluster will be:

- **Platform: Components Platform for Component Modelling and Verification** (this was the platform-related activity of the former Components cluster, it continues as such). Responsible is Susanne Graf, from Verimag.

- **Cluster integration: Development of UML for Real-Time Embedded Systems** (this was the standard-related activity of the former Components cluster, it continues as such). Responsible is Sébastien Gérard, from CEA.

- **NoE integration: Forums with specific industrial sectors**. This is a totally new activity. Its scope will encompass all research topics of the former clusters HRT and Components (diagnosis, semantic platform, heterogeneity, interfaces and composition, ET&TT, and, more generally, what is relevant to the concept of Real-Time Component). This activity will consist in in-depth meetings and forums with engineers from industry. This will be jointly managed by Alberto Sangiovanni-Vincentelli from PARADES and Albert Benveniste from INRIA.

- **NoE integration: Seeding new research directions**. This is a totally new activity. Its scope will encompass all research topics of the former clusters HRT and Components (diagnosis, semantic platform, heterogeneity, interfaces and composition, ET&TT, and, more generally, what is relevant to the concept of Real-Time Component). This activity will consist in in-depth meetings among researchers. This will be jointly managed by Bengt Jonsson from Uppsala and Albert Benveniste from INRIA.

To perform better, the cluster requires a light weight board where meetings and forums will be discussed and planned, and responsibilities for each future event will be appointed. In addition, organizational and budgeting aspects need to be better managed. The corresponding board will consist of the following people:

- The above activity leaders

- Alain Girault from INRIA will manage organization and budget

- Paul Caspi from Verimag and Tom Henzinger from EPFL will join for planning meetings.

Accordingly, the organization of the RTC cluster workplan is as follows:

- Platform: Components Platform for Component Modelling and Verification: summary of work and planned activities.

- Cluster Integration: Development of UML for Real-Time Embedded Systems: summary of work and planned activities.

- Cluster Integration: Diagnosis in distributed Hard real-Time Systems: summary of work.

- Cluster Integration: Component Modelling and Composition: summary of work.

- NoE Integration: Semantic Framework for Hard Real-Time Design Flow: summary of work.

- NoE integration: Merging the ET and TT paradigms: summary of work.

- NoE integration: Forums with specific industrial sectors: planned activities.

- NoE integration: Seeding new research directions: planned activities.

3.1.1 Platform: Components Platform for Component Modelling and Verification

Activity leader: Susanne Graf (Verimag)

Artist Participants and roles

Team Leader: Susanne Graf (Verimag)
Contributions of her team: Semantic level modelling formalisms, IF validation platform for real-time and embedded systems.

Team Leader: Jean-Marc Jezequel (INRIA)
Contributions of his team: UML-based model transformation technology.

Team Leader: Sebastien Gerard (CEA)
Contributions of his team: Definition of UML modelling notation. CEA model transformation and analysis tools

Team Leader: Pierre Combes (France Telecom R&D)

Contributions of his team: connection of performance analysis tools to UML case tools.

Team Leader: Bengt Jonsson (Uppsala)
Contributions of his team: Connection between modelling and verification tools, Times tool

Team Leader: Noel Plouzou (INRIA)
Contributions of his team: Model transformations and aspect orientation, tools

Team Leader: Bernhard Josko (OFFIS,)
Contributions of his team: OFFIS UML validation toolset

Team leader: Alberto Sangiovanni-Vincentelli (PARADES)
Contributions of his team: Metropolis tool

Affiliated partners and Roles

Team Leader: Julio Medina (U. of Cantabria)
Contributions of his team: connection to Adaptive real-time cluster, notations and tools for scheduling analysis.

Team Leader: Bernhard Steffen (University Dortmund)
Contributions of his team: tool integration platform.

Team Leader: Thierry Coupaye (FTRD)
Contributions of his team: Fractal/Think and integration with validation tools.

Team Leader: David Lesens (EADS)
Contributions of his team: Case study on architecture modelling and schedulability analysis.

Summary of Work Already Achieved: Sept 2004 – August 2005

The main objective of the first year of the project was to obtain an inventory of potentially interesting work on tools, to do some developments within these tools towards a possible integration and finally to define a concrete vision of the Artist platform for component-based design and validation.

Due to the large span of applications covered by the tools to be integrated into to the platform, this integration is not intended to be a strong integration in the classical sense of an integrated toolset, but rather a set of components that can be used in combination with specific components to form different tool chains. The baseline of the tools is that they are UML compatible and share subsets of UML profiles. Some components will be specific to particular tool-chains and whereas others are useful in several ones.

Presently considered sub platforms are identified by the following working titles:

- A platform for the development of safety-critical embedded systems

- A platform for the analysis of performance critical service-based systems

- A platform for the certification of smart-card applications

The relevant subsets of UML used in the context of these three environments are specific for the concerned target application types, at the level of requirements and abstract design which is the main focus of the platform in a first phase. We intend to share some of the analysis tools amongst the platforms thanks to the mapping into a common semantic level

model. Also the profile concerning architecture modelling may be shared, but will be considered later.

All the tools developed are or will be ported to Eclipse.

High-Level Objectives: Sept 2005 – February 2007

The motivations for organising the activity on platforms was the existence of existing independent efforts on tool development by the cluster partners on closely related areas, based on some profile of UML. The need to make these efforts somehow converge has been clearly identified, and the main aim of the platform is to be able to share some of the developed tools in an efficient manner. Some tools are specific to some application domain, but others, such as verification tools, model transformation tools and tool integration tools are more generic tools that can be used in different contexts.

The use of UML as modelling language is common to all the existing approaches, and here we are yielding maximal harmonisation between profiles, taking into account and influencing on the standard activities around the MARTE profile.

Description of Work Planned: Sept 2005 – February 2007

The goal of the next 18-month period is to obtain initial versions of the planned subsets based on the developed UML extensions for real time, as well as the definition of a semantic profile, suitable for analysis tools, as well as some of the needed mappings, integrating some forms of abstraction.

Fig. 1: architecture of the platform
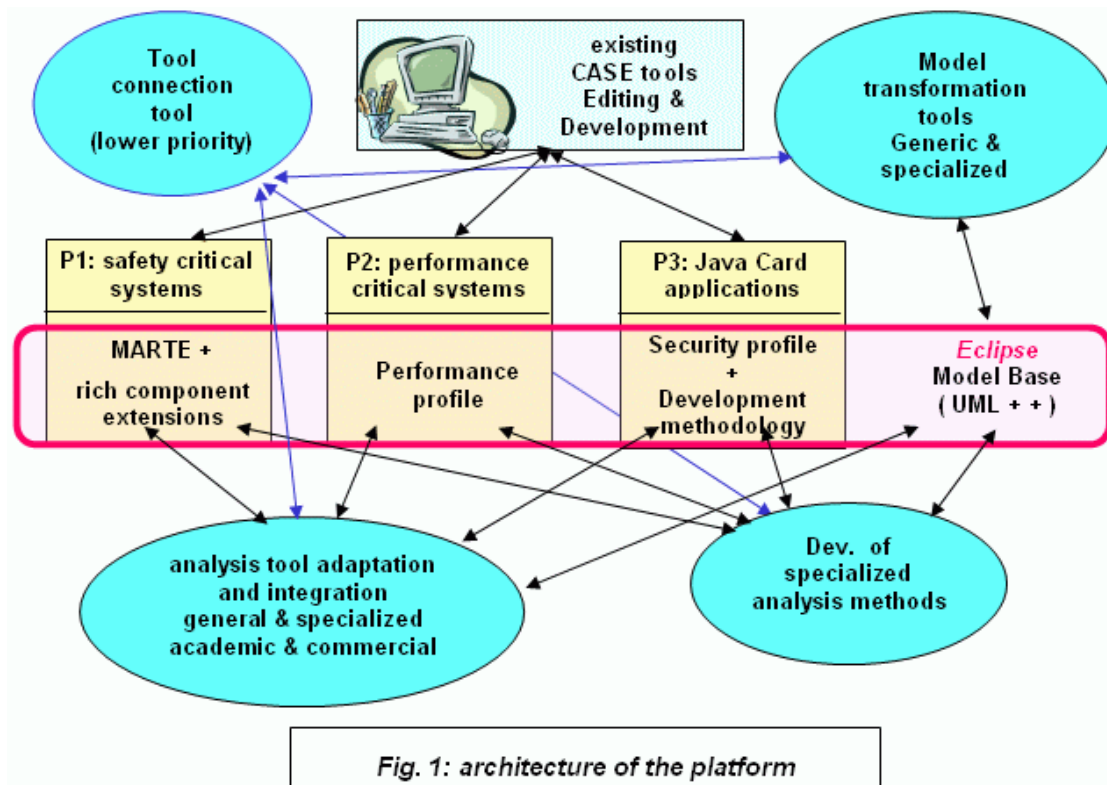
The individual activities that will be carried out in a coordinated fashion concern:

- Implementation *MARTES* profile (Protes Project & Carroll) → JPRA "UML for embedded systems".

- *KerMeta* model transformation language and tool (IRISA); generic tool; connection with IF (OpenEmbedd).

- *jETI* (Dortmund), a redesign of the Electronic Tools Integration platform for building complex functionalities from individual components.

- *IF* tools for validation and simulation: porting to Eclipse, extension of existing connection to Omega UML-RT profile, use of verification technology for scheduling and performance model extractions (ASSERT, Persiform & OpenEmbedd).

- *SaveCCM* (Save & Astec projects) component model and tools for the development of real-time controllers and *Times* Tool for schedulability analysis.

- *MAST* environment (Cantabria): extraction of schedulability analysis models, analysis and code generation tools.

- More analysis tools (STACS, CLIPS project): adaptation to UML2/MARTES.

- *TL-FIT* (EDEN project): development of a UML profile for security properties and formal verification of Smart card applications using *IF* and *Agatha.*

- Integration of commercial modelling tools and academic validation tool in a semantic level formalism for system modelling (SPEEDS).

The tools will be demonstrated on some realistic case-studies at the end of the period.

Meetings Planned

Two kinds of meetings are planned. First, regular brief coordination meetings will be held in the form of phone conferences. They will take place every 2 months and more often if needed.

In addition, we plan to hold a physical meeting 2 to 3 times a year in which the status of progress will be presented by the different partners and discussed. We plan to hold at least two of these meeting together with a global cluster meeting. The third one might be a meeting on its own, probably collocated with some conference of general interest in the community. The next meeting is planned for March 2005, and we envisage co-location with the date conference.

Also, we will again organise the workshop MARTES in late 2006 or early 2007 on Modelling and Analysis of Real Time Embedded Systems as a joint event of the platform and the standardisation activities.

3.1.2   Cluster Integration: Development of UML for Real-time Embedded Systems

Activity leader: François Terrier (CEA)

Artist Participants and roles

Team Leader: Susanne Graf (VERIMAG)
Areas of his team's expertise: modelling of real-time components.

Team Leader: Jean-Marc Jezequel (INRIA)
Areas of his team's expertise: UML Meta-model.

Team Leader: Julio Medina (Cantabria University)
Areas of his team's expertise: model-based schedulability analysis.

Team Leader: Sébastien Gérard (CEA)
Areas of his team's expertise: standard modelling and RT/E domains.

Affiliated Partners and Roles

Team Leader: Ivica Crnkovic (MdH)
Areas of his team's expertise: component models.

Team Leader: Stefan van Baelen (K.U. Leuven)
Areas of his team's expertise: QoS specification.

Team Leader: Bernhard Josko (OFFIS)
Areas of his team's expertise: real-time UML.

Team Leader: Alan Moore (ARTiSAN Software)
Areas of his team's expertise: UML standard evolutions.

Team Leader: Dominique Potier (Thalès Research and Technology)
Areas of his team's expertise: standardization and case study from the aerospace or telecommunication domain.

Team Leader: Matthias Grochtmann (DaimlerChrysler)
Areas of his team's expertise: specification, design and implementation of automotive systems.

Summary of Work Already Achieved: Sept 2004 – August 2005

Within this period, the job consisted in the three following action (main part of this work has been performed within the French CARROLL-Protes project):

- The first objective of this first period was first to influence on the writing of the request for proposal (RFP) of the new UML profile for real-time and embedded systems. This RFP expresses all the requirements the new standard will have to satisfy. The RFP, document referenced at OMG web server as realtime/05-02-06 (UML Profile for Modelling and Analysis of Real-Time and Embedded systems (MARTE) RFP)) has been voted in the context of the Real-time, Embedded, and Specialized Systems (RTESS) Platform Task Force in February 2005: http://www.omg.org/cgi-bin/doc?realtime/05-02-06.

- The second objective was to setup an OMG submitter team in order to answer to the RFP. The team that has been organized is called the ProMARTE team: www.promarte.org. This team consists of the main companies (end users and tool provider) involved in this aspect at the OMG. It is composed of: Artisan, Carlton university, CEA, IBM, I-Logix, INRIA, Looked-Martin, Thales, Tri-Pacific. We continue this effort in order to improve the force of our consortium.

- Finally, a framework for the unification of the two analysis sub-profiles in the original SPT profile was proposed and some effort was made to simplify the way final models will be annotated.

In the context of the Omega project, a UML profile has been developed appropriately for real-time embedded systems based on the existing SPT profile. The extension done in Omega introduces a notion of "observer" and emphasizes the importance of capturing the relevant events which make reference to the system at execution and is used to capture its dynamic properties. A successful profile has been defined in [GOO05] and successfully applied in the Omega project [OME05, OGOL05a, OGY05] and elsewhere [HCBA05]. This work yields maximal expressiveness and semantic level foundation.

Finally, during this first year period, we tried as much as possible to give all the required information about OMG standardisation processes and specially points related to RT/E to all ARTIST partners.

High-Level Objectives: Sept 2005 – February 2007

Three major goals are scheduled within this period:

- For November, the 14th 2005, an initial submission of the standard document is due to the OMG. This first document will contain the architecture model of the standard, basic concepts for modelling and analysis RT/E systems.

- For June 2006, we have to provide the revised version of the document which is the version that has to be voted to be a formal version of the document.

- For the rest of the period, the plan is to take into account all received feedback to provide a finalized version of the specification.

Description of Work Planned: Sept 2005 – February 2007

From September to December 2005, the work will consist in refining the correct architecture of the profile taking into account all contributions supplied by the participants to this work and covering all the requirements expressed in the MARTE request of proposal. This work will lead to the initial submission of the document that will be presented during the OMG meeting of December held in Burlingham (USA).

From January 2006 to September 2006, the work consists in completing the initial submission in order to have a clear and consistent document to propose to vote to become the standard for modelling and analysis of RT/E systems.

From October 2006 to September 2007 (approximate deadline that may be changed depending on OMG decision), the remaining actions will be to consolidated the final version of the standard integrating responses of the issues received by the OMG relating the revised version of the proposal.

Meetings Planned

Two kinds of meeting are scheduled:

- OMG meetings:
  - December 5-9, 2005 (Burlingame, CA, USA)
  - February 13-17, 2006 (Tampa, FL, USA)
  - April 24-28, 2006 (St. Louis, MO, USA)
  - June 26-30, 2006 (Boston, MA, USA)
  - September 25-29, 2006 (Location TBA)
  - December 4-8, 2006 (Location TBA)

- ARTIST meetings:
  - Still have to be scheduled.

3.1.3 NoE Integration: Forums with Specific Industrial Sectors

Activity leader: Albert Benveniste (INRIA)

NB: since this is a new activity, we have included a more complete description, which the reviewers will not have had the chance to see in earlier documents.

Activity Leader

Team Leader: Albert Benveniste (INRIA) and Alberto Sangiovanni-Vincentelli (PARADES)
Areas of their team's expertise:
- INRIA: synchronous languages, heterogeneous embedded systems;
- PARADES: platform based design, embedded systems and hardware.

Clusters

Real-Time Components

Adaptive Real-Time

Control for Embedded Systems

Policy Objective

This is a totally new activity. Its scope will encompass all research topics of the former clusters HRT and Components (diagnosis, semantic platform, heterogeneity, interfaces and composition, ET&TT, and, more generally, what is relevant to the concept of Real-Time Component). This activity will consist in in-depth meetings and forums with engineers from industry.

Industrial Sectors

Addressing heterogeneity in embedded systems design is essential in the industrial sectors where large systems are built, involving multiple skills with different paradigms and tools. This includes the following sectors, with the first two sectors being the leading ones:

- Avionics (Event and Time-triggered systems are developed and effectively used at Airbus Industries);

- Automobile;

- Rail Transport;

- Energy Production.

Artist Participants and roles

Team Leader: Alberto Sangiovanni-Vincentelli (PARADES)
Areas of his team's expertise: strong interaction with automotive, design software and semiconductor industry; expertise in design flows, tools and modelling methodologies with particular attention to Hard Real-Time; Platform-Based Design and Metropolis design framework for integration of design processes from OEMs to suppliers involving functional and non functional aspects.

Team Leader: Albert Benveniste (INRIA)
Areas of his team's expertise: synchronous languages and heterogeneous systems modelling and deployment.

Team Leader: Hermann Kopetz (TU Vienna)
Areas of his team's expertise: inventor of the TTA concept.

Team Leader: Werner Damm (OFFIS)
Areas of his team's expertise: embedded system modelling and validation, deep involvement in cooperation with the automotive industries.

Team Leader: Paul Caspi (Verimag)
Areas of his team's expertise: synchronous languages and heterogeneous systems modelling and deployment; tight cooperation with Airbus.
Team Leader: Petru Eles (Linköping University)
Areas of his team's expertise: schedulability analysis for heterogeneous systems.

Team Leader: Tom Henzinger (EPFL)
Areas of his team's expertise: development of abstract programming models for real-time computing [Giotto: time-triggered; xGiotto: both time- and event-triggered].

Team Leader: Rolf Ernst (University Braunschweig)
Areas of his team's expertise: formal performance models for networks-on-chip.

Affiliated partners and Roles
Team Leader: Jan Romberg (TU Munich)
Areas of his team's expertise: synchronous dataflow notations and tools, distributed architectures in automobile.

Team Leader: Luciano Lavagno (Politecnico di Torino)
Areas of his team's expertise: IC design and algorithms for synchronous and asynchronous design.

Team Leader: Stefan Kowalewski (Bosch)
Areas of his team's expertise: automotive industrial case study.

Team Leader: Jakob Axelsson (Volvo)
Areas of his team's expertise: automotive industrial case study.

Team Leader: Team Leader: Francois Pilarski (Airbus France)
Areas of his team's expertise: avionics industrial case study.

Team Leader: Thomas Thurner / Hermann von Hasseln (DaimlerChrysler)

Areas of his team's expertise: automotive industrial case study.

Team Leader: Stephan Kowalewski (Bosch)
Areas of his team's expertise: automotive industrial case study.

Team Leader: Jakob Axelsson (Volvo)
Areas of his team's expertise: automotive industrial case study.

Team Leader: Jan Romberg (TU München)
Areas of this team's expertise: Synchronous languages, model-based development, automotive applications.

Team Leader: Christofer Kirsch (University of Salzburg)
Areas of this team's expertise: development of abstract programming models for real-time computing [Giotto: time-triggered; xGiotto: both time- and event-triggered].

Description of Work Planned: Sept 2005 – February 2007

This activity aims at reproducing more systematically the type of meeting and discussion forum the former HRT cluster held in Rome, in January 2005, where engineers from GM and BMW participated to the discussion on *merging ET with TT.* The minutes collected from this meeting were quite rich and useful for us in guiding our research activities. We think that this type of prospective activity must be sustained by the academic community, and we believe that ARTIST2 is the adequate place to handle it.

The scope of this activity will comprise all research topics of the former clusters HRT and Components (diagnosis, semantic platform, heterogeneity, interfaces and composition, ET&TT, and, more generally, what is relevant to the concept of Real-Time component).

We therefore plan to hold a set of meetings with top quality engineers from various industries, on selected topics within the scope of this activity. The aim of such 2-3 days meetings is to invite key industrial persons on some given topic, for extensively discussing the following matters:

- What the problems are for them, what the degrees of freedom are. To this end, we shall have somebody from industry deeply explaining the issues; this presentation shall be prepared jointly between some ARTIST person and the industrialist(s).

- Each one of ARTIST2 participants would try to relate what she or he's doing, to the above presentation, on-line during the meeting.

- Minutes will be carefully recorded and subsequently lifted to the status of an ARTIST2 document and deliverable. These will contain in addition suggestions for further research directions. The aim is not to solve the immediate needs of the industrial, but rather to lift these to longer term and more fundamental research activities aiming at possibly deeply changing the industrial practice.

We plan 2 such meetings for the next 18 month period.

Meetings Planned

Since automobile is an industry where embedded electronics is currently experiencing deep revolution and Real-Time Components and Architectures are one of the major issues, we

plan to have a meeting on this sector for the considered period. The topics we expect being relevant will cover Semantic Platform, Merging ET&TT, and Diagnosis, and probably other topics as well. Which topic will be central in this meeting remains to be decided. We plan to invite the clusters on Execution Platform and Control to participate to this meeting and possibly co-organize it.

3.1.3.1.1 Meeting: Embedded electronics in automobile beyond AUTOSAR

Meeting Title	Embedded electronics in automobile beyond AUTOSAR
Approximate Date	The meeting is to be held during winter 2006. Werner Damm from OFFIS has offered to host it, and co-organize it with the RTC board.
Objectives and expected output	The aim of this 2-3 days meeting is to invite key industrial AUTOSAR actors, for extensively discussing the following matters: • What the problems are for them, what the degrees of freedom are. To this end, we shall have somebody from industry deeply explaining the issues; this presentation shall be prepared jointly between some ARTIST person and the industrialist(s). • Each one of ARTIST2 participants would try to relate what she or he's doing, to the above presentation, on-line during the meeting. • Minutes will be carefully recorded and subsequently lifted to the status of an ARTIST2 document and deliverable. These will contain in addition suggestions for further research directions.

The next sector we would like to address is Integrated Modular Avionics. This sector is undoubtedly the most complex one, where Real-Time Components and Architectures are a central concern. We plan to invite the clusters on Execution Platform and Verification and Testing to participate to this meeting and possibly co-organize it.

3.1.3.1.2 Meeting: Fundamental Challenges raised by Integrated Modular Avionics

Meeting Title	Fundamental Challenges raised by Integrated Modular Avionics
Approximate Date	This is one of our other candidate meetings planned. We will have it either in fall 2006 or winter 2007. Which partner will organize and host it is still open.
Objectives and expected output	The aim of this 2-3 days meeting is to invite key industrial actors from aeronautics, for extensively discussing the following matters: • What the problems are for them, what the degrees of freedom are. To this end, we shall have somebody from industry deeply explaining the issues; this presentation shall be prepared jointly between some ARTIST person and the industrialist(s). • Each one of ARTIST2 participants would try to relate what she or he's doing, to the above presentation, on-line during the meeting. • Minutes will be carefully recorded and subsequently lifted to the status of an ARTIST2 document and deliverable. These will contain in addition suggestions for further research directions.

There is a totally different category of industrial sector where Real-Time Components and Architectures are important, namely telecommunications and consumer electronics. More generally, we seek for industrial sectors where the overall performance and service delivery can be achieved by acting on architecture, OS and scheduling, and application, jointly. This is a situation totally different from that in the above discussed industrial sectors. And this raises clearly other fundamental issues. We will probably not have the resources to organize this meeting *in addition to* the previous one. It may however be an interesting backup if we fail identifying high quality invitees for our previous meeting. In case we plan to organize such a meeting, this would be jointly performed with the Adaptive Real-Time and Control clusters.

3.1.3.1.3 Meeting: Fundamental Challenges related to Real-Time Components raised by Consumer Electronics and Telecommunications

Meeting Title	Fundamental Challenges related to Real-Time Components raised by Consumer Electronics and Telecommunications
Approximate Date	This is one of our other candidate meetings planned. We see it as a backup for our previous mentioned meeting. We may have it either in fall 2006 or winter 2007. Which partner will organize and host it is still open.
Objectives and expected output	The aim of this 2-3 days meeting is to invite key industrial actors from this sector, for extensively discussing the following matters: • What the problems are for them, what the degrees of freedom are. To this end, we shall have somebody from industry deeply explaining the issues; this presentation shall be prepared jointly between some ARTIST person and the industrialist(s). • Each one of ARTIST2 participants would try to relate what she or he's doing, to the above presentation, on-line during the meeting. • Minutes will be carefully recorded and subsequently lifted to the status of an ARTIST2 document and deliverable. These will contain in addition suggestions for further research directions.

3.1.4 NoE Integration: Seeding New Research Directions

Activity leaders: Bengt Jonsson (Uppsala) and Albert Benveniste (INRIA)

NB: since this is a new activity, we have included a more complete description, which the reviewers will not have had the chance to see in earlier documents.

Activity Leader

Team Leader: Bengt Jonsson (Uppsala) and Albert Benveniste (INRIA)
Areas of their team's expertise:
• Uppsala: verification theory and tools, timed systems
• INRIA: synchronous languages, heterogeneous embedded systems;

Clusters

Real-Time Components

Execution Platforms

Adaptive Real-Time

Control for Embedded Systems

Policy Objective

This is a totally new activity. Its scope will encompass all research topics of the former clusters HRT and Components (diagnosis, semantic platform, heterogeneity, interfaces and composition, ET&TT, and, more generally, what is relevant to the concept of Real-Time Component). This activity will consist in in-depth meetings among researchers.

Industrial Sectors

Addressing heterogeneity in embedded systems design is essential in the industrial sectors where large systems are built, involving multiple skills with different paradigms and tools. This includes the following sectors, with the first two sectors being the leading ones:

- Avionics (Event and Time-triggered systems are developed and effectively used at Airbus Industries);

- Automobile;

- Rail Transport;

- Energy Production.

Artist Participants and Roles

Team Leaders: Bengt Jonsson (Uppsala) and Albert Benveniste (INRIA)
Areas of their team's expertise:
- Uppsala: verification theory and tools, timed systems
- INRIA: synchronous languages, heterogeneous embedded systems;

Team Leader: Alberto Sangiovanni-Vincentelli (PARADES)
Areas of his team's expertise: strong interaction with automotive, design software and semiconductor industry; expertise in design flows, tools and modelling methodologies with particular attention to Hard Real-Time; Platform-Based Design and Metropolis design framework for integration of design processes from OEMs to suppliers involving functional and non functional aspects.

Team Leader: Albert Benveniste (INRIA)
Areas of his team's expertise: synchronous languages and heterogeneous systems modelling and deployment.

Team Leader: Hermann Kopetz (TU Vienna)
Areas of his team's expertise: inventor of the TTA concept.

Team Leader: Werner Damm (OFFIS)
Areas of his team's expertise: embedded system modelling and validation, deep involvement in cooperation with the automotive industries.

Team Leader: Paul Caspi (Verimag)
Areas of his team's expertise: synchronous languages and heterogeneous systems modelling and deployment; tight cooperation with Airbus.
Team Leader: Petru Eles (Linköping University)
Areas of his team's expertise: schedulability analysis for heterogeneous systems.

Team Leader: Tom Henzinger (EPFL)
Areas of his team's expertise: development of abstract programming models for real-time computing [Giotto: time-triggered; xGiotto: both time- and event-triggered].

Team Leader: Rolf Ernst (University Braunschweig)
Areas of his team's expertise: formal performance models for networks-on-chip.

Affiliated partners and Roles
Team Leader: Jan Romberg (TU Munich)
Areas of his team's expertise: synchronous dataflow notations and tools, distributed architectures in automobile.

Team Leader: Luciano Lavagno (Politecnico di Torino)
Areas of his team's expertise: IC design and algorithms for synchronous and asynchronous design.

Team Leader: Stefan Kowalewski (Bosch)
Areas of his team's expertise: automotive industrial case study.

Team Leader: Jakob Axelsson (Volvo)
Areas of his team's expertise: automotive industrial case study.

Team Leader: Team Leader: Francois Pilarski (Airbus France)
Areas of his team's expertise: avionics industrial case study.

Team Leader: Thomas Thurner / Hermann von Hasseln (DaimlerChrysler)
Areas of his team's expertise: automotive industrial case study.

Team Leader: Stephan Kowalewski (Bosch)
Areas of his team's expertise: automotive industrial case study.

Team Leader: Jakob Axelsson (Volvo)
Areas of his team's expertise: automotive industrial case study.

Team Leader: Jan Romberg (TU München)
Areas of this team's expertise: Synchronous languages, model-based development, automotive applications.

Team Leader: Christofer Kirsch (University of Salzburg)
Areas of this team's expertise: development of abstract programming models for real-time computing [Giotto: time-triggered; xGiotto: both time- and event-triggered].

Description of Work Planned: Sept 2005 – February 2007

This activity aims at reproducing more systematically the type of meeting and discussion forum the former HRT cluster held in Vienna and Grenoble, for the topic of Diagnosis. The minutes collected from this meeting were quite rich and useful for us in guiding our research activities in this particular topic (whether or not this will actually happen depends on available resources and is not related to the actual interest of these research suggestions). The work done in the JPRA on Diagnosis involved skills originating from communities not meeting at existing conferences (dependability, control and signal processing, statistics, verification). We think that this type of "trans-skills" prospective activity must be sustained by the academic community, and we believe that ARTIST2 is the adequate place to handle it.

The scope of this activity will comprise all research topics of the former clusters HRT and Components (diagnosis, semantic platform, heterogeneity, interfaces, ET&TT, and, more generally, what is relevant to the concept of Real-Time component).

We therefore plan to hold a set of meetings between us (and possibly inviting affiliates, academic and/or industrial), on selected topics within the scope of this activity. The aim of such 2-3 days meetings is to gather, for extensively discussing the following matters:

- A vision of the issues the area of embedded systems is faced with, in relation with the selected topic.

- Participants having different backgrounds would present their perspective on the subject of the meeting and what tools and techniques their community may have developed, if any.

- Possible connections and blending would be explored, by combining presentations and working sessions.

- Minutes will be carefully recorded and subsequently lifted to the status of an ARTIST2 document and deliverable. These will contain in addition suggestions for further research directions. The aim is to identify long term fundamental research activities aiming at possibly deeply changing the industrial practice.

We plan 1 or 2 such meetings for the next 18 month period.

The aim of the first meeting proposed is the study of research toward a conceptual model and a description of the associated concepts and terms, an *ontology*, covering the field of distributed real-time embedded computer system. At present, there seems to be no general agreement concerning the precise meaning of many commonly used terms. For example, the important concept of a *component* is viewed differently by different authors, depending whether they come from the software or the hardware arena. The same is true for other fundamental concepts, such as *time*, *state,* and *determinism*. We feel that ARTIST2 can make a substantial contribution to establish a commonly accepted *ontology* for distributed embedded systems.

We propose to build on the results of the DSoS (Dependable Systems of Systems) Conceptual Model (IST Project-1999-11585). It was a key objective of the DSoS Conceptual Model to analyze and unify the concepts in the field Dependable Systems-of-Systems and to establish a common ontology that brings together the differing viewpoint s and terms of a number of the involved communities. The final version of the DSoS conceptual model makes a significant contribution towards this objective. However, a number of important terms, such as interface, software module, middleware, need further deliberations and more detailed descriptions.

Having participated in a number of community wide initiatives that had the objective to establish and clarify fundamental concepts (e.g. in the field of fault-tolerance), we know about the difficulties and the effort required to achieve a community wide agreement on fundamental concepts and terms. However, we feel such an effort is needed to further advance the field of distributed embedded systems.

Meeting: Conceptual Model for Distributed Embedded systems, and a taxonomy of MoCCs (Models of computation and Communication)

Meeting Title	Conceptual Model for Distributed Embedded systems, and a taxonomy of MoCCs (Models of computation and Communication)
Approximate Date	The meeting is to be held during spring or fall 2006. Hermann Kopetz from TU Vienna has offered to host it, and will co-organize it with Paul Caspi and the rest of the RTC board.
Objectives and expected output	The aim of this 2-3 days meeting is to gather, for extensively discussing the following matters: • A vision of the issues the area of embedded systems is faced with, in relation with the selected topic. • Participants having different backgrounds would present their perspective on the subject of the meeting and what tools and techniques their community may have developed, if any. • Possible connections and blending would be explored, by combining presentations and working sessions. • Minutes will be carefully recorded and subsequently lifted to the status of an ARTIST2 document and deliverable. These will contain in addition suggestions for further research directions. The aim is to identify long term fundamental research activities aiming at possibly deeply changing the industrial practice.

Other possible topics are still left open at the moment.

Planned Staff Mobility

A two week visit of PS Thiagarajan (National University of Singapore, School of Computing) to INRIA-Rennes is planned for year 2006.

3.1.4.1.1   Mobility:

Sending Institution	**ARTIST2 Affiliate Partner** National University of Singapore
	Contact: PS Thiagarajan
Receiving Institution	**ARTIST2 Partner** INRIA
	Contact: Benoît Caillaud
Persons	PS Thiagarajan, plus possibly student(s)

Area of Collaboration	Control and diagnosis of distributed communicating systems
Technical Work	This is collaboration between the teams of Benoît Caillaud and Albert Benveniste on the INRIA side and the National University of Singapore. The main research theme is the control and diagnosis of distributed communicating systems. Two application areas are targeted: Real-time embedded systems and telecommunications systems and services. Although very different in nature, both areas make fundamental use of models of concurrency. Several types of formal models are considered: scenario languages, communicating automata and Petri-nets. The two teams have a very significant overlap in terms of their theoretical areas of research -- see below. Cooperation has started in 2005, with visits of researchers from both teams. More specifically, we work together on the following problems: • An extension of scenario models for distributed systems diagnosis. • Distributed control synthesis, with applications to the quasi-static scheduling problem.
Approximate Dates and Duration	Spring 2006, 2 weeks
Approximate Costs	Nb people : 1 people Travel : 1200 € Stay: 1350 €
Long-range Impact on Integration	PS Thiagarajan is a major international researcher in all domains of interest to RTC cluster. We hope to take advantage of this visit in Rennes in order to have a larger RTC meeting. This is to be scheduled.

3.2 Cluster: Adaptive Real Time

The following is a description of the activities and overall objectives for the period: September 2005 – February 2007. The next reporting period will cover September 2005 – August 2006.

3.2.1 Platform: A Common Infrastructure for Adaptive Real-time Systems

Activity leader: Giorgio Buttazzo (Pisa)

Summary of Work Already Achieved: Sept 2004 – August 2005

After analyzing the state of the art of real-time kernel technology, the Shark operating system (http://shark.sssup.it/) was selected to be used as a shared platform in the ART cluster for experimenting novel real-time algorithms for control applications. Shark was selected because its modular structure enables the user to easily replace the scheduler or the mutual exclusion protocol with a different one, without changing the application code. Moreover, it supports applications with explicit timing constraints, it includes several advanced algorithms for task scheduling and shared resource management, which can be dynamically selected by the user through a configuration file, it includes drivers for the most common I/O peripherals, it complies with the POSIX standard (PSE51 profile) and includes user manuals and several sample real-time applications. Finally, Shark was developed at the ReTiS Lab of the Scuola Superiore Sant'Anna of Pisa, in collaboration with the Robotic Laboratory of the University of Pavia, hence the know-how for maintaining and updating the kernel is internal to the ART cluster.

The University of Pavia, in collaboration with the affiliates Evidence and the Scuola Superiore Sant'Anna, developed a web site (http://feanor.sssup.it/retis-projects) to create a forum for the various Shark users, in which it is possible to exchange messages, search for questions, etc. The web site also includes a page with web links to the various research groups that are using the kernel for control applications, and a page of *Frequently Asked Questions*, to quickly address the most common problems encountered by the developers.

The main activity was to organize a workshop to introduce the Shark kernel to all the partners of the ART cluster, enabling the participants to quickly use the kernel, develop simple real-time applications, and implement novel scheduling algorithms. The workshop was held in Pontedera, Pisa (Italy), at the Scuola Superiore Sant'Anna, from February 28 to March 4, 2005. During the workshop, participants were asked to develop a small software project using Shark. They were divided into groups and each group had to develop a software module or at least design the structure of the application. The time available for programming was not much, therefore some group developed some simple demo, while some other participant just sketched the idea of a more complete kernel component.

High-Level Objectives: Sept 2005 – February 2007

The high-level objective for this period is to develop a research platform for real-time systems to share competencies, resources, and tools targeting at the development of control applications with performance and timing requirements.

The use of a shared platform is essential for experimenting new real-time software technology, including novel scheduling algorithms, resource management techniques, energy-aware policies and overload handling approaches to increase robustness and predictability.

A shared platform will also facilitate the transfer of research results to industry, as it allows teaching practical knowledge of concepts and techniques. In addition, several solutions could be developed and tested in parallel in different partner sites, allowing the evaluation of the most appropriate approach for the specific application.

Description of Work Planned: Sept 2005 – February 2007

In the period from September 2005 to February 2006, each partner of the ART cluster will continue to practice with the Shark kernel, and the Scuola Superiore S. Anna of Pisa, in collaboration with Evidence s.r.l. and the University of Pavia, will provide support for maintaining the kernel and developing low-level drivers for specific peripheral devices that may be used by partners.

In the period from March 2006 to August 2006, the partners of the ART cluster will develop some real-time applications to experiment and test the behaviour of specific scheduling policies and resource management protocols on real systems. The Scuola Superiore S. Anna of Pisa, in collaboration with Evidence s.r.l. and the University of Pavia, will provide support during such a phase, helping the partners in structuring the applications, and solving possible problems that may appear at the kernel level.

In the period from September 2006 to February 2007, the Scuola Superiore S. Anna of Pisa, in collaboration with Evidence s.r.l. and the University of Pavia, will gradually develop a repository to collect the software developed by the partners (e.g., scheduling algorithms, feasibility analysis, communication protocols, concurrency control policies, applications, etc.) and make it available to the cluster. All the software contributions will be tested, documented and published using a common format.

During the entire period, all the partners will be involved in the development of specific real-time applications and internal kernel mechanisms, with the objective of testing the performance of new algorithms and making embedded systems more adaptive to parameters variations. In particular, University of Aviero, Polytechnic Institute of Porto and University of Catania (aff. of Pavia) will develop distributed applications and will contribute to extend the network layer with new protocols; University of Cantabria and University of York will experiment the possibility of developing a scheduler at the application level; Polytechnic University of Madrid will develop middleware algorithms for quality-of-service management; and Malardalen University, with University of Catalonia (aff. to Malardalen), will focus on real-time control applications.

Concerning the activity related to Spreading Excellence, a repository will be developed to collect all the software developed by the ART partners (e.g., scheduling algorithms, feasibility analysis, communication protocols, concurrency control policies, applications, etc.) and make it available to the all clusters, and possibly to the world. All software contributions will be tested, documented and published using a common format.

Moreover, the ART cluster will organize a graduate course aimed at teaching how to apply real-time technology to the development of embedded control systems. The course will introduce the most important methodologies used to develop a real-time embedded system, including fundamentals of real-time scheduling, control, and distributed systems. At the same time, the course will also show how to apply these methods to develop simple real-time distributed control applications using the Shark real-time operating system, specifically developed for education. The course will be organized in collaboration with the Control cluster.

Meetings Planned

3.2.1.1.1 Meeting: Coordinating on the use of the shared platform

Meeting Title	Coordinating on the use of the shared platform
Approximate Date	February 2006
Objectives and expected output	The objective of the meeting is to coordinate the work to be done in the cluster on the shared platform, taking into account the specific expertise of each partner. Possible contributions may include real-time control applications, real-time experiments on multimedia systems, network protocols, or novel scheduling algorithms.
	As a result of the meeting each partner will provide a description of the work expected to be done on the shared platform.

3.2.1.1.2 Meeting: Building a repository of real-time software

Meeting Title	Building a repository of real-time software
Approximate Date	July 2006
Objectives and expected output	The objective of the meeting is to discuss on the structure of the repository for real-time software that will be developed for sharing the results achieved in the ART cluster.
	The result of the meeting will be a description of the repository, explaining its structure, the type of information it should contain, access issues, etc.

Planned Staff Mobility

3.2.1.1.3 Mobility: Pavia-Aveiro

Sending Institution	**ARTIST2 Partner:** Pavia
	Contact: Giorgio Buttazzo
Receiving Institution	**ARTIST2 Partner**: Aveiro
	Contact: Luis Almeida
Persons	Tullio Facchinetti
Area of Collaboration	Distributed Real-Time Systems
Technical Work	The main objective of the collaboration is to investigate an operative system level methodology for supporting the hard real-time communication over a dedicated Ethernet network. A typical scenario is made by several distributed peers who need to reliably exchange both periodic and sporadic messages while meeting their communication timing constraints.
	The investigated approach does not modify the standard Ethernet infrastructure. The communication system is built upon cheap and common off-the-shelf Ethernet hardware, which definitely limits the overall system cost. While addressing the cost issues, the timing requirements needed by the real-time communication are fulfilled through a careful implementation

	of the proposed infrastructure, which properly takes into account the source of communication jitter and latency, such as message buffering, direct memory access techniques utilization and timer programming.
	The described approach will be implemented as a module of the S.Ha.R.K. real-time kernel, allowing the performance evaluation of real working applications.
Approximate Dates and Duration	November 2, 2005 - November 18, 2005 - 16 days
Approximate Costs	Nb people : 1 person Travel : 246 € Stay: 150 €
Long-range Impact on Integration	The Ethernet standard, which is the most common solution for office communication, is spreading into the industrial scenario due to the decreasing hardware costs and the large support. However, the Ethernet standard does not natively support message timeliness. The research brings a useful contribution in the field of distributed communication in industrial environments.

3.2.1.1.4   *Mobility: MDH-Catania*

Sending Institution	**ARTIST2 Partner** MDH Contact: Gerhard Fohler
Receiving Institution	**ARTIST2 Partner** Catania (Affiliate of Pavia) Contact: Lucia Lo Bello
Persons	Thomas Nolte
Area of Collaboration	Flexible scheduling in distributed real-time systems
Technical Work	The research will address flexible scheduling of distributed systems relying on networks that are fairly static in terms of physical size. These networks can be found, for example, in automotive systems and industrial robotics. The research work will focus on automotive systems, where multiple distributed systems relying on several different networking technologies currently exist. In this context, new applications push for these distributed systems to interact for coordination activities (e.g., Vehicle Dynamics Control (VDC) systems designed to assist the driver in over-steering, under-steering and roll-over situations.). Although they share the network, these applications should be developed fairly independently, and, in addition, impose major requirements on support for timeliness, composability and reliability. The timelines requirement comes from the fact that the applications are safety-critical, so guaranteed message delivery times are needed. The composability requirement derives from the fact that applications are developed in parallel, so it should be possible to develop any of them without too much knowledge of the rest of the system sharing the network. Finally, the reliability requirement is due to the need for fault-tolerant, dependable communication support for safety-critical applications.

Approximate Dates and Duration	March 2006 – August 2006: 6 months
Approximate Costs	Nb people : 1 person Travel : 500 € Stay: 8000 €
Long-range Impact on Integration	The research activity aims at achieving dependable communication and composability in real-time distributed systems with safety-critical requirements.

3.2.2 Cluster Integration: Flexible Scheduling Technologies

Summary of Work Already Achieved: Sept 2004 – August 2005

The work on flexible scheduling has focused on building a flexible scheduling framework that can be used to safely mix real-time and non real-time processes, and manage the available resources using the necessary flexibility to support the desired quality of level and maximizing the resource usage. Management of different resources has been studied in the previous work. New methodologies for integrating overload management techniques with energy-aware strategies have been developed. Resource reservation mechanisms that reduce intertask interference and provide temporal protection among the concurrent activities have been proposed. Techniques for integrating offline and online scheduling have been developed, and in particular on the coexistence of fixed priority and table-driven scheduling. The flexible scheduling techniques have been adapted to distributed systems by providing the ability to make dynamic bandwidth reservations using a distributed acceptance test that ensures the overall network schedulability.

Work has also been performed to ensure that the techniques developed can be used in different application domains. Work has been done towards using flexible scheduling techniques in adaptive resource management for media processing. Image processing applications associated to robotic vision and control, has been studied, a situation that is known for its varying load; in particular work for this environment has focused on the online adaptation of the processes attributes to enhance the quality-of-service of the application. A dynamic adaptation scheme has been developed for the control part of distributed embedded systems, which reduces the bandwidth requirements while maintaining the control performance. Implementation techniques for the developed novel scheduling techniques have been designed to port them to kernels that have to run on small microprocessors with scarce resources.

High-Level Objectives: Sept 2005 – February 2007

The main objective for this activity is the development of a real-time scheduling framework for applications demanding various types of tasks, constraints, and scheduling paradigms within the same system.

After the experience gathered during the first period, work in the next period will consist of the integration of the management of the different scheduled resources into a common scheduling framework. In particular, the resources should be: the processors, the networks, dynamically reconfigurable modules, interrupts with time protection, shared resources with time protection, memory protection, and energy/power-aware scheduling.

Work should also continue to ensure that the techniques developed can be used in different application domains. The targeted application domains are industrial control systems, media processing applications, automotive embedded systems, and telecommunications.

Description of Work Planned: Sept 2005 – February 2007

During the period of September 2005 to February 2006 work will continue on the flexible scheduling of different resources, exploring new methodologies for integrating flexible scheduling with the management and temporal protection of resources such as energy, networks in distributed systems, interrupts, shared resources and memory.

In March 2006 a cluster meeting will be held, with the objective of deciding on the integration of the management of all these system resources into a flexible scheduling framework. The results of the framework developed by some of the partners in the past FIRST IST project will be used as a basis, and will be extended to accommodate the new resources. From March 2006 to September 2007 work will be carried out by all the partners to implement the resulting integrated flexible scheduling framework.

During the period of October 2006 to February 2007 the developed flexible scheduling framework will be evaluated. For this purpose, it will be used in real and/or simulated applications for the application environments that we have identified as interested in using this technology: industrial control systems, media processing applications, automotive embedded systems, and telecommunications. In February 2007 a meeting will be held to discuss the results of the evaluation and draw some conclusions. These conclusions will set the work agenda on the subject for the following period.

Meetings Planned

3.2.2.1.1   Meeting: Integration of flexible scheduling techniques

Meeting Title	Integration of multiple resource management into a common flexible scheduling framework
Approximate Date	March 2006
Objectives and expected output	The main objective of this meeting is the design of a framework for the integration of the management of all the system resources involved in an embedded application requiring flexible scheduling: processors, energy, networks in distributed systems, interrupts, shared resources and memory.
	The meeting will be for the partners within the cluster but it will be open also to participation of external parties, and specially from industry, so that we can check whether the framework meets the requirements of different application domains
	The output of the meeting will be a set of requirements that would lead to the design of the integrated framework for flexible scheduling of multiple resources.

3.2.2.1.2 Meeting: Evaluation of the integration of flexible scheduling techniques

Meeting Title	Evaluation of the a common flexible scheduling framework
Approximate Date	Feb 2007
Objectives and expected output	The main objective of this meeting is the evaluation of the framework for the integration of the management of all the system resources involved in an embedded application requiring flexible scheduling. In particular, the applicability of the framework to different application environments should be checked. These environments should include industrial control systems, media processing applications, automotive embedded systems, and telecommunications.

The output of the meeting will be a set of conclusions on the evaluation of the framework, which will set the work agenda on the subject for the following period. |

Planned Staff Mobility

There are no planned staff mobility actions.

3.2.3 Cluster Integration: Adaptive Resource Management for Consumer Electronics

Summary of Work Already Achieved: Sept 2004 – August 2005

In the first period, the technical results were achieved in the following areas: video stream demand analysis, identification of scheduling algorithms and kernel mechanisms for stream adaptations based on integrated, flexible scheduling; adaptive resource management for network bandwidth management, multi resource management, in particular with respect to cache aware scheduling; middleware support for QoS management.

Furthermore, the ART cluster has been in active contacts with relevant industry to gather understanding of realistic requirements and to identify research topics and baselines relevant for industrial and academic research. Partners has been giving presentations at the Philips Software Conference – Real-time Workshop and had meetings with Nokia, Ericsson mobile platforms and Visual tools from Spain. The goal has been to go as far as possible towards the actual engineers for better understanding and prepare for a specific industry – academia workshop with selected participants.

High-Level Objectives: Sept 2005 – February 2007

Middleware for supporting distributed and integrated resource management, investigation of embedded device capabilities for consumer electronics and identification of specific issues related to real-time management. Special focus will be given to adaptation methods.

The application of feedback scheduling techniques requires modelling the QoS resource management problem as a feedback control problem. Several components have to be identified, such as the inputs, outputs, actuators, sensors, structure and controller type, and the modelling mechanisms.

Multi-resource management, in particular with respect to the integration of real-time scheduling and cache behaviour. Integrated management of a number of resources such as cache, memory, buses to provide predictable timing.

Description of Work Planned: Sept 2005 – February 2007

We will study a number of consumer electronic specific devices and platforms and will investigate the actual resource capabilities. From these, and input from industrial engineer, we will define actual, realistic resource management problems, including issues related to limited resource availability, overheads etc. This will feed into the other activities, such as the feedback control methods and the resource management framework. Specifically, we will work on the adaptation of the distributed QoS negotiation policies of HOLA-QoS for Shark and the integration of this middleware with communication protocols developed by cluster members.

We will investigate the following for the feedback scheduling methods: the inputs (the means by which a controller changes the resource allocation), the outputs (variables that the controller aims to maintain under control), the actuator (mechanism through which the input is entered into the system) and the sensor (mechanism used to actually measure the outputs). The structure and type of controller: controllers have different structures and are of different types. For example, in a feedback/feedforward structure, the feedforward path is used to provide a fast response to setpoint changes whereas the feedback path is used to compensate for errors caused by disturbances acting on the controlled system. An analysis must be carried on to assess the appropriate structure.

Classic real-time scheduling is concerned with CPU scheduling. With a number of scarce resources in addition and contributing to timing, such as cache, memory, buses, how can integrated management be carried out to provide predictable timing. In particular, we will look into the interaction between scheduling and L2 cache management.

Meetings Planned

3.2.3.1.1   Meeting: Research Meeting, CE

Meeting Title	Research Meeting, CE
Approximate Date	Nov 2nd -4th ,Milano
Objectives and expected output	Subgroup meeting for CE issues and planning.

3.2.3.1.2   Meeting Specific Research Meeting Philips - MDH

Meeting Title	Specific Research Meeting Philips - MDH
Approximate Date	Nov 14th-18th. MDH
Objectives and expected output	Invited lecture in Advanced Real Time Systems at Malardalen University. Cache partitioning discussions.

3.2.3.1.3   Meeting Specific Research Meetings Philips - TUKL

Meeting Title	Specific Research Meeting Philips - TUKL
Approximate Date	Jan. 2005, TUKL, Feb 2005, Philips
Objectives and expected output	Multi-resource management issues.

3.2.3.1.4   Meeting CE – RT Workshop

Meeting Title	CE – RT Workshop
Approximate Date	TBD, Philips
Objectives and expected output	Issues in CE and real-time, workshop industrial engineers, researchers.

3.2.3.1.5   Meeting Specific Research Meeting UPC - TUKL

Meeting Title	Specific Research Meeting UPC - TUKL
Approximate Date	Jan. 2005, TUKL
Objectives and expected output	Control issues in resource adaptation

3.2.3.1.6   Meeting Specific Research Meeting UPM – UC3M - SSSA

Meeting Title	Specific Research
Approximate Date	Jan. 2005
Objectives and expected output	porting of HOLA-QoS to Shark

Planned Staff Mobility

3.2.3.1.7   Mobility: UC3M - Aveiro

Sending Institution	**ARTIST2 Partner** UC3M Contact: Marisol Garcia Valls
Receiving Institution	**ARTIST2 Partner** Aveiro Contact: Luis Almeida
Persons	NN
Area of Collaboration	QoS Middleware.
Technical	Study and integration of network communication protocols into RMI.

Work	
Approximate Dates and Duration	Feb 2006 – July 2006: 5 months
Approximate Costs	Nb people : 2 persons Travel : 500 € Stay: 5000 €
Long-range Impact on Integration	The research activity aims at including adaptive QoS management over the network infrastructure.

3.2.4   Cluster Integration: QoS Aware Components

Summary of Work Already Achieved: Sept 2004 – August 2005

The main result of this work was the concrete identification of the integration topics and the start of this work. The identified integration topics were:

- Consistent alignment between the QoS modelling style of MARTE (with basis on Schedulability, Performance and Time) and that of the UML Profile for QoS and Fault Tolerance. The fist one is mainly related to time and performance aspects, while the second is more general, as it tries to provide means for specifying any other QoS characteristic. Partners involved: CEA, INRIA, and UPM.

- With respect to composability, the interest is focused upon the development of a contract model with well founded semantics with respect to time and execution. This contract model will support (some) QoS characteristics. Partners involved: CEA, INRIA, UC3M, UPM

- Finally, the support for the execution of QoS aware components requires components infrastructures with this support. UPM (QoS in the Robocop framework), UC3M and THALES (CCM based extensions) have done previous work on this topic. They have also proposed containers to simplify components development. The goal will be to interchange the approaches to try to get their particular merits and to propose new concepts for their future evolution.

The work on these topics has started during this period.

High-Level Objectives: Sept 2005 – February 2007

The work on this activity will continue the most important interest topics identified during the first year, that are the development of techniques and methods required for the industrial use of QoS aware components, such as:

- Notations for the description of components models including functional and QoS (also know as non-functional" aspects). The integration of this information in the interfaces is of primary importance.

- Composition mechanisms for determining whether it is feasible their interconnection and for deriving the non-functional characteristics of a group of connected components and the resources needed to fulfil them.

- Component frameworks to support the runtime composition of QoS aware components and to interact with the QoS management subsystems.

Description of Work Planned: Sept 2005 – February 2007

1. Description of QoS-aware components. The goal is to continue with the development of techniques for the description of these types of components.

   - There is a work in progress towards the development of tool support for adding the description of QoS characteristics in components, following the OMG standard "UML profile for QoS and FT". This tool will be made available within the participants, to facilitate the experimentation with different QoS characteristics in components.

   - Participation and follow-up of the MARTE OMG standard proposal.

   - Experimentation with specific QoS characteristics, such as safety and timeliness.

2. Platform dependent transformations for including resource usage information to the quality levels that a component can provide. Components infrastructures based on containers and configurations will be developed, in order to ease the development of these types of components.

3. On relation with the composition of components, the goal is to provide methods to assemble relevant quality properties and resource requirements. There are actions to develop contract models where the provided and required qualities between components are considered and ensured.

4. QoS component frameworks. There are some works in the group related with this topic. The goal will be to try to propose an API that integrates the functionality required for this work and to try to promote it.

5. Continue with the participation in standard and follow-up current work on this topic. Participants in this activity are active on OMG and IOS/IEC standardization bodies.

Meetings Planned

3.2.4.1.1   Meeting: QoS-Aware Components: integration review and planning

Meeting Title	QoS-Aware Components: integration review and planning
Approximate Date	April-2006
Objectives and expected output	The main goal is to evaluate the evolution of the integration work and to plan the next steps. The topics and results of the meeting will be centred around the presentation and discussion of the work performed, mainly on relation to: • Standards for description of QoS characteristics. • Tool support to the description of QoS characteristics. Describe some specific characteristics supported. • Composition technique for these characteristics • Review of the contract model • Review of a proposed QoS framework APIs

	Specific plan and topics for the future integration work.

3.2.4.1.2 Meeting: QoS aware components: consolidation

Meeting Title	QoS aware components: consolidation
Approximate Date	December 2006
Objectives and expected output	The goal of this meeting will be to consolidate the work done so far and to plan for making an effort to disseminate the most relevant results of the integration. This meeting should help to consolidate the work performed on the description techniques, some QoS characteristics, contract models, composition algorithms and QoS frameworks. It will be important to evaluate the experimentation results with the tools supporting the notations and, possibly, the transformations. The meeting should conclude with the identification of the topics to be subject of research in the future.

Planned Staff Mobility

There is no staff mobility planned, except for the meetings and short visits.

3.2.5 Real-Time Languages

Summary of Work Already Achieved: Sept 2004 – August 2005

This activity was not active during this period.

High-Level Objectives: Sept 2005 – February 2007

Ada 2005 is now (almost) defined and it is time to assess its expressive power in terms of the easy with which it will support the programming of flexible real-time systems. Much of the expertise surrounding Ada now lies within Europe, it is therefore important to build upon this situation to ensure that the continuation of this lead.

Supporting real-time functionality via language constructs rather than operating system calls eases the programmer's task when writing complex applications. Over the years, the partners have strived to improve real-time programming abstractions by participating in the main international real-time arenas. Initially these have focused on POSIX (and its C interface) and Ada. More recently, interest has been shown in adding real-time abstraction to Java via the Real-Time Specification for Java (RTSJ).

Description of Work Planned: Sept 2005 – February 2007

The work in this activity will focus on planning the next International Workshop on Real-Time Ada Issue (IWRTA) – this is the main international arena for discussing language evaluation. We shall also look to participate in similar events for Real-Time Java and other relevant languages. Planning will take the form of technical meeting where these languages will be subject to detailed assessment and evaluation. The next IWRTA will be held in early 2007, probably in the US and hence will involve international cooperation.

The other work planned for this period is the continuing participation in the Standardisation efforts around Ada. This is likely to be at a low level of activity as the Standard is almost complete. At most one meeting is envisaged (in Europe).

Meetings Planned

3.2.5.1.1   Meeting: Evaluating Ada 2005

Meeting Title	Evaluating Ada 2005 for programming flexible real-time applications – 1
Approximate Date	March 2006.
Objectives and expected output	There are many new features in Ada 2005 (e.g. timers, CPU clocks, budget controllers, EDF scheduling, interfaces, etc), these open up the possibility of considerable expressive power. But patterns of use and programming paradigms need to be developed. This meeting will address this development.

3.2.5.1.2   Meeting: Evaluating Ada 2005

Meeting Title	Evaluating Ada 2005 for programming flexible real-time applications - 2
Approximate Date	Nov 2006.
Objectives and expected output	A further meeting to evaluate the new compilers and run-time systems that will be developed by the Ada community (including at the University of Cantabria). This will further the development of usage patterns and aim to produce industrial strength reusable code that will be made available via the ARTIST web site.

Planned Staff Mobility

3.2.5.1.3   Mobility: Interaction with development of Ada 2005 Run-time

Sending Institution	**ARTIST2 Partner** York Contact: Alan Burns
Receiving Institution	**ARTIST2 Partner** Cantabria Contact: Michael Gonzalez Harbour
Persons	1 person
Area of Collaboration	Evaluations and further development of MARTE for Ada 2005
Technical Work	Bring together the language expertise of York and the implementation expertise of Cantabria
Approximate Dates and Duration	Oct 2006 – 2 weeks
Approximate Costs	cost are very approximate, no costing has been done yet Travel : 300 € Stay: 1000 €

Long-range Impact on Integration	Improve the quality of the tool surrounding Ada that originate in Europe

3.3 Cluster: Compilers and Timing Analysis

The following is a description of the activities and overall objectives for the period: September 2005 – February 2007. The next reporting period will cover September 2005 – August 2006.

3.3.1 Platform: Timing Analysis Platform

Summary of Work Already Achieved: Sept 2004 – August 2005

CRL2 has been chosen as intermediate representation language to be used among partners. An efficient C/C++ library for CRL2 is created, providing API to data structures. Parts of analysis tool chain communicate via CRL2. AbsInt started to develop definition and documentation of external text format for CRL2.

Several industrial case studies have been performed by students at Mälardalen.

Integration of Bound-T with Mälardalen flow analysis.

High-Level Objectives: Sept 2005 – February 2007

No changes.

Description of Work Planned: Sept 2005 – February 2007

AbsInt will produce a specification of a useful subset of CRL2 (e.g., without modification syntax at the first step), which is to be used by Tidorum. AbsInt also will prublish the attribute database for CRL2.

Mälardalen will maintain set of benchmarks for WCET tools on their web-page and will create guidelines for future benchmarks contributions.

TU Vienna together with Mälardalen will perform a study for a common annotation language which could be used for WCET analysis.

Mälardalen will use WCET-Tools (Bound-T) in Real-time systems education as a part of JPASE.

Meetings Planned

3.3.1.1.1   Meeting: ARTIST2 Timing Analysis Cluster Meeting

Meeting Title	ARTIST2 Timing Analysis Cluster Meeting
Approximate Date	March, 7th (DATE'06, Munich)
Objectives and expected output	Discussion of specified CRL2 subset.

Planned Staff Mobility

3.3.1.1.2   Mobility: Compiler + TA Integration

Sending Institution	**ARTIST2 Partner:** Mälardalen Contact: Björn Lisper
Receiving Institution	**ARTIST2 Partner:** Dortmund Contact: Peter Marwedel
Persons	TBD
Area of Collaboration	Compiler-Timing Analysis Integration
Technical Work	TBD
Approximate Dates and Duration	TBD
Approximate Costs	Nb people : TBD Travel : TBD Stay: TBD
Long-range Impact on Integration	

3.3.2   Platform: Compilers Platform

Summary of Work Already Achieved: Sept 2004 – August 2005

Members of the compilers platform activity have evaluated different options for a common compiler platform that can be shared for most intra-cluster activities. After a review of these options, including platforms like gcc, lcc, SUIF, and OCE, it was concluded that the CoSy platform from ACE will be selected as the primary platform, due to its flexibility and robustness. However, due to the partners´ specific preferences and interests, also other secondary platforms (ROSE, ICD-C) will be used.

A dedicated free CoSy research license for ARTIST2 partners has been agreed with ACE. ACE has supported the cluster teams, especially at ST and Aachen, in their use of the CoSy compiler development system by providing advice on its use as well as modification and extensions. Periodic face-to-face meetings, including two global cluster meetings, helped facilitate this.

Furthermore, the compilers cluster has been organized into a set of mini-clusters with 2-3 parties each that focus on specific research and integration aspects.

A number of discussions were held between AbsInt and ACE to consider the design issues involved in CoSy-PAG integration. The project has been put on hold until sufficient commercial interest reasserts itself as, despite the inherent interest of ACE and AbsInt in the work, engineering more than a point solution or proof of concept requires more resource than the companies are able to justify at present.

TU Vienna worked on development of the PAG Interface Generator (PIG) to simplify the integration of PAG into existing infrastructures. PIG was successfully used to integrate PAG into different C/C++ infrastructures. The integration in ROSE covers all C language features. For testing the PAG integration a constant propagation for C was specified and evaluated for different infrastructures.

High-Level Objectives: Sept 2005 – February 2007

Provision of advice and extensions to CoSy in its role as a platform technology for the cluster. Over the next year we expect more researchers will be using CoSy and see ACE providing workshops, lectures, fielding more requests for platform extensions and having more interaction within the cluster by way of whiteboard design discussions and assistance with the preparation of academic papers.

TU Vienna works on specifying different alias analyses to cover the broad range of different forms of aliasing in real-world C/C++ applications. The specifications are done with the Program Analysis Generator (PAG) from AbsInt. Moreover, Vienna is defining an external text format for aliasing information of C/C++ programs. The format permits representing the results of the implemented alias analyses algorithms.

Due to the central role of ACE in the cluster, it has been decided to include ACE as a full ARTIST2 partner after project year 1. Simultaneously, the cluster members will be open to further affiliate members with complementary areas of excellence related to the compiler platform activity.

Description of Work Planned: Sept 2005 – February 2007

The key plan is to continue the mini-cluster level cooperation already described in previous reports/deliverables, as illustrated in the figure below. There are no major changes in the work program. While the PAG integration is currently on hold (see 3.2.1), good progress has been made in other cooperation, and these will be continued towards full software prototypes. Furthermore, joint publications on selected topics are envisioned.

An important aspect is that ACE intends to continue supporting and promoting CoSy as the Compiler Cluster's preferred platform, with Aachen and ST probably being joined by TU Berlin and Bologna as users of the platform. We would hope to see more come on board in due course. An interesting result of CoSy's position as a platform technology for ARTIST2 has been to show how conservative the eco-system community is in adopting or switching technologies – something of an irony for a high tech community.

Cooperation with Aachen with be deepened on SIMD optimisations and will extend to more sophisticated work on conditional execution. Cooperation with ST will continue on inter-procedural optimisation – ACE and ST also cooperate in the context of the MEDEA+ project NEVA which is an IP.

TU Vienna will be working on the specification of different alias analysis algorithms using the Program Analysis Generator (PAG) from AbsInt. The work will focus on C and C++ and will include the implementation of a post-analysis of the alias analysis results to permit querying different aspects of aliasing such as access conflicts, reachability in heap allocated data structures, array accesses, etc. The analysis results will be made available in an external format. This external format can be used as source code annotations and allows other groups and compilers to utilize the analysis results in optimizations. The integration of PAG in ROSE will be extended from C language features to cover C++ features. Our PAG Interface Generator (PIG) will be extended to generate glue code for accessing PAG analysis results from a C++ interface. The work on PIG is enabling technology for integrating PAG in general.
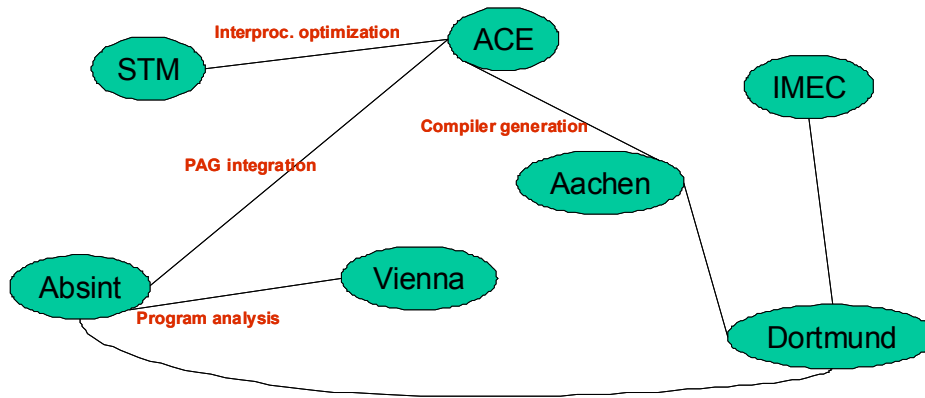
Meetings Planned

A global cluster synchronisation meeting took place at ACE, Amsterdam, on Nov 8, 2005. The next global meeting is planned for Mar 6, 2006, at the DATE conference in Munich. Bilateral and mini-cluster meetings are planned short term on a case-by-case basis and can therefore not be projected in detail here.

Planned Staff Mobility

3.3.2.1.1   Mobility:

Sending Institution	**ARTIST2 Partner** RWTH Aachen Contact: Rainer Leupers
Receiving Institution	**ARTIST2 Partner** ACE Contact: Hans van Someren
Persons	Gerrit Bette
Area of Collaboration	Architecture aware optimization
Technical Work	Aachen and ACE will work to incorporate and extend some research on conditional execution related optimization into CoSy.
Approximate Dates and Duration	January 2006 for 6 months.
Approximate Costs	Nb people 1 Travel : 1,000€ Stay: 6,000 €
Long-range Impact on Integration	Adds a new optimization tool to the compiler platform.

3.3.3 Cluster Integration: Architecture-aware compilation

**Summary of Work Already Achieved: Sept 2004 – August 2005**

Cluster members have been studying compiler requirements for modern embedded processor architectures. As a result, several specific code optimizations have been identified that need to be supported, e.g. SIMD instructions, fast local memories, as well as reconfigurable architectures.

The compilers cluster has then been organized into a set of mini-clusters with 2-3 parties each that focus on code optimization aspects. Alpha versions and software prototypes have become available (see year 1 deliverables).

The common compiler platform CoSy (see 3.2) has been supported whenever possible. Furthermore, tight links to the Execution Platforms cluster, specifically with Bologna, have been established.

High-Level Objectives: Sept 2005 – February 2007

One key objective for the forthcoming ARTIST2 period is the continuation of the successful mini-cluster level cooperation. Furthermore, a tighter integration between the architecture aware compilation and compiler platform activities is envisioned, as sketched in the below figure. Moreover, different activities outside of the compilers cluster will be pursued, e.g. inter-cluster cooperation, dissemination, as well as university-industry cooperation originating from ARTIST2 results.
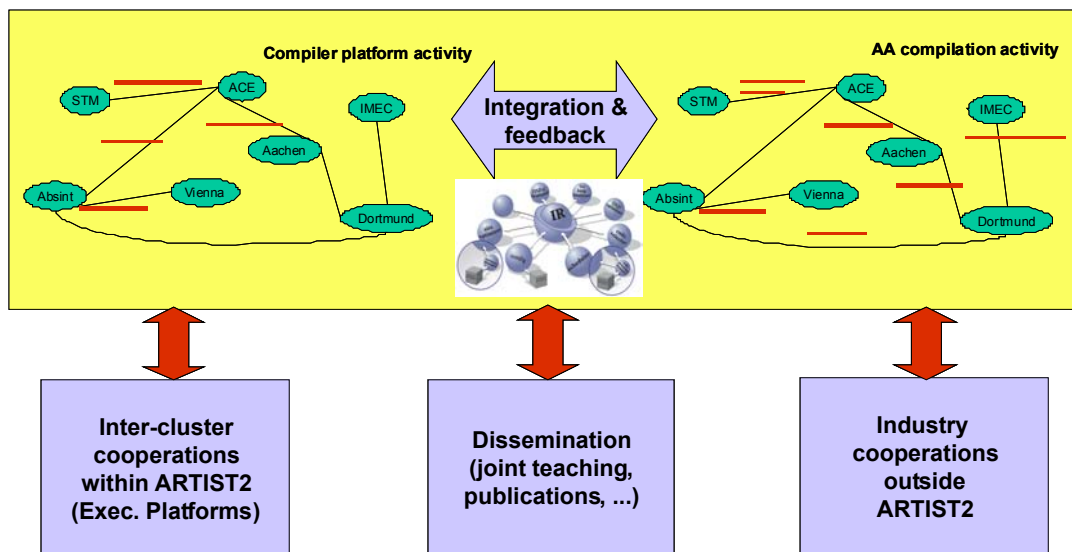
Description of Work Planned: Sept 2005 – February 2007

The key plan is to continue the mini-cluster level cooperation already described in previous reports/deliverables, as illustrated in the figure below. There are no major changes in the work program. Furthermore, joint publications on selected topics are envisioned.
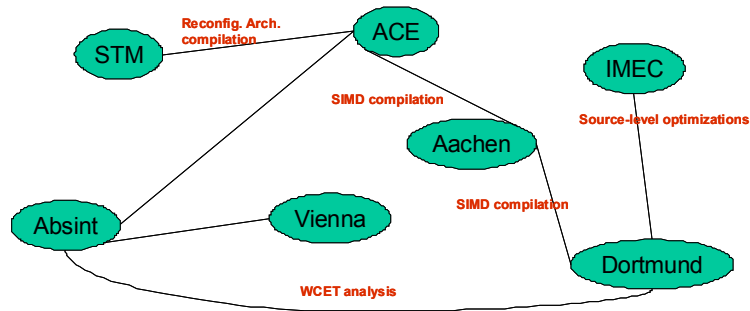
Meetings Planned

A global cluster synchronisation meeting took place at ACE, Amsterdam, on Nov 8, 2005. The next global meeting (concerning both the architecture aware compilation and compiler platform activities) is planned for Mar 6, 2006, at the DATE conference in Munich. Bilateral and mini-cluster meetings are planned short term on a case-by-case basis and can therefore not be projected in detail here.

Planned Staff Mobility

None

3.4 Cluster: Execution Platforms

The following is a description of the activities and overall objectives for the period: September 2005 – February 2007. The next reporting period will cover September 2005 – August 2006.

3.4.1 Platform: System Modelling Infrastructure

Summary of Work Already Achieved: Sept 2004 – August 2005

The work during the first 12 months was focused on two different approaches to system modelling:

- Simulation-based modelling, with the aim to integrate cycle-true models with transaction level and abstract models in order to be able to do cross-layer and –level modelling and analysis.

- Formal modelling, with the aim to integrate different formalisms in order to be able to perform worst-case and response time analysis as well as schedulability analysis.

The main results from the simulation-based modelling are:

- University of Bologna established a consistent SystemC based and cycle accurate simulation environment for on-chip multi-processor systems, with software support and hardware extensions for multi-processing (synchronization, inter-core communication, optimized transfer engines, etc.) targeting the embedded computing domain.

- Technical University of Denmark established a system-level simulation framework based on SystemC which allows to model and simulate cross-layer dependencies between application software, RTOS middleware and platform architecture, including processors, memories and interconnect structures.

- University of Bologna and Technical University of Denmark developed and demonstrated an advanced traffic generator model, featuring extensive reactive capabilities to mimic the behaviour of the core when facing unpredictable environmental events and network performance, and awareness of the multiprocessor nature of the target platforms, which implies synchronization requirements.

The main results from the formal modelling are:

- Technical University of Braunschweig made considerable extensions to the SymTA/S tool to model and analyse power consumption of complex heterogeneous embedded systems. The task model was extended to take multiple remote transactions during the task's execution into account during response time analysis. Finally, sensitivity analysis was introduced into the model. Sensitivity analysis allows the designer to determine the maximum head room achievable for each component in the system with respect to various system performance properties.

- University of Linköping developed modelling and analysis methods for heterogeneous distributed embedded systems within automotive applications. The methods are based on formal techniques, allowing for a holistic schedulability analysis.

High-Level Objectives: Sept 2005 – February 2007

The aim is to provide a scalable and realistic modelling platform which is abstract enough to provide complete system representations and some form of functional models even for billion-transistor future systems, while at the same time providing the needed flexibility for modelling a number of different embodiments (e.g. multi-processors, homogeneous and heterogeneous, reconfigurable, etc.).

In the first 12 months the focus has been on assessing the state-of-the-art within the two different modelling approaches. In the next 18 months the integration within simulation- and formal-based modelling will be further researched and in particular modelling extensions which allow combinations of simulation- and formal-based modelling approaches.

Consistent progress has been reported with respect to the integration indicators. An active and productive cooperation between DTU and UoB for simulation-based modelling has been setup and will be further developed. Cooperation between TU Braunschweig and ETHZ for formal-based modelling and between Linköping University and DTU for modelling automotive applications has been initiated.

Description of Work Planned: Sept 2005 – February 2007

- The work of University of Bologna and Technical University of Denmark will continue focusing on the advanced traffic generator models and on integrating/linking the MPARM and ARTS environment to support mix-level simulations.

- University of Bologna will continue development on the MPARM environment, focusing on extensions to model external memory controllers, advanced memory controllers, and more support for heterogeneous processing.

- The work of University of Linköping and Technical University of Denmark on extending the ARTS environment to support modelling and simulation of heterogeneous distributed embedded systems for automotive applications will be continued. In particular support for various scheduling policies and communication protocols. One of the main goals is the comparison of the protocols with regard to pessimism, average delay, robustness, etc.

- Technical University of Denmark will continue research on the ARTS environment, focusing on extensions for modelling wireless sensor network applications and linking with formal models.

- Technical University of Braunschweig will continue research in formal performance analysis, focusing on extending the model to capture more details of the execution platform. The existing power analysis in SymTA/S will be extended to consider more detailed (real-world) processor models and arbitrary scheduling policies. Based on these models heuristic and stochastic power optimization methods, e.g. by means of dynamic voltage scaling (DVS), will be created.

- Technical University of Braunschweig will develop algorithms for multi-dimensional sensitivity analysis, i.e. considering the simultaneous variation of multiple system parameters. This is an extension of the sensitivity analysis methods developed in the first 12 months, which were capable of capturing the global impact of single system parameter variations, including core execution times, resource frequency/voltage and activation periods.

- Technical University of Braunschweig will further improve their modelling technique for remote memory accesses in complex embedded systems with shared memory. Since the current approach is based on the assumption of blocking memory

accesses, the focus will lay on the consideration of more complex memory access semantics.

Meetings Planned

3.4.1.1.1 Meeting: Workshop on system modelling for communication centric systems

Meeting Title	Workshop on system modelling for communication centric systems
Approximate Date	Summer 2006
Objectives and expected output	Technical University of Denmark will organize a workshop on system modelling infrastructure for communication centric design. The objective is to explore combinations of simulation- and formal-based modelling approaches. Since different models (interval models, statistical models, etc.) are coupled in order to describe heterogeneous embedded systems, it would be interesting to explore how different optimization methods available for these models can be coupled, and thus reused. The expected output is the modelling and analysis of (application-) scenarios including transition between scenarios.

Planned Staff Mobility

3.4.1.1.2 Mobility: Visit at University of Bologna

Sending Institution	**ARTIST2 Partner** Technical University of Denmark, DTU (www.dtu.dk) Contact: Prof. Jan Madsen
Receiving Institution	**ARTIST2 Partner** University of Bologna, UoB (www.unibo.it) Contact: Prof. Luca Benini
Persons	Post Doc Shankar Mahadevan
Area of Collaboration	MPSoC modelling
Technical Work	Integrating/linking the MPARM and ARTS environment to support mix-level simulations. The linking of the two modelling environments will be done through OCP interfaces.
Approximate Dates and Duration	First half 2006, 2 weeks
Approximate Costs	Number of people : 1 from DTU Travel : 300 € Stay: 1000 €
Long-range	The modelling support for mix-level MPSoC system models will allow for

Impact on Integration	the modelling and analysis of more complex hardware platforms.
	The combination of cycle-accurate and TLM modelling styles will provide an environment where existing and yet-to-be-developed components can co-exist.

3.4.1.1.3 Mobility: Visit at University of Linköping

Sending Institution	**ARTIST2 Partner** Technical University of Denmark, DTU (www.dtu.dk)
	Contact: Prof. Jan Madsen
Receiving Institution	**ARTIST2 Partner** University of Linköping
	Contact: Prof. Petru Eles
Persons	Shankar Mahadevan
	Jan Madsen
Area of Collaboration	Modelling and simulation of heterogeneous distributed embedded systems for automotive applications.
Technical Work	The aim is to extend the multiprocessor simulation framework (ARTS) developed at DTU, with capabilities of modelling Time-Triggered and Event-Triggered protocols used by the automotive industry.
Approximate Dates and Duration	First half 2006, 1 week
Approximate Costs	Number of people : 2 from DTU
	Travel : 400 € Stay: 1000 €
Long-range Impact on Integration	Simulation-based modelling of heterogeneous distributed embedded systems supporting various scheduling policies and communication protocols. One of the main goals is the comparison of the protocols with regard to pessimism, average delay, robustness, etc.

3.4.1.1.4 Mobility: Visit at Technical University of Denmark

Sending Institution	**ARTIST2 Partner** University of Linköping
	Contact: Prof. Petru Eles
Receiving Institution	**ARTIST2 Partner** Technical University of Denmark, DTU (www.dtu.dk)
	Contact: Prof. Jan Madsen
Persons	N.N.
Area of Collaboration	Modelling and simulation of heterogeneous distributed embedded systems for automotive applications.
Technical Work	The aim is to extend the multiprocessor simulation framework (ARTS) developed at DTU, with capabilities of modelling Time-Triggered and Event-Triggered protocols used by the automotive industry.
Approximate Dates and	Second half 2006, 2 weeks

Duration	
Approximate Costs	Number of people : 1 from University of Linköping Travel : 200 € Stay: 1000 €
Long-range Impact on Integration	Simulation-based modelling of heterogeneous distributed embedded systems supporting various scheduling policies and communication protocols. One of the main goals is the comparison of the protocols with regard to pessimism, average delay, robustness, etc.

3.4.2 Cluster Integration: Communication-centric systems

Summary of Work Already Achieved: Sept 2004 – August 2005

The most important results during the first 18 month were achieved through the integration work of the activity partners.

First, the stat-of-the-art in modelling and performance verification was assessed:

- ETH Zurich and the Embedded Systems Institute Eindhoven investigated how different performance verification approached can be integrated into the system design process. In a case study different approaches were utilized for analysis in order to identify their strengths and limitations in the design process.

- Technical University of Braunschweig and University of Linköping compared and evaluated so-called holistic and compositional performance analysis approaches. Also, methodologies for the analysis of complex hierarchical and dynamic priority schedulers were investigated.

The results of the comparisons and case studies were considered for the creation of new powerful techniques and models for the performance evaluation and optimization of complex real-time systems:

- ETH Zurich and University of Bologna utilized formal performance analysis to speed up cycle accurate simulation.

- University of Bologna and University of Linköping established high-level models for shared communication.

- Technical University of Denmark and University of Bologna created a methodology for mixed level simulation allowing an efficient evaluation and optimization of NoC architectures.

- Technical University of Braunschweig and ETH Zurich investigated a mixed performance analysis approach using SymTA/S and Real-Time Calculus.

- University of Braunschweig and University of Notre Dame developed a power analysis for complex heterogeneous embedded systems, which is currently used for power optimization.

High-Level Objectives: Sept 2005 – February 2007

The work aims at new best-case/worst-case models for hard real-time systems and at combined statistical and interval models for QoS applications in multi-media. These models will combine communication and computation, different models of computation, event models and scheduling policies.

In the first 18 month the state-of-the-art in models was assessed taking into consideration the particularities of various (quasi)standard communication protocols during system analysis and scheduling. The second 18 month will extend the modelling scope to emerging hierarchical protocols such as FlexRay, and include the new aspect of fault tolerant systems.

While at end of the first 18 month, a report was produced unifying and relating the different approaches to communication-centric systems and low power design, the second 18 month will combine statistical timing models, interval models and simulation to handle complex QoS requirements.

Description of Work Planned: Sept 2005 – February 2007

ETH Zurich and University of Bologna will continue their work unifying analytic methods and simulation (hybrid performance evaluation approach). They will also investigate energy driven scheduling policies in the context of sensor networks.

ETH Zurich and Technical University of Braunschweig will pursue their efforts for creating a mixed performance analysis approach using SymTA/S and Real-Time Calculus. Final objective is the creation of a real-time calculus based library for SymTA/S allowing a per component analysis of heterogeneous distributed systems (i.e. parts of the system are evaluated using real-time calculus, whereas others are evaluated using SymTA/S). This requires interfaces between the two methods.

ETH Zurich and Embedded Systems Institute Eindhoven will further investigate strengths and weaknesses of different performance analysis methods in the system design process.

Technical University of Braunschweig and University of Notre Dame will extend the existing power analysis to more detailed processor models and arbitrary scheduling policies and create power optimization methods (stochastic and heuristic) based on these models.

Technical University of Denmark and University of Bologna will continue their integration work combining ARTS and MPARM for NoC exploration.

University of Bologna will perform a cross benchmarking of the Xpipes architecture with state-of-the-art interconnects, considering performance, area and power. Based on the obtained results the Xpipes architecture will be tuned to improve weaknesses and to allow an industrial deployment.

In the context of the effort spent on the high-level modelling of system interconnects, University Bologna will augment the underlying methods to account for variable voltage/frequency processor cores. The main intention of this refinement is the determination of optimal voltage and frequency assignments for system power minimization.

University of Linköping will investigate analysis and optimization techniques for distributed embedded systems with fault tolerance constraints. Therefore, systems in the presence of transient faults will be considered to address the following issues:
- Scheduling with the requirement that deadlines are satisfied even in the presence of transient faults.
- Task mapping and optimisation of checkpoints.
- Study of various trade-offs, such as transparency vs. schedule length.

University of Linköping will continue their work in analysis and optimization of communication protocols from the automotive industry. In particular the emerging FlexRay protocol will be considered.

The activity partners will multiply efforts in combining statistical methods with interval models and simulation to obtain efficient approaches to formally handle QoS requirements of embedded and distributed applications. The emphasis will thereby lie on highly distributed systems such as sensor networks and intra-car networks.

Meetings Planned

3.4.2.1.1 Meeting: Workshop on distributed embedded systems in Leiden

Meeting Title	Workshop on distributed embedded systems in Leiden
Approximate Date	21.11.2005 – 24.11.2005
Objectives and expected output	ETH Zurich will organize a workshop on distributed embedded systems.
	The purpose of the workshop is to understand and compare the different performance analysis methods.
	One of the goals will be to define a set of sample problems that help to refine existing methods and to make clear strengths and weaknesses. Available methods include timed automata, real-time calculus, holistic scheduling and Symta/S.

3.4.2.1.2 Meeting: Summer school on communication centric systems

Meeting Title	Summer school on communication centric systems
Approximate Date	Summer 2006
Objectives and expected output	Technical University of Braunschweig will organize a summer school on communication centric systems.
	Top academic and industry speakers will be invited to outline the state-of-the-art in communication-centric system design, simulation and formal performance verification.

Planned Staff Mobility

3.4.2.1.3 Mobility: Participation in the distributed systems workshop in Leiden

Sending Institution	**ARTIST2 Partner** TU Braunschweig
	Contact: Prof. Rolf Ernst
Receiving Institution	**ARTIST2 Partner** ETH Zurich
	Contact: Prof. Lothar Thiele

Persons	Arne Hamann, Rafik Henia, Razvan Racu
Area of Collaboration	See workshop description above
Technical Work	See workshop description above
Approximate Dates and Duration	See workshop description above
Approximate Costs	Nb people : 3 Travel : 400 € Stay: 1000 €
Long-range Impact on Integration	Better understanding of the weaknesses and strength of different performance analysis approaches. Combination of several techniques profiting from individual strength and eliminating weaknesses to increase applicability in industry.

3.4.2.1.4 Mobility: Participation in the distributed systems workshop in Leiden

Sending Institution	**ARTIST2 Partner** University of Linköping Contact: Prof. Petru Eles
Receiving Institution	**ARTIST2 Partner** ETH Zurich Contact: Prof. Lothar Thiele
Persons	Petru Eles, Paul Pop, Traian Pop, Sorin Manolache
Area of Collaboration	See workshop description above
Technical Work	See workshop description above
Approximate Dates and Duration	See workshop description above
Approximate Costs	Nb people : 4 Travel : 2000 € Stay: 960 €
Long-range Impact on Integration	Better understanding of the weaknesses and strength of different performance analysis approaches. Combination of several techniques profiting from individual strength and eliminating weaknesses to increase applicability in industry.

3.4.2.1.5 Mobility: Visit at Linköping University

Sending Institution	**ARTIST2 Partner** TU Braunschweig Contact: Prof. Rolf Ernst

Receiving Institution	**ARTIST2 Partner** University of Linköping
	Contact: Prof. Petru Eles
Persons	N.N.
Area of Collaboration	Statistical Models
Technical Work	Extension of the SymTA/S approach with statistical models.
Approximate Dates and Duration	Second half 2006, 2 weeks
Approximate Costs	Nb people : 1
	Travel : 300 €
	Stay: 700 €
Long-range Impact on Integration	Modelling and analysis of embedded systems with mixed real-time requirements (hard, soft and firm) with SymTA/S.
	Verification of QoS requirements with SymTA/S.

3.4.2.1.6   Mobility: Visit at University of York

Sending Institution	**ARTIST2 Partner** TU Braunschweig
	Contact: Prof. Rolf Ernst
Receiving Institution	**ARTIST2 Partner** University of York
	Contact: Prof. Alan Burns
Persons	N.N.
Area of Collaboration	Statistical Models
Technical Work	Extension of the SymTA/S approach with statistical models.
Approximate Dates and Duration	Second half 2006, 1 weeks
Approximate Costs	Nb people : 1
	Travel : 300 €
	Stay: 350 €
Long-range Impact on Integration	Modelling and analysis of embedded systems with mixed real-time requirements (hard, soft and firm) with SymTA/S.
	Verification of QoS requirements with SymTA/S.

3.4.2.1.7   Mobility: Visit at ETHZ

Sending Institution	**ARTIST2 Partner** University of Bologna
	Contact: Prof. Luca Benini

Receiving Institution	**ARTIST2 Partner** ETHZ
	Contact: Prof. Lothar Thiele
Persons	N.N.
Area of Collaboration	Mixed formal-simulation based models
Technical Work	Merging MPARM with network calculus models.
Approximate Dates and Duration	Second half 2006, 1 week
Approximate Costs	Nb people : 1
	Travel : 300 €
	Stay: 500 €
Long-range Impact on Integration	Fast and accurate verification of communication-related properties. First steps toward a mixed formal and simulation-based modelling infrastructure

3.4.3 Cluster Integration: Low-Power design

Summary of Work Already Achieved: Sept 2004 – August 2005

The main contribution of University of Bologna has been in the extension of a complete power-modelling infrastructure for all components of current multi-processor systems-on-chip platforms and for future Network-on-Chip-based platform. Several extensions have been developed, including the model for variable frequency and variable voltage cores, as well as a prototype model for estimating the power consumption of IOs and external memories (this work has been performed in cooperation with associate partner STMicroelectronics). Techniques for energy optimization in system interconnects have been explored with the help of this platform

Additionally, Bologna has started a research effort on energy aware mapping of multi-task applications on multi-processor SoC execution platforms. The approach is based on variable-voltage processors where execution speed and voltage supply can be independently adapted to the processor's workload. The first result of this effort has been a design space exploration technique that automatically finds Pareto points in the power vs. throughput design space. The technique has been tested on streaming-like signal processing applications.

The Technical University of Denmark has started the development of a sensor network platform (Hogthrob project), with focus on: (1) Low Power processor design based on low-power synthesis (e.g., clock-gating), power modes and de-synchronizing (2) Power modelling: Simulation-based power modelling and estimation techniques have been investigated, with emphasis on stochastic modelling of batteries and investigation into the macro-modelling of various hardware components.

Additionally, DTU has also worked on empirical power estimation: Based on the prototype sensor network platform developed within Hogthrob, various test bench programs have been run on an AVR core synthesized on the FPGA and a number of physical measurements have been conducted.

Linköping University has developed a technique for static routing on NoC, with guaranteed delays and arrival probabilities in the presence of transient faults. For fault-tolerance, a combination of spatial and temporal redundancy is considered. Reduced communication energy is one of the goals. More recently the analysis of the worst-case buffer space needed has been performed. Based on this analysis, it is possible to develop an approach to buffer space minimization in the context described above.

Linköping University's has also performed additional work aiming at a more accurate modelling of actual communication and memory techniques used in MP SoC. Work is concentrating on: (1) Capturing the background communication due to cache misses in system level models. (2) Capturing the bus load due to system-wide synchronization. Once these modelling issues are solved, different optimization techniques can be used for e.g. task mapping and scheduling, as well as voltage selection. Results can be validated using accurate and fast simulation in the environment developed at Bologna.

High-Level Objectives: Sept 2005 – February 2007

The high-level objectives are in two directions: strengthening integration and making inroads in effective techniques for system-level power optimization

Strengthening integration: **work will be performed aiming at defining abstractions and models suitable for very-high-level system power estimation, both for localized and distributed platforms. Example platforms will be used to drive the integration effort, in the domain of multi-processor-systems on chip (leveraging the MPARM infrastructure) and in the domain of distributed sensor networks (leveraging the ARTS simulation model and the prototype sensor networks).**

System-level power optimization: **in this area, the interaction between resource allocation and scheduling and power optimization will be explored both for localized and distributed systems. Furthermore, the interplay between power and other cost metrics (reliability, performance) will be explored.**

Description of Work Planned: Sept 2005 – February 2007

System Power modelling: University of bologna and DTU will cooperate to enhance the power modelling capabilities for on-chip communication fabrics, integrating and extending the power models to multi-hop, synchronous and asynchronous interconnects.

Power optimization via system-level resource allocation and scheduling for MPSoC: Linköping University and University of Bologna will work on developing static allocation and scheduling techniques for complex multi-processor systems on chip that minimize power consumption in computation, communication and storage while satisfying performance constraints. Realistic models of variable-voltage processors with shut-down sates will be used, and scheduling and allocation results will be validated on the MPARM cycle accurate virtual platform.

Scheduling based energy optimization for energy-scavenging wireless sensor networks:
ETHZ and University of Bologna will cooperate to the development of new abstract models
and scheduling algorithms that aim at maximizing the number of sensing events successfully
processed by wireless sensor networks equipped with both energy storage and energy
scavenging devices.

Meetings Planned

3.4.3.1.1   Meeting: Winter meeting of the Low-power design

Meeting Title	ARTIST2 Cluster meeting in Bologna
Approximate Date	2.2005
Objectives and expected output	University of bologna will organize a workshop/meeting of the ARTIST2 cluster focusing on platforms. Within the workshop a focused meeting of the low-power design activity will be held.
	The goal of the meeting will be to focus on a common strategy for power modelling at high levels of abstraction and on exchanging ideas and developing a research agenda on techniques for power-aware scheduling and allocation.

Planned Staff Mobility

3.4.3.1.2   Mobility: Visit to ETHZ of University of Bologna's staff

Sending Institution	**ARTIST2 Partner** University of Bologna Contact: Prof. Luca Benini
Receiving Institution	**ARTIST2 Partner** ETH Zurich Contact: Prof. Lothar Thiele
Persons	David Brunelli, Elisabetta Farella
Area of Collaboration	Scheduling techniques for energy-scavenging sensor networks
Technical Work	Joint development of scheduling algorithms, modelling of sensor networks for analysis of the scheduling results.
Approximate Dates and Duration	03-05 One month
Approximate Costs	Nb people : 1 Travel : 400 € Stay: 1000 €
Long-range Impact on	Developing a common strategy for scheduling for energy-scavenging sensor networks

Integration	

3.4.3.1.3   Mobility: Visit at Linköping University

Sending Institution	**ARTIST2 Partner** University of Bologna
	Contact: Prof. Luca Benini
Receiving Institution	**ARTIST2 Partner** University of Linköping
	Contact: Prof. Petru Eles
Persons	N.N.
Area of Collaboration	Energy aware scheduling and allocation for MPSoC Platforms
Technical Work	Develop optimization-based strategies for scheduling and allocation for MPSoC platforms.
Approximate Dates and Duration	Second half 2006, 2 weeks
Approximate Costs	Nb people : 1 Travel : 400 € Stay: 800 €
Long-range Impact on Integration	Better understanding of abstract models in power optimization, development of aggressive optimization-based system-level power optimization strategies

3.4.4   NoE Integration: Resource-aware Design

Summary of Work Already Achieved: Sept 2004 – August 2005

During the first six months of the project, several cooperations have been set up. Cooperation has been established between Università di Bologna and Dortmund University. The objective is to integrate the memory-aware compiler developed in Dortmund with the multi-processor platform simulator developed in Bologna. The first results have been development of a new source-level transformation tool for performing memory optimization by Dortmund, and the development of compatible memory organization models by Bologna (including I and D caches as well as scratchpad memories).

A second cooperation has been established between Università di Bologna and Aachen University. The objective is to extend the modelling capabilities of the platform simulator developed in Bologna toward heterogeneous multi-core architectures, exploiting the Application-specific Processor development framework based on the LISA architecture description language developed in Aachen. The first result of this work has been the re-design of Bologna's core interfacing protocol within the platform simulator. On the other hand, Aachen has provided extensive technical support on Lisatek core wrapping architectures, and toolsets.

An additional cooperation between Bologna and Saarland University has been established. The objective of this cooperation is the exploitation of the platform simulator developed by Bologna, and more specifically of the timing accurate core models incorporated in the simulator, as targets for the worst case execution analysis framework developed in Saarland University.

High-Level Objectives: Sept 2005 – February 2007

The goal is to provide, through the integration of research activities of many participants a viable path for resource-aware software and hardware development. The final objective is to achieve integration of research activities in concrete deliverables:

- A set of tools that can interact and work together and demonstrate the achievable optimizations on a particular hardware platform.

A methodology that enables the design of predictable embedded systems with a special focus on issues that cut several layers of abstraction, such as hardware and compiler design is to be found.

Description of Work Planned: Sept 2005 – February 2007

ETH and U. Bologna will cooperate on resource awareness in sensor networks. In particular, by combining the mutual expertise available the researchers intend to develop energy-driven schemes for power distribution and scheduling in case of energy harvesting components.

The coupling of MPARM tools from Bologna with LISATek tools from RTWH Aachen und with memory aware compilers from Dortmund University will continue. TUD, STM and the University of Linköping with contribute to the power modelling of MPARM. Modelling of applications executing on MPARM will be looked at by EPFL. USaar will provide the partners will input on the analyzability of synthesized code (code generated from high tools like StateMate or MatLab), in particular in the context of the MPARM platform.

Meetings Planned

A meeting involving all partners is scheduled to be held during DATE in March 2006. Another general meeting is scheduled for DATE 07. An intermediate general meeting will be scheduled in the fall of 2006, if a resynchronization becomes necessary. In addition, there will be several meetings between limited sets of partners, focussing on specific topics of the cooperation.

3.4.4.1.1 Meeting: General meeting "Resource aware design" at DATE 06

Meeting Title	Meeting: General meeting "Resource aware design" at DATE 06
Approximate Date	March 2006
Objectives and expected output	The purpose of this meeting is an overall update on the synchronization of the activity. Synergies between the cooperation between two partners will be discussed with the objective of a tighter integration of the work of more partners.

3.4.4.1.2 Meeting: Meeting: General meeting "Resource aware design" at DATE 07

Meeting Title	Meeting: General meeting "Resource aware design" at DATE 06
Approximate Date	April 2007
Objectives and expected output	The purpose of this meeting is an overall update on the synchronization of the activity. The output will depend on the results of the DATE 06 meeting.

Planned Staff Mobility

A short term stay of PhD students from Bologna at Dortmund is expected to take place in the spring of 2006. Additional stays may be scheduled as they become necessary.

3.4.4.1.3 Mobility: MOMPARM/Memory-aware compilation integration

Sending Institution	**ARTIST2 Partner** U. Bologna Contact: Luca Benini
Receiving Institution	**ARTIST2 Partner** Dortmund University Contact: Peter Marwedel
Persons	open
Area of Collaboration	Integration of compiler optimizations into multiprocessor simulation framework.
Technical Work	The objective of the visit is to provide a better understanding of the potential and the limitations of the work on compiler optimizations at Dortmund
Approximate Dates and Duration	Unknown
Approximate Costs	Nb people : 2 people Travel : 400 € Stay: 400 €
Long-range Impact on Integration	This visit is expected to explore the potential for a structured exploration of the design space and the constraints for having the same type of integration also for heterogeneous multiprocessor systems.

3.5 Cluster: Control for Embedded Systems

The following is a description of the activities and overall objectives for the period: September 2005 – February 2007. The next reporting period will cover September 2005 – August 2006.

3.5.1 Platform: Design Tools for Embedded Control

Summary of Work Already Achieved: Sept 2004 – August 2005

A survey on co-design tools for modelling and design of real-time control systems has been completed. In addition to this a state of the art survey on approaches for model/tool integration and model management has been initiated.

The individual tools have been further developed. For example, the TrueTime tool from LUND has been extended with support for wireless network blocks, battery-powered devices, and local clocks with drift and offset. The TORSCHE tool from CTU and the tools from UPVLC have also been further developed.

The tools have been promoted. For example, course and training material has been developed for TrueTime and a tutorial on TrueTime was given at the IFAC World Congress, Prague, July 3.

High-Level Objectives: Sept 2005 – February 2007

The objectives for the coming period involve tool integration, coordination with other clusters, and further development, coordination and promotion of the individual tools. A tool integration plan will be developed as well as use cases and integration scenarios describing how the individual tools can be used together during different phases of the design process. In addition to this, case studies involving initial integration between individual tools will be developed.

Concerning coordination with the platform activities within other clusters, the objective is to invite the other clusters to join in a refined tool survey, to create a better cross-cluster map of tools for embedded control systems development. It is also our opinion that a joint tool/platform meeting involving all the clusters should be organised within Artist2.

Description of Work Planned: Sept 2005 – February 2007

A tool integration plan will be produced describing the integration of the individual tools. A number of use cases or integration scenarios will be developed. Examples of local integration where a small number of tools are used in an integrated fashion will be developed. . A state of the art survey will also be completed and used to define a framework with which different model/tool integration approaches can be compared.

Meetings Planned

3.5.1.1.1 Meeting: Cluster Meeting in Seville, Dec 2005

Meeting Title	Cluster meeting: Platform

Approximate Date	December 2005
Objectives and expected output	The initial integration examples will be defined and responsibilities assigned.

Meeting: Cluster Meeting in Prague, April 2006

Meeting Title	Cluster meeting: Platform
Approximate Date	April 2006
Objectives and expected output	As a part of the general cluster meeting in Prague the platform activities will be discussed. • Tool integration plan will be organized and responsibilities assigned • Integration scenarios will be defined • Integration example definitions will be completed.

Meeting: Platform Meeting in connection with CACSD, Munich, October 2006

Meeting Title	Platform meeting
Approximate Date	October 2006
Objectives and expected output	Finalize the year 2 deliverables.

Planned Staff Mobility

3.5.1.1.2   *Mobility: PhD exchange from CTU to LUND*

Sending Institution	**ARTIST2 Partner:** CTU Contact: Zdenek Hanzalek
Receiving Institution	**ARTIST2 Partner:** LTH Contact: Karl-Erik Årzén
Persons	Not known
Area of Collaboration	Tool integration
Technical Work	Integration between TORSCHE and TrueTime
Approximate Dates and Duration	1-2 months during Feb-May 2005

Approximate Costs	Nb people : 1 PhD student Travel : 400 € Stay: 1500 €
Long-range Impact on Integration	The integration will make it possible to use TrueTime also for simulation of FPGA-based control systems in combination with TORSCHE for the scheduling of the FPGA

3.5.1.1.3 Mobility: PhD exchange from KTH to LUND

Sending Institution	**ARTIST2 Partner**: KTH Contact: Martin Törngren
Receiving Institution	**ARTIST2 Partner:** LUND Contact: Karl-Erik Årzén
Persons	Not known
Area of Collaboration	Tool integration
Technical Work	Integration between TrueTime and response-time analysis tools from KTH Discussion of tool integration scenarios and the general survey on tool/model integration conducted at KTH.
Approximate Dates and Duration	0.5 month during Spring 2005
Approximate Costs	Nb people : 1 PhD student and 1 senior researcher Travel : 300 € Stay: 600 €
Long-range Impact on Integration	The integration increases the usability of TrueTime and contributes to the creation of an integrated tool set for co-design of embedded control systems.

3.5.2 Cluster Integration: Control in real-time computing

Summary of Work Already Achieved: Sept 2004 – August 2005

Since this a rather new research area it was decided that the main activity during the first year should be the creation of a research roadmap. This roadmap has been completed. The aim of the roadmap is to chart the area, provide a common platform for the coming work, and to identify the most important research directions.

An international workshop in Control for Embedded Systems was held in Lund with 20 participants. The international affiliates Lui Sha and Tarek Abdelzaher participated and gave value input. A separate research agenda for the work within Artist2 was written as the output from the workshop. Karl-Erik Årzén and Anders Robertsson were invited to participate as the only non-US participants at a workshop on the future of control of computing systems organized by NFS and held at IBM, May 3-4, 2005. •   RTC 2005, a workshop on real-time control and control of real-time computing systems was organized in association with ECRTS 05 at Mallorca. An invited session on control over sensor networks and control of sensor network resources (co-organized with RUNES) has been accepted for the IEEE Conf on Decision and Control and the European Control Conference, Sevilla, Dec 2005.

A new feedback scheduling method was developed for control loops by Dan Henriksson and Anton Cervin. A paper will appear at the CDC-ECC'05 in Sevilla – LUND. KTH has been working on control-based error-correction in packet-switched networks, on the use of radio network feedback to improve TCP performance over cellular networks, and on network state estimation.

High-Level Objectives: Sept 2005 – February 2007

The overall objective of this activity is to advance the state of the art in applying control methods for uncertainty handling and as a way to provide flexibility and improved performance in embedded computing and communication systems. The application areas include performance control of web server systems, feedback-based reservation management in embedded real-time systems, feedback scheduling of control systems, and control of communication and sensor networks.

Description of Work Planned: Sept 2005 – February 2007

Much of the work for the next time period will be based on the road map. Currently the roadmap contains no time dimension. Hence, based on the road map we will extract milestones at the short, medium and long time-scale. We will also use the roadmap to define the interaction points with the other clusters and the requirements from the other clusters. We will also disseminate the roadmap in the form of, e.g. a quality journal article.

A follow-up workshop to the successful workshop on Control for Embedded Systems is planned for the summer 2006. The focus will be dynamics and models of computer software systems.

The research on feedback-based scheduling, performance control of web server systems and control of communication and sensor networks will continue. The collaboration with our US affiliate partners will continue to be important.

Meetings Planned

3.5.2.1.1   Meeting: Cluster Meeting in Seville, Dec 2005

Meeting Title	Cluster meeting: Control in real-time computing
Approximate Date	December 2005
Objectives and expected output	To extract research milestones from the roadmap.

Meeting: Cluster Meeting in Prague, April 2006

Meeting Title	Cluster meeting: Control in real-time computing
Approximate Date	April 2006
Objectives and expected output	Technical research presentation. Planning for the workshop on Dynamics and Models of Computer Software Systems

3.5.2.1.2 Meeting: Workshop on Dynamics and Models of Computer Software Systems

Meeting Title	Workshop on Dynamics and Models of Computer Software Systems
Approximate Date	June-August 2006
Objectives and expected output	To define what the appropriate models should be for different types of computer software systems. To define what type of support that is needed from the underlying RTOS/middleware. Several clusters and industrial affiliates will be invited to participate.

Planned Staff Mobility

3.5.2.1.3 Mobility: PhD student visit from UPC to LUND

Sending Institution	**ARTIST2 Affiliated Partner**: Universidad Politechnica de Catalunya, UPC (affiliated to Mälardalens Högskola / TU Kaiserslautern – Gerald Fohler)
	Contact: Pau Marti
Receiving Institution	**ARTIST2 Partner** Lund University
	Contact: Karl-Erik Årzén
Persons	PhD student candidate Rosa Castane Selga: Feedback scheduling of control systems
Area of Collaboration	Feedback scheduling of control loops
Technical Work	Theory development, modelling and simulation, thesis production
Dates	August 8 2005 – December 31 2005
Approximate Costs	Nb people : 1 person Travel : 400 € Stay: 4000 €
Long Range Impact on Integration	Important integration effort for the collaboration between LUND, Mälardalen and UPC.

Published Work	Is planned
Further Collaboration Planned	The collaboration between UPC, LUND and Mälardalen will continue

3.5.2.1.4 Mobility: PhD visit to Univ of Illinois

Sending Institution	**ARTIST2 Partner** LUND Contact: Karl-Erik Årzén
Receiving Institution	**ARTIST2 Partner** Univ of Illinois Contact: Lui Sha
Persons	Not known
Area of Collaboration	Control of server systems and/or error control of software
Technical Work	Joint research work
Approximate Dates and Duration	3 months Spring-Summer 2006
Approximate Costs	Nb people : 1 PhD student Travel : 600 € Stay: 3000 €
Long-range Impact on Integration	The integration will maintain the good research connections with the US partners

3.5.2.1.5 Mobility: Research visit from Univ of Illinois to LUND

Sending Institution	**ARTIST2 Partner** Univ of Illinois Contact: Lui Sha
Receiving Institution	**ARTIST2 Partner** LUND Contact: Karl-Erik Årzén
Persons	Not known
Area of Collaboration	Control of server systems and/or error control of software
Technical Work	Joint research work
Approximate Dates and Duration	1-2 months Summer – Fall 2006

Approximate Costs	Nb people : 1 person Travel : 600 € Stay: 1500 €
Long-range Impact on Integration	The integration will maintain the good research connections with the US partners

3.5.3 Cluster Integration: Real-time techniques in control system implementations

Summary of Work Already Achieved: Sept 2004 – August 2005

Since this a rather new research area it was decided that the main integration activity during the first year should be the creation of a research roadmap. The aim of the roadmap is to chart the area, provide a common platform for the coming work, and to identify the most important research directions. The roadmap consists of approx 60 pages.

Another important integration activity was the International Workshop in Control for Embedded Systems was held in Lund with 20 participants. The international affiliates Lui Sha and Tarek Abdelzaher participated and gave value input. A separate research agenda for the work within Artist2 was written collectively as the output from the workshop.

A third important integration activity was the Valencia Graduate Course on Embedded Control Systems in April where all the cluster members lectured and the course material was developed jointly.

Additionally, a number of civilities have been performed. RTC 2005, a workshop on real-time control and control of real-time computing systems was organized in association with ECRTS 05 at Mallorca. An invited session on control over sensor networks and control of sensor network resources (co organized with RUNES) has been accepted for the IEEE Conf on Decision and Control and the European Control Conference, Sevilla, Dec 2005. An invited session about the research in the cluster was organized at the IFAC World Congress, Prague, July 8. The IFAC Summer School on Control, Computing and Communication, Prague, June 27 – July 1 was co-organized by the cluster. A special session on Model Driven Engineering at Euromicro, Porto, August 30 – September 3 was organized by the cluster. A number of quality publications have been produced by the members of the cluster during the year. For example, Årzen and Cervin are co-authors of the RTSS 25 year anniversary article "Real-Time Scheduling: A Historical Perspective" (has appeared in the Real-Time Systems journal). Several of the cluster members are also authors of chapters in the recently published "Handbook of Networked and Embedded Control Systems" (Birkhäuser), with Årzén in the editorial board.

High-Level Objectives: Sept 2005 – February 2007

The overall objective for this activity is too advance the state of the art in applying real-time system methodology for embedded control system implementation.

The 18 months objective is to provide a common framework of the control parameters that can be influenced by an embedded control system implementation and the real time operating systems criteria that can be adjusted to increase the robustness of the control system.

The long term goal is to provide a common framework model in order to facilitate the control and computing co-design.

The actual research that will be performed within the cluster and/or coordinated by the cluster will include the following items:

- Scheduling and control co-design including new techniques for analyzing control performance as a function of latency and jitter, and techniques to map implementation-specific parameters such as priorities to these timing variations (KTH/Lund/CTU/UPVLC)
- Development of components for control system applications including communication protocols (UPVLC/CTU)
- Mode change techniques for the control algorithms (e.g. control parameter updates taking performance and stability into account) and for the scheduling (e.g. mode change protocols) (UPVLC/KTH/Lund)

Description of Work Planned: Sept 2005 – February 2007

Much of the work for the next time period will be based on the road map. Currently the roadmap contains no time dimension. Hence, based on the road map we will extract milestones at the short, medium and long time-scale, and the items to be considered in the definition of the common framework. We will also use the roadmap to define the interaction points with the other clusters and the requirements from the other clusters. When that is done we the functionalities and criteria to develop the common framework for control development will be defined.

In addition to the work on the common framework the individual research on the real-time techniques in control system implementation will be continued.

Meetings Planned

3.5.3.1.1   Meeting: Cluster Meeting in Seville, Dec 2005

Meeting Title	Cluster meeting: Real-time techniques in control system implementation
Approximate Date	December 2005
Objectives and expected output	To extract research milestones from the roadmap. Define the common interface

Meeting: Cluster Meeting in Prague, April 2006

Meeting Title	Cluster meeting: Real-time techniques in control system implementation
Approximate Date	April 2006
Objectives and expected output	Continued work on the definition of the common framework

3.5.3.1.2   Meeting: Workshop on control over networks, KTH

Meeting Title	Control over networks
Approximate Date	June 2006
Objectives and expected output	A workshop on control over communication networks organized jointly by Artist2 and HYCON. The aim is to investigate the temporal and functional aspects of networked control loops, including network communication protocol issues. The output consists of the meeting notes and the presentation material.

Planned Staff Mobility

3.5.3.1.3   Mobility: Staff visit CTU to LUND/KTH

Sending Institution	**ARTIST2 Partner** CTU Contact: Zdenek Hanzalek
Receiving Institution	**ARTIST2 Partner** KTH + LUND Contact: Martin Törngren / Karl-Erik Årzén
Persons	Zdenek Hanzalek
Area of Collaboration	Real-time techniques in control system implementation
Technical Work	Research discussions concerning collaboration activities within Artist2
Approximate Dates and Duration	2 weeks, end of September 2005
Approximate Costs	Nb people : 1 person Travel : 400 € Stay: 700 €
Long-range Impact on Integration	Organization of the long-range collaboration between the Swedish Artist2 partners and CTU

3.5.3.1.4   Mobility: Staff visit UPVLC to KTH

Sending Institution	**ARTIST2 Partner** UPVLC Contact: Pedro Albertos
Receiving Institution	**ARTIST2 Partner** KTH Contact: Martin Törngren
Persons	Pedro Albertos
Area of Collaboration	Real-time techniques in control system implementation

Technical Work	Research discussions concerning collaboration activities within Artist2
Approximate Dates and Duration	1 week, Spring 2006
Approximate Costs	Nb people : 1 person Travel : 300 € Stay: 400 €
Long-range Impact on Integration	Organization of the long-range collaboration between KTH and UPVLC

3.5.3.1.5   Mobility: PhD student visit from UPVLC to KTH

Sending Institution	**ARTIST2 Partner**: Universidad Politechnica de Valencia Contact: Pedro Albertos
Receiving Institution	**ARTIST2 Partner** Royal Institute of Technology, KTH Contact: Martin Törngren
Persons	PhD student candidate Vicente Casanova: Embedded control systems
Area of Collaboration	Embedded control systems
Technical Work	Theory development, modelling and simulation
Dates	August - September
Approximate Costs	Nb people : 1 person Travel : 400 € Stay: 2000 €
Long Range Impact on Integration	Important integration effort for the collaboration between KTH and UPVLC
Published Work	Not yet decided
Further Collaboration Planned	The collaboration KTH and UPVLC will continue

3.5.3.1.6   Mobility: PhD student visit LUND to UPVLC

Sending Institution	**ARTIST2 Partner** LUND Contact: Karl-Erik Årzén

Receiving Institution	**ARTIST2 Partner** UPVLC Contact: Alfons Crespo
Persons	Martin Andersson
Area of Collaboration	Real-time kernel and OS support for flexible control system implementation
Technical Work	Investigation of the control kernel concept and of the OCERA RT-LINUX extensions
Approximate Dates and Duration	Three weeks in September 2005
Approximate Costs	Nb people : 1 person Travel : 400 € Stay: 300 €
Long-range Impact on Integration	Part of the long-term collaboration between UPVLC and LUND

3.5.3.1.7 Mobility: PhD student visit from UPVLC to LUND

Sending Institution	**ARTIST2 Partner**: Universidad Politechnica de Valencia Contact: Pedro Albertos
Receiving Institution	**ARTIST2 Partner** Lund University Contact: Karl-Erik Årzén
Persons	PhD student/lecturer Pedro Garcia Gil : dead-time compensation
Area of Collaboration	New methods for dynamic compensation for time delays, caused, e.g., by communication networks, in control loops
Technical Work	Theory development. Continuation of collaboration started in reporting period 1
Dates	1-2 months Spring 2005
Approximate Costs	Nb people : 1 person Travel : 400 € Stay: 1000 €
Long Range Impact on Integration	Temporal robustness and dynamic delay compensation in control loops simplifies the design problem for embedded control systems
Published Work	In the planning stage
Further Collaboration Planned	The collaboration between UPVLC and LUND will continue

3.5.4   NoE Integration: Adaptive Real-Time, Hard Real-Time, and Control

Summary of Work Already Achieved: Sept 2004 – August 2005

Mälardalen (Fohler) and LUND (Cervin) are working on the integration of the jitter margin and flexible scheduling. The jitter margin is an extension of the classical delay margin to time-varying delays. The jitter margin, J(L), is defined as the largest input-output latency jitter for which closed-loop stability is guaranteed for any time-varying latency $\Delta \in$ [L, L+J(L)], where L is the constant part of the input-output latency. The jitter margin is based on small-gain theory, but is not particularly conservative. The stability test is expressed in the frequency domain and a simple graphical interpretation involving the magnitude of the frequency curve exists.

The jitter margin can be used to derive hard deadlines that guarantee closed-loop stability, provided that the scheduling method employed can provide bounds on the worst-case and best-case response times of the controller tasks. The jitter margin can also be used when selecting network protocol for networked control loops.

In the context of the flexible scheduling framework, the jitter margin is used as a design tool for finding optimal static schedules for multiple concurrent control loops. The proposed design procedure can be outlined in three steps. The first step is to find a static schedule for the controllers that give acceptable control performance in terms of the apparent phase margin. The second step is to use nonlinear optimization techniques to optimize the schedule with regard to the control performance, again as measured by the apparent phase margin. The third step is to compute how much additional jitter can be tolerated in each task and use this information to allow sporadic tasks to execute. The tasks are then scheduled on-line using the slot-shifting technique.

Lund (Cervin) and Ericsson (Eker) are continuing their development of the control server model, with focus on distributed systems. The control server is a scheduling mechanism tailored to control tasks that combines three different ideas:

- *Reservation-based scheduling*. Each task is scheduled by a modified constant bandwidth server, where a dynamic server period is used.

- *Subtask scheduling*. A task may be divided in several segments that are scheduled as subtasks. Scheduling the two main parts of a control algorithm (Calculate and Update) as subtasks, the input-output latency of the controller can be reduced.

- *Time-triggered I/O*. Inputs can be read and outputs can be written at predefined points in time by the kernel, minimizing the jitter in the control actions.

The basic resource allocation model in the Control Server uses the concept of shares. To allocate a share x% of a resource to a component means that that component appears to be using its own private resource with x% of the original capacity. This is called ideal resource reservation. Note that the resource allocation is uniform over time. This means that, even if a component is not using a resource during a time interval, the resource will still be allocated.

In the single-CPU case, time-uniform resource allocation makes sense. In distributed systems, however, this would incur a delay of one period per node—something which is intolerable for many applications. For networked applications, the delay in a node can be shortened by increasing the resource usage. The downside is that quite large amounts of slack may result in the schedule.

Another complication in the distributed case is that the same resource may be used several times by the same end-to-end task. In a wireless networked control loop, for instance, it is likely that the same shared medium will be used both for the transmission of the measurement signal (from the sensor node to the control node) as for the control signal (from the control node to the actuator node). Hence, some time scheduling is inevitable to prevent further resource waste.

Pavia/Pisa (Buttazzo) and Lund (Cervin) have collaborated on adding support for the control server model in the SHARK kernel with the aim to use SHARK as a shared platform for implementing control applications.

Collaboration has started involving Lund, UPC, and Mälardalen. Rosa Castane Selga is a PhD student candidate from UPC that is spending August – December 2005 in Lund working on feedback scheduling methods for control. At Lund a new feedback scheduling strategy for multiple control tasks has been developed that uses feedback from the plant states to distribute the computing resources optimally among the tasks. Linear-quadratic controllers are analyzed, and expressions relating the expected cost to the sampling period and the plant state are derived and used for on-line sample-rate adjustments. In the case of minimum-variance control of multiple integrator processes, an exact expression for the optimal sampling periods can be obtained. For the general case, an on-line optimization procedure is used.

In the collaboration this approach is extended in several directions. One extension is the combination of this feedback scheduling method with the control server model in order to achieve deterministic input output latencies in the control loop. Another extension is to use a cost function that is based on the integrated absolute error instead of quadratic cost functions.

Several integration activities were performed involving CTU, UPVLC and SSSA (affiliated to Pavia) related to the OCERA project. UPVLC (Crespo) has evaluated the performance of the scheduling policies related to offer constant bandwidth behaviour. In conjunction with SSSA (Lipari), a new version of the CBS called IRIS was developed. This new algorithm was implemented and evaluated in a real-time environment providing both hard and soft real-time constraints. The IRIS algorithm was implemented in RTLinux and included in the distribution of the OCERA project.

In order to add flexibility to the real-time applications UPVLC has developed a nano-kernel called Xtratum. Xtratum is a thin layer of software that provides a simple and convenient API to access interrupt mechanisms and timer devices. Xtratum permits the execution of environments/applications under spatial and temporal isolation. Xtratum has been developed under the OCERA project.

CTU has built up several demonstrators for communication components based on the OCERA architecture (UPVLC, SSSA, CTU) including fish breeding control and supervision system (process control application), remote programming of mobile robot (robotics and supervision), human machine interface for autogyro (data acquisition and visualization), and a robotic arm demonstrator (servo-control).

In addition, the ART, Control, and HRT cluster members were strongly involved in mutual workshops and seminars.

High-Level Objectives: Sept 2005 – February 2007

The overall purpose of the cross cutting activity is to integrate research among ARTIST2 control and real-time teams on different computational models for embedded control systems and the use of control techniques to provide flexibility in embedded systems.

The long term objective:

- Increased understanding of how the jitter and delay introduced by the operating system on control activities affect the performance of the controlled system. The definition of performance measures will be also investigated to precisely define some quality of control requirements.

- A unified design and implementation approach for resource-aware embedded control requires a combination of hard real-time techniques, adaptive real-time techniques, event-triggered formalisms, and time-triggered formalisms.

- Reservation-based scheduling of control systems and signal processing systems, combined with hierarchical and feedback-based scheduling is an approach that promises to resolve many of the problems associated with conventional fixed-priority-based control system implementations. The joint actions of Lund and Pavia together with the affiliated partners Ericsson, and Enea will make a strong impact in this field.

The 18-month objective is to demonstrate that applications of diverse type can be specified in terms of resource-aware tasks, and scheduling algorithms can be made adaptive by means of control schemes.

We will:

- study the advantages and disadvantages of different modelling and implementation formalisms for embedded control systems with respect to which levels of temporal determinism that can be achieved and how well they can handle implementation-level resource constraints

- investigate to what extent current robust control design methods cover temporal uncertainties emanating from the implementation platform

- investigate how the control server model can be combined with hierarchical feedback-based scheduling in order to combine flexibility with latency guarantees.

Investigate a control-based model for real time tasks in which computing resources and application performance are jointly considered. The model should allow each task to trigger itself in a flexible basis: at each task instance execution, the executing instance will inform the scheduler when the next instance should be executed. The next instance execution point in time should be dynamically obtained as a function of the utilization factor and the application dynamics and performance.

Description of Work Planned: Sept 2005 – February 2007

The work planned for the coming 18 month period involved the following items:

- Continuation of the integration activities that already have started

- Identify and start new activities that possibly also involve the RT Components cluster

- Develop a "demonstrator" that exemplifies how applications of diverse type can be specified in terms of resource-aware tasks, and that scheduling algorithms can be made adaptive by means of control schemes. The Shark operating system will be used as a shared platform to run experiments on robot control systems available within the cluster sites. Also a simulation tool, TrueTime, developed at the University of Lund, will be used to run simulation experiments on synthetic task sets to evaluate the effect of delay and jitter.

- Investigation on quality-of-control management policies will be also carried out at the theoretical level, by combining control theory with adaptive scheduling techniques.

- Arrange a joint summer school between the ART and the Control cluster

- Organize one or two workshops on topics within the area of the activity. The structure and organization of the workshops will be modelled after the successful workshops that were organized by the HRT cluster in reporting period one. The exact topics are yet to be decided. Industrial participation is crucial for these workshops.

Meetings Planned

3.5.4.1.1   Meeting: Activity Meeting

Meeting Title	Network integration activity meeting
Approximate Date	Spring 2006
Objectives and expected output	Organize and coordinate the activities within the activity, with a particular emphasis on how to involve the RT Components cluster.

3.5.4.1.2   Meeting: Workshop 1

Meeting Title	Adaptive RT, HRT and Control Workshop 1
Approximate Date	Late Spring 2006
Objectives and expected output	Focus on a particular sub theme of the activity with a strong industrial interest. Identify the objectives, challenges and research directions for the particular area. The output consists of the meeting notes and the presentation material.

3.5.4.1.3   Meeting: Summer school

Meeting Title	Adaptive real-time and control summer school
Approximate Date	Summer 2006
Objectives and expected output	Joint summer school between the control and the ART cluster.

3.5.4.1.4   Meeting: Workshop 2

Meeting Title	Adaptive RT, HRT and Control Workshop 2
Approximate Date	Late Fall 2006
Objectives and expected output	Focus on a particular sub theme of the activity with a strong industrial interest. Identify the objectives, challenges and research directions for the particular area. The output consists of the meeting notes and the presentation material.

Planned Staff Mobility

3.5.4.1.5   Mobility: Mobility between LUND and SSSA/Pisa

Sending Institution	**ARTIST2 Partner** LUND Contact: Karl-Erik Årzén
Receiving Institution	**ARTIST2 Partner** Pisa Contact: Giorgio Buttazzo
Persons	Not known
Area of Collaboration	Demonstrator development and planning for joint summer school
Technical Work	Demonstrator development
Approximate Dates and Duration	Two weeks during Spring 2006
Approximate Costs	Nb people : 1 person Travel : 600 € Stay: 600 €
Long-range Impact on Integration	Necessary in order to plan the joint demonstrator and the summer school.

3.6 Cluster: Testing and Verification

The following is a description of the activities and overall objectives for the period: September 2005 – February 2007. The next reporting period will cover September 2005 – August 2006. On top of the individual actions within the cluster, 1-2 joint cluster meetings will be held, and also a joint summer school will be planned. Further interactions with other clusters will be emphasized – this will be discussed on the upcoming joint meeting, to be held within the next couple of months.

3.6.1 Platform: T&V Platform for Embedded Systems

Summary of Work Already Achieved: Sept 2004 – August 2005

During the first 12 months a number of improvements have been made on the individual tools as developed by the partners:

- The Vertecs team (IRISA) supports two test generation tools: TGV and STG. During the period, a new version of TGV (based on on-the-fly enumerative algorithms) linked to the IF toolbox (Verimag) has been developed using STL libraries (in place of CADP libraries).

- Results have been implemented in the TIMES tool for automated schedulability checking.

- CFV supports the verification tool LASH and hosts powerful servers dedicated to verification tools.

- A number of improvements have been made on the Uppaal real-time model checker (www.uppaal.com). This includes the possibility to enrich the timed automaton models with C code. An extension of Uppaal (Uppaal Cora), dedicated to solving optimal scheduling and planning problems, has been introduced. Recently, a version of Uppaal (Uppaal Tron), dedicated to online testing of real time systems, has been announced.

Also, a general distributed verification environment (DiVinE, Brno) has been deployed. The environment supports the development of distributed enumerative model checking algorithms, enables unified and credible comparison of these algorithms, and makes the distributed verification available for public use in a form of a distributed verification tool.

Finally, an overview of existing tools has been accessible via a common web portal (the Yahooda web-page maintained by Brno).

High-Level Objectives: Sept 2005 – February 2007

As for the next 18 months period, the individual tools will be evaluated more carefully through case studies, and the results will be disseminated. Also, the work on distributed analysis tools will be strengthened.

Description of Work Planned: Sept 2005 – February 2007

The ongoing work on the individual tools will be continued. However, emphasis will also be made on evaluation of the tools through case studies in order to identify the most stable and mature versions with respect to integration. These will be made available for download via the Yahooda web page at Brno. The web page will also extended with information on tools for testing (until now, it has mainly included model checking tools).

The tool evaluation work will be extended to parallel and distributed model checkers (PMDC's) on the partners individual PC-clusters. Also, joint work on identifying a common coordination layer for such model checkers will be initiated, in order to enable the integration of various PMDC methods.

Finally, the possibility of exploiting national and European Grid activities will be pursued through the design of a Grid infrastructure for PMDC.

Meetings Planned

A joint meeting on PMDC with European teams outside Artist2 is planned on November 16-17 at INRIA Rhônes Alpes. It is expected that this will be followed by a series of meetings on coordination and infrastructure for distributed model checking.

Planned Staff Mobility

A number of exchange visits between Aalborg and Brno are expected on development and implementation of algorithms and methods for parallel and distributed model checking.

3.6.2 Cluster Integration: Quantitative Testing and Verification

Summary of Work Already Achieved: Sept 2004 – August 2005

In the first period a number of achievements within quantitative aspects of testing and verification have been made. These include cost guided searching techniques, testing theories and their implementations in tools like Uppaal, IF and Torx. Also, work on testing of infinite state systems has been made by INRIA. Finally a number of industrial case studies have been undertaken.

Considerable effort has been made on dissemination of results: The partners have been very active as invited speakers on Quantitative Testing and Verification at a number of conferences, and they have co-arranged a Dagstuhl meeting on testing (September 2004) and a summer school on 'Modelling and Components, Testing and Verification, Static Analysis' (September 2005).**High-Level Objectives: Sept 2005 – February 2007**

In the next period, work on test cases will be continued and the results disseminated in a repository made accessible on the web. Also, further development of testing theories and analysis techniques for quantitative aspects of models and their implementation will be sought.

Description of Work Planned: Sept 2005 – February 2007

The planned theoretical work includes the continuation of: metrics for testing coverage, abstraction methods, comparison of the results wrt. cost models with those of mixed-integer linear programming and operations research. New important areas include robustness and implementation of real time models, stochastic model checking (which integrates verification, performance and reliability analysis), and controller synthesis (which includes formal methods, game theory and control theory).

The theoretical work will be supplemented by experimental work on tool prototypes and case studies.

Meetings Planned

1-2 joint meetings will be held on the above subjects.

Planned Staff Mobility

Apart from the joint meetings, the exchange visits between partners will be continued in the coming period.

3.6.3 Cluster Integration: Verification of Security Properties

Summary of Work Already Achieved: Sept 2004 – August 2005

The main achievements during the period from Sept 2004 to August 2005 can be summarized as follows:

- We developed a proof that the Dolev-Yao model is a sound abstraction of the complexity theoretic model for protocols that combine several cryptographic primitives. This is a major result as: 1.) it provides a justification of the existing automatic verification methods for security protocols and 2.) It allows bridging a gap between the cryptology community, that has its own models and definitions of security properties and protocols as well as proof techniques of security, which are essentially complexity-theoretic, and the formal methods community that uses the Dolev-Yao model for which automatic verification methods and tools have been developed.

- We organized an international workshop dedicated to the verification of security protocols. The workshop, named Workshop on the link between formal and computational models, took place in Paris from 23-24 June 2005 and was very successful. We had approximately seventy participants and twenty-two presentations. The worldwide groups working on the subject were represented with an important participation from Industry.

- We developed a data base for security protocols and their properties that accessible vie the internet : the Security Protocols Open Repository at http://www.lsv.ens-cachan.fr/spore/

- We have developed a methodology with tool support for the certification of Smart card applications. More specifically, the Common Criteria (CC for short) are an international standard widely used in the Smart Card sector. The CC defines seven levels of certification for EAL 1 to EAL 7 with increasing demand on formal proofs and testing. While there is a number of applications certified up to the EAL5 very few certification exist for the EAL 6 and almost none for the EAL 7. While certifying an application at the highest levels can be a strong marketing argument, the cost of the development and the evaluation of a product that fulfils the CC requirements for these levels are too high. In particular, while there exists tool support and a methodology for the lower levels such support is missing for the EAL 6 and EAL 7. We developed a tool supported methodology for the EAL 6 and EAL 7. This work has been done in a collaboration involving an industrial tool editor Trusted Logic, a smart card applications developer Axalto, an evaluation body CEA-LETI and two research labs CEA-LIST and VERIMAG. A patent concerning the developed methodology is actually under study.

- There is a variety of specification methods for security protocols. As a first step toward integrating verification tools that use these methods, we developed a classification and relation of the different existing specification methods (multi-set rewriting and process algebra).

- We have studied the expressive power of a process calculus that allows one to express arbitrarily many runs of ping-pong protocol thanks to the presence of recursive definitions. We have established a number of decidability results that indicate the limitations of automatic verification even in this simple setting. Most prominently, we show that our process calculus is Turing-powerful.

- We have developed a general verification method for security protocols that can handle unbounded sessions, unbounded message size and unbounded fresh nonce creations.

- We have developed a sound and complete inference system for bounded-sessions cryptographic protocols (the messages size is still unbounded), method that has been extended to take into account protocols that can use timestamps.

- We have considered the problem of access control for the Calculus of Mobile Resources due to Godskesen, Hildebrandt, and Sassone. We establish a type system that lets us establish security policies for processes and show that our type system satisfies the usual requirements of type preservation under reduction and safety (i.e. that well-typed processes cannot misbehave.) Moreover, we present a sound type inference algorithm that will let us extract minimal security policies.

- We have uses of standard model-checkers for analysing various security protocols (e.g. use of muCRL, SPIN and CADP) and for addressing security treats based on real-time issues (using UPPAAL).

High-Level Objectives: Sept 2005 – February 2007

Engineering tools for security protocols:
Construction of powerful and accessible engineering tools for the engineering of security and communication protocols for embedded systems. The platform builds on existing work carried out by the various partners, and aims at identifying the best engineering tools and methodologies for the different security solutions being studied. The platform will provide a uniform access and to all testing and verification tools of the academic as well as industrial partners of the consortium.

Security and Trust management:
Construction of a resource aware decentralized access control and trust management system for the specification and the enforcement of high level access control (and privacy) policies in embedded systems, with a special emphasis on the smart surrounding context. Development of a rigorous semantics and computational models for security and trust for embedded system.

Description of Work Planned: Sept 2005 – February 2007

Engineering tools for security protocols:
The technical objective is the development and the integration more dedicated, open, rigorous engineering tools for security and communication protocols. The tools will capitalize on the experience produced in the first year and facilitate the link between embedded system industry and academia.

Security and Trust management:
The technical objective is to develop a rigorous and enforceable model for the specification of security and trust policies of embedded systems. Long term target include the design and implementation of tools for the specification, the prototyping and the verification of distributed trust management policies for embedded systems.

Meetings Planned

3.6.3.1.1   Meeting: Meeting on security protocols tool integration

Meeting Title	Meeting on security protocols tools integration
Approximate Date	January
Objectives and expected output	The purpose of this meeting is to discuss the specification languages underlying the tools, their semantics, and the underlying verification methods and to discuss weak and strong points of the different tools.
	Another purpose is to agree on a small but representative set of protocols that will be used to compare the different tools.

3.6.3.1.2   Meeting: Workshop on the link between formal and computational models

Meeting Title	Workshop on the link between formal and computational models
Approximate Date	July 9-16, 2006, Venice, Italy
Objectives and expected	We plan to reorganize this workshop probably as a satellite workshop of ICALP. We are also considering merging this workshop with others.

output	An important aspect of this meeting is that it allows protocol and cryptographic algorithms designer to meet with formal verification people.
	This is important for both communities.

Planned Staff Mobility

3.6.3.1.3　　Mobility:

Sending Institution	**ARTIST2 Partner** FT R&D
	Contact: Francis Klay
Receiving Institution	**ARTIST2 Partner** VERIMAG
	Contact: Yassine Lakhnech
Persons	Francis Klay
Area of Collaboration	Verification of security protocols
Technical Work	The purpose of the stay is to work on a real case study which is the electronic purse protocol.
Approximate Dates and Duration	June 2006, duration: one month
Approximate Costs	Nb people :　1
	Travel :　　　300 €
	Stay:　　　1500 €
Long-range Impact on Integration	