Information Society Technologies

Year 1 Review

Grenoble, October 5th and 6th, 2005

Perspectives and Discussion

Joseph Sifakis, Bruno Bouyssounouse

VERIMAG Laboratory

To discuss

Avoid effort duplication for reporting - reconsider using the IMT tool

Contract Amendments :

- Clause 23
- Clause 39 : recommendation that partners make audit certificates

Are costs of audit certificates eligible if they are not in Management ?

Difference between manpower for integration and manpower in the area
Amend the Technical Annex to reduce the difference

EPFL: finalize asap

Replace Pavia w/ Pisa

- Pavia becomes an affiliated partner,
- Catania, Evidence become affiliated to Pisa

Gerhard Fohler moves from Malardalen TU of Kaiserslautern

ST will remain core partner

To discuss

Add Tidorum as a partner: Budget comes from within the CTA budget

Add ACE as a partner. If ST leaves, then Ace gets ST's budget
Otherwise, an amount of 15k can be used from the cluster's JPASE budget

Components w/ HRT => RT Components

Spreading Excellence Budget Distribution

Rule: JPASE is 12% (enforced by the Commission) – to be spent only on schools, inviting visiting researchers and similar – not manpower.

Proposals for spending common JPASE:

- Graduate course on RT & control – discuss detailed proposal
- Leiden WS on distributed embedded systems – Nov 21st approved for about 8-9k€
- Artist day after the next year review

ARTIST2 NoE : Team Leaders

Real Time Components

Hard Real Time

Albert Benveniste – INRIA
Alberto Sangiovanni – PARADES
Paul Caspi – Verimag
Hermann Kopetz – TU Vienna
Werner Damm – OFFIS

Modeling and Components

Bengt Jonsson – Uupsala
François Terrier – CEA/LIST
Jean-Marc Jezequel – INRIA
Susanne Graf – Verimag
Tom Henzinger - EPFL

Adaptive Real-time

Giorgio Buttazzo – ~~Pavia~~ Pisa
Alan Burns – University of York
Michael Gonzalez - Cantabria
Luis Almeida – Aveiro
Gerhard Fohler – ~~Malardalen~~ TU of Kaiserslautern
Juan de la Puente – Polytechnic de Madrid

Testing & Verification

Kim Larsen - Aalborg/ CISS
Ed Brinksma – Twente/Eindhoven
Pierre Wolper – Centre Fédéré de Verification
Michel Bidoit - LSV
Thierry Jeron - INRIA

Control for Embedded

Karl-Erik Arzen – Lund
Martin Torngren – KTH
Alfons Crespo – UP Valencia
Vladimir Kucera - Czech TU

Compilers and Timing Analysis

Reinhard Wilhelm - Saarland
Rainer Leupers - Aachen
Christian Bertin – ST Microelectronics
Christian Ferdinand – AbsInt
Peter Marwedel - Dortmund
Puschner, Krall – TU Vienna
Bjorn Lisper –Maalardalen
Guillem Bernat – University of York

Execution Platforms

Lothar Thiele – ETH Zurich
Jan Madsen –DTU (TU Denmark)
Luca Benini – UoB
Petru Eles – ESLAB/Liu
Rolf Ernst – UBR
~~Martin Rem – Eindhoven~~
Josef Hooman - Eindhoven

Budget Distribution by Cluster

Real-Time Components

Components	HRT	ART	Compilers TA	Exec Platforms	Control	T&V	Non-Cluster
11,5%	10,7%	13,7%	14,3%	13,7%	11,5%	11,5%	13,0%

Non-Cluster : 7% Management + 6% Spreading Excellence

An additional 6% Spreading Excellence controlled by the clusters

21.2% for the new RT Components cluster 21.2%
Distribute 1% over the other clusters

Key Points

- Despite a relatively low level of funding, and heavy administrative overhead there is good basis for making headway
- We are leading the area in Europe and are the main player in the world (Driving force in Conferences, WG, International Societies)
- Reporting needs to be improved – focus on integration – provide evidence about progress (significant facts such as joint publications, technical results, transfer)
- Decentralised management of the clusters - strong coordination: OK
- Strong integration (new cluster on RT components, Platforms/CTA, Control/ART, ….)
- Simplify as much as possible managerial tasks while respecting administrative rules and contractual obligations

13:30 ***Management Activities***

- **ARTIST2 Management Structure**
  Joseph Sifakis (VERIMAG)
- Discussion

14:30 ***Components and Modelling Cluster***

- **Achievements and Perspectives**
  Overall Aims and Achievements + Future Evolution: 18-month Workprogramme
  Cluster leader: Bengt Jonsson (UPPSALA)
- **Component Modelling and Composition**
  Activity leader: Bengt Jonsson (Uppsala)
- **Development of UML for Real-time Embedded Systems**
  Activity leader: Francois Terrier (CEA)
- **Platform: Component Modelling and Verification**
  Actvity leader: Susanne Graf (VERIMAG)
- Discussion

15:30 break *(change venue)*

15:45 ***Hard Real-Time Cluster***

- **Achievements and Perspectives**
  Overall Aims and Achievements + Future Evolution: 18-month Workprogramme
  Cluster leader: Albert Benveniste (INRIA)
- **Diagnosis in Distributed Hard Real-time Systems**
  Activity leaders: Hermann Kopetz, Philipp Peti (TU Vienna)
- **NoE Integration: Semantic Framework for Hard Real-Time Design Flow**
  Activity leaders: Albert Benveniste (INRIA), Alberto Sangiovanni-Vincentelli (PARADES)
- **NoE Integration: Merging the Event-triggered and Time-triggered Paradigms**
  Activity leaders: Paul Caspi (VERIMAG), Nicolas Halbwachs (VERIMAG)
- Discussion

16:45 break

17:15 ***Adaptive Real-Time Cluster***

- **Achievements and Perspectives**
  Overall Aims and Achievements + Future Evolution: 18-month Workprogramme
  Cluster leader: Giorgio Buttazzo (PAVIA)
- **Flexible Scheduling Technologies**
  Activity leader: Giorgio Buttazzo (Pavia)
- **Adaptive Resource Management for Consumer Electronics**
  Activity leader: Gerhard Fohler (Mälardalen University)
- **NoE Integration: QoS aware Components**
  Activity leader: Alejandro Alonso (UP Madrid)
- **Platform: A Common Infrastructure for Adaptive Real-time Systems**
  Activity leader: Giorgio Buttazzo (Pavia)
- Discussion

18:00 *closing*

19:00 *cocktail dinner*

Tuesday October 4th

8:30 ***Compilers and Timing Analysis Cluster***

- **Achievements and Perspectives**
  - Overall Aims and Achievements
  - Future Evolution: 18-month Workprogramme
  Cluster leader: Reinhard Wilhelm (Saarland)
- **Architecture-aware compilation**
  Actvity leader: Rainer Leupers (RWTH Aachen)
- **Platform: Timing-Analysis**
  Actvity leader: Reinhard Wilhelm (Saarland University)
- **Platform: Compilers**
  Actvity leader: Rainer Leupers (RWTH Aachen)
- *Discussion*

9:30 ***Execution Platforms Cluster***

- **Achievements and Perspectives**
  - Overall Aims and Achievements
  - Future Evolution: 18-month Workprogramme
  Cluster leader: Lothar Thiele (ETHZ)
- **Communication-centric systems**
  Actvity leader: Rolf Ernst (TU Braunschweig)
- **Design for Low Power**
  Actvity leader: Luca Benini (University of Bologna)
- **NoE Integration: Resource-aware Design**
  Actvity leaders: Luca Benini (University of Bologna), Peter Marwedel (University of Dortmund)
- **Platform: System Modelling Infrastructure**
  Actvity leader: Jan Madsen (TU Denmark)
- Discussion

10:30 break

10:45 ***Control for Embedded Systems***

- **Achievements and Perspectives**
  - Overall Aims and Achievements
  - Future Evolution: 18-month Workprogramme
  Cluster leader: Karl-Erik Arzen (Lund)
- **Control in Real-time Computing**
  Actvity leader: Karl-Erik Årzén (Lund)
- **Real-time techniques in control system implementations**
  Actvity leader: Alfons Crespo (UPVLC)
- **NoE Integration: Adaptive Real-time, HRT and Control**
  Actvity leader: Karl-Erik Årzén (Lund University)
- **Platform: Design Tools for Embedded Control**
  Actvity leader: Karl-Erik Årzén (Lund University)
- *Discussion*

11:45 ***Coordinator (CDC) Presentation***

- *Jean-Noel Forget (CDC)*
- Discussion

12:20 *buffet lunch*

13:30 ***Testing and Verification***

- **Achievements and Perspectives**
  - Overall Aims and Achievements
  - Future Evolution: 18-month Workprogramme
  Cluster leader: Kim Larsen (Aalborg)
- **Cluster Integration: Quantitative Testing and Verification**
  Actvity leader: Ed Brinksma (University of Twente)
- **Cluster Integration: Verification of Security Properties**
  Actvity leader: Yassine Lakhnech (VERIMAG)
- **Platform: Testing and Verification Platform for Embedded Systems**
  Actvity leader: Kim Larsen (BRICS/Aalborg)
- *Discussion*

14:30 ***Joint Programme of Acitvities for Spreading Excellence (JPASE)***

- *Bruno Bouyssounouse (VERIMAG)*
- *Discussion*

15:00 ***18-Month Perspectives***

- *Discussion*

Parallel meetings:

16:00 - 18:00 **Reviewers' Meeting**

16:00 - 17:15 **General Assembly Meeting**

16:00 - 17:15 **Industrial Advisory Board Meeting**

17:15 - 17:30 break

17:30 -18:00 ***Industrial Advisory Board Feedback & Discussion***

18:00 ***Reviewers' Feedback & Discussion***

18:45 *closing*

19:30 ***Gala Dinner***
Chateau de la Commanderie
see the chartered buses for details

22:30/ 23:00 *Buses return to hotels*