Information Society Technologies

Year 1 Review

Grenoble, October 5th and 6th, 2005

Objectives, General Structure, and Management

Joseph Sifakis, Bruno Bouyssounouse

VERIMAG Laboratory

History

ARTIST - FP5 Accompanying Measure (2002-2005):

- Coordinate the R&D effort in the area of Advanced Real-time Systems
- Improve awareness of academics and industry in the area
- Define innovative and relevant work directions

Achieved through activities along 3 axes:

- Roadmaps for selected actions:
  (*Hard Real Time, Component-based Design, Adaptive Real Time, Execution Platforms*)
- International Collaboration
- Education

Information about these results is publicly available:

http://www.artist-embedded.org/Roadmaps/

Embedded Systems Design

Building embedded systems of
guaranteed functionality and quality,
at an acceptable cost,
is a major technological and scientific challenge.

The challenge is to produce theoretical and practical tools, which allow *system-centric* design approaches, with high:

- *Optimality of the overall product for its intended market segment*
  cost and time to market, quality/safety/security//reliability/dependability, use of resources (energy, bandwidth, processor, memory, etc)

- *Interactability in the embedded system environment*
  access to all available resources via seamless interaction, cooperating and concurrent devices/applications

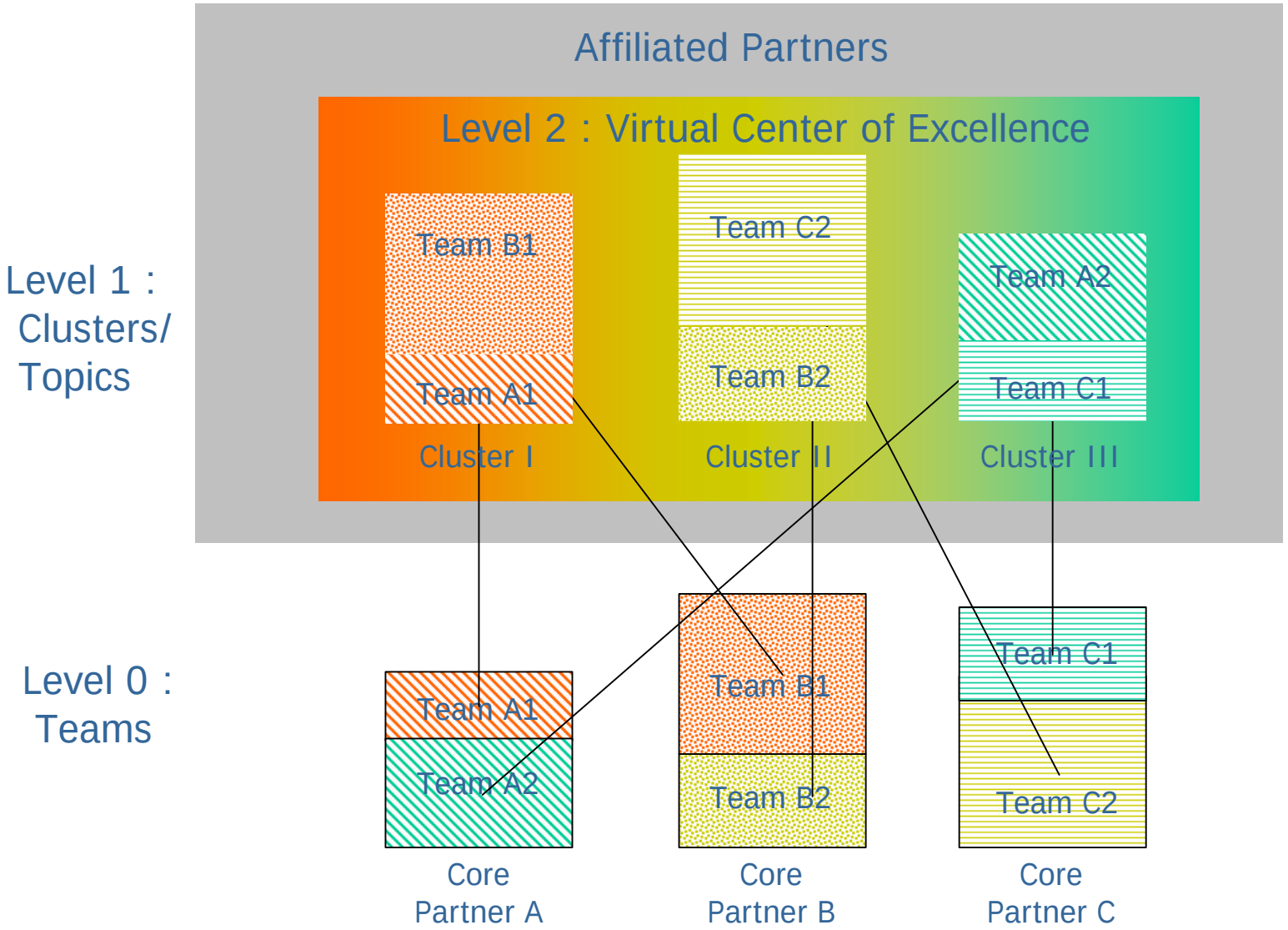
This requires a *multi-disciplinary approach*, integrating competencies covering the whole spectrum of activities in system development

Objectives

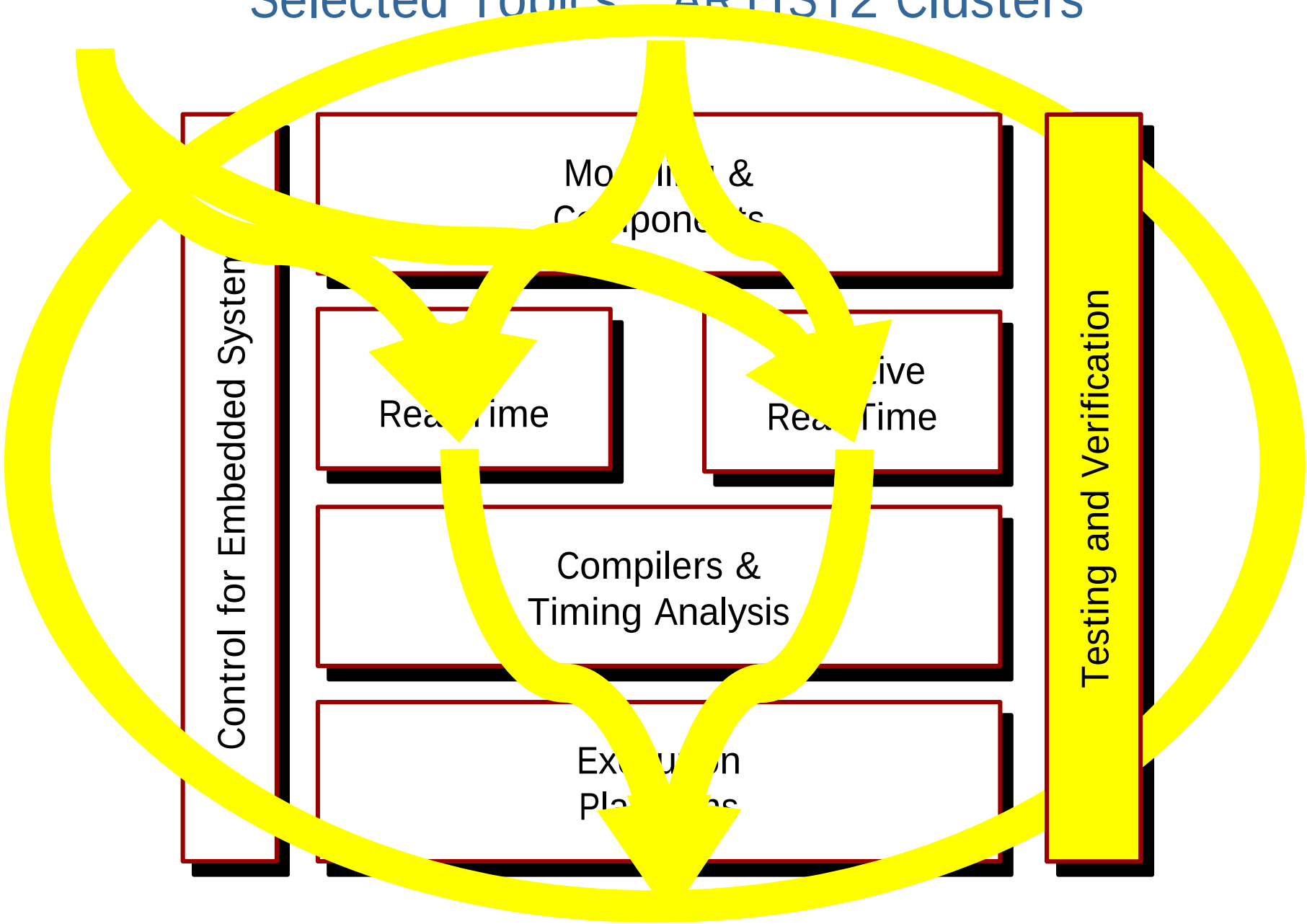
Reinforce and strengthen scientific and technological excellence in Embedded Systems Design:

- The NoE will act as a Virtual Center of Excellence
- **Two levels** of integration
  to create critical mass from selected European teams
  - Strong integration **within selected topics**
    by assembling the best European teams,
    to advance the state of the art in the topic.
  - Integration **between** topics
    to achieve the *multi-disciplinary* excellence and skills required for the development of future embedded technologies.
- Integration will be around a Joint Programme of Activities

Principle of Construction



Selected Topics : ARTIST2 Clusters



Core Participants (1/2)

	Short Name	Full Name and Country	Key researchers
1	CDC	Caisse des Dépots et Consignations (France)	**None**
2	UJF/ Verimag	University Joseph Fourrier / Verimag (France)	Paul Caspi, Susanne Graf, Nicolas Halbwachs, Yassine Lakhnech, Oded Maler, Joseph Sifakis
3	Aachen	RWTH Aachen (Germany)	Rainer Leupers
4	Aalborg	BRICS – Aalborg University (Denmark)	Kim Larsen, Anders Ravn
5	AbsInt	AbsInt Angewandte Informatik GmbH (Germany)	Christian Ferdinand
6	Aveiro	University of Aveiro (Portugal)	Luis Almeida
7	Cantabria	Universidad de Cantabria (Spain)	Michael Gonzalez Harbour
8	CEA	Commissariat à l'Énergie Atomique – Laboratoire LIST (France)	François Terrier
9	CFV	Centre Fédéré en Vérification, Université de Liège (Belgium)	Pierre Wolper
10	Czech TU	Czech Technical University (Czech Republic)	Vladimir Kucera
11	Dortmund	Dortmund University (Germany)	Peter Marwedel
12	DTU	Technical University of Denmark (Denmark)	Jan Madsen
13	ETHZ	Swiss Federal Institute of Technology – Zurich (Switzerland)	Lothar Thiele, Manfred Morari
14	FTR&D	France Telecom R&D	Pierre Combes, Kathleen Milsted
15	INRIA	Institut National de Recherche en Informatique et Automatique (France)	Albert Benveniste, Benoit Caillaud, Alain Girault, Thierry Jéron, Jean-Marc Jézéquel, Paul Le Guernic, Eric Rutten, Yves Sorel, Robert de Simone
16	KTH	Royal Institute of Technology (Sweden)	Martin Törngren
17	Linköping	Linköping University (Sweden)	Petru Eles

Core Participants (2/2)

Core Partner	Short Name	Full Name and Country	Key scientists
18	LSV / CNRS	Centre National de la Recherche Scientifique / Laboratoire LSV (France)	Michel Bidoit, Hubert Comon, Philippe Schnoebelen
18	Lund	Lund University (Sweden)	Karl-Erik Årzén
20	Mälardalen	University of Mälardalen (Sweden)	Gerhard Fohler
21	OFFIS	Kuratorium OFFIS e. V. (Germany)	Werner Damm, Bernhard Josko
22	PARADES	PARADES EEIG (Italy)	Alberto Sangiovanni Vincentelli
23	Pavia	University of Pavia (Italy)	Giorgio Buttazzo
24	UP Madrid	Universidad Politecnica de Madrid (Spain)	Juan de la Puente
25	Saarland	Saarland University	Reinhard Wilhelm
26	STM	ST Microelectronics – Central R&D (France)	Christian Bertin
27	Eindhoven	Technical University of Eindhoven (Netherlands)	Martin Rem
28	TU Vienna	Technical University of Vienna (Austria)	Hermann Kopetz, Peter Puschner, Philipp Petti
29	TUBS	Technical University Braunschweig (Germany)	Rolf Ernst
30	Twente	University of Twente (Netherlands)	Ed Brinksma
31	UoB	University of Bologna (Italy)	Luca Benini
32	Uppsala	Uppsala University (Sweden)	Bengt Jonsson
33	UPVLC	Universidad Polytecnica de Valencia (Spain)	Alfons Crespi
34	York	University of York (UK)	Guillem Bernat, Alan Burns, Iain Bate, Andy Wellings
35	Porto	Polytechnic of Porto	Eduardo Tovar
36	EPFL	Ecole Polytechnique Fédérale de Lausanne	Tom Henzinger

ARTIST2 NoE : Team Leaders

Real Time Components

Hard Real Time

Albert Benveniste – INRIA
Alberto Sangiovanni – PARADES
Paul Caspi – Verimag
Hermann Kopetz – TU Vienna
Werner Damm – OFFIS

Modeling and Components

Bengt Jonsson – Uupsala
François Terrier – CEA/LIST
Jean-Marc Jezequel – INRIA
Susanne Graf – Verimag
Tom Henzinger - EPFL

Adaptive Real-time

Giorgio Buttazzo – ~~Pavia~~ Pisa
Alan Burns – University of York
Michael Gonzalez - Cantabria
Luis Almeida – Aveiro
Gerhard Fohler – ~~Malardalen~~ **??**
Juan de la Puente – Polytechnic de Madrid

Testing & Verification

Kim Larsen - Aalborg/ CISS
Ed Brinksma – Twente/Eindhoven
Pierre Wolper – Centre Fédéré de Verification
Michel Bidoit - LSV
Thierry Jeron - INRIA

Control for Embedded

Karl-Erik Arzen – Lund
Martin Torngren – KTH
Alfons Crespo – UP Valencia
Vladimir Kucera - Czech TU

Compilers and Timing Analysis

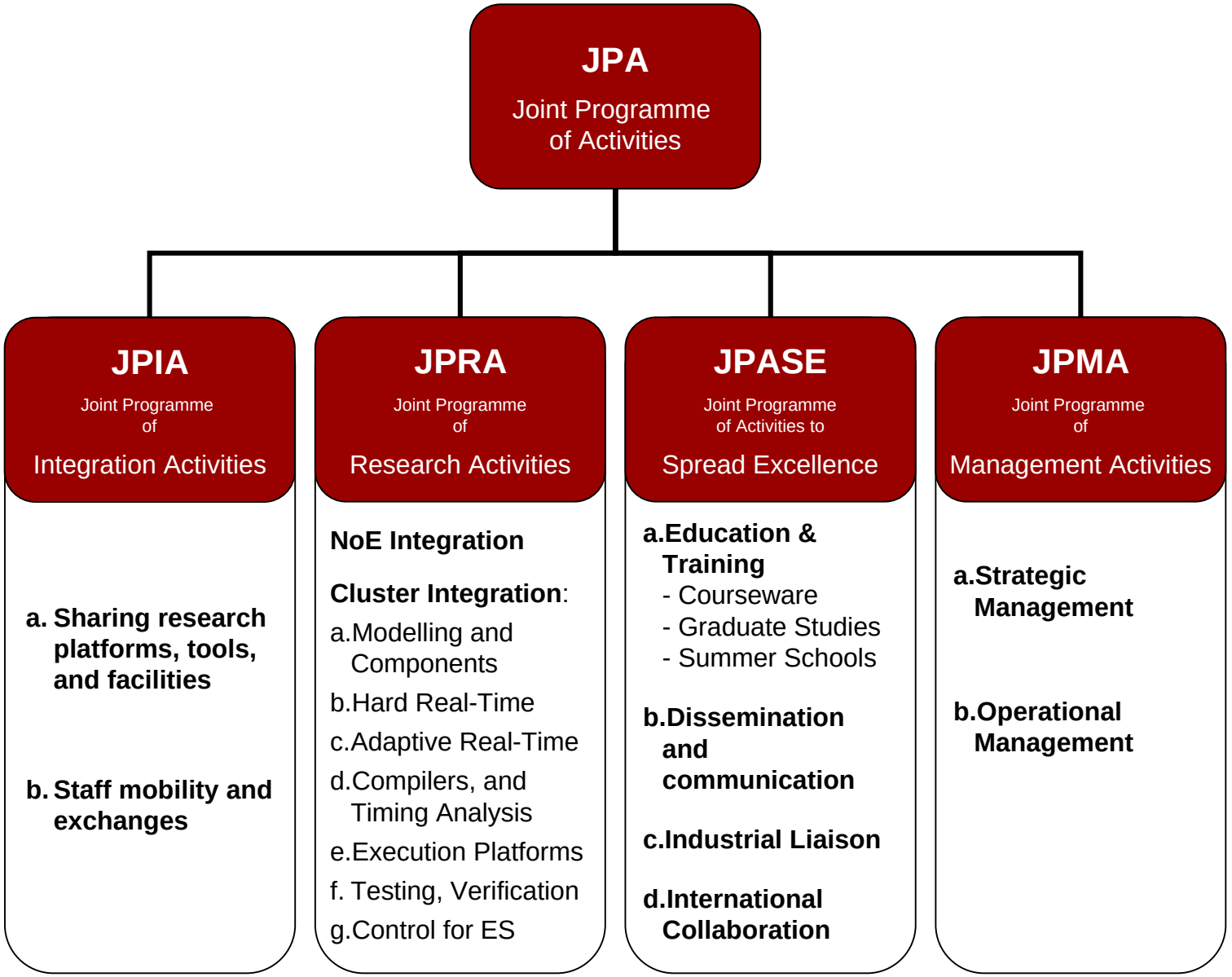
Reinhard Wilhelm - Saarland
Rainer Leupers - Aachen
~~Christian Bertin – ST Microelectronics~~
Christian Ferdinand – AbsInt
Peter Marwedel - Dortmund
Puschner, Krall – TU Vienna
Bjorn Lisper –Maalardalen
Guillem Bernat – University of York

Execution Platforms

Lothar Thiele – ETH Zurich
Jan Madsen –DTU (TU Denmark)
Luca Benini – UoB
Petru Eles – ESLAB/Liu
Rolf Ernst – UBR
~~Martin Rem – Eindhoven~~
Josef Hooman - Eindhoven

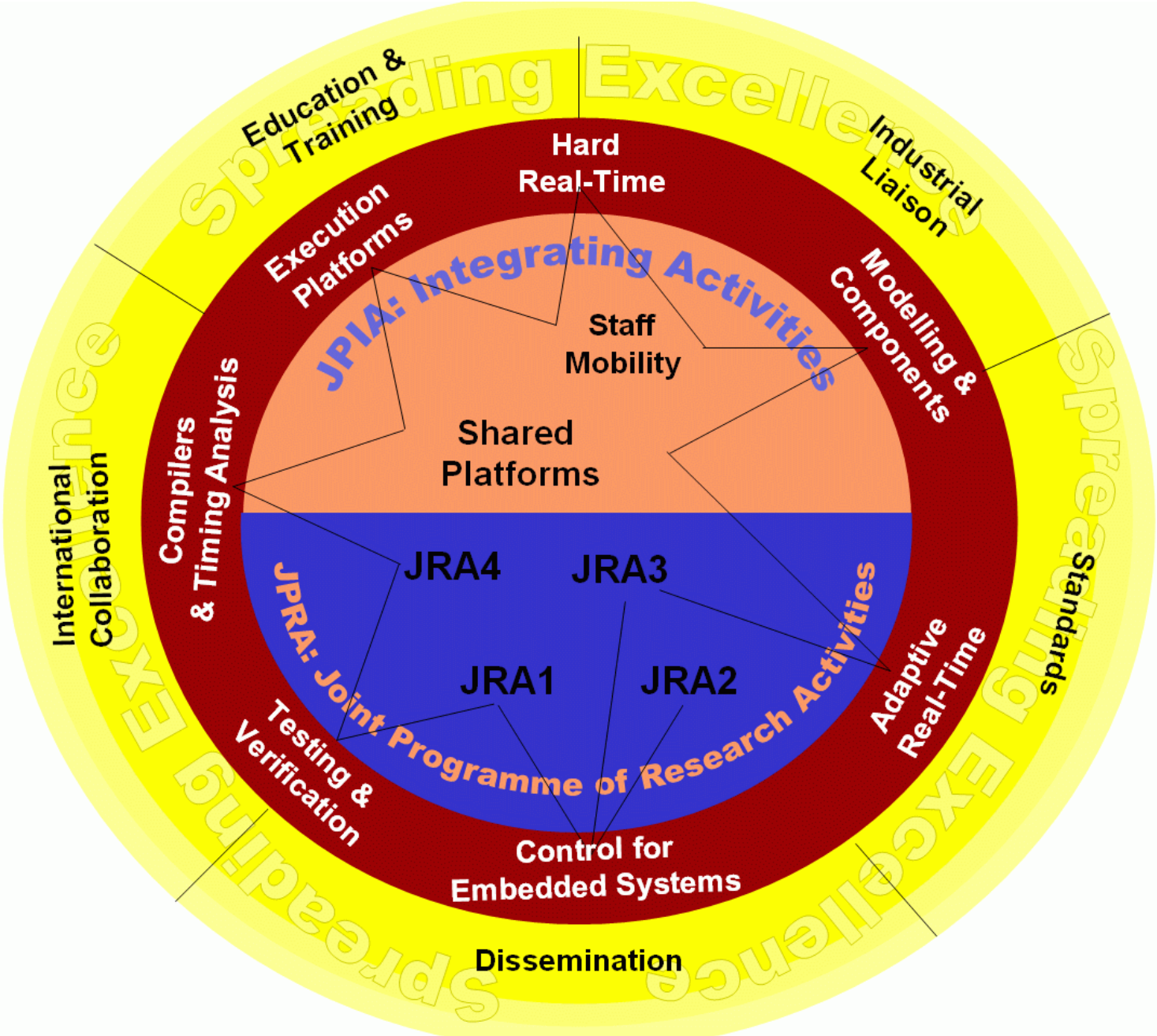
ARTIST2

Joint Programme of Activities



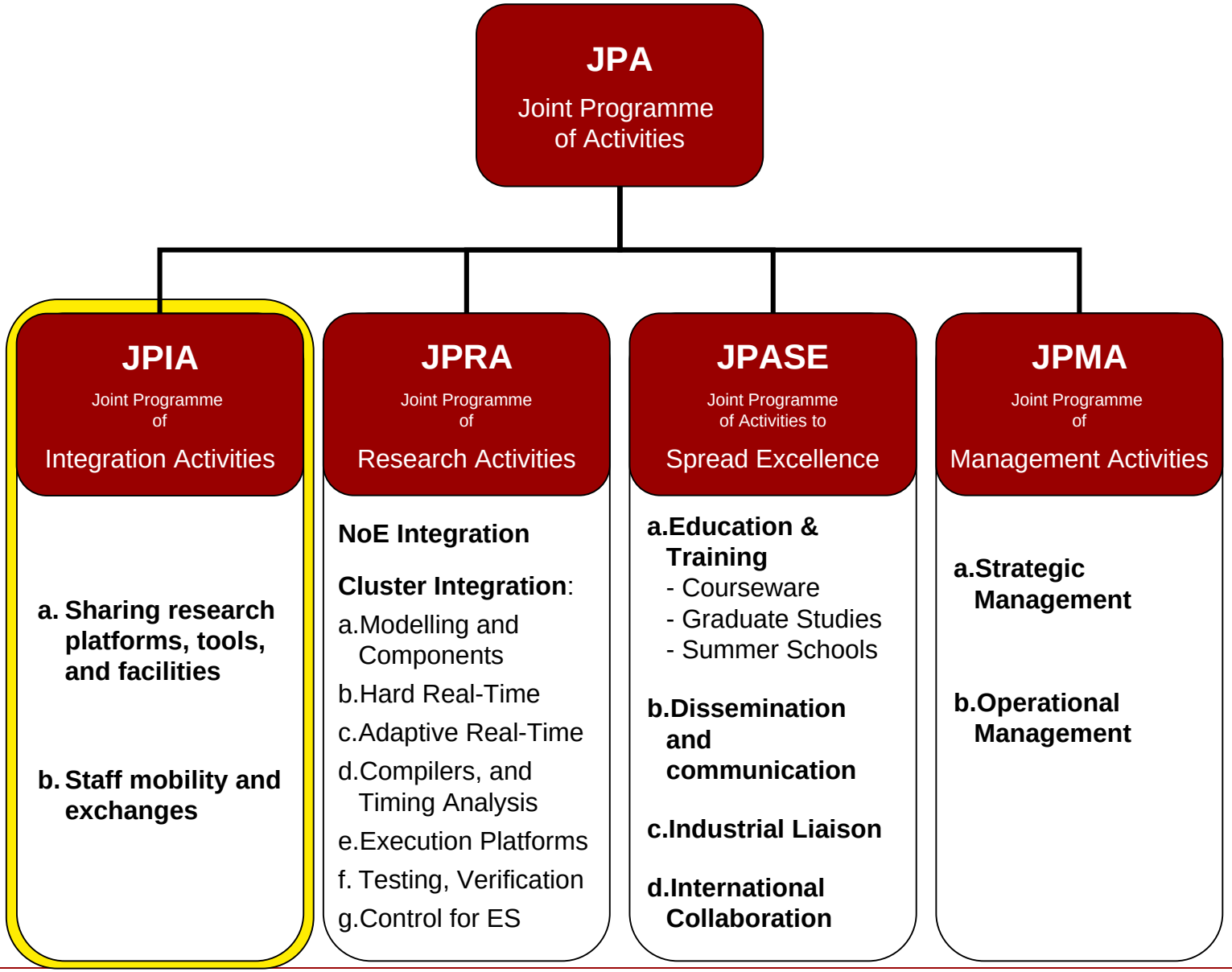
Artist2 Structure

Artist2 Structure



ARTIST2

Joint Programme of Activities

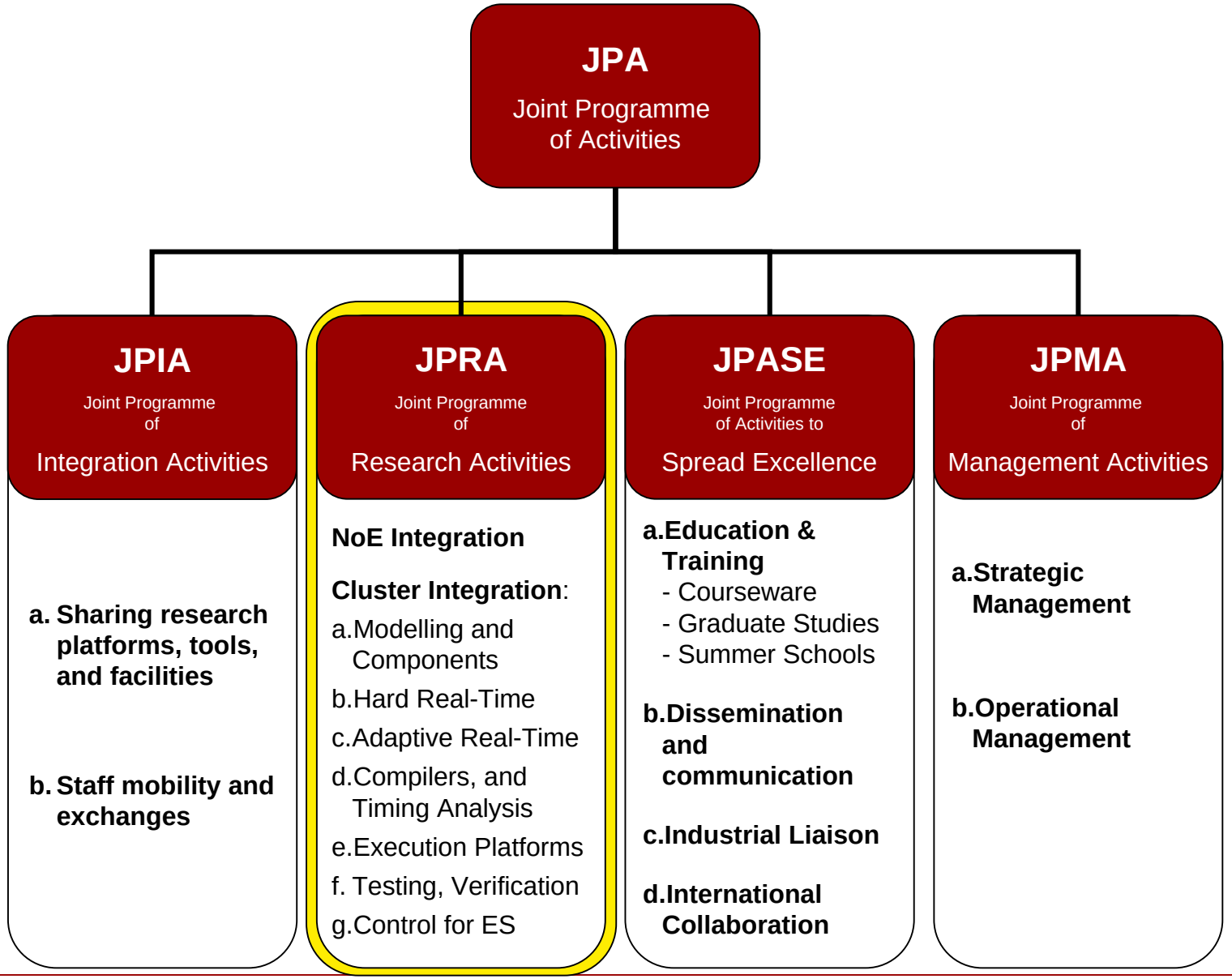


Sharing Research Platforms, Tools, and Facilities

Cluster	*JPIA - Platform*
Modelling and Components	Platform for Component Modelling and Verification *This platform will support translations to semantic kernel languages to leverage associated powerful analysis tools, in particular those from the "Testing and Verification" cluster.*
Adaptive Real-Time	A common infrastructure for adaptive Real-time Systems *Promote extension of operating systems (eg: RT-POSIX and OSEK) and network protocols to support emerging real-time applications having a high degree of complexity and operating in dynamic environments.*
Testing and Verification	Testing and Verification Platform for Embedded Systems *Will also make available new powerful analysis tools developed within the network, in particular those from the related Joint Research Activities ("Testing and Verification", "Verification, Testing and Control" and "Verification of Security Properties").*
Control for Embedded Systems	Design Tools for Embedded Control *Develop a suite of tools, for developing resource-constrained embedded control systems* - taking *control, computing, and communication aspects into account.*
Compilers and Timing Analysis	Timing - Analysis Platform *Combine the best existing Timing-Analysis tools in a standard tool architecture with well-defined textual interfaces, to preserve the existing lead of European Research and Industry in this important sector.*
	Compilers Platform *Provide world-class code-synthesis and compiler tools for the generation of efficient machine code. Integration of existing compiler-generation approaches allowing compilers for new architectures to be built quickly, efficiently and reliably.*
Execution Platforms	System Modelling Infrastructure *Integrate ongoing research efforts on infrastructure modelling. This would replace prototyping hardware to reduce the cost and time required for designing embedded systems.*

ARTIST2

Joint Programme of Activities



NoE Integration

Clusters	*JPRA – NoE Integration*
❖Hard Real-Time ❖Adaptive Real-Time ❖Control for Embedded Systems	Semantic Framework for Hard Real-Time Design Flow *Develop a mathematically sound framework, supporting system modelling, to incorporate the underlying models of computation and communication of different design tools. It should be effective and rich enough to provide formal analyses, algorithms, and support methods to deal with heterogeneity.*
❖Hard Real-time ❖Adaptive Real-time ❖Execution Platforms	Merging the Event-triggered and Time-triggered Paradigms *Fundamental work on merging two of the main paradigms in synchronous real-time systems design. Strong impacts on distributed embedded systems and network on chip applications.*
❖Control for Embedded Systems ❖Hard Real-Time ❖Adaptive Real-Time	Adaptive Real-time, HRT and Control *Integrate research among control and real-time teams on different computational models for embedded control systems and the use of control techniques to provide flexibility in embedded systems.*
❖Adaptive Real-Time ❖Modelling and Components	QoS aware Components *Develop holistic frameworks and models for QoS management to combine features of component models, component frameworks, middleware infrastructure, OS and Kernel support, and networking.*
❖Execution Platforms ❖Compilers and Timing Analysis	Resource-aware Design *Provide a viable path for resource-aware software and hardware development.*

Cluster Integration (1/2)

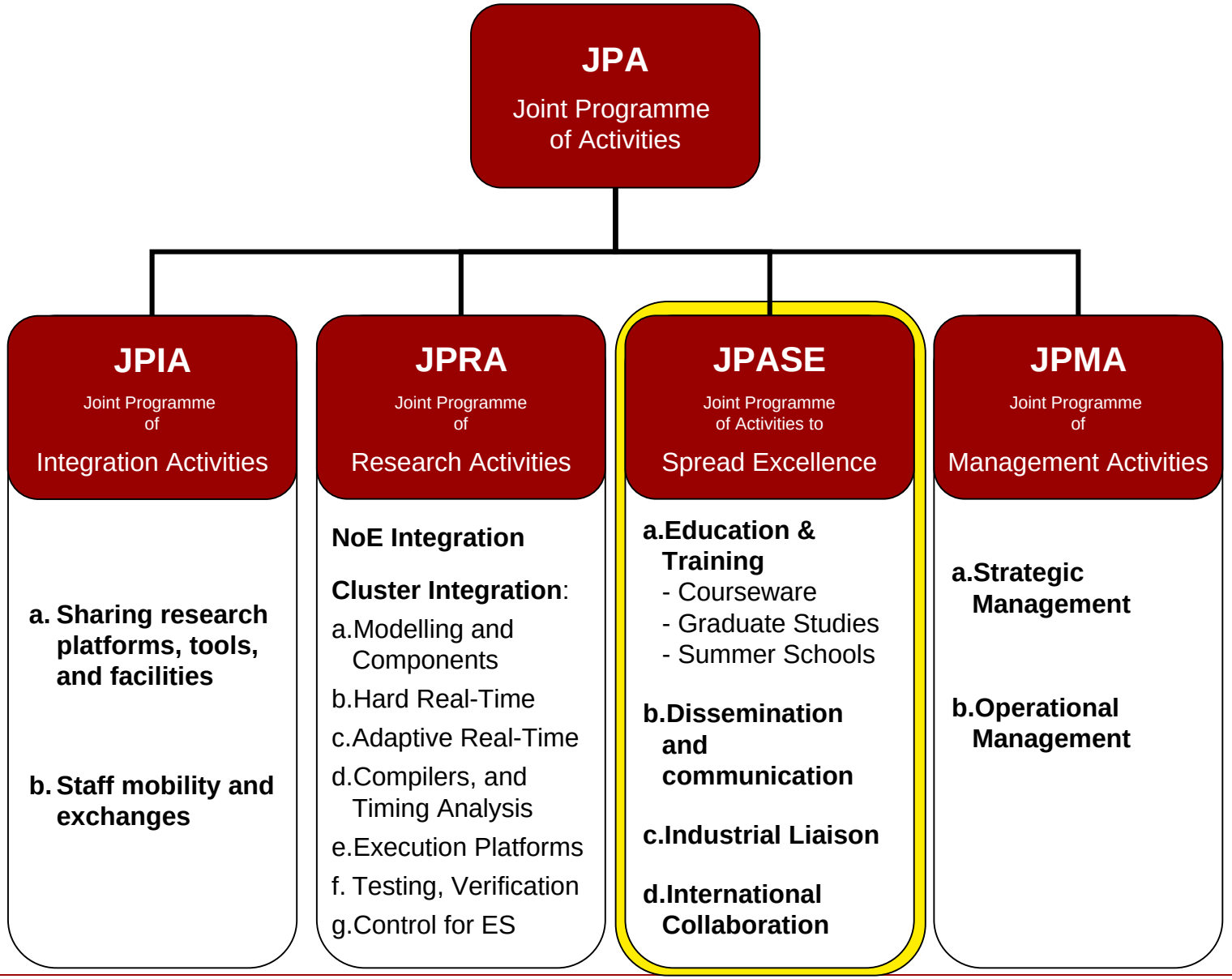
Cluster	*JPRA-Cluster Integration*
Modelling and Components	**Component Modelling and Composition** Development of a general framework for component-based engineering of complex heterogeneous systems.
	Development of UML for Real-time Embedded Systems Development of a general framework for component-based engineering of complex heterogeneous systems.
Hard Real-Time	**Diagnosis in Distributed Hard Real-time Systems** integrated approach to diagnosis of distributed real-time systems, in particular with respect to transient anomalies.
Adaptive Real-Time	**Flexible Scheduling Technologies** Develop a real-time scheduling framework capable of handling different real-time requirements in the same system – to be used in next-generation OS kernels for adaptive QoS control of dynamic behavior.
	Adaptive Resource Management for Consumer Electronics Higher efficiency in managing extra-functional properties of consumer electronics applications (power, bandwidth, memory security, functionality, etc.)

Cluster Integration (2/2)

Cluster	*JPRA-Cluster Integration*
Compilers and Timing Analysis	**Architecture-aware compilation** Provide a unified architecture-aware code-synthesis and compiler methodology.
Execution Platforms	**Communication-centric systems** Use formal methods to increase design productivity and quality. **Design for low power** Address low-power issues across several layers of abstraction
Control for Embedded Systems	**Control in real-time computing** Applying control methods for handling uncertainty and to provide flexibility in real time applications. **Real-time techniques in control system implementations** Advances in real-time control applications
Testing and Verification	**Quantitative Testing and Verification** Advances in verification and testing methodologies **Verification of Security Properties** Develop the basic technology needed to certify security applications at levels EAL6, and EAL7, from the Common Criteria.

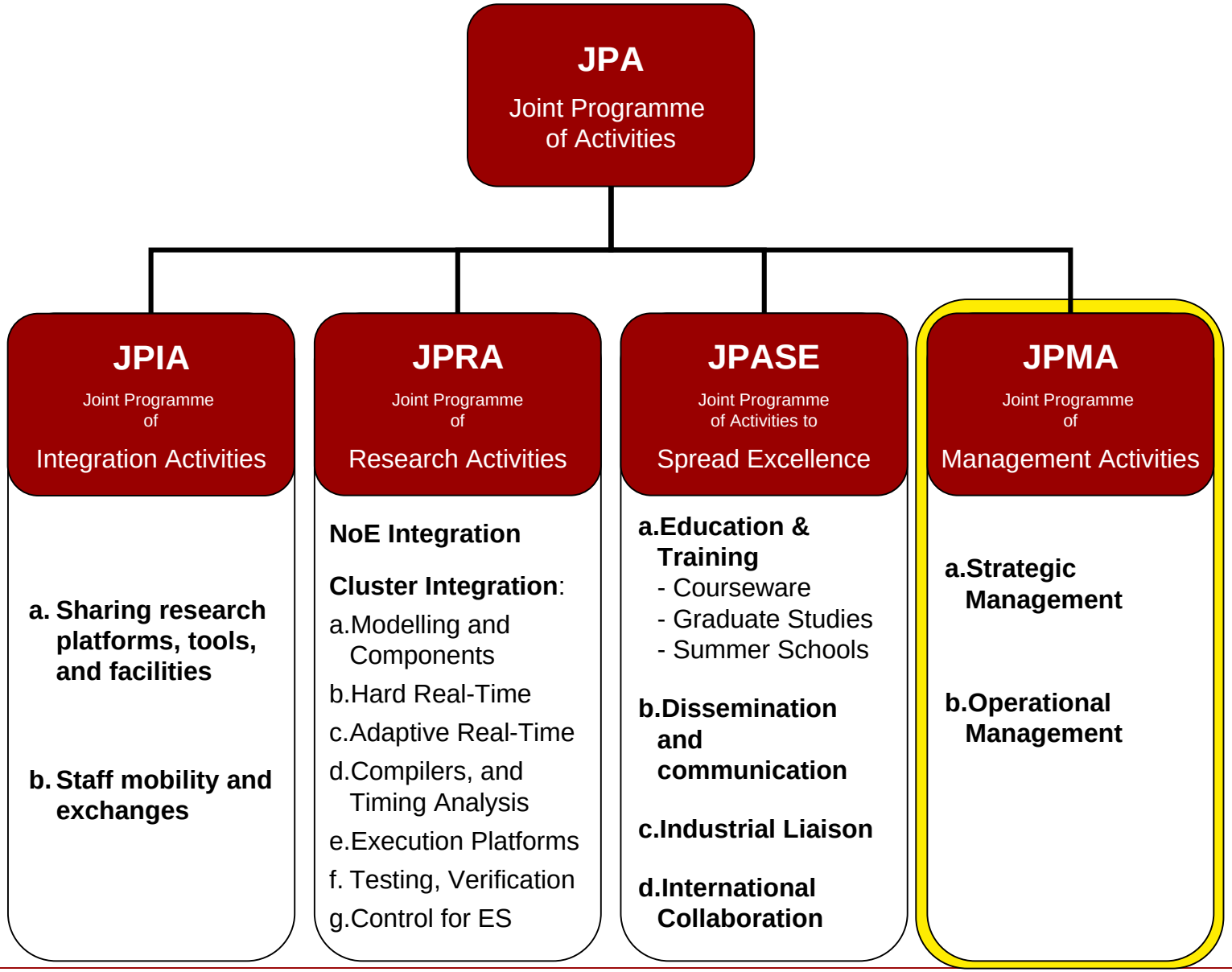
ARTIST2

Joint Programme of Activities

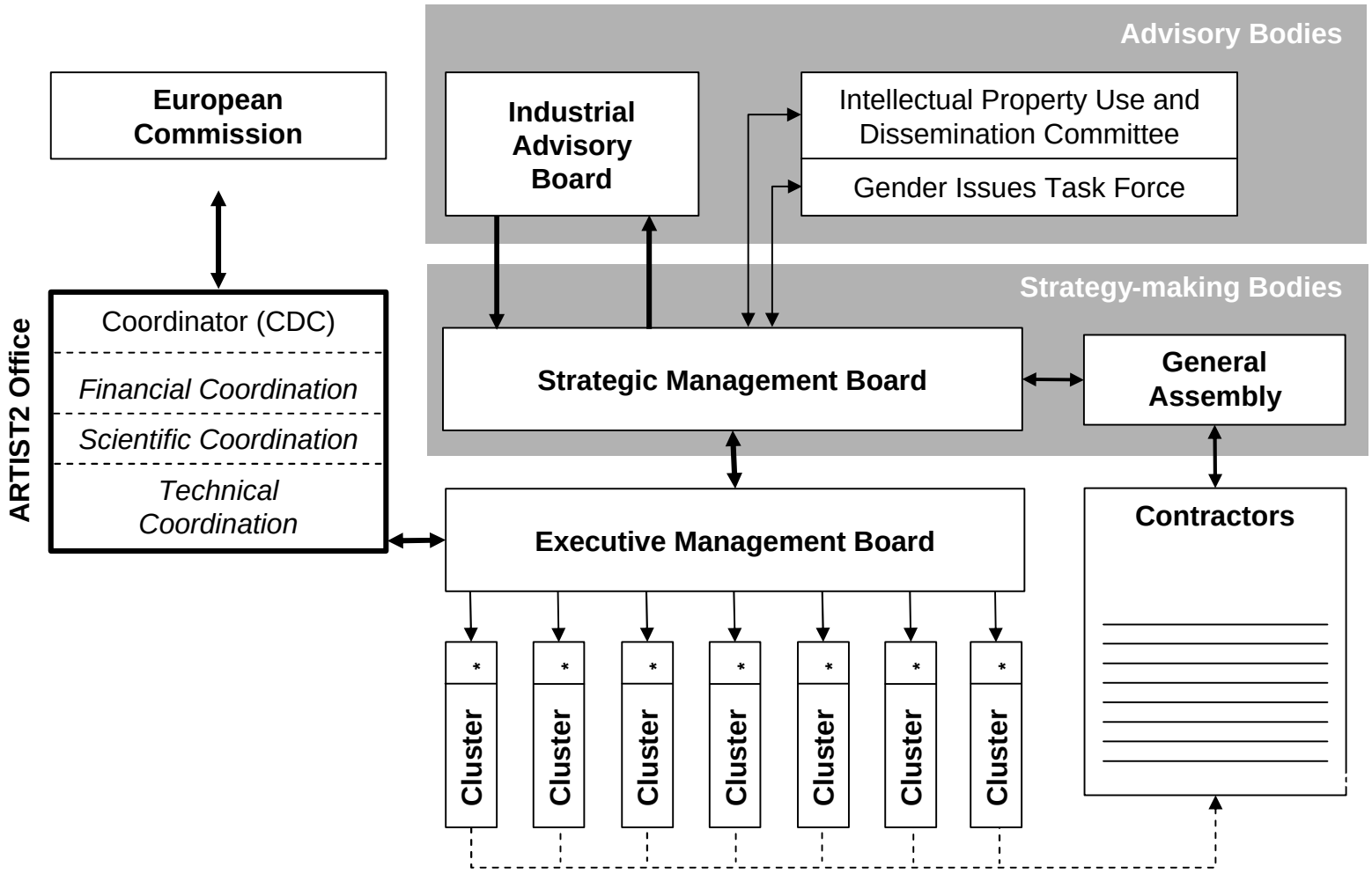


ARTIST2

Joint Programme of Activities



Management Structure



Strategy Making Bodies

General Assembly

The General Assembly is composed of one institutional representative (or its substitute) per Contractor and duly authorised for this purpose. It is chaired by the Scientific Manager.

The General Assembly is convened at the beginning of the Network of Excellence and meets physically at least once a year.

It discusses and ratifies proposals from the Strategic Management Board for modifying the Consortium, the Consortium Agreement, or any other decision requiring approval and signature by all the core partners.

Strategic Management Board

The Strategic Management Board leads the scientific policy of the NoE.

The Strategic Management Board is chaired by the Scientific Manager, assisted by the Technical Manager. Initially, it has 14 members, but the Scientific Manager can propose additional members as required.

The Coordinator is member “ex officio” of the Strategic Management Board with voice but no vote.

Its members are elected between all Contractors by the General Assembly every two years. The renewal does not include the Scientific and Technical Managers and the Coordinator.

Decisions such as bringing in new partners, or ending membership for one or more existing core partners, must be ratified by the General Assembly.

Strategic Management Board

JPMA – Strategic Management	
Policy Objective	ARTIST2 Strategic and Scientific Management
Members	Albert Benveniste (INRIA, France) Giorgio Buttazzo (University of Pavia, Italy) Alberto Sangiovanni (PARADES, Italy) Alan Burns (University of York, UK) Bengt Jonsson (Uppsala University, Sweden) Kim Larsen (Aalborg, Denmark) Ed Brinksma (Twente, Netherlands) Karl-Erik Årzén (Lund University, Sweden) Reinhard Wilhelm (Saarland University, Germany) Rainer Leupers (Aachen, Germany) Lothar Thiele (ETHZ, Switzerland) Luca Benini (Bologna, Italy) Claude Oytana (CDC, France)
Chairman	Joseph Sifakis (VERIMAG, ARTIST2 Scientific Manager), Assisted by: Bruno Bouyssounouse (VERIMAG, ARTIST2 Technical Manager)
Scope of the activity	The activity is piloted by the Strategic Management Board, in close interaction with the General Assembly.

Operational Management

Executive Management Board

It implements the decisions of the Strategic Management Board, and supervises the day-to-day management for implementing the JPA.

Composed of one representative from each cluster, amongst the Cluster Leaders, and a representative of the Coordinator – who attends, with no voting rights.

Chaired by the Scientific Manager, assisted by the Technical Manager.

Cluster Leaders

Responsible for the overall coordination of the activities led by their cluster. A cluster functions as a virtual team, with a degree of autonomy for defining its internal meetings and day to day management.

Monitor the day-to-day JPRA activities driven by the cluster, and report to the ARTIST2 Executive Management Board as a whole.

Executive Management Board

JPMA – Operational Management	
Policy Objective	The Executive Management Board is composed of one Leader from each Cluster, the Scientific and Technical Managers and of the Coordinator – who attends, with no voting rights. It is chaired by the Scientific Manager, assisted by the Technical Manager. It meets on roughly a monthly basis – either in person or via phone conference. It implements the decisions of the Strategic Management Board, and supervises the day-to-day management for implementing the JPA.
Members of the Executive Management Board	Karl-Erik Årzén, “Control for Embedded Systems” Albert Benveniste, “Hard Real-Time” Kim Larsen, “Testing and Verification” Giorgio Buttazzo, “Adaptive Real-Time” Bengt Jonsson, “Modelling and Components” Reinhard Wilhelm, “Compilers and Timing Analysis” Joseph Sifakis, VERIMAG, Scientific Manager Lothar Thiele, “Execution Platforms” Claude Oytana, CDC, France
Members of the ARTIST2 Office	Bruno Bouyssounouse, VERIMAG, Technical Manager Joseph Sifakis, VERIMAG, Scientific Manager Claude Oytana, Caisse des Dépots et Consignations
Scope of the activity	The activity is piloted by the Executive Management Board, in close interaction with the ARTIST2 Office.

Operational Management

ARTIST2 Office

Financial Management (Caisse des Dépots et Consignations)

- *Receives EC payments, dispatches funds.*
- *Negotiates contracts, agreement, and annual amendments. Ensures signatures.*

Technical Management (UJF/Verimag)

- *Checks the milestones, work progress, deliverables, consumption against the planned schedule*
- *Organises meetings to prepare and finalize reports, internal audits and submits deliverables and schedules to the European Commission.*
- *Organizes the information flow throughout the consortium*

Scientific Management (UJF/Verimag)

- *Responsible for implementing the scientific policy*
- *Reports to the Executive Management Board, and is especially in charge of informing this body of any eventual modifications in manpower, or resource consumption and planning compared to the original contract, so that the Executive Management Board may take corrective actions in a timely fashion.*

Affiliated Academic Partners

Name	Key researchers
RWTH Aachen	Stefan Kowalewski
University of the Balearic Islands	Julián Proenza
Masaryk University Brno	Prof. Lubos Brim
ENST – Distributed Real-Time Embedded Systems Group	Laurent Pautet
Politecnico di Milano	Prof. Donatella Sciuto
Royal Institute of Technology (KTH)	Prof. Axel Jantsch
Leiden University	Prof. Dr. Ed F. Deprettere
University of Nijmegen	Dr.ir. G.J. Tretmans
Politecnico di Torino	Prof. Luciano Lavagno
Universitat Politècnica de Catalunya	Dr. Pau Martí Colom
University of Catania	Prof. Lucia Lo Bello
EPFL (Swiss Federal Institute of Technology)	Prof. Thomas A. Henzinger
IMEC	Dr. Francky Catthour
IRISA/INRIA	Dr. Isabelle Puaut
Polytechnic Institute of Porto	Prof. Eduardo Tovar
Katholieke Universiteit Leuven (K.U. Leuven)	Prof. Pierre Verbaeten
Katholieke Universiteit Leuven (K.U. Leuven)	Prof. Geert DECONINCK
LIAFA - Université Paris 7 & CNRS UMR 7089	Prof. Ahmed Bouajjani
Timisoara - Institute e-Austria Timisoara	Dr. Marius Minea

Affiliated Industrial Partners

Name	Key persons
ABB Automation Technology	Göran Arinder
ABB Automation Technology Products AB/ Robotics	Christer Norström
Airbus	Francois Pilarski
DaimlerChrysler AG	Thomas Thurner
DaimlerChrysler	Matthias Grochtmann
Electricité de France (EDF)	Alain Ourghanlian
Ericsson Mobile Platforms AB	Johan Eker
Hispano Suiza	Philippe Baufreton
Honeywell Prague Laboratory	Vladimir Havlena
Israel Aircraft Industries	Dr. Michael Winokur
Nokia Denmark A/S	Peter Mårtensson
Siemens Mobile Phones A/S	Sven Holme Sørensen
STMicroelectronics	Roberto Zafalon
Thalès	Dominique Potier
Volkswagen AG	Fabian Wolf
Volvo Car Corporation	Jakob Axelsson
Volvo Technology Corporation	Magnus Hellring

Affiliated SME Partners

Name	Key persons
ACE Associated Compiler Experts bv	Hans van Someren
ARTiSAN Software	Alan Moore
BullDAST s.r.l.	Dr. Monica Donno
dSPACE Gmbh	Joachim Stroop
Enea Embedded Technology	Jan Lindblad
Esterel Technologies	Bernard Dion
Evidence Srl	Paolo Gai
IAR Systems AB	Carl von Platen
LifTech	António Garrido
Micro I/O Serviços de Electrónica Lda	Fernando Santos
Space Systems Finland Ltd.	Dr. Niklas Holsti
TNI-Valiosys	Jean-Luc Lambert

Budget Distribution – First 12 months

CDC	56875	**Lund**	46312,5
UJF/Verimag	135167,5	**Malardalen**	48961,25
Aachen	48197,5	**OFFIS**	18135
Aalborg	45662,5	**PARADES**	27365
Absint	24050	**Pavia**	69192,5
Aveiro	20361,25	**Madrid**	37521,25
Cantabria	16412,5	**Saarland**	61360
CEA	43777,5	**ST**	15925
CFV	19337,5	**Eindhoven**	16250
Czech	34937,5	**Vienna**	52520
Dortmund	31248,75	**TUBS**	36625
DTU	39750	**Twente**	25837,5
ETHZ	30500	**Bologna**	39750
FTRD	18102,5	**Uppsala**	79868,75
INRIA	66657,5	**UPVLC**	46312,5
KTH	46312,5	**York**	20637,5
Linkoping	54475	**Porto**	18898,75
CNRS	20670	**EPFL**	35295

Budget Distribution by Cluster

Components	HRT	ART	Compilers TA	Exec Platforms	Control	T&V	Non-Cluster
11,5%	10,7%	13,7%	14,3%	13,7%	11,5%	11,5%	13,0%

Non-Cluster : 7% Management + 6% Spreading Excellence

An additional 6% Spreading Excellence controlled by the clusters

Key Points

- Despite a relatively low level of funding, and heavy administrative overhead there is good basis for making headway
- Focus on the essential - the implementation of the workprogramme : workplan, role and contribution of partners, coordination to achieve valuable results.
- Reporting needs to be improved – focus on integration – provide evidence about progress (significant facts such as joint publications, technical results, transfer)
- Decentralised management of the clusters - strong coordination
- Simplify as much as possible managerial tasks while respecting administrative rules and contractual obligations

13:30 ***Management Activities***

- **ARTIST2 Management Structure**
  Joseph Sifakis (VERIMAG)
- Discussion

14:30 ***Components and Modelling Cluster***

- **Achievements and Perspectives**
  Overall Aims and Achievements + Future Evolution: 18-month Workprogramme
  Cluster leader: Bengt Jonsson (UPPSALA)
- **Component Modelling and Composition**
  Activity leader: Bengt Jonsson (Uppsala)
- **Development of UML for Real-time Embedded Systems**
  Activity leader: Francois Terrier (CEA)
- **Platform: Component Modelling and Verification**
  Actvity leader: Susanne Graf (VERIMAG)
- Discussion

15:30 break *(change venue)*

15:45 ***Hard Real-Time Cluster***

- **Achievements and Perspectives**
  Overall Aims and Achievements + Future Evolution: 18-month Workprogramme
  Cluster leader: Albert Benveniste (INRIA)
- **Diagnosis in Distributed Hard Real-time Systems**
  Activity leaders: Hermann Kopetz, Philipp Peti (TU Vienna)
- **NoE Integration: Semantic Framework for Hard Real-Time Design Flow**
  Activity leaders: Albert Benveniste (INRIA), Alberto Sangiovanni-Vincentelli (PARADES)
- **NoE Integration: Merging the Event-triggered and Time-triggered Paradigms**
  Activity leaders: Paul Caspi (VERIMAG), Nicolas Halbwachs (VERIMAG)
- Discussion

16:45 break

17:15 ***Adaptive Real-Time Cluster***

- **Achievements and Perspectives**
  Overall Aims and Achievements + Future Evolution: 18-month Workprogramme
  Cluster leader: Giorgio Buttazzo (PAVIA)
- **Flexible Scheduling Technologies**
  Activity leader: Giorgio Buttazzo (Pavia)
- **Adaptive Resource Management for Consumer Electronics**
  Activity leader: Gerhard Fohler (Mälardalen University)
- **NoE Integration: QoS aware Components**
  Activity leader: Alejandro Alonso (UP Madrid)
- **Platform: A Common Infrastructure for Adaptive Real-time Systems**
  Activity leader: Giorgio Buttazzo (Pavia)
- Discussion

18:00 *closing*

19:00 *cocktail dinner*

Tuesday October 4th

8:30 ***Compilers and Timing Analysis Cluster***

- **Achievements and Perspectives**
  - Overall Aims and Achievements
  - Future Evolution: 18-month Workprogramme
  Cluster leader: Reinhard Wilhelm (Saarland)
- **Architecture-aware compilation**
  Actvity leader: Rainer Leupers (RWTH Aachen)
- **Platform: Timing-Analysis**
  Actvity leader: Reinhard Wilhelm (Saarland University)
- **Platform: Compilers**
  Actvity leader: Rainer Leupers (RWTH Aachen)
- *Discussion*

9:30 ***Execution Platforms Cluster***

- **Achievements and Perspectives**
  - Overall Aims and Achievements
  - Future Evolution: 18-month Workprogramme
  Cluster leader: Lothar Thiele (ETHZ)
- **Communication-centric systems**
  Actvity leader: Rolf Ernst (TU Braunschweig)
- **Design for Low Power**
  Actvity leader: Luca Benini (University of Bologna)
- **NoE Integration: Resource-aware Design**
  Actvity leaders: Luca Benini (University of Bologna), Peter Marwedel (University of Dortmund)
- **Platform: System Modelling Infrastructure**
  Actvity leader: Jan Madsen (TU Denmark)
- Discussion

10:30 break

10:45 ***Control for Embedded Systems***

- **Achievements and Perspectives**
  - Overall Aims and Achievements
  - Future Evolution: 18-month Workprogramme
  Cluster leader: Karl-Erik Arzen (Lund)
- **Control in Real-time Computing**
  Actvity leader: Karl-Erik Årzén (Lund)
- **Real-time techniques in control system implementations**
  Actvity leader: Alfons Crespo (UPVLC)
- **NoE Integration: Adaptive Real-time, HRT and Control**
  Actvity leader: Karl-Erik Årzén (Lund University)
- **Platform: Design Tools for Embedded Control**
  Actvity leader: Karl-Erik Årzén (Lund University)
- *Discussion*

11:45 ***Coordinator (CDC) Presentation***

- *Jean-Noel Forget (CDC)*
- Discussion

12:20 *buffet lunch*

13:30 ***Testing and Verification***

- **Achievements and Perspectives**
  - Overall Aims and Achievements
  - Future Evolution: 18-month Workprogramme
  Cluster leader: Kim Larsen (Aalborg)
- **Cluster Integration: Quantitative Testing and Verification**
  Actvity leader: Ed Brinksma (University of Twente)
- **Cluster Integration: Verification of Security Properties**
  Actvity leader: Yassine Lakhnech (VERIMAG)
- **Platform: Testing and Verification Platform for Embedded Systems**
  Actvity leader: Kim Larsen (BRICS/Aalborg)
- *Discussion*

14:30 ***Joint Programme of Acitvities for Spreading Excellence (JPASE)***

- *Bruno Bouyssounouse (VERIMAG)*
- *Discussion*

15:00 ***18-Month Perspectives***

- *Discussion*

Parallel meetings:

16:00 - 18:00 **Reviewers' Meeting**

16:00 - 17:15 **General Assembly Meeting**

16:00 - 17:15 **Industrial Advisory Board Meeting**

17:15 - 17:30 break

17:30 -18:00 ***Industrial Advisory Board Feedback & Discussion***

18:00 ***Reviewers' Feedback & Discussion***

18:45 *closing*

19:30 ***Gala Dinner***
Chateau de la Commanderie
see the chartered buses for details

22:30/ 23:00 *Buses return to hotels*