

# *ARTIST2 – Year 1 Review*

*Grenoble, October 3rd-4th, 2005*

*Activity*

## Architecture Aware Compilation

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# Outline of the Presentation

## **Industrial Needs and Experience**

### **Year 1 Activities**

- Achievements & Ongoing Work
- Interaction and Building Excellence Between Partners
- Management Perspective

### **18 Month Perspective**

- Work planned for the next 18 months
- Significant events or achievements expected

# Industrial Needs and Experience

## ❖ ARTIST2 Interaction with Industry

- 3 out of 8 cluster partners are from industry (STM, ACE, Absint)
- Academic partners have tight industry cooperations beyond ARTIST2, e.g.
  - Aachen – CoWare
  - Saarbrücken – Absint
  - Dortmund – ICD
  - IMEC - Thales



## ❖ Industrial Needs

- Need for highest code quality in embedded SW development
- Support for special-purpose architectures (e.g. DSP, ASIP, reconfigurable, ...)
- Compiler technology must keep pace with processor architecture trends

## ❖ Possible Global Impacts of Research Results

- Embedded system design in many application areas, e.g. wireless communication and consumer electronics, is all about efficiency (MIPS/Watt)
- Advanced architecture-aware compilation permits full utilization of underlying HW platforms and avoids time-consuming assembly programming
- Increased design productivity and dependability
- Use of common compiler platform facilitates technology transfer

*Year 1 activities*

# Achievements & Ongoing Work

## ❖ Brief State of the Art

- Success stories: “**DSP-aware**” and “**VLIW-aware**” compilation
- Currently few support for **application specific + reconfigurable processor architectures, source-level optimizations, memory + power aware compilation** etc.

## ❖ Achievements in Year 1

- **Requirements analysis** for modern embedded architectures
- Formation of “**mini-clusters**” (2-3 partners) focusing on specific platform aspects
- Alpha versions of several **SW tools** available
- Common **compiler platform** taken into account
- Cooperation with **other ARTIST2 clusters**, e.g. Execution Platforms

## ❖ Ongoing Work

- Formation of new, and strengthening of existing **cooperations**, e.g.
  - *Aachen – Dortmund: SIMD code generation*
  - *Dortmund – IMEC: Memory aware source-level code optimization*
  - *ACE – STM: Reconfigurable architecture compilation*
  - *Absint – Dortmund: Memory aware WCET analysis*

*Year 1 activities*

# Interaction & Building Excellence

## ❖ Interaction Between Partners

- Get together **leading European R&D teams**
- Two **global synchronization** meetings (3rd scheduled for Nov 2005)
- Numerous **“mini-cluster” level meetings** in year 1

## ❖ Building Excellence

- Leverage each other's results for **more efficient R&D**
- Involve industry partners for more efficient **results exploitation**
- Intensify contacts to **related research communities**
  - *E.g. compiler platform activities in HiPEAC Network of Excellence*
- **Teaching** activities
  - *E.g. common compiler course at ALARI (Aachen, Dortmund, ACE)*
  - *Embedded system design textbook (Dortmund)*
- **Conference** organization
  - *E.g. organization of SCOPES workshop series (Dortmund, Aachen)*

**SCOPES 2005****HiPEAC**  
COMPILED ARCHITECTUREUniversità  
della  
Svizzera  
italiana**ALaRI**Advanced Learning and Research Institute  
Education for leading-edge information technologies in  
Embedded Systems Design

*Year 1 activities*

# Management Perspectives

## ❖ What worked well

- Cluster **team structure** (core and affiliate) established quickly
- Good **academia/industry balance** avoids “blue-sky” research
- Cluster meetings permit **regular synchronization** and information exchange
- **“Mini-Cluster”** formation enables meaningful, effective day-to-day cooperations

## ❖ Difficulties encountered

- Some **late drop-outs** and no-shows (e.g. IAR)
- General: too much **bureaucratic overhead** (reporting/financials) for the level of NoE funding provided

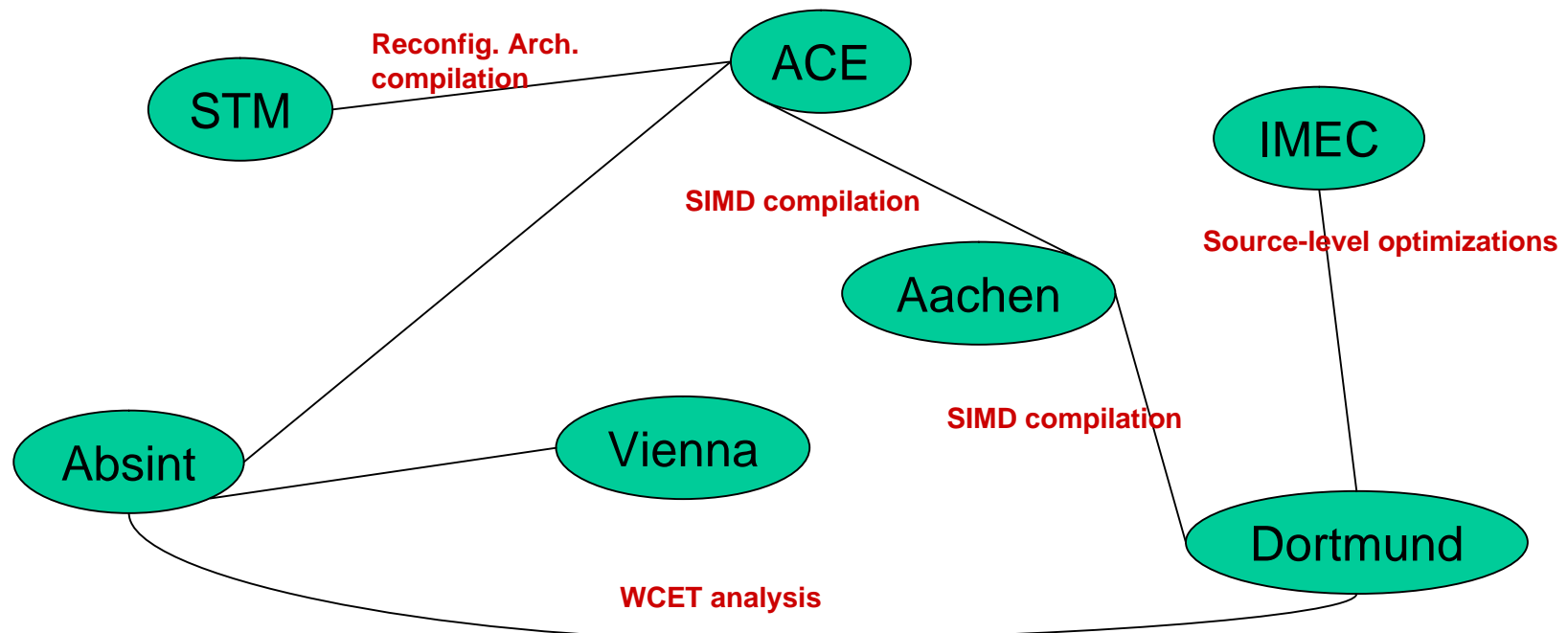
## ❖ Structural changes in the activity

- Look out for **more affiliate partners** with complementary research activities to cover broader spectrum, e.g. interest signaled by:
  - *J. Teich, U Erlangen, architecture exploration*

*18 Month Perspective*

# Work Planned for the next 18 months

- ❖ **Continuation of mini-cluster cooperations**
  - Retain loose coupling, yet a connected graph (see below)
- ❖ **Continuation of building excellence**
  - E.g. common compiler course at EPFL, Oct 6 (Aachen, Dortmund)
- ❖ **Review of potential new partners' activities**
- ❖ **Next global cluster meeting**
  - Nov 8, 2005 @ ACE, Amsterdam



*18 Month Perspective*

## Significant Events or Achievements Expected

### ❖ Refine/finish SW tool prototypes

- E.g. SIMD-aware code generation engines (Dortmund, Aachen), to be plugged into CoSy (ACE) and LISATek (Aachen) environments

### ❖ Work towards first joint publications

- Some are already underway

### ❖ Refine cluster structure

- Potential adding of new affiliate partners

### ❖ Strengthen inter-cluster cooperation, e.g.

- Aachen – Bologna: LISATek/MPARM compiler/simulator coupling
- Dortmund – Bologna: Memory-aware compilation/simulation