

# *ARTIST2 – Year 1 Review*

*Grenoble, October 3rd-4th, 2005*

*Cluster*

## Execution Platforms

*Activity leader : Lothar Thiele (ETHZ)*

# Outline of the Presentation

## **Description of the Area**

- Main Research Trends
- Industrial Applications

## **State of Integration in Europe**

- Interaction of the Cluster with other Communities
- Main Aims for Integration through Artist2

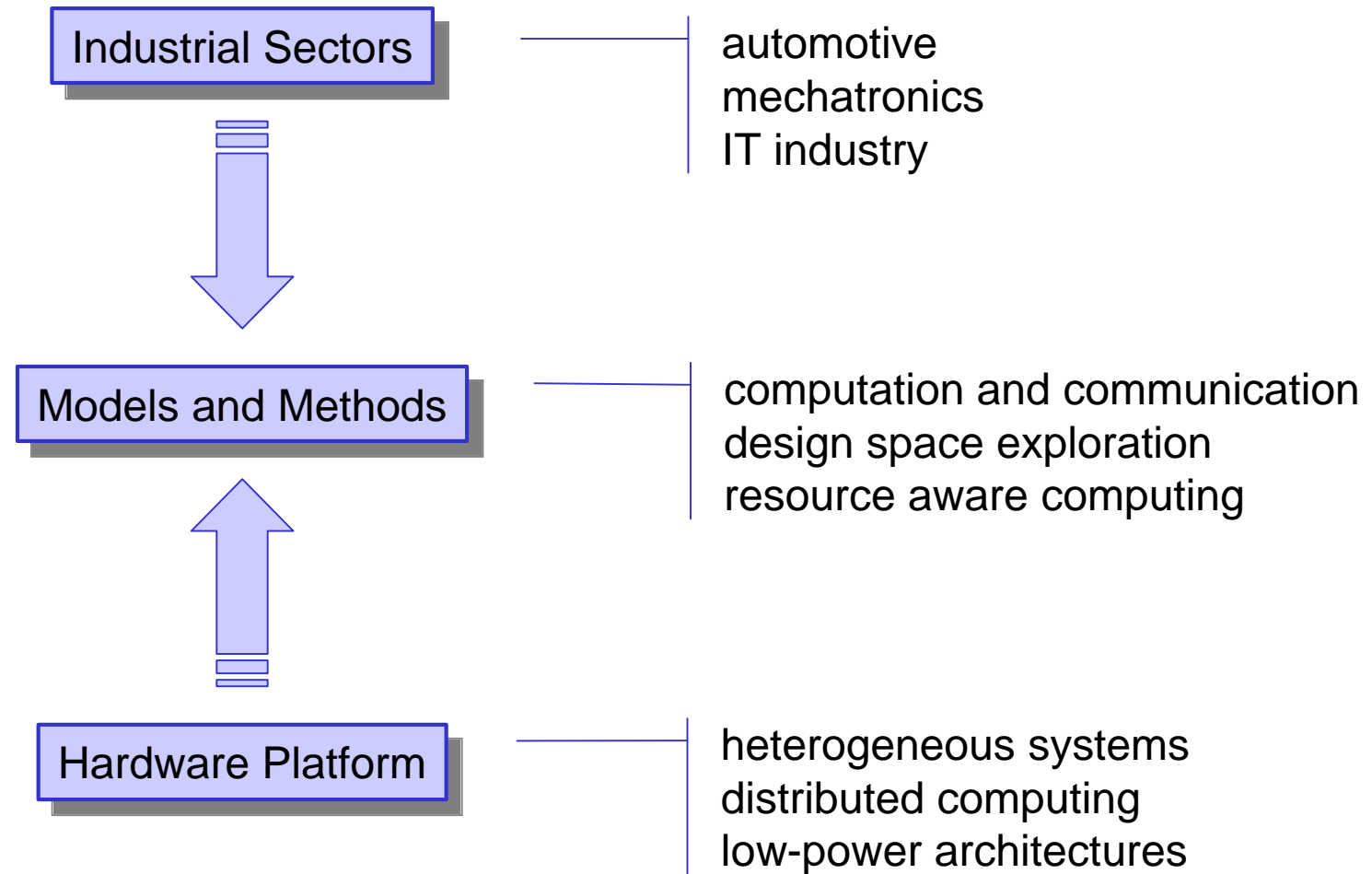
## **Presentation of the Cluster**

- Core and Affiliated Partners, Competencies and Roles
- Research Activities & Platform

## **Overall Aims and Achievements, Vision for the Cluster**

- Aims and Achievements
- Vision and Long-Term Goals
- 18 month work programme

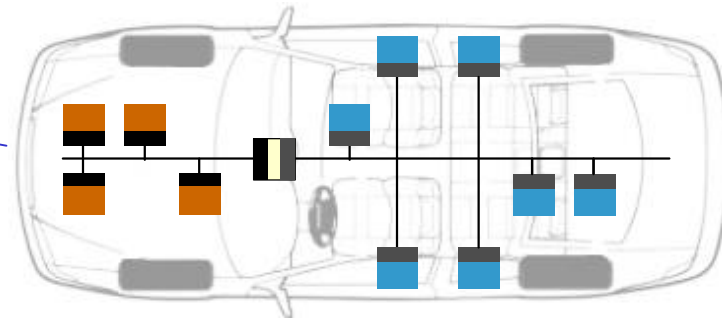
# Global Picture



# Industrial Sectors and Needs

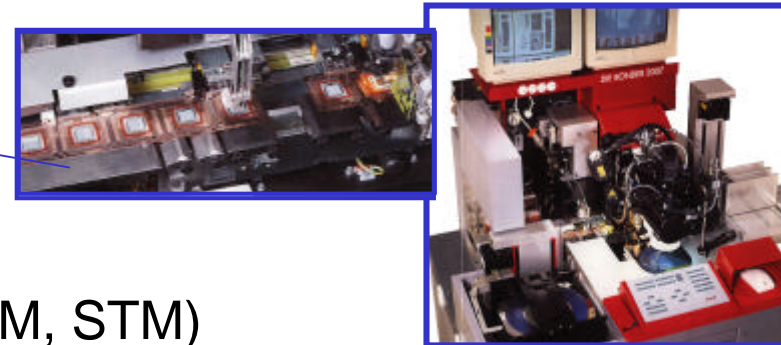
## ❖ Automotive (Volvo, Volkswagen)

increasingly distributed  
 complex integration



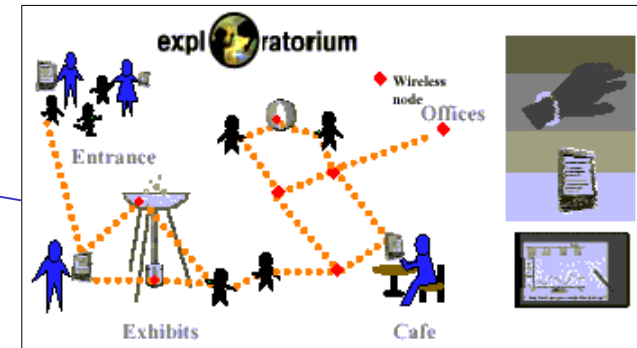
## ❖ Mechatronics (Océ, ASML)

increasingly networked  
 predictability



## ❖ IT Industry (Philips, Nokia, Ericsson, IBM, STM)

resource awareness  
 short product cycles  
 distributed operation



# Challenges

Resource Aware Computing

Communication Centric Systems

Predictability and Efficiency

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# Interaction with other Communities

## ❖ Hybrid Systems and Control

- There needs to be a link between control, algorithms/theory, appropriate models of computation and underlying execution platform.
- First attempts have been made, e.g. organizing HSCC05 (Hybrid Systems, Control and Computation Conference)

## ❖ (Hard) Real-Time Systems

- There is a need to consider the use of resources across several layers of abstraction, e.g. WCET, compiler, cooperating tasks, end-to-end analysis.
- Predictability and efficiency should be joined.

## ❖ System-on-Chip and Networks-on-Chip

- Higher layer concepts must be integrated into execution platforms.
- Still, it is not clear what kind of information should flow through layer interfaces and what appropriate models are.

# Collaboration with Industry

## ❖ Performance Analysis of Distributed Systems

- **VW**: currently introduction of integration process in series product development process; already used for contracting between Volkswagen and suppliers.
- Evaluation of tools and methods at **Bosch, Philips Research, Eindhoven, and Samsung, Seoul**.
- **Volvo**: Analysis and mapping of safety critical distributed applications.
- **VW**: cooperation in cache analysis
- **SymtaVision**: Performance Analysis

## ❖ Communication-Centric Systems

- **Nokia**: Asynchronous Low-Power Network-on-Chip
- **IBM, BridgeCo, NetModule**: HW and SW architectures for packet processing.
- **Ericsson**: Testing for Systems-On-Chip.
- **IO Technology**: Distributed wireless sensor networks for sow monitoring
- **Samsung**: Evaluation of Network-On-Chip Architecture.



# Collaboration with Industry

## ❖ Resource-Aware Computing

- **STM**: Energy-efficient mapping of application to MpSOC.
- **Bulldast**: Leakage power modeling and reduction.
- **Freescale semiconductors**: Software based dynamic power management for SoC platforms (wireless multimedia).
- **Coware**: Models and Tools for multi-processor platform.
- **ICD**: Infrastructure for Compiler Development

## ❖ Mechatronic Systems

- **Océ**: Distributed embedded real-time controllers of complex systems. Digital Printers are used as a driver.
- **ASML**: Test methodology, supported with processes and tools, for complex systems. Wafer scanners are investigated as case study.
- **Philips**: Conflict between networking, security and safety in medical systems.

## General Objectives

The cluster on execution platforms will consider

- ❖ the **hardware** architecture and **software** components in their **interaction**,
- ❖ investigate **models and methods** for accurate **estimation** of important properties (energy, timing),
- ❖ provide the designer with adequate support for **design space exploration** and **optimisation**.

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## **Presentation of the Cluster**

- Core and Affiliated Partners, Competencies and Roles
- Research Activities & Platform
- Spreading Excellence & Mobility

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# Presentation of the Cluster

*Core and Affiliated Partners*

*Competencies and Roles*

## Core Partners:

- Lothar Thiele (ETH Zurich)  
*Areas: Design Space Exploration, Performance Analysis*  
*Cluster leader*
- Jozef Hooman (Embedded System Institute)  
*Areas: Performance Modeling*
- Petru Eles (Linköping University)  
*Areas: Low Power Design, Scheduling*
- Luca Benini (University Bologna)  
*Areas: Low Power Design, Communication Centric Architectures*  
*Activity leader: Resource Aware Design, Low-Power Design*
- Jan Madsen (Technical University of Denmark)  
*Areas: Embedded Systems Design and Modeling*  
*Activity leader: System Modeling Infrastructure*
- Rolf Ernst (University Braunschweig)  
*Areas: Embedded System Design*  
*Activity leader: Communication Centric Design*

# Presentation of the Cluster

*Core and Affiliated Partners*

*Competencies and Roles*

## **Affiliated Partners:**

- **Industrial Partners:**

Magnus Hellring (Volvo), Roberto Zafalon (STM), Maria Cristina Avalle (BullDast), Fabian Wolf (Volkswagen), Kai Richter (SymtaVision), Dirk Ziegenbein (Bosch), Peter Martensson (Nokia)

- **Research Partners:**

Axel Jantsch (KTH), Giovanni De Micheli (EPF Lausanne), Donatella Sciuto (Politecnico di Milano), Ed Deprettere (U. Leiden), Eugenio Villar (Cantabria), Pablo Pedro Sanchez (Cantabria), Geert Deconinck (K.U. Leuven), Luciano Lavagno (Politecnico di Torino), Pablo Sanchez (KTH), Sharon Hu (University Notre Dame)

# Overview: Cluster-Owned Activities

## ❖ JPIA (Joint Program of Integrating Activities)

*Staff Mobility and Exchange (all)*

*System Modeling Infrastructure (Jan Madsen, Petru Eles, Luca Benini, Rolf Ernst, Nokia, STM)*

## ❖ JPRA (Joint Program of Research Activities)

### ➤ NoE Integration

*Resource-aware Design (Luca Benini, Petru Eles, Jan Madsen, Peter Marwedel, Reinhard Wilhelm, Rainer Leupers, STM, Bulldast)*

### ➤ Cluster Integration

*Communication-Centric Systems (Rolf Ernst, Lothar Thiele, Petru Eles, Luca Benini, Jan Madsen, VW, Volvo)*

*Design Low Power (Luca Benini, Petru Eles, Jan Madsen, Martin Rem, Bulldast)*

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## Aims and Achievements

- ❖ *All deliverables* provided in time.
- ❖ Global *Cluster Report* provided in time.
- ❖ *All goals* (and much more) have been *achieved* in the different activities:
  - See respective activity presentations.
- ❖ *Standards*
  - Participating in AUTOSAR Timing Model Standard
- ❖ *Meetings:*
  - Predictability and Efficiency (Cross-Cluster, Frankfurt)
  - Cluster Meeting Execution Platforms (Zurich)
  - HSCC 05 (Computation and Control, Zurich)



# Aims and Achievements

## ❖ *Raising Public Awareness*

- Keynote at MpSoC
- Presentation at Intel Academic Forum
- Symta/S presentation at Embedded World
- ARTIST results presented at Bits&Chips Embedded Conference
- DATE 2005 Workshop on System Modeling Infrastructure
- Invited Keynote Presentation at FORMATS 2005

## Changes: Cluster-Owned Activities

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#### ➤ NoE Integration

*Resource-aware Design (Luca Benini, Petru Eles, Jan Madsen, **Peter Marwedel**, Reinhard Wilhelm, Rainer Leupers, **Lothar Thiele**, STM, Bulldast)*

#### ➤ Cluster Integration

*Communication-Centric Systems (Rolf Ernst, Lothar Thiele, Petru Eles, Luca Benini, Jan Madsen, **Jozef Hooman**, VW, Volvo, **SymtaVision**)*

*Design Low Power (Luca Benini, Petru Eles, Jan Madsen, Martin Rem, Bulldast, **IMEC**, **Freescale**)*

**Add Application Focus on Sensor Networks**

## Common Publications

- ❖ Lothar Thiele, Reinhard Wilhelm: Design for Timing Predictability. Dagstuhl Online, 2004.
- ❖ Lothar Thiele, Reinhard Wilhelm: Design for Timing Predictability. Journal on Real Time Systems, 2004.
- ❖ S.Mahadevan, F. Angiolini, M. Storgaard, R. G. Olsen, J. Sparsø, and J. Madsen. A network traffic generator model for fast network-on-chip simulation. In Proceedings of Design, Automation and Testing in Europe Conference 2005 (DATE05)
- ❖ F. Angiolini, S. Mahadevan, J. Madsen, L. Benini, and J. Sparsø. Realistically rendering soc traffic patterns with interrupt awareness. In IFIP International Conference on Very Large Scale Integration (VLSI-SoC), September 2005.
- ❖ Ernesto Wandeler, Lothar Thiele, Marcel Verhoef, Paul Lieverse: System Architecture Evaluation Using Modular Performance Analysis - A Case Study. Paphos, Cyprus, October, 2004. Appears in an extended form in STTT Journal.
- ❖ Paul Pop, Petru Eles, Zebo Peng, Viacheslav Izosimov, Magnus Hellring, Olof Bridal: Design Optimization of Multi-Cluster Embedded Systems for Real-Time Applications. I Design, Automation and Test in Europe (DATE 2004).
- ❖ M. Loghi, F. Angiolini, D. Bertozzi, L. Benini, R. Zafalon, "Analyzing on-chip communication in a MPSoC environment", IEEE/ACM Design, Automation and Test in Europe, Paris, France, Feb 2004.
- ❖ Jan Staschulat, Rolf Ernst, Andreas Schulze, Fabian Wolf. Context Sensitive Performance Analysis of Automotive Applications. In Designer's Forum at Design, Automation and Test in Europe (DATE), 2005.
- ❖ Bren C. Mochocki, Xiaobo S. Hu, Razvan Racu, Rolf Ernst. Dynamic Voltage Scaling for the Schedulability of Jitter-Constrained Real-Time Embedded Systems, to appear ICCAD 2005.