Information Society Technologies

ARTIST2 – Year 1 Review

Grenoble, October 3rd-4th, 2005

Activity *NoE Integration*

Resource-Aware Design

Activity leaders: Luca Benini (UNIBO)
Peter Marwedel (Dortmund)

Outline of the Presentation

Participants + Objectives

Industrial Needs and Experience

Year 1 Activities

- Achievements & Ongoing Work
- Interaction and Building Excellence Between Partners
- Management Perspective

18 Month Perspective

- Work planned for the next 18 months
- Significant events or achievements expected

JPRA-NoE: Resource-Aware Design

- ***Participants***: Thiele-ETHZ, Wilhelm-Saarland
- ***Objectives***: Predictable design of embedded systems.
- ***M1-M18***: Develop methods to combine performance analysis on various levels of abstraction.

- ***Participants***: Leupers-Aachen, Benini-Bologna
- ***Objective***: Explore and demonstrate the benefits of an application-specific processor generation flow in resource-aware multiprocessor platform design..
- ***M13-M18***: Integration of ASIP simulation models in multiprocessor modelling and performance analysis environment.

- ***Participants***: Marwedel-Dortmund, Benini-Bologna
- ***Objective***: Develop a detailed understanding of the enhancements required in architecture and compilers to support predictable memory management.
- ***M1-M9***: First demonstrator of an integrated compiler+target platform.

Partner's Roles

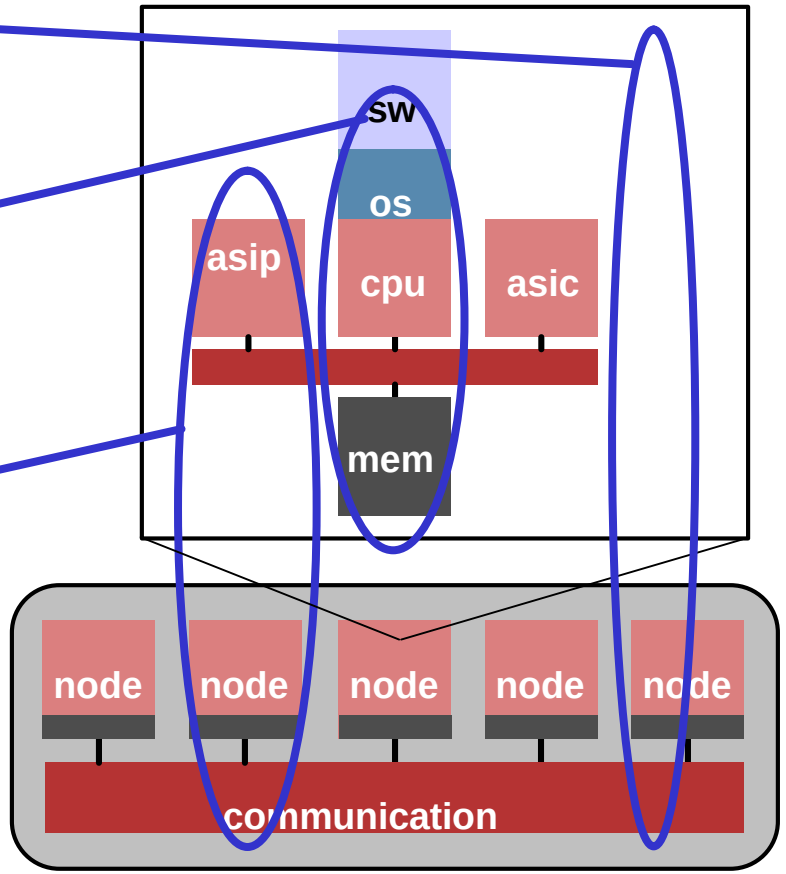
Simulation, Analysis, Design

Thiele-ETHZ, Wilhelm-Saarland: predictable systems design

Marwedel-Dortmund, Benini-Bologna: evaluate predictable memory management

Leupers-Aachen, Benini-Bologna: ASIP design flow ↔ utilization, performance and energy

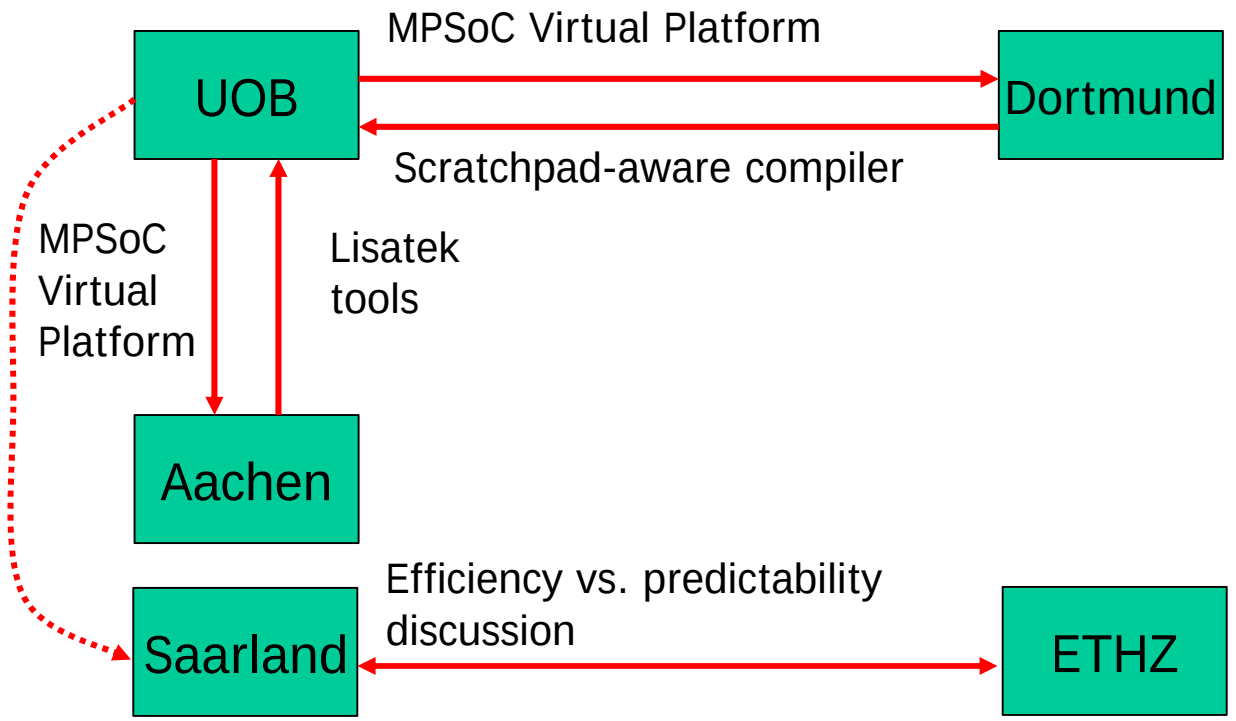
Execution Platform



Industrial Needs and Experience

- Artist2 Interaction with Industry
  - HW Platform providers (STM); ESL EDA vendors (Coware), embedded SW tools development (ICD),
- Industrial Needs
  - Improve predictability: provide WC guarantees, reduce BC-WC interval, reduce variance
  - Preserve efficiency: reduce or eliminate waste of resource (.e.g., power, cost)
- Possible Global Impacts of Research Results
  - Efficient (high performance, low power), but well behaved systems
  - Reduce design time and effort

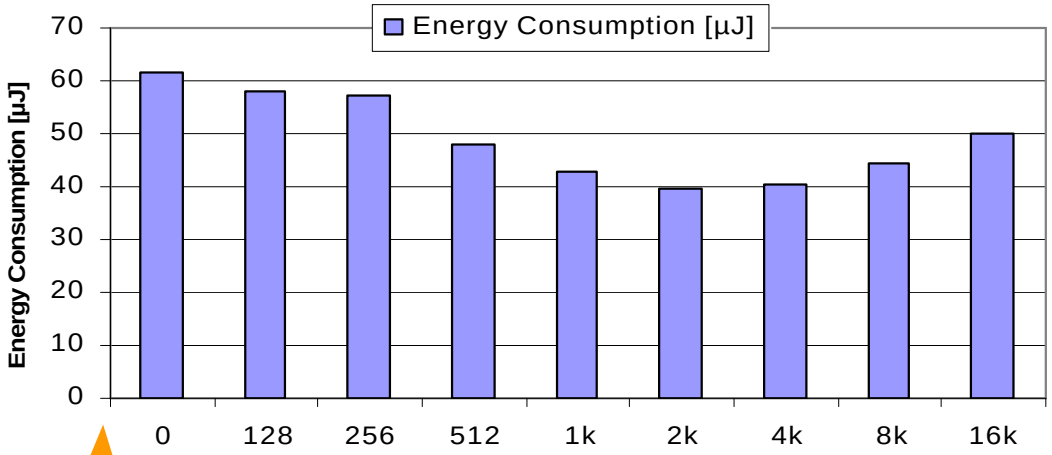
Achievements: our integration work



Year 1 activities

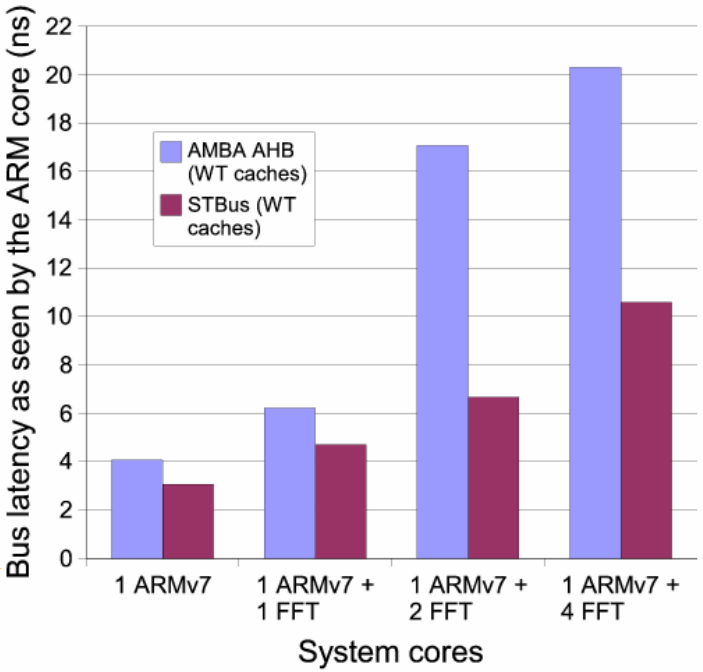
Achievements: technical Work

- State of the Art
  - Several approaches available: Scratchpad management compilers (Dortmund), ASIP creation (Aachen), WCET analysis (Saarland), Virtual platform (BOLOGNA)
  - Lack of integration, lack of holistic approaches, mostly work on single-processor platforms
- Achievements in Year1
  - Combined SP-aware compilation with VP analysis: the compiler can now target a multi-core platform
  - Developed an approach for modeling heterogeneous multi-core platforms



DES-Encryption: 4 processors: 2 Controllers+2 Compute Engines

Power in .13µm technology from STM
Functional bus model provided by STM



Year 1 activities

Management Perspectives

- What worked well:
  - the interactions between partners would not have taken place without the common ground provided by Artist2.
  - Artist2 has provided the framework (meetings, reciprocal visits, workshops) for envisioning, planning, and carrying out cooperation actions
  - Industry has cooperated actively with the activities: Coware support for Lisatek technology (models and tools), and STM provided functional model of STBUS, ICD for compiler development
- Difficulties encountered:
  - No major difficulties

Year 1 activities

Spreading Excellence

- **Numerous publications at leading international conferences:**
  - DATE, DAC, Codes-ISSS, ICCAD, CASES, ISLPED, etc.
- **Tutorials and industrial training**
  - Philips, Samsung, Freescale, EPFL-Advanced digital design Course,
- **Installation of the tools in several universities inside and outside Europe including:**
  - EPFL, POLITO, STANFORD, PENN STATE, KAIST,
- **Evaluation and utilization of the modeling infrastructure by several companies including:**
  - STM, Samsung, Freescale,

Plan and Expected Achievements

- ***Participants***: Aachen, Bologna
- ***Objective***: Demonstrate the benefits of an application-specific processor generation flow in resource-aware multiprocessor platform design.
- ***M19-M36***: Demonstrate the advantages in terms of hardware utillization, performance and power of an heterogeneous multiprocessing platform which includes application specific processors, with respect to a homogeneous multiprocessing platform.

- ***Participants***: ETHZ, Saarland
- ***Objectives***: Predictable design of embedded systems.
- **M19-M36**: Design rules and methods for time-predictable embedded systems. Establish research area.

- ***Participants***: Dortmund, Bologna
- ***Objective***: Develop a comprehensive approach to multi-core memory hierarchy management.
- ***M19-M36***: Enhance architectural model of level 1 and level 2 memories to deal with coherency issues (synchronzation and data coherency). Compiler-supported design-space exploration