Information Society Technologies

ARTIST2 NoE on
Embedded Systems Software Design

Structuring the Research Area in Europe

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ARTIST2 Technical Coordinator

VERIMAG Laboratory

History

ARTIST - FP5 Accompanying Measure:

- Coordinate the R&D effort in the area of Advanced Real-time Systems
- Improve awareness of academics and industry in the area
- Define innovative and relevant work directions

Achieved through activities along 3 axes:

- Roadmaps for selected actions:
  (*Hard Real Time, Component-based Design, Quality of Service, Execution Platforms*)
- International Collaboration
- Education

Information about these results is publicly available on our web site:

http://www.artist-embedded.org/Roadmaps/

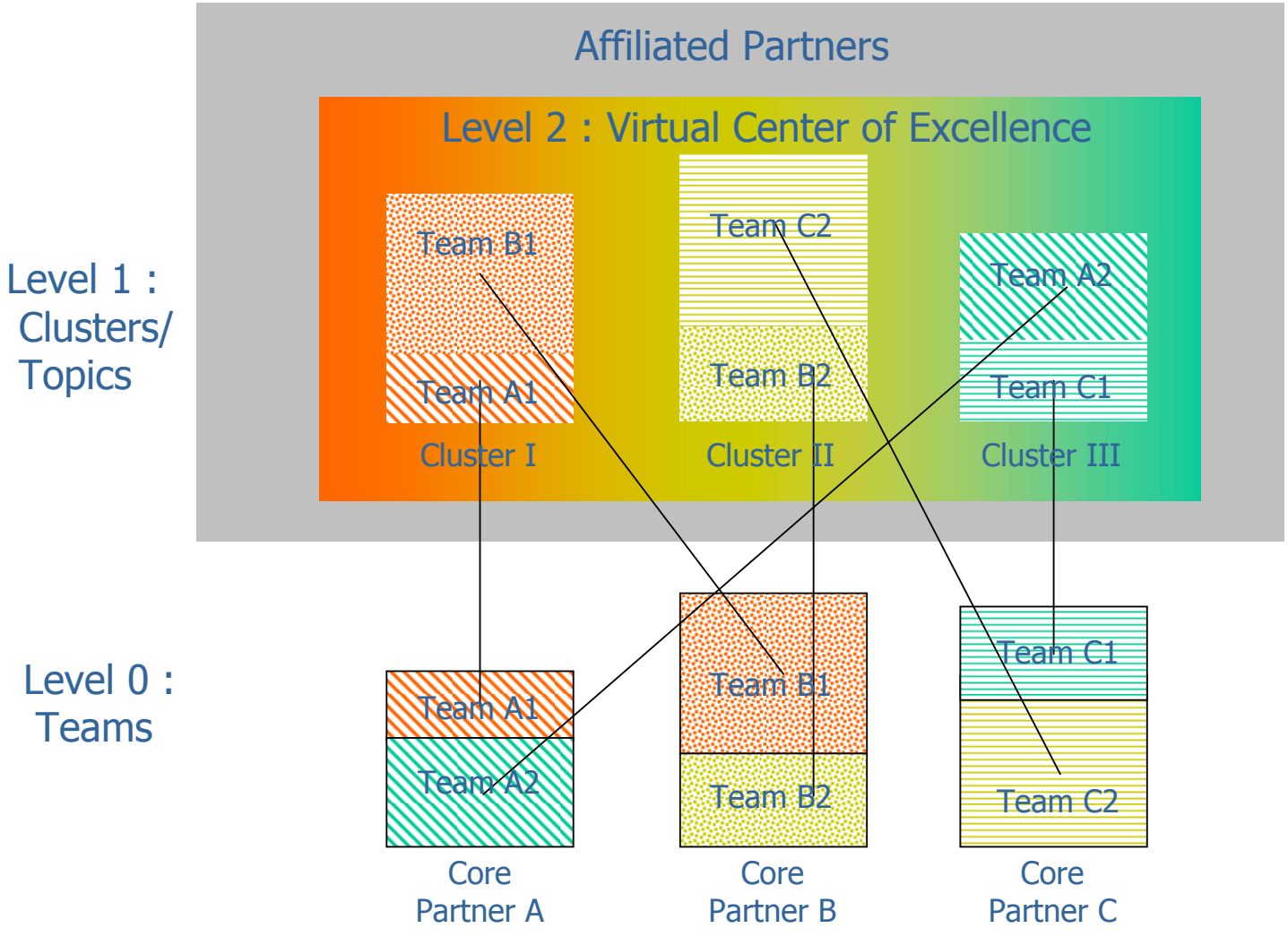
http://www.artist-embedded.org/ACM_Education/

Objectives

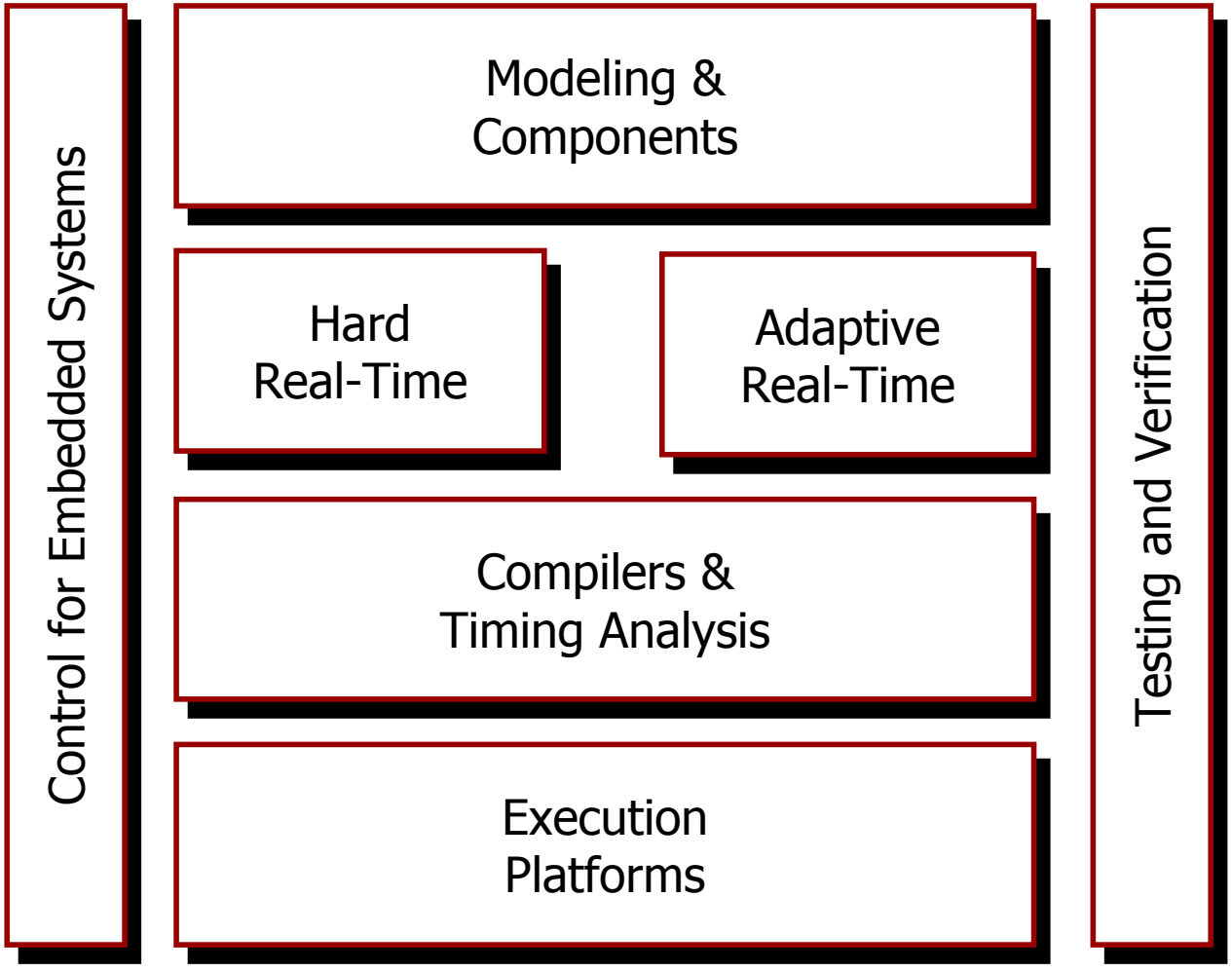
Reinforce and strengthen scientific and technological excellence in Embedded Systems Design:

- The NoE will act as a Virtual Center of Excellence
- **Two levels** of integration
  to create critical mass from selected European teams
  - Strong integration **within selected topics**
    by assembling the best European teams,
    to advance the state of the art in the topic.
  - Integration **between** topics
    to achieve the *multi-disciplinary* excellence and skills required for the development of future embedded technologies.
- Integration will be around a Joint Programme of Activities

Principle of Construction



Selected Topics : ARTIST2 Clusters



Core Participants (1/2)

	Short Name	Full Name and Country	Key researchers
1	CDC	Caisse des Dépots et Consignations (France)	**None**
2	UJF/ Verimag	University Joseph Fourrier / Verimag (France)	Paul Caspi, Susanne Graf, Nicolas Halbwachs, Yassine Lakhnech, Oded Maler, Joseph Sifakis
3	Aachen	RWTH Aachen (Germany)	Rainer Leupers
4	Aalborg	BRICS – Aalborg University (Denmark)	Kim Larsen, Anders Ravn
5	AbsInt	AbsInt Angewandte Informatik GmbH (Germany)	Christian Ferdinand
6	Aveiro	University of Aveiro (Portugal)	Luis Almeida
7	Cantabria	Universidad de Cantabria (Spain)	Michael Gonzalez Harbour
8	CEA	Commissariat à l'Énergie Atomique – Laboratoire LIST (France)	François Terrier
9	CFV	Centre Fédéré en Vérification, Université de Liège (Belgium)	Pierre Wolper
10	Czech TU	Czech Technical University (Czech Republic)	Vladimir Kucera
11	Dortmund	Dortmund University (Germany)	Peter Marwedel
12	DTU	Technical University of Denmark (Denmark)	Jan Madsen
13	ETHZ	Swiss Federal Institute of Technology – Zurich (Switzerland)	Lothar Thiele, Manfred Morari
14	FTR&D	France Telecom R&D	Pierre Combes, Kathleen Milsted
15	INRIA	Institut National de Recherche en Informatique et Automatique (France)	Albert Benveniste, Benoit Caillaud, Alain Girault, Thierry Jéron, Jean-Marc Jézéquel, Paul Le Guernic, Eric Rutten, Yves Sorel, Robert de Simone
16	KTH	Royal Institute of Technology (Sweden)	Martin Törngren
17	Linköping	Linköping University (Sweden)	Petru Eles

Core Participants (2/2)

Core Partner	Short Name	Full Name and Country	Key scientists
18	LSV / CNRS	Centre National de la Recherche Scientifique / Laboratoire LSV (France)	Michel Bidoit, Hubert Comon, Philippe Schnoebelen
18	Lund	Lund University (Sweden)	Karl-Erik Årzén
20	Mälardalen	University of Mälardalen (Sweden)	Gerhard Fohler
21	OFFIS	Kuratorium OFFIS e. V. (Germany)	Werner Damm, Bernhard Josko
22	PARADES	PARADES EEIG (Italy)	Alberto Sangiovanni Vincentelli
23	Pavia	University of Pavia (Italy)	Giorgio Buttazzo
24	UP Madrid	Universidad Politecnica de Madrid (Spain)	Juan de la Puente
25	Saarland	Saarland University	Reinhard Wilhelm
26	STM	ST Microelectronics – Central R&D (France)	Miguel Santana
27	Eindhoven	Technical University of Eindhoven (Netherlands)	Martin Rem
28	TU Vienna	Technical University of Vienna (Austria)	Hermann Kopetz, Peter Puschner, Philipp Petti
29	TUBS	Technical University Braunschweig (Germany)	Rolf Ernst
30	Twente	University of Twente (Netherlands)	Ed Brinksma
31	UoB	University of Bologna (Italy)	Luca Benini
32	Uppsala	Uppsala University (Sweden)	Bengt Jonsson
33	UPVLC	Universidad Polytecnica de Valencia (Spain)	Alfons Crespi
34	York	University of York (UK)	Guillem Bernat, Alan Burns, Andy Evans, Andy Wellings
35	Porto	Polytechnic of Porto	Eduardo Tovar

ARTIST2 NoE : Team Leaders

Hard Real Time
Albert Benveniste – INRIA
Alberto Sangiovanni – PARADES
Paul Caspi – Verimag
Hermann Kopetz – TU VIenna
Werner Damm – OFFIS

Adaptive Real-time
Giorgio Buttazzo – Pavia
Guillem Bernat – University of York
Michael Gonzalez - Cantabria
Luis Almeida – Aveiro
Gerhard Fohler – Malardalen
Juan de la Puente – Polytechnic de Madrid

Modeling and Components
Bengt Jonsson – Uupsala
François Terrier – CEA/LIST
Jean-Marc Jezequel – INRIA
Susanne Graf – Verimag

Testing & Verification
Kim Larsen - Aalborg/ BRICS
Ed Brinksma – Twente
Pierre Wolper – Centre Fédéré de Verification
Michel Bidoit - LSV
Thierry Jeron - INRIA

Control for Embedded
Karl-Erik Arzen – Lund
Martin Torngren – KTH
Alfons Crespo – UP Valencia
Vladimir Kucera - Czech TU

Compilers and Timing Analysis
Reinhard Wilhelm - Saarland
Rainer Leupers - Aachen
Miguel Santana – ST Microelectronics
Christian Ferdinand – AbsInt
Peter Marwedel - Dortmund
Puschner, Krall – TU Vienna
Björn Lisper - Uppsala

Execution Platforms
Lothar Thiele – ETH Zurich
Jan Madsen –DTU (TU Denmark)
Luca Benini – LPOS
Petru Eles – ESLAB/Liu
Rolf Ernst – UBR
Martin Rem – Eindhoven

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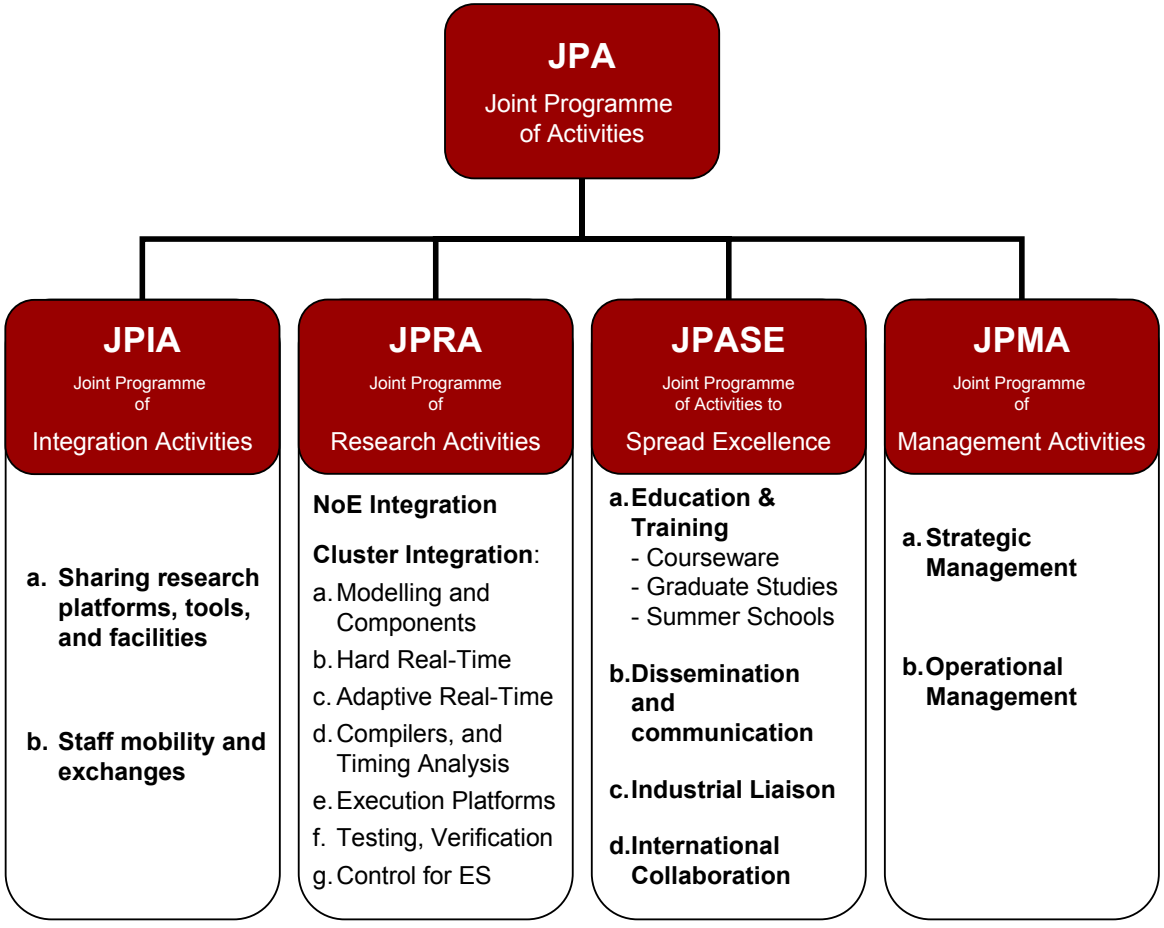
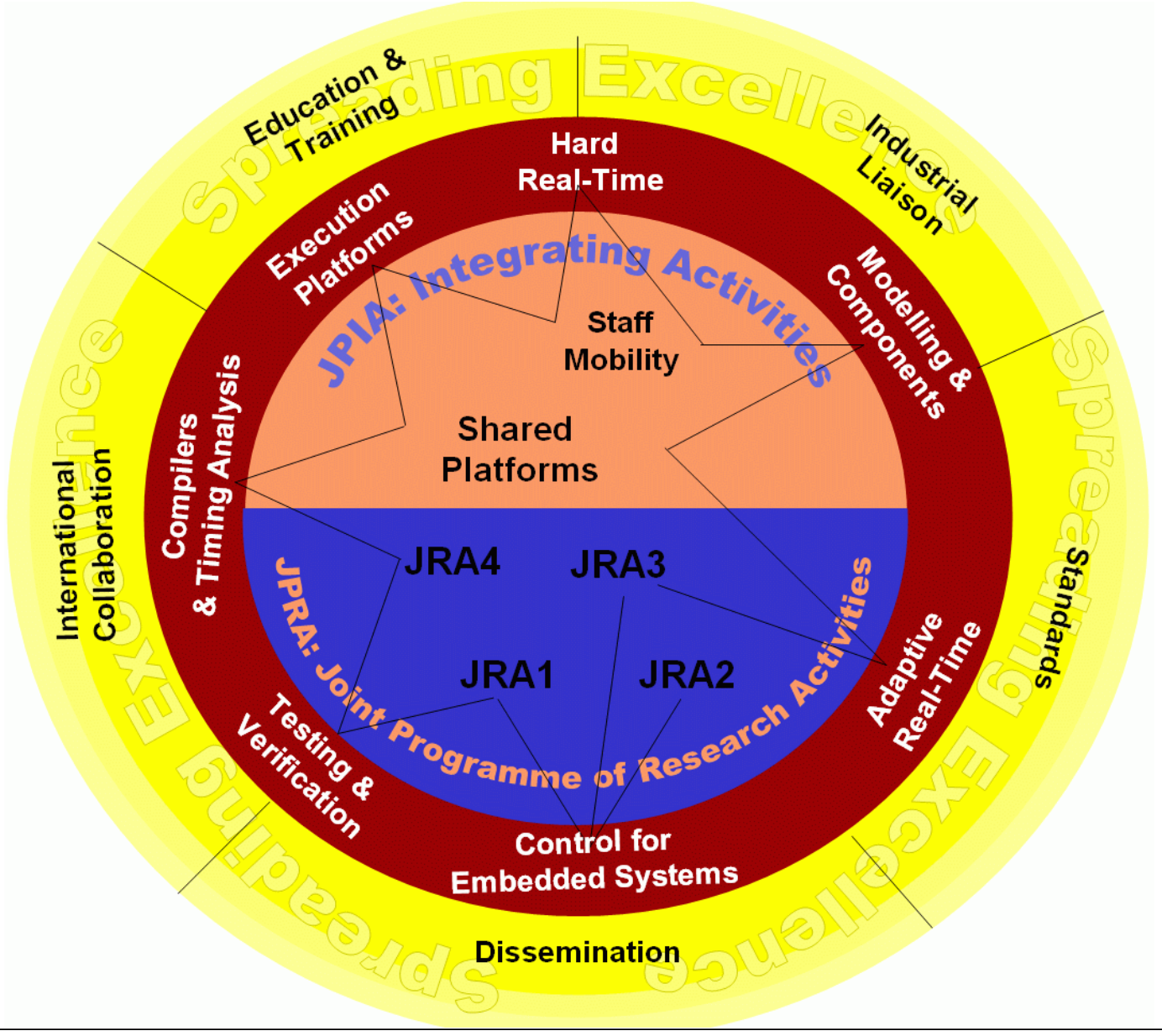
Joint Programme of Activities



Artist2 Structure



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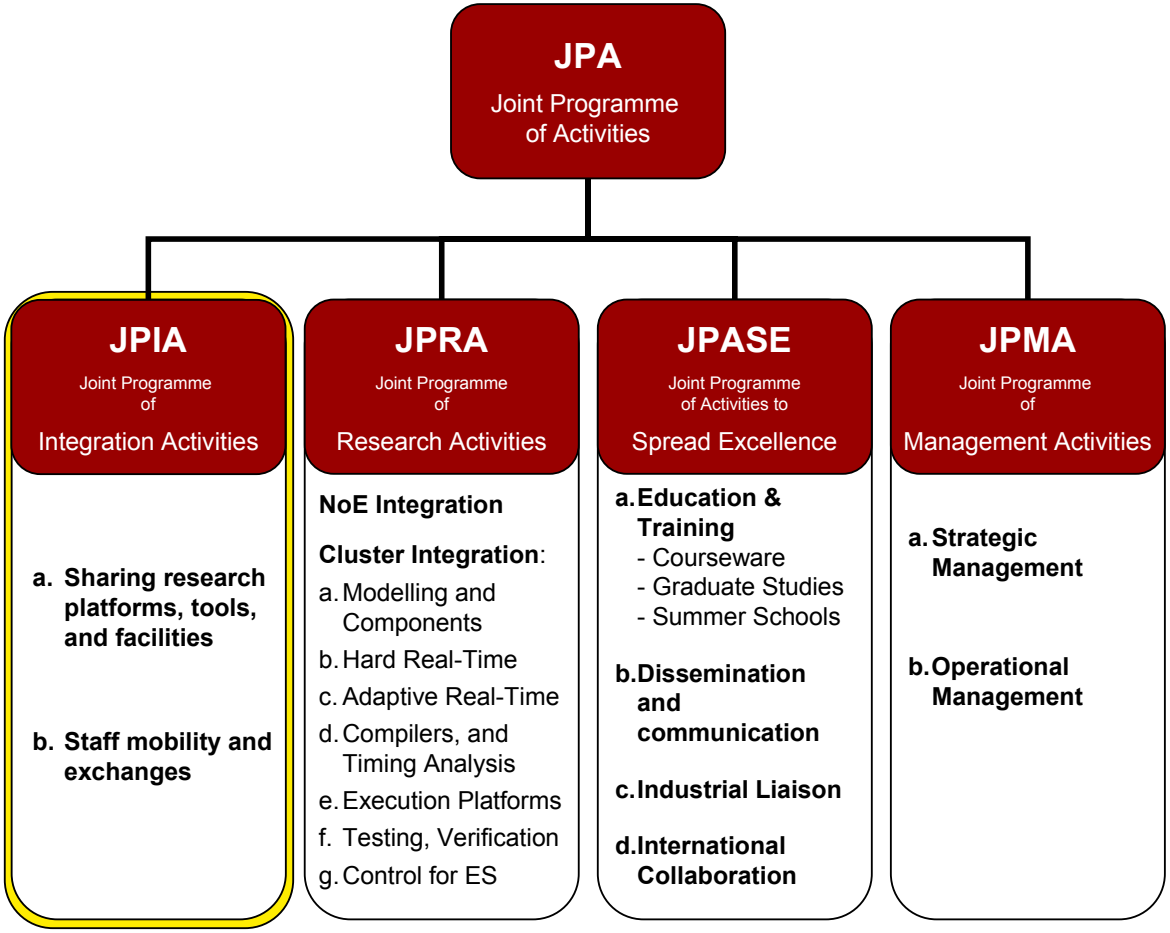

Sharing Research Platforms, Tools, and Facilities

Cluster	*JPIA - Platform*
Modelling and Components	Platform for Component Modelling and Verification *This platform will support translations to semantic kernel languages to leverage associated powerful analysis tools, in particular those from the "Testing and Verification" cluster.*
Adaptive Real-Time	A common infrastructure for adaptive Real-time Systems *Promote extension of operating systems (eg: RT-POSIX and OSEK) and network protocols to support emerging real-time applications having a high degree of complexity and operating in dynamic environments.*
Testing and Verification	Testing and Verification Platform for Embedded Systems *Will also make available new powerful analysis tools developed within the network, in particular those from the related Joint Research Activities ("Testing and Verification", "Verification, Testing and Control" and "Verification of Security Properties").*
Control for Embedded Systems	Design Tools for Embedded Control *Develop a suite of tools, for developing resource-constrained embedded control systems* - taking *control, computing, and communication aspects into account.*
Compilers and Timing Analysis	Timing - Analysis Platform *Combine the best existing Timing-Analysis tools in a standard tool architecture with well-defined textual interfaces, to preserve the existing lead of European Research and Industry in this important sector.*
	Compilers Platform *Provide world-class code-synthesis and compiler tools for the generation of efficient machine code. Integration of existing compiler-generation approaches allowing compilers for new architectures to be built quickly, efficiently and reliably.*
Execution Platforms	System Modelling Infrastructure *Integrate ongoing research efforts on infrastructure modelling. This would replace prototyping hardware to reduce the cost and time required for designing embedded systems.*

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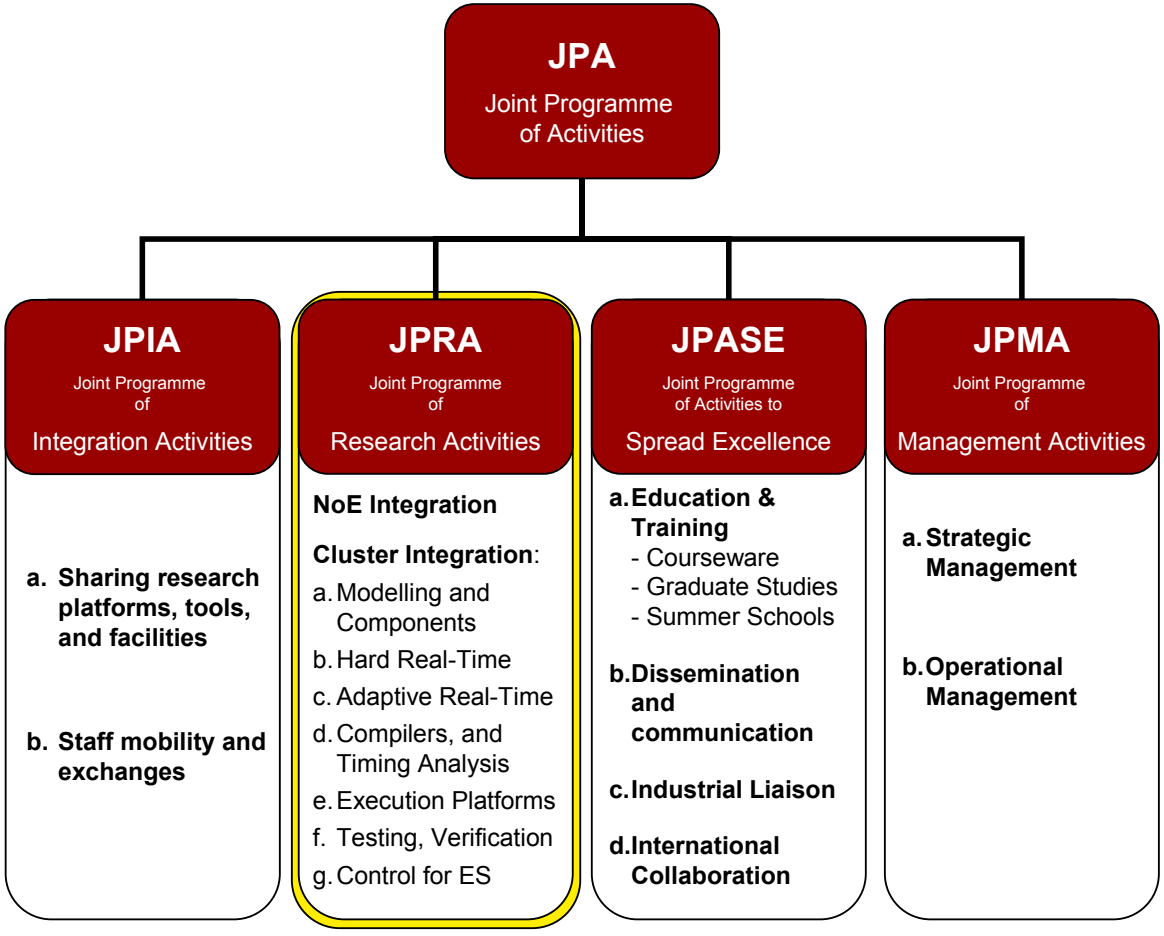
Joint Programme of Activities



NoE Integration

Clusters	*JPRA – NoE Integration*
❖Hard Real-Time ❖Adaptive Real-Time ❖Control for Embedded Systems	Semantic Framework for Hard Real-Time Design Flow *Develop a mathematically sound framework, supporting system modelling, to incorporate the underlying models of computation and communication of different design tools. It should be effective and rich enough to provide formal analyses, algorithms, and support methods to deal with heterogeneity.*
❖Hard Real-time ❖Adaptive Real-time ❖Execution Platforms	Merging the Event-triggered and Time-triggered Paradigms *Fundamental work on merging two of the main paradigms in synchronous real-time systems design. Strong impacts on distributed embedded systems and network on chip applications.*
❖Control for Embedded Systems ❖Hard Real-Time ❖Adaptive Real-Time	Adaptive Real-time, HRT and Control *Integrate research among control and real-time teams on different computational models for embedded control systems and the use of control techniques to provide flexibility in embedded systems.*
❖Compilers and Timing Analysis; ❖Adaptive Real-Time; ❖Execution Platforms	Timing Analysis for Adaptive Real-Time Systems *Integrate research among ARTIST2 partners on knowledge of both worst-case and less than worst-case timing behaviour of programs for Adaptive real-time systems and its integration in RTOS*

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❖Adaptive Real-Time ❖Modelling and Components	QoS aware Components *Develop holistic frameworks and models for QoS management to combine features of component models, component frameworks, middleware infrastructure, OS and Kernel support, and networking.*
❖Execution Platforms ❖Compilers and Timing Analysis	Resource-aware Design *Provide a viable path for resource-aware software and hardware development.*

Cluster Integration (1/2)

Cluster	*JPRA-Cluster Integration*
Modelling and Components	**Component Modelling and Composition** Development of a general framework for component-based engineering of complex heterogeneous systems.
	Development of UML for Real-time Embedded Systems Development of a general framework for component-based engineering of complex heterogeneous systems.
Hard Real-Time	**Diagnosis in Distributed Hard Real-time Systems** integrated approach to diagnosis of distributed real-time systems, in particular with respect to transient anomalies.
Adaptive Real-Time	**Flexible Scheduling Technologies** Develop a real-time scheduling framework capable of handling different real-time requirements in the same system – to be used in next-generation OS kernels for adaptive QoS control of dynamic behavior.
	Adaptive Resource Management for Consumer Electronics Higher efficiency in managing extra-functional properties of consumer electronics applications (power, bandwidth, memory security, functionality, etc.)

Cluster Integration (2/2)

Cluster	*JPRA-Cluster Integration*
Compilers and Timing Analysis	**Architecture-aware compilation** Provide a unified architecture-aware code-synthesis and compiler methodology.
Execution Platforms	**Communication-centric systems** Use formal methods to increase design productivity and quality. **Design for low power** Address low-power issues across several layers of abstraction
Control for Embedded Systems	**Control in real-time computing** Applying control methods for handling uncertainty and to provide flexibility in real time applications. **Real-time techniques in control system implementations** Advances in real-time control applications
Testing and Verification	**Quantitative Testing and Verification** Advances in verification and testing methodologies **Verification of Security Properties** Develop the basic technology needed to certify security applications at levels EAL6, and EAL7, from the Common Criteria.

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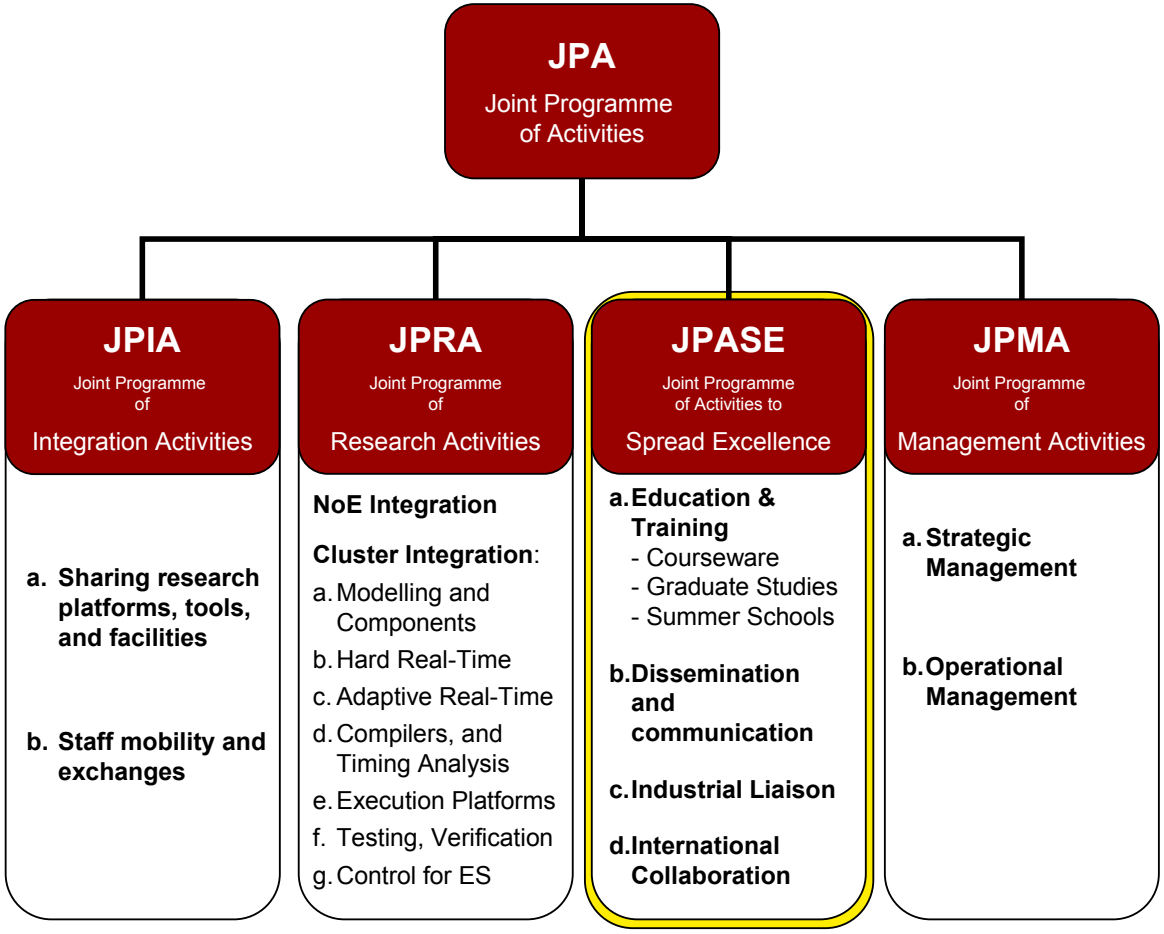
Joint Programme of Activities



Education and Training

JPASE - Education
Courseware *Achieve a consensus and a unified approach for teaching embedded systems that meets current and future needs for industry and research.*
Graduate Studies *ARTIST2 will provide support for selected graduate studies programmes, both as an incubator for integrated education for the area, and also to spread excellence within Europe. The purpose is to gain experience in setting up a full Master program on embedded systems given by international experts distributed over Europe.*
Support for Summer Schools *ARTIST2 will provide support for selected schools and seminars. As with Graduate Studies, these will serve both as incubators for integrated education for the area, and also to spread excellence within Europe.*
ARTIST2 Summer School *ARTIST2 will set up and run its own summer school, which will serve as an incubator for developing and refining a graduate curriculum in embedded systems design.*

Dissemination and Communication

JPASE – Dissemination and Communication
Conferences, workshops, seminars, publication in journals *ARTIST2 will take the measures and initiatives needed to:* *- Promote a structured landscape of conferences, workshops and scientific events* *- Publication of articles in scientific journals, and media targeting a wider audience.*

Industrial Liaison

JPASE - Industrial Liaison

The objective is to structure and further improve the efficiency of NoE consortium's numerous industrial relations. For this, all the NoE's resources for dissemination and communication will be used, and particularly specific events for triggering projects, definition of strategic directions, standards.

The Industrial Advisory Board will play a pivotal role in the definition of this policy.

International Collaboration

JPASE - International Collaboration

This activity will prolong existing cooperation with leading international experts and institutions. The goal is to initiate collaboration between ARTIST2 researchers and the counterparts in the USA and Asia.

Industrial Advisory Board

Industrial Advisory Board

The Industrial Advisory Board aims to deliver to the network the vision of the potential future business and to provide an objective assessment of success factors to drive innovation in key industrial activities.

It advises the NoE on the current industrial needs and trends relevant to the embedded systems design. It may also recommend changes to the consortium, notably in adding strategic partners, or to the Joint Programme of Activities.

The Industrial Advisory Board is composed of selected top industrial figures in the area.

Dominique Potier
Group Scientific Director, Software Technologies
Thalès - Technical Directorate
ARTIST2 Industrial Advisory Board chairman

Eric Conquet SW Engineering and Standards ESA - ESTEC	**François Pilarski** Systems Framework Systems Department Airbus	**Henrik Lönn** Systems and Architecture Volvo Technology Corporation
Sjir van Loo Principal Systems Architect Information Processing Architectures Philips Research Laboratories - Eindhoven	**Miguel Santana** Director Center of Expertise on Software Debugging, Analysis, Simulation & IDEs ST Microelectronics	**Andras Toth** Ericsson Research, IP Networks Ericsson AB

Affiliated Academic Partners

Name	Key researchers
RWTH Aachen	Stefan Kowalewski
University of the Balearic Islands	Julián Proenza
Masaryk University Brno	Prof. Lubos Brim
ENST – Distributed Real-Time Embedded Systems Group	Laurent Pautet
Politecnico di Milano	Prof. Donatella Sciuto
Royal Institute of Technology (KTH)	Prof. Axel Jantsch
Leiden University	Prof. Dr. Ed F. Deprettere
University of Nijmegen	Dr.ir. G.J. Tretmans
Politecnico di Torino	Prof. Luciano Lavagno
Universitat Politècnica de Catalunya	Dr. Pau Martí Colom
University of Catania	Prof. Lucia Lo Bello
EPFL (Swiss Federal Institute of Technology)	Prof. Thomas A. Henzinger
IMEC	Dr. Francky Catthour
IRISA/INRIA	Dr. Isabelle Puaut
Polytechnic Institute of Porto	Prof. Eduardo Tovar
Katholieke Universiteit Leuven (K.U. Leuven)	Prof. Pierre Verbaeten
Katholieke Universiteit Leuven (K.U. Leuven)	Prof. Geert DECONINCK
LIAFA - Université Paris 7 & CNRS UMR 7089	Prof. Ahmed Bouajjani
Timisoara - Institute e-Austria Timisoara	Dr. Marius Minea

Affiliated Industrial Partners

Name	Key persons
ABB Automation Technology	Göran Arinder
ABB Automation Technology Products AB/ Robotics	Christer Norström
Airbus	Francois Pilarski
DaimlerChrysler AG	Thomas Thurner
DaimlerChrysler	Matthias Grochtmann
Electricité de France (EDF)	Alain Ourghanlian
Ericsson Mobile Platforms AB	Johan Eker
Hispano Suiza	Philippe Baufreton
Honeywell Prague Laboratory	Vladimir Havlena
Israel Aircraft Industries	Dr. Michael Winokur
Nokia Denmark A/S	Peter Mårtensson
Siemens Mobile Phones A/S	Sven Holme Sørensen
STMicroelectronics	Roberto Zafalon
Thalès	Dominique Potier
Volkswagen AG	Fabian Wolf
Volvo Car Corporation	Jakob Axelsson
Volvo Technology Corporation	Magnus Hellring

Affiliated SME Partners

Name	Key persons
ACE Associated Compiler Experts bv	Hans van Someren
ARTiSAN Software	Alan Moore
BullDAST s.r.l.	Dr. Monica Donno
dSPACE Gmbh	Joachim Stroop
Enea Embedded Technology	Jan Lindblad
Esterel Technologies	Bernard Dion
Evidence Srl	Paolo Gai
IAR Systems AB	Carl von Platen
LifTech	António Garrido
Micro I/O Serviços de Electrónica Lda	Fernando Santos
Tidorum	Dr. Niklas Holsti
TNI-Valiosys	Jean-Luc Lambert

Affiliated International Collaboration Partners

Name	Key persons
University of Illinois Urbana-Champaign	Lui Sha
Stanford University	Giovanni De Micheli
National University of Singapore	P.S. Thiagarajan
University of Virginia	Tarek Abdelzaher
University of California at Berkeley	CHESS Project
Vanderbilt University	Janos Sztipanovits