Towards a System Modelling Infrastructure

ARTIST2

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Execution Platform Cluster

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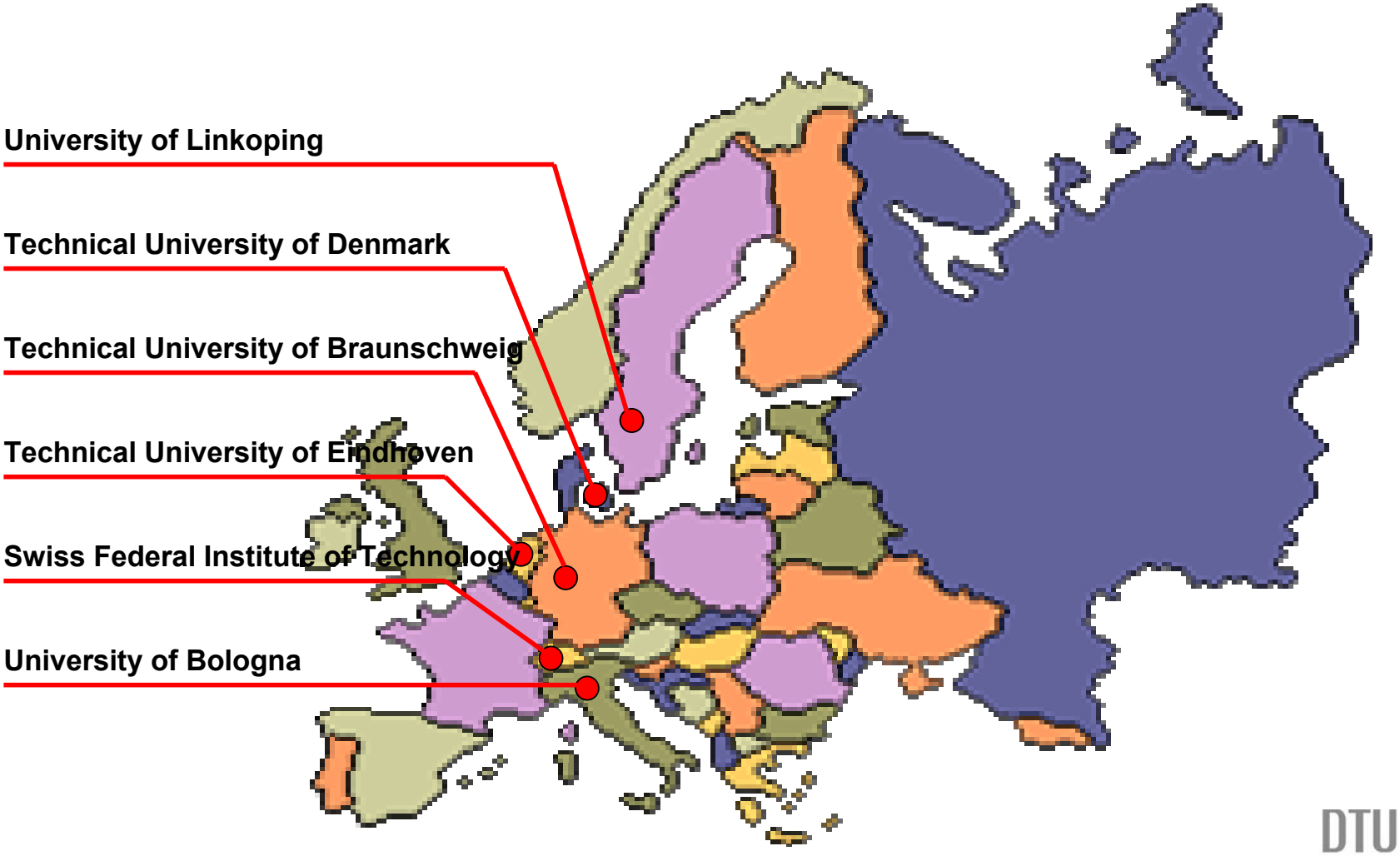

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System Modelling Infrastructure

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- Objectives
  - Integrate ongoing research efforts on infrastructure modelling
  - Replacing prototyping of hardware
  - Reducing the cost and time required for designing embedded systems
  - Tackling the growing *complexity* of embedded systems
- Baseline
  - A key research and research integration enabler is a *scalable* and *realistic* modelling platform which is abstract enough to provide complete system representations and some form of functional models even for billion-transistor future systems, while at the same time providing the needed flexibility for modelling a number of different *embodiments* (e.g. multi-processors, homogeneous and heterogeneous, reconfigurable, etc.).
- Approach
  - Develop a system of formal models
  - Describing their dependencies
  - Develop associated tools (e.g. simulation, worst case analysis)

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Objectives

- System-level modeling framework
- Bridging,
  - Application
  - RTOS
  - Execution platform

  } *Cross-layer optimization*
- Supporting
  - System-level analysis
  - Early design space exploration

Agenda

- Systems?
- System modelling
  - Formal models
  - Simulation models
- Simulation model
  - MPARM
  - ARTS
  - MPARM/ARTS Integration
- Examples

Agenda

- **Systems?**
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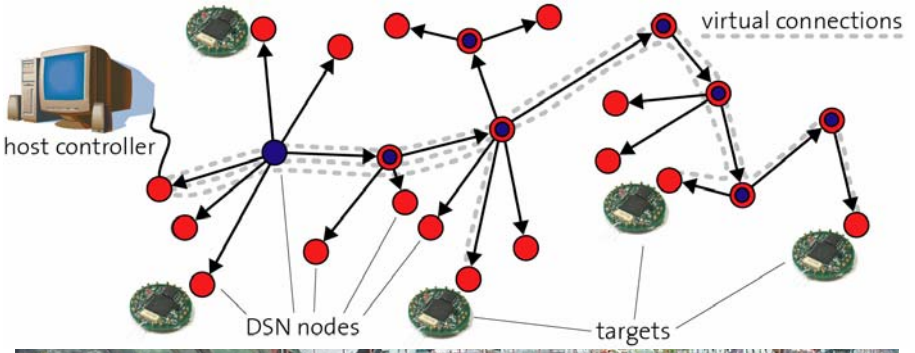
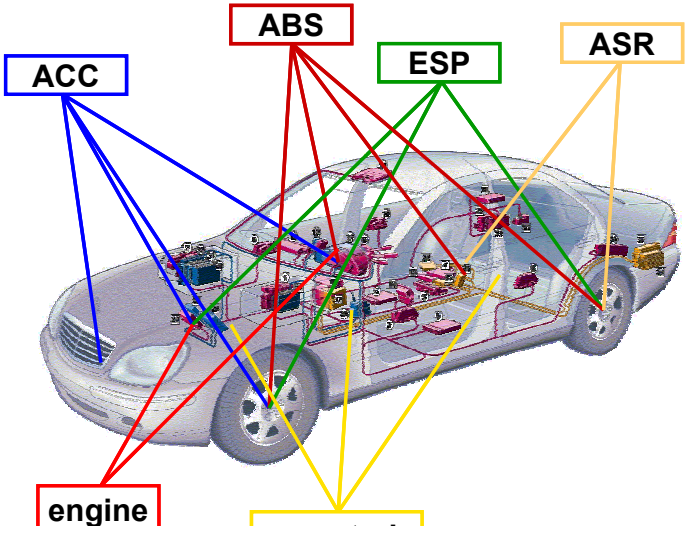
Systems?

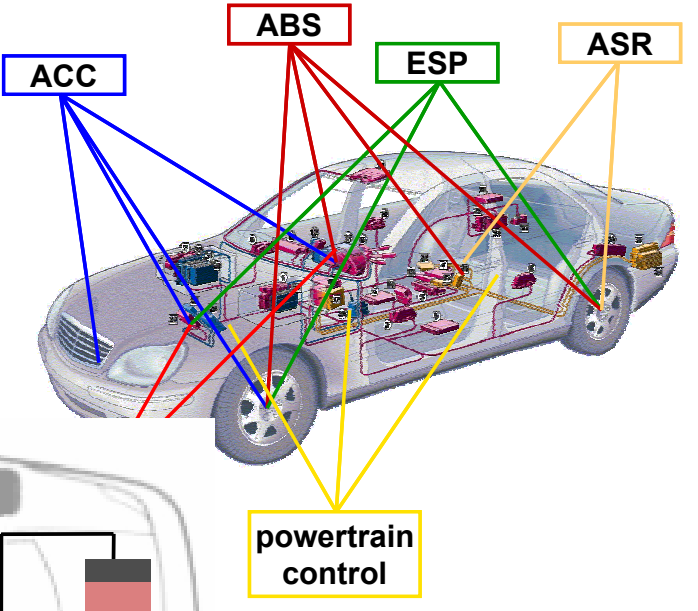

host controller
virtual connections
DSN nodes
targets

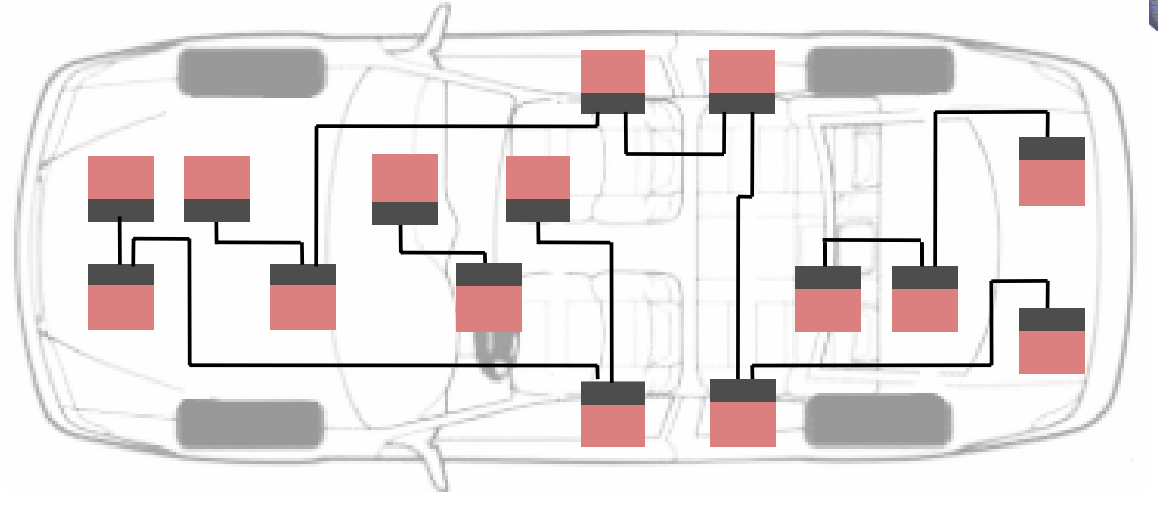

ABS
ACC
ESP
ASR
engine


NOKIA
Options
Zoom

Automotive systems

- Point-to-point wiring
- Modern high-end vehicles
  ~ 100 microcontrollers!
- ⇨ 5 km of wires (50 kg)





Automotive systems

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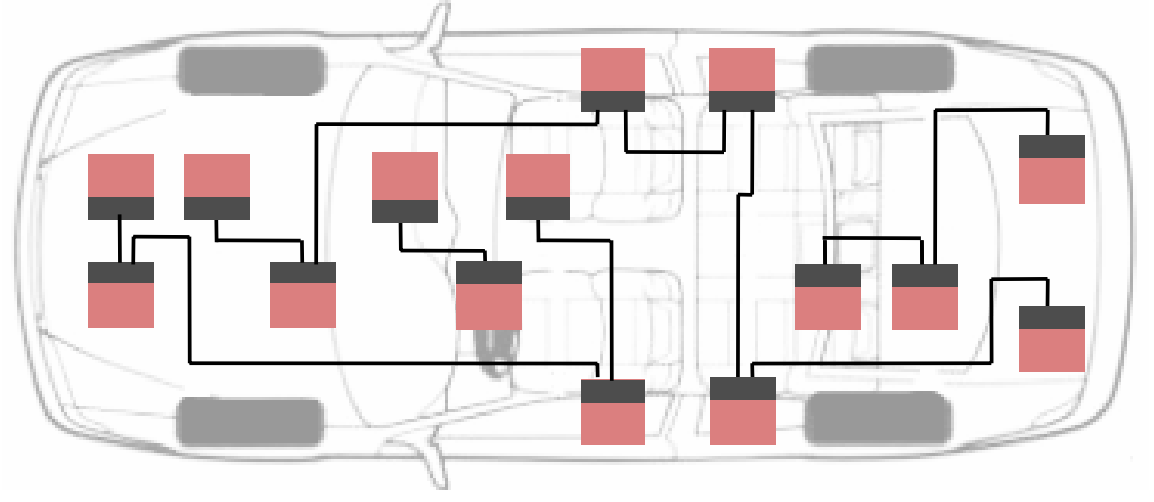
- Broadcast communication channels
- *Clustered networks*
- Several functions mapped onto a single node in order to decrease number of nodes in system
- Single function mapped onto several nodes
- Challenge for *safety-critical* systems



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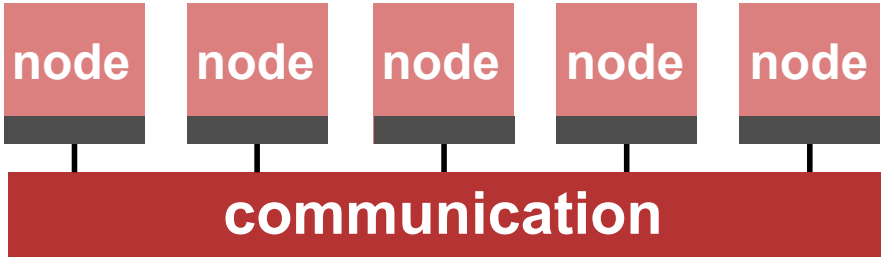
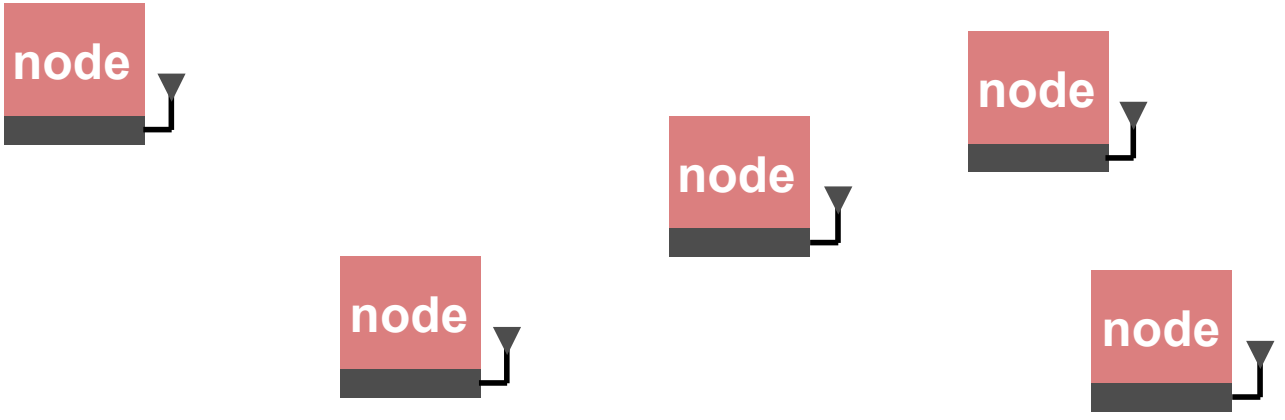
Multimedia systems

- High performance systems
- Interconnections are the major source of *delay* and *power* consumption in nanometer technologies
- Packet switching communication networks (”internet on a chip”)
- *Network-on-Chip*
- *Interconnect-centric* design methodologies



Wireless Sensor Networks



- Sensing, processing and communicating
- Mixture of technologies (MEMS, RF, digital, CPU, OS, ...)
- Broadcast communication channels (range linked with power)
- Clustered networks
- *Low power* and *reliability* are key issues

Agenda

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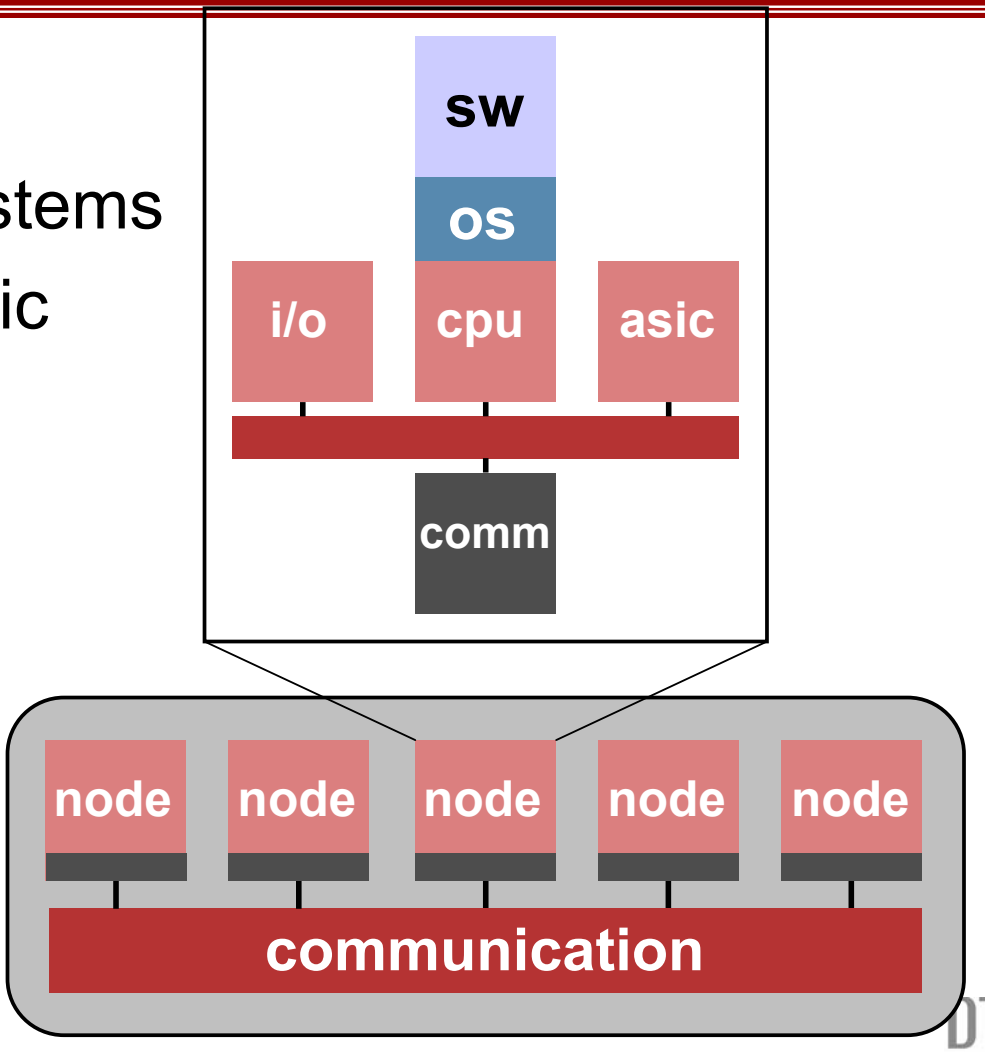
System modelling

- Heterogeneous multiprocessor systems
- Interconnect-centric
- Low-power
- Hierarchical
- Clustered



Platform mapping

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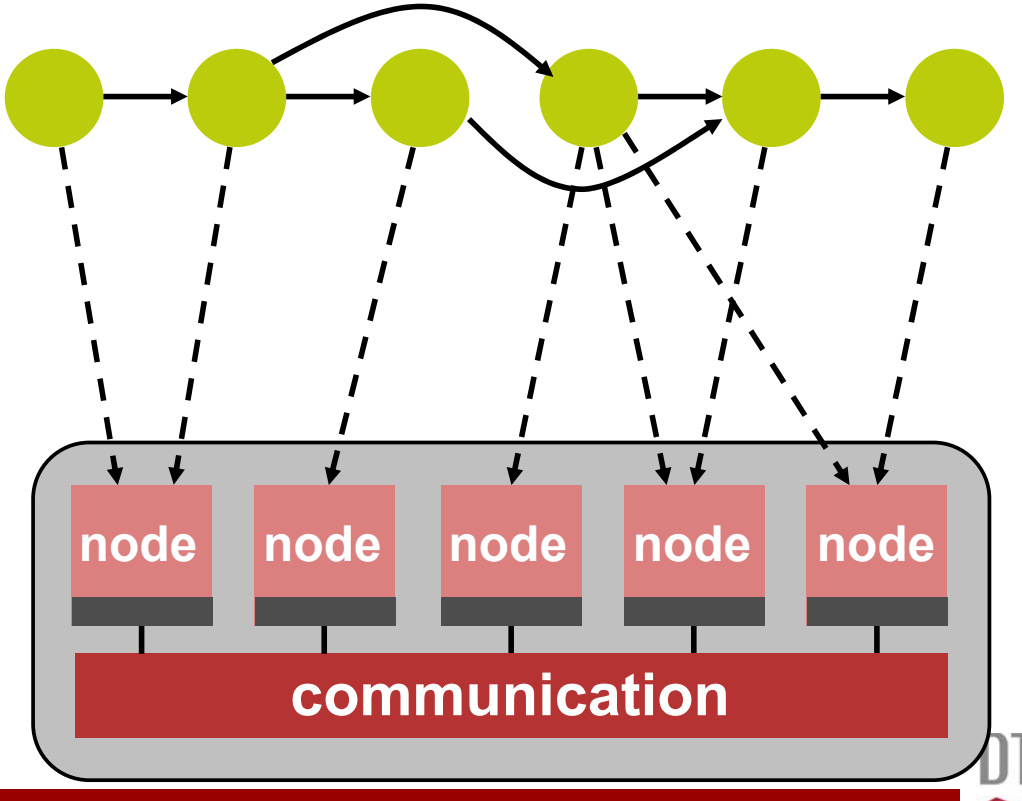

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System analysis

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- Consequences of different mappings of tasks to processors – software or hardware
- Effects of different RTOS selections – scheduling, synchronization and resource allocation policies
- Effects of different Network topologies and communication protocols.
- Approaches:
  - Formal analysis
  - Simulation based analysis

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Agenda

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Formal models

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- SymTA/S (TU Braunsweigh)
- Real-Time Calculus (ETH Zurich)
- Holistic schedulability analysis (TU Linkoping)

- Worst case performance analysis

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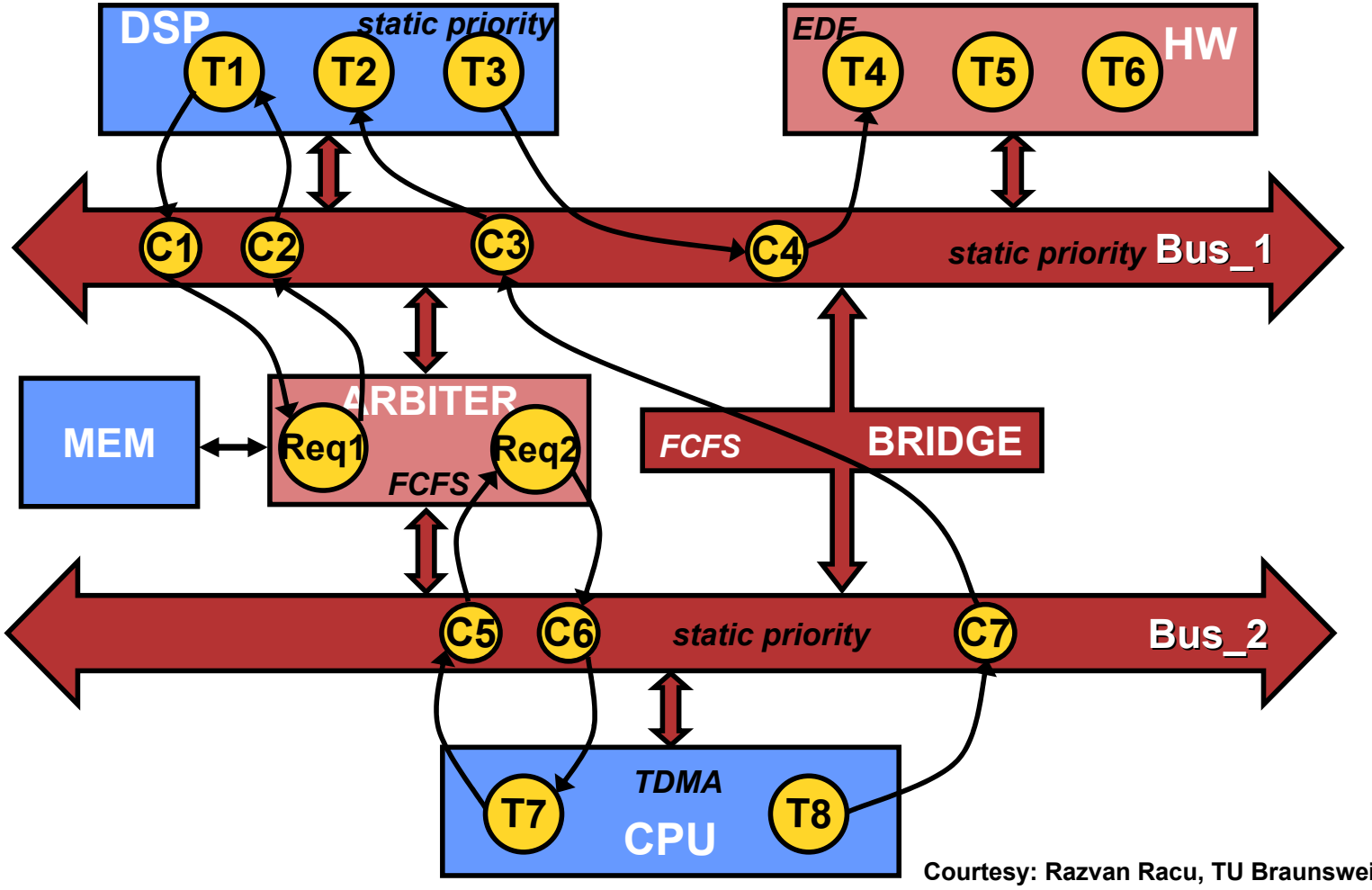
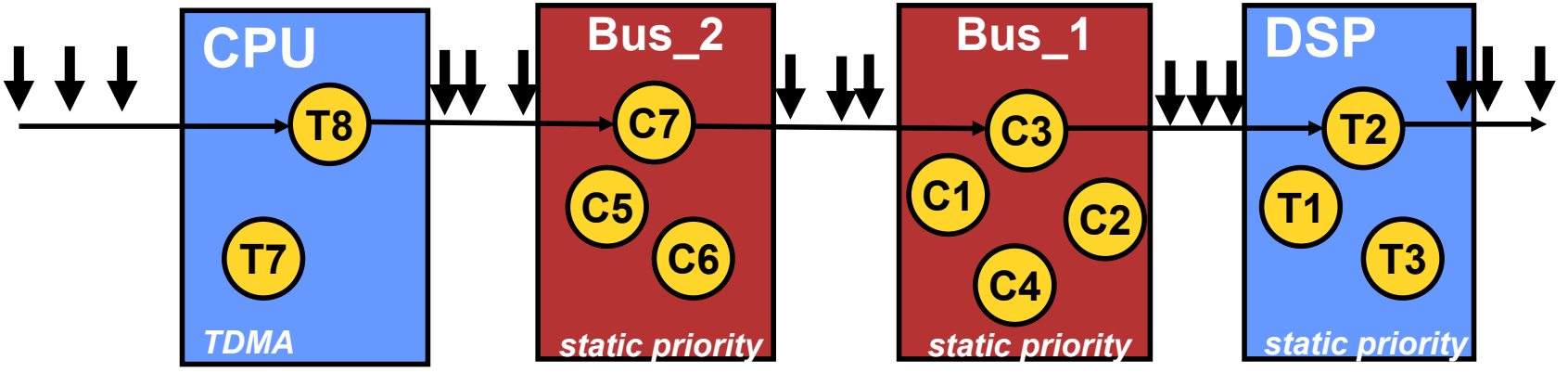
Multiple Scheduling Strategies



Courtesy: Razvan Racu, TU Braunsweig

Compositional Approach



- Tasks are coupled by data flows (tasks inter-communication)
- Interpreted as activating events (event models)
- Composition by means of event stream propagation
  - determine the output streams
  - propagate to the next component

Courtesy: Razvan Racu, TU Braunsweig

System Analysis Loop

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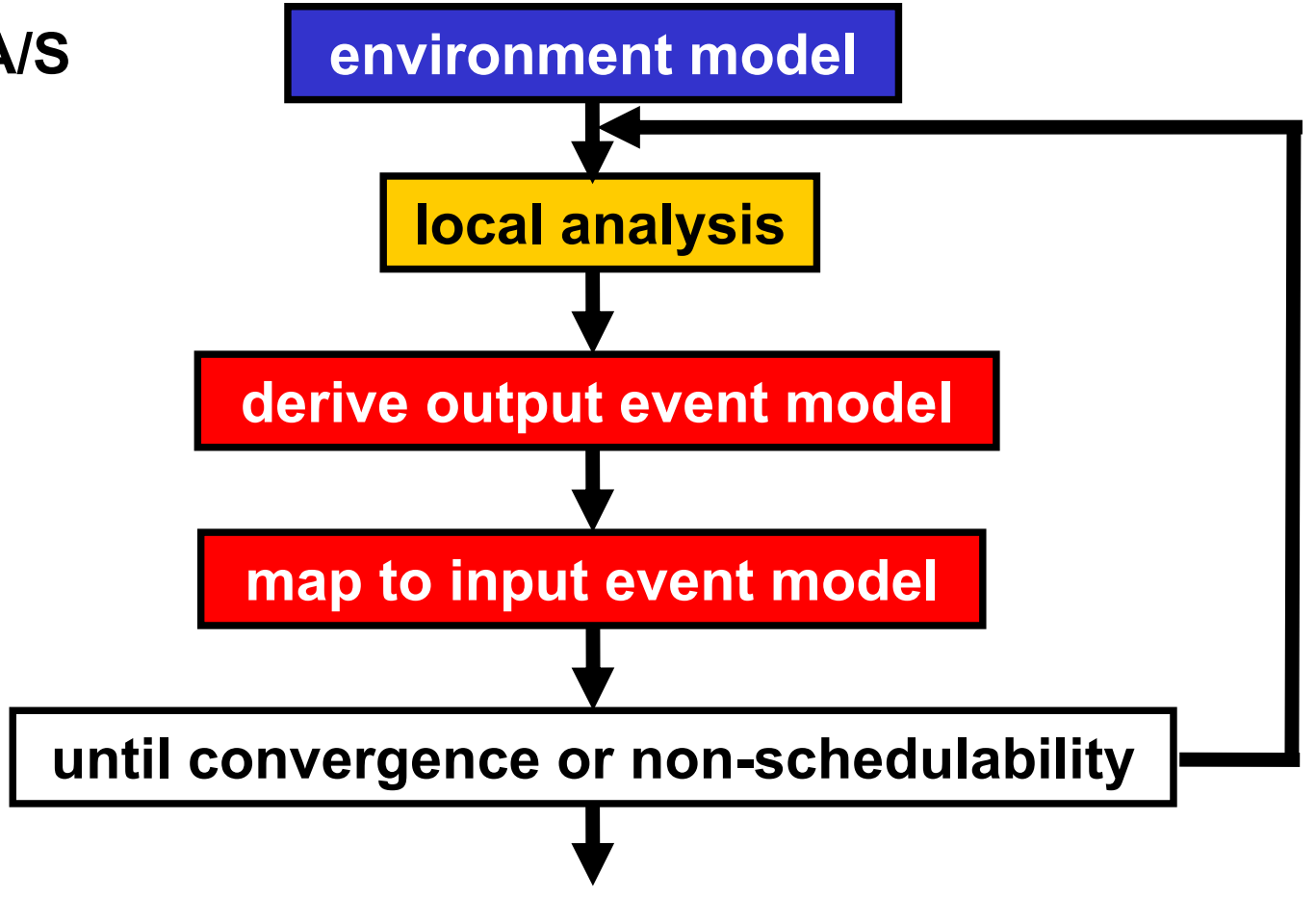
SymTA/S



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System simulation models

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- MPARM (TU Bologna)
- ARTS (TU Denmark)

- Average case performance analysis

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Platform-based design

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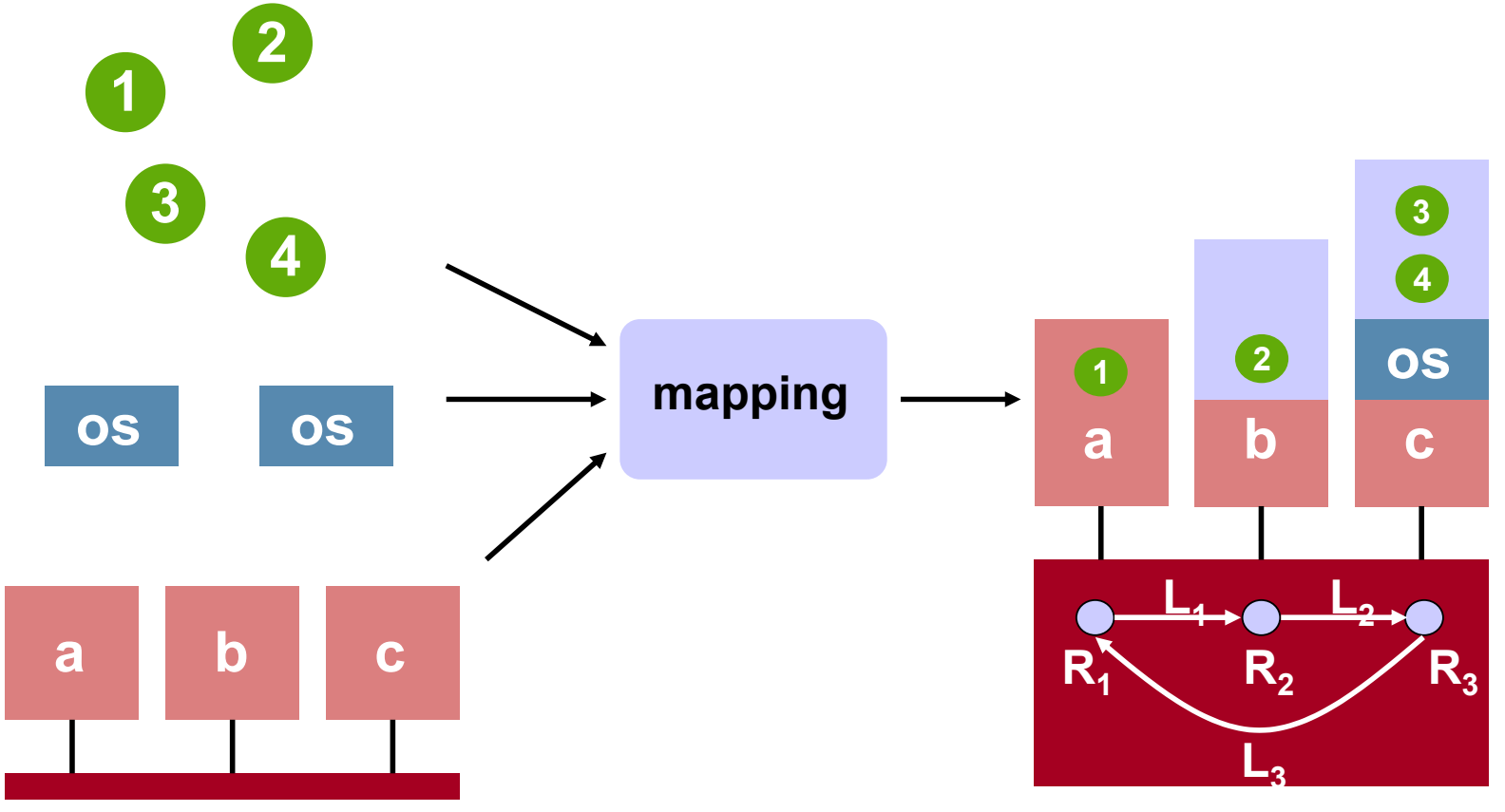

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- Systems?
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  - **MPARM**
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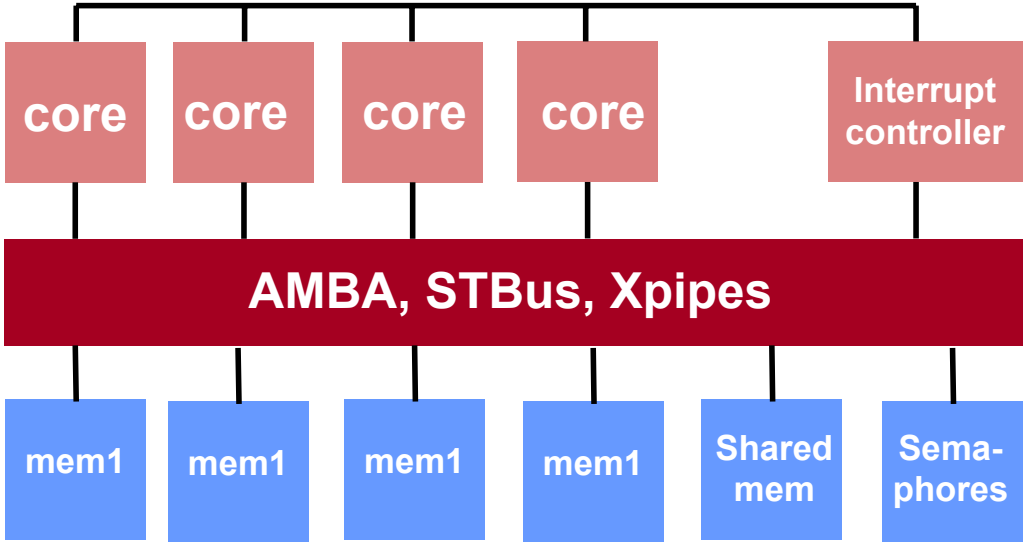
MPARM

- MPARM from University of Bologna



- Cycle-accurate environment with pluggable CPUs and interconnects
- Based on SystemC

MPARM

- Cores
  - Existing IP devices: memories, interrupts, semaphores, FFT engines
  - Memory hierarchy exploration tools: scratchpad memories, cache coherency devices, DMA engines
  - Variable frequency support
  - Power models for cores and memories
- Interconnect
  - AMBA, STBus, Xpipe, ...
  - OCP based
- Software/OS
  - Port of the RTEMS OS, with support for multiprocessing
  - Supports the standard GNU ARM cross-compiler toolchain
  - Libraries for message passing
- Benchmarks
  - DES, FFT, JPEG, H.263, MPEG, …

Cycle-true SoC exploration

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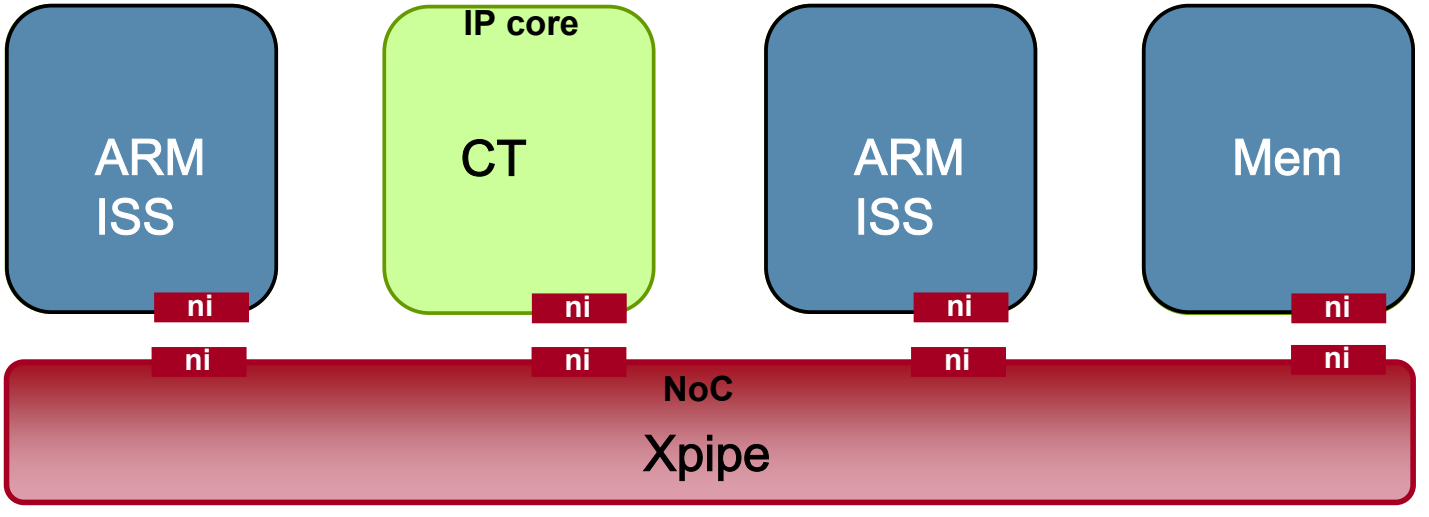

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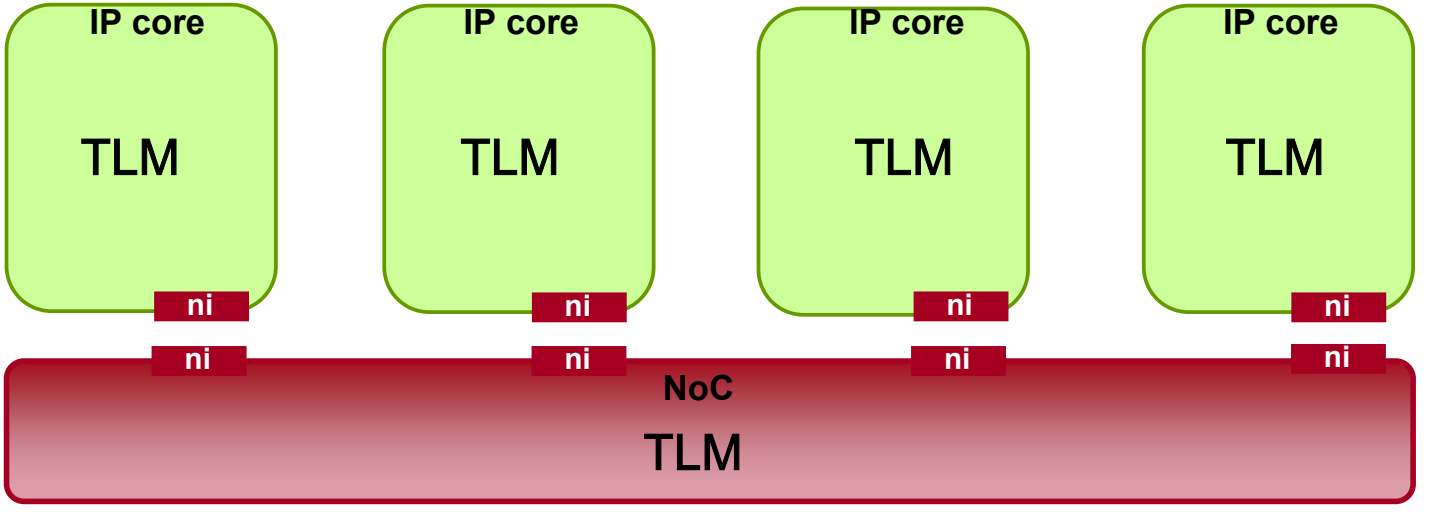
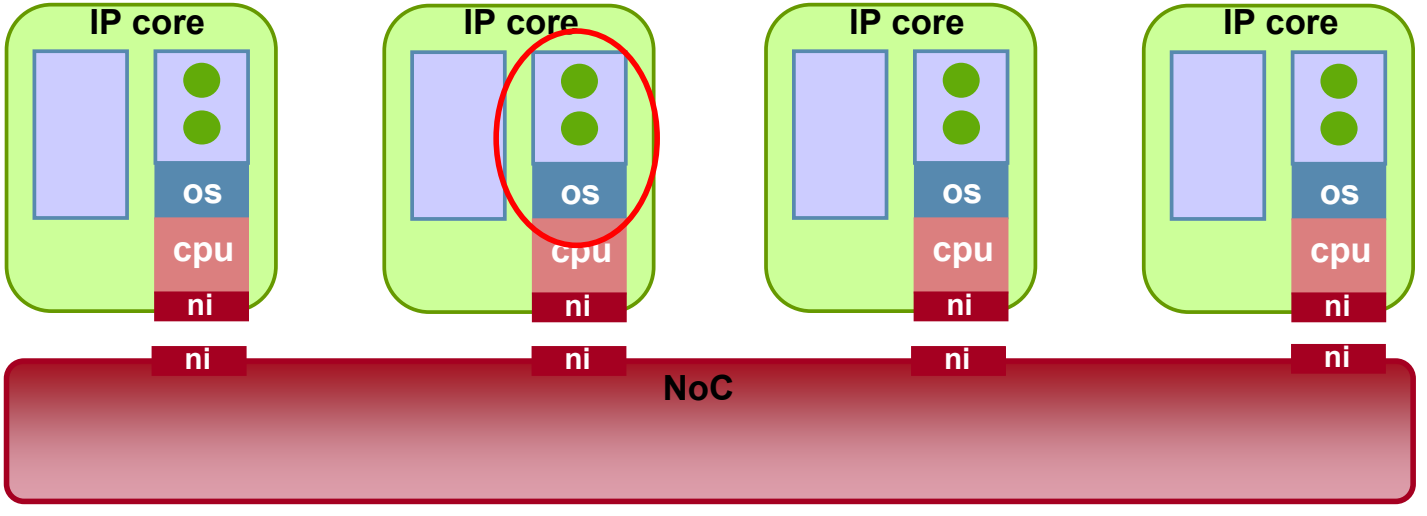
ARTS

- ARTS from TU Denmark
- Transaction-Level model
- Based on SystemC




IP core
os
cpu
ni
IP core
os
cpu
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NoC

ARTS System-on-Chip model

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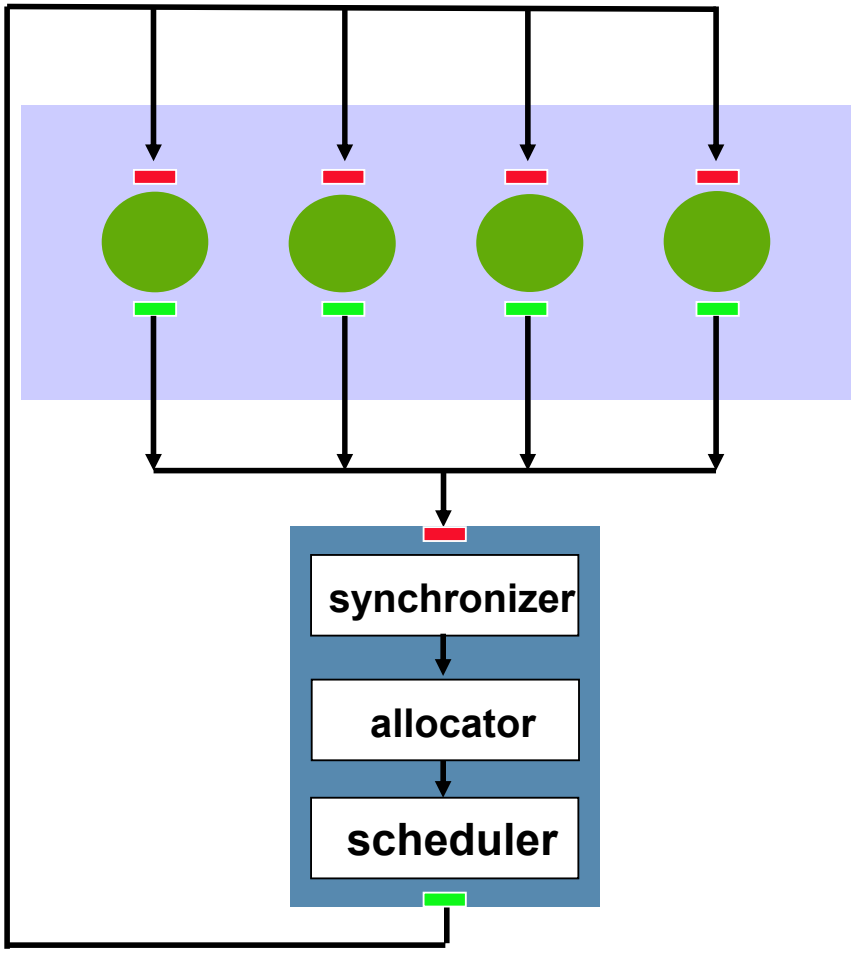

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ARTS Multiprocessor model

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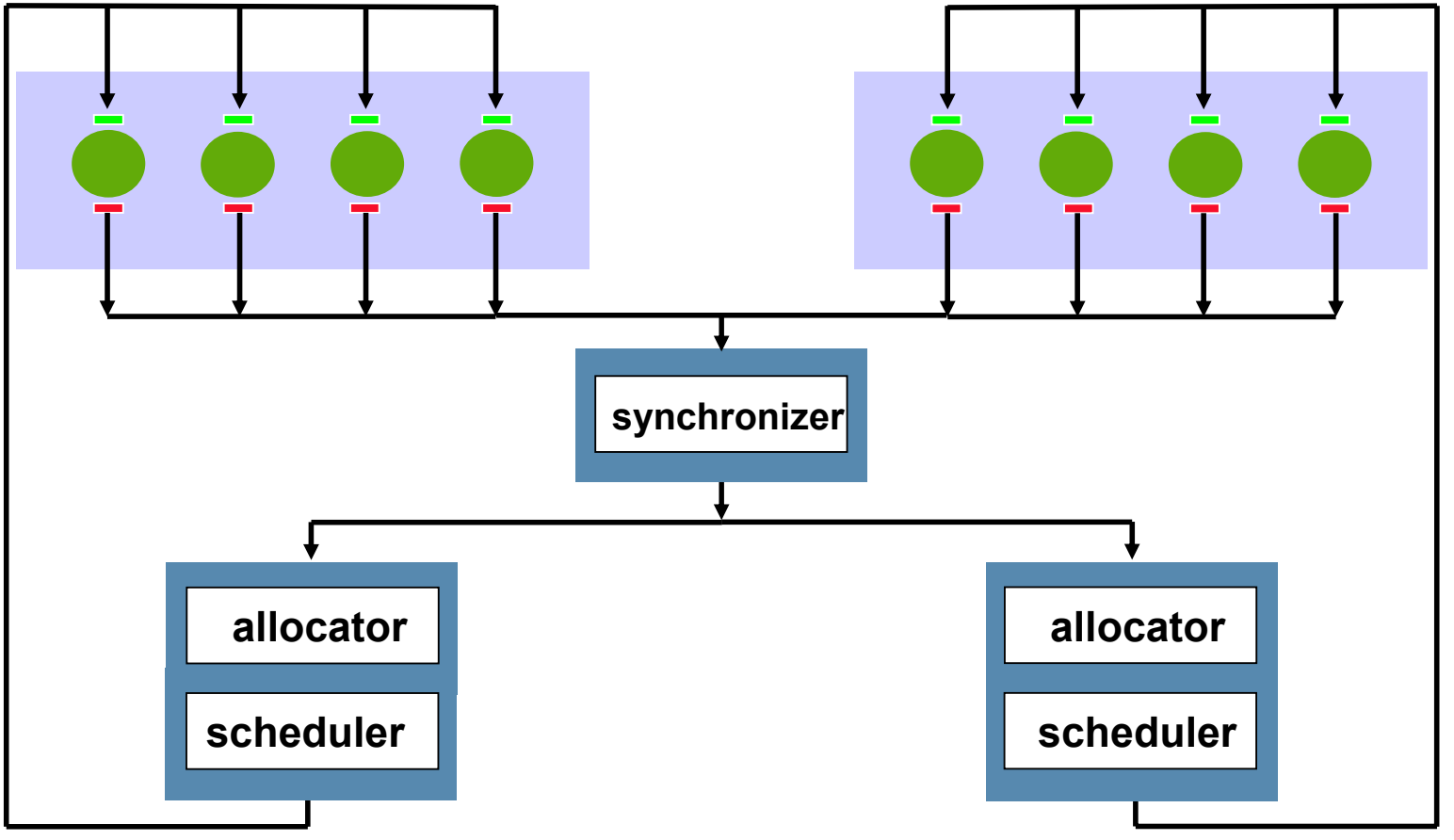

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MPARM/ARTS model integration

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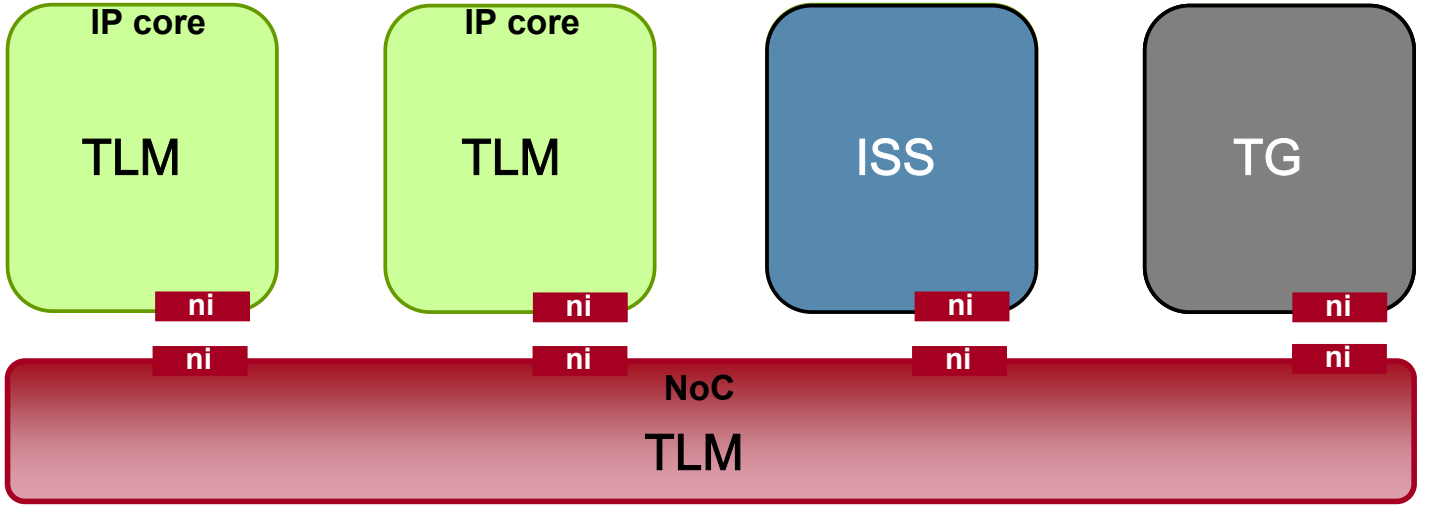
- Based on SystemC
- Separating cores and interconnects through OCP



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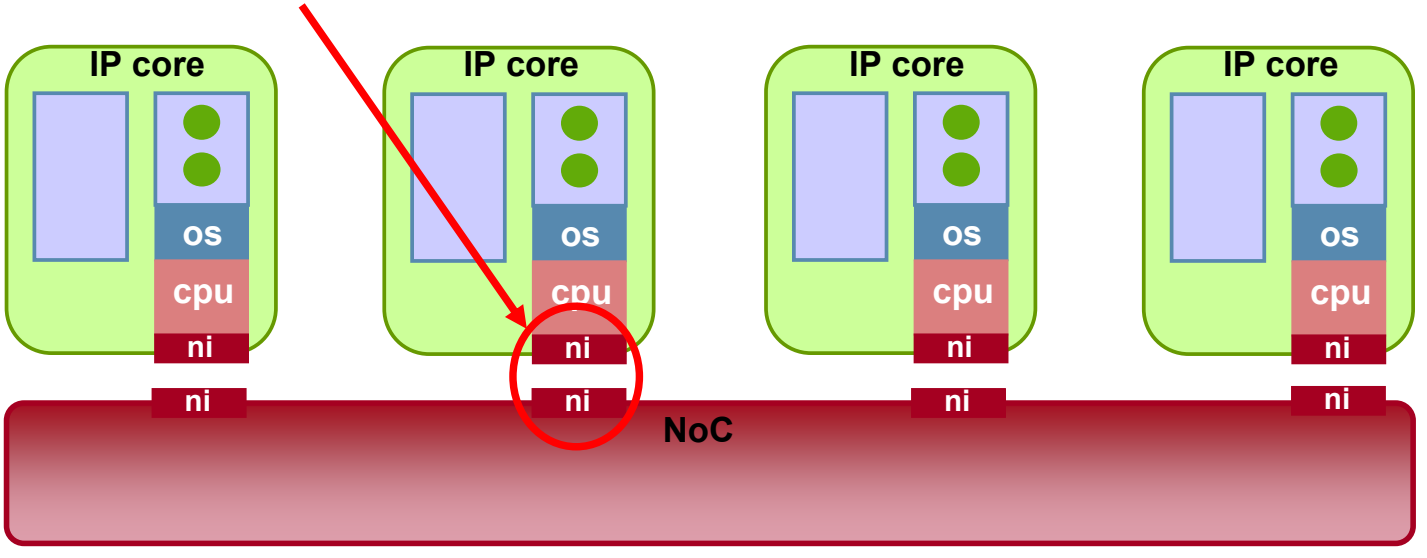
MANGO

Message-passing
Asynchronous
NoC providing
Guaranteed services through
OCP interfaces



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Wireless Sensor Networks

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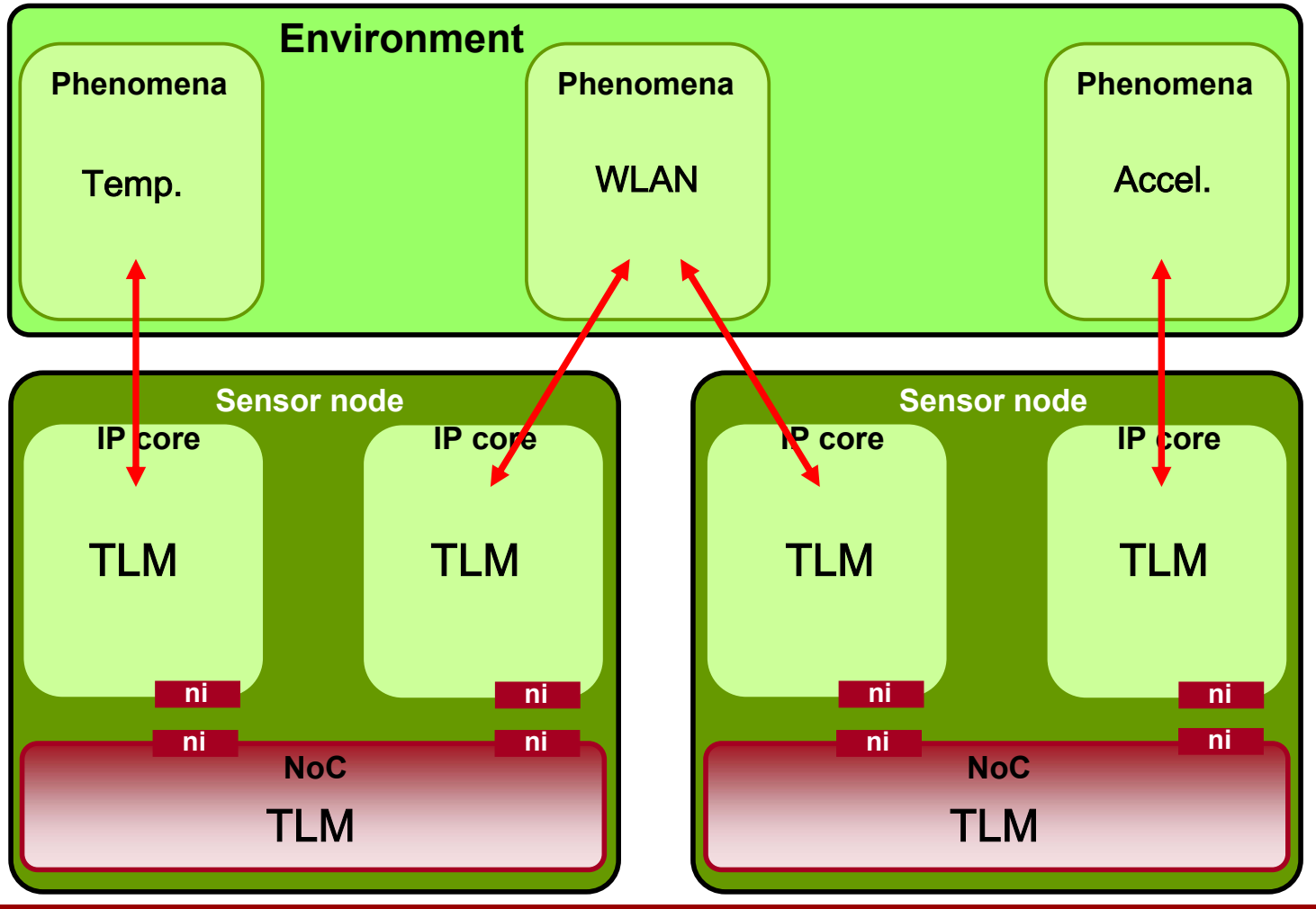

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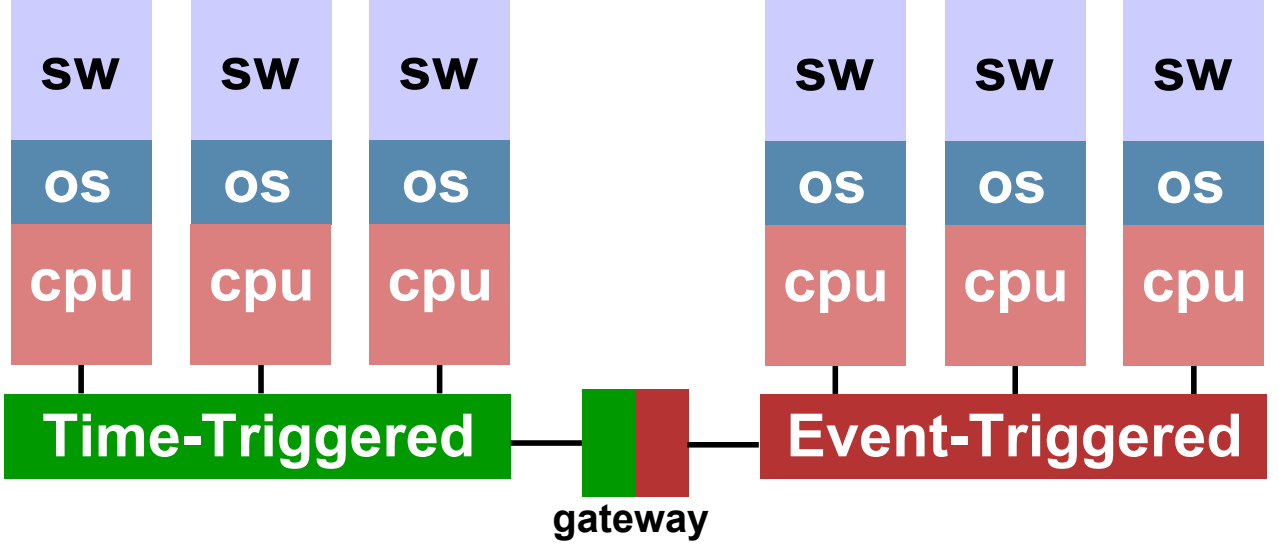
Automotive systems

- Comparison of protocols
  - FlexRay more pessimistic for worst case analysis?
  - Average throughput - quality of service?
- Fault tolerance
  - Simulate with fault injection



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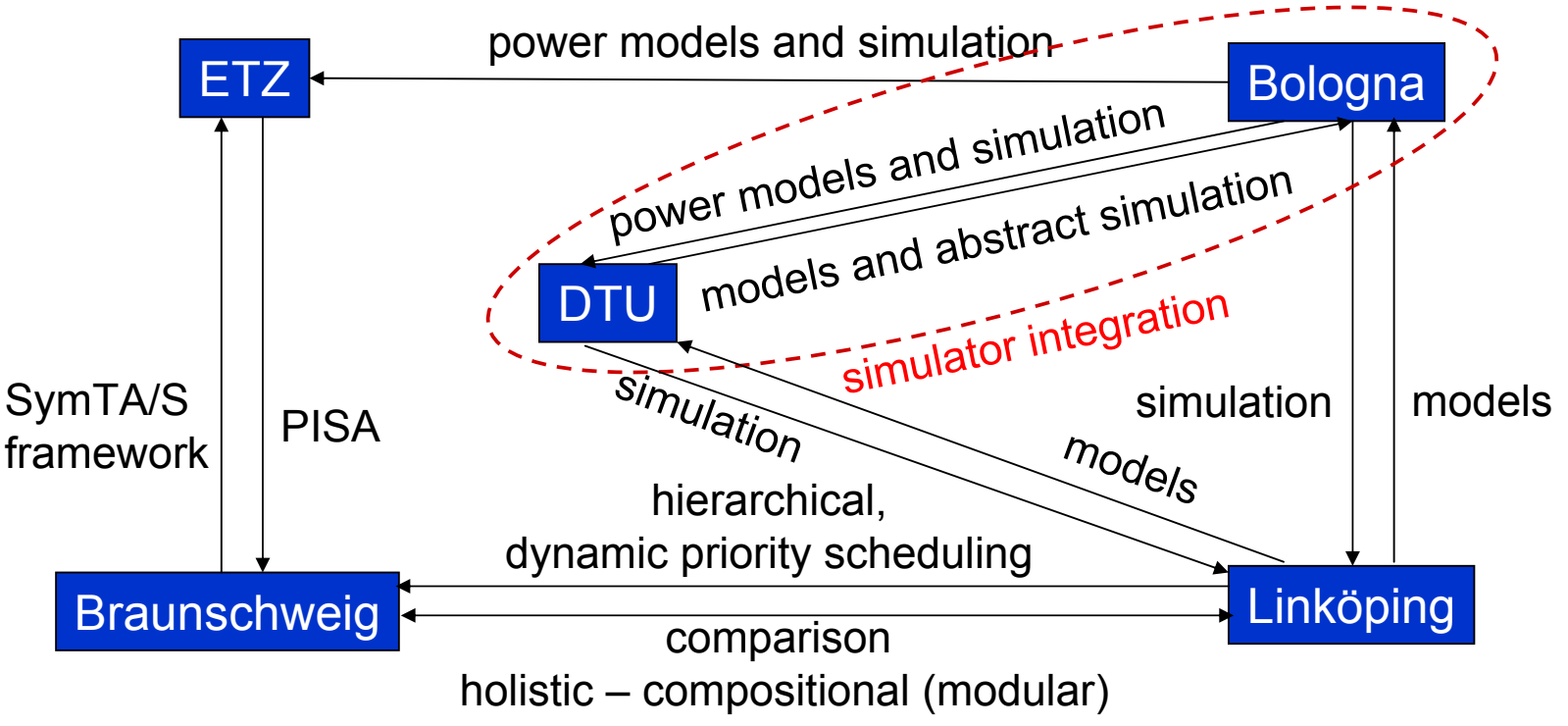

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Execution Platform Cluster

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