ARTIST 2

Network of Excellence

IST-004527 ARTIST2:
Embedded Systems Design

Activity Progress Report for Year 2

JPRA-Cluster Integration

Communication-Centric Systems

Clusters:

Execution Platforms

Activity Leader:

Prof. Dr. Rolf Ernst (IDA, TU Braunschweig)
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The activity assesses the state-of-the-art in models that take into consideration the particularities of various quasi-standard communication protocols during system analysis and scheduling. The communication infrastructure can be optimised in order to be adapted to the particularities of the implemented application. That meets a growing need in industry to consider formal techniques in embedded system design as a complement to traditional prototyping and simulation based approaches.

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1. Overview of the Activity

1.1 ARTIST2 Participants: Expertise and Roles

Prof. Lothar Thiele – TIK, ETH Zürich (Switzerland)
developing a calculus to describe the performance of communication-centric systems, unifying the models for computation and communication.

Prof. Petru Eles – ESLAB, Linköping University (Sweden)

schedulability analysis for heterogeneous distributed systems, communication synthesis.

Prof. Rolf Ernst – IDA, TU Braunschweig (Germany)
formal performance models for networks-on-chip.

Prof. Luca Benini – Micrel Lab, University of Bologna (Italy)
analytic and simulation based models for performance, power and area of NoCs.

Prof. Jan Madsen – Technical University of Denmark (Denmark)
power issues in network on chip architectures.

1.2 Affiliated Participants: Expertise and Roles

Dr. Fabian Wolf – Volkswagen AG (Germany)
Software integration under real-time constraints

Dr. Magnus Hellring – Volvo (Sweden)
Requirements analysis

Dr. Kai Richter – Symtavision (Germany)
Performance analysis of complex distributed systems

Prof. Sharon Hu – University of Notre Dame (USA)
Power analysis and optimization

1.3 Starting Date, and Expected Ending Date

Starting date: September 1st, 2004

Ending date: when the different techniques for integration have been successfully combined

1.4 Baseline

Formal communication modelling has been investigated by Zebo Peng and Petru Eles at Linköping University, Lothar Thiele at ETH Zurich (ETHZ) and Rolf Ernst at Braunschweig. The ETH Zurich and Linköping University have outstanding expertise in modelling and analysing packet flow communication and network processors (ETH) and conditional task graphs combined with statistical modelling. UoB is one of the most widely recognized centres of expertise in NoC design, analysis and road mapping. DTU has a long experience in asynchronous circuits design and in NoC design based on this technology. Embedded architectures and heterogeneous distributed embedded systems have grown to extremely complex computation and communication patterns. New performance models and a

corresponding theory are urgently needed Europe needs to develop skills to safely design such systems.

1.5 Problem Tackled in Year2

The industry increasingly applies hierarchical communication protocols, such as the automotive FlexRay Standard. Timing analysis has to follow that trend. Since system dependability and flexibility are growing demands in embedded systems, fault tolerance and robustness have to be included in communication modelling and optimization. Further case studies are needed to demonstrate the feasibility and practicability of the research results. Power optimization is a new and urgent requirement in mobile and streaming applications.

1.6 Comments from Previous Review

1.6.1 Reviewers' Comments

This task is focused on new best/worst-case models for hard real-time systems and on combined statistical and interval models for QoS applications in multi-media. Integrative efforts were progressed on a number of fronts.

The deliverable document describes the problems to be addressed, the current state of the art, what was achieved using ARTIST2 funds in the past year, and natural integrative next steps for the coming 12/18 months.

The document is accepted as is.

1.6.2 How These Have Been Addressed

There were no issues in the reviewers' comments, which needed to be addressed.

2. Summary of Activity Progress

2.1 Previous Work

Mixed Performance Analysis in Communication Centric Systems
In a first step, the SymTA/S tool framework that was initially designed to support only the evaluation methods designed at TU Braunschweig was extended with a dynamic library concept, such that different analytical libraries can be loaded into the tool to perform the system-level analysis of embedded systems. In a next step, at ETH Zürich, the formal analysis method Real-Time Calculus was implemented as a Java library that can be used from within the SymTA/S tool. This library was then integrated into the tool and can now be used for performance evaluation.

Hybrid Approach for Performance Analysis of Communication Centric Embedded Systems
After an initial meeting (3 days in Bologna) in March 2004 to discuss the possibilities for a joint effort towards this new approach and exchange the knowledge of the existing performance evaluation methods used, Simon Künzli spent 3 weeks in May 2005 in Bologna for the actual implementation of a case study using such a hybrid approach.

The existing simulation framework was extended by the interfaces needed for the proposed hybrid approach. Further, an example application was analyzed using the new approach. The hybrid analysis can be performed automated and exposes the expected speed-up for the simulation of embedded systems, with only a small deterioration of the accuracy of the results.

Performance Analysis in the System Design Process
In February 2004, Ernesto Wandeler spent 10 days at the ESI. During this time, an appropriate case-study system was identified and analyzed using a formal performance analysis method developed at TIK, ETH Zürich (Real-Time Calculus). Further, Ernesto Wandeler held 3 talks at ESI, to introduce people at ESI to the performance analysis research at TIK. In April 2005, Marcel Verhoef spent 5 days at ETH. During this time, a journal paper was written, based on a former conference paper. Further, new potential case-study systems, as well as plans for a performance analysis tool were discussed.

As a first case study, an existing distributed in-car radio navigation system was chosen and was specified in UML. For this case study, Real-Time Calculus was used to evaluate and compare 5 different potential system architectures. Sensitivity analysis was applied to all architectures to identify their robustness and potential bottlenecks. For the architecture that is actually used in the commercial implementation of the case study system, the robustness and the bottlenecks could be identified correctly using formal performance analysis methods.

Optimization and analysis of distributed embedded systems
Prof. Eles and his research group, University Linköping, have continued their work in the context of optimization and analysis of distributed embedded systems. They have concentrated on the following issues:

- Analysis of hierarchically scheduled systems
- Timing analysis of distributed task sets communicating through the FlexRay protocol
- Analysis and optimization of distributed embedded systems with fault tolerance requirements

Power analysis and optimization
To initiate the joint activity, Bren Mochocki, University of Notre Dame, spent 2 month at TU Braunschweig. During this time, interfaces between the power analysis tool developed at

University of Notre Dame and SymTA/S were created. Based on these interfaces SymTA/S could be extended with an analysis technique to determine the power consumption of a given embedded system. Since then the power models and the interfaces were regularly extended and refined.

On-chip interconnections for single-chip execution platforms

The work on communication-centric systems by the group of Prof. Madsen, Technical University of Denmark (DTU), has focused on on-chip interconnections for single-chip execution platforms. The starting point for this work has been the development of a clock less NoC architecture (MANGO) and a system-level NoC model based on the multiprocessor simulation environment (ARTS) developed at DTU. The MANGO NoC architecture is based on asynchronous message-passing and provides guaranteed services. Its interface is based on the standard OCP interface protocol which makes the architecture very suited for a modular SoC design flow. The use of a clockless circuit technique has a number of advantages, among which are; inherent global timing closure, low forward latency in pipelines, and zero dynamic idle power consumption. The ARTS modelling framework, which is developed as part of the System Modelling Infrastructure activity of ARTIST2, was extended with capabilities to model interconnect structures. At the system-level, the details of the processing elements and the NoC need to be abstracted in a way that allows for an accurate modelling of the global performance of the system, including the interrelationships among the diverse processors, software processes and physical interfaces and interconnections. To support the designer of single-chip based embedded systems, which includes multi-processor platforms running dedicated RTOS's, with the ability to analyse effects of on-chip interconnect network, the ARTS framework was required to support the analysis of network performance under different traffic and load conditions. This was achieved by extending the model with capabilities for NoC modelling.

Highly scalable communication architectures

The design objective was to develop a NoC targeting heterogeneous systems and featuring support for customizable, domain-specific NoC realizations. This implies designing Xpipes network building blocks as soft cores and to arbitrarily instantiate these blocks so to obtain custom-tailored irregular topologies. All Xpipes components were modelled in SystemC at the cycle accurate level, and integrated in an overall system simulation environment. Network interface was designed with the objective to allow frequency decoupling and efficient protocol conversion between system cores domain and network domain. Moreover, a standard OCP interface protocol with the cores was implemented to increase portability across different platforms. Links design was characterized by the concern to avoid limiting effects of signal propagation time on overall system clock period. This was achieved by providing support for link pipelining and latency-insensitive design. Finally, switch modules design followed the following guidelines: latency minimization, minimum impact of routing logic, output buffering to avoid head-of-line blocking, initial support for best-effort traffic only. Parameters that can be set at design time include number of switch input/output ports, buffer sizing, flit width, over clocking factor, etc.

High level modelling of system interconnects

High level models for system interconnects were at first derived for state-of-the-art busses, validated on a virtual platform and potentials for their deployment were explored. In particular, a cooperation with Linköping University paved the way for exploring different high level models for shared communication resources and for exploiting them within theoretical frameworks for efficient allocation, mapping and scheduling of tasks onto MPSoC hardware platforms. Specifically, we identified two modelling approaches to on-chip communication (additive models and coarse-grain modelling of communication tasks) and addressed the issue of modelling implicit communication in a predictive way (cache misses, semaphore polling). Then, we developed the theoretical framework taking the Benders Decomposition approach: an Integer Programming model to assign tasks to computation and storage resources and a

Constraint Programming model to schedule tasks onto processors. Non-feasible schedules generate a no-good for the IP problem, which is then re-iterated. The procedure is proved to converge to the optimum.

Hybrid system-level performance analysis approach
High level bus models can also be used for performance estimation. However, it is well known that formal models by themselves may turn out to be inaccurate for exploring the performance of complex multi-processor systems, because abstractions might fail to capture the system behaviour. Similarly, accurate simulation of the entire system might turn out to be infeasible due to the long simulation times. Therefore, we set up a cooperation with ETH Zürich with the objective to assess the efficiency of a hybrid approach: combining simulation and formal methods for system-level performance analysis. This approach enables a faster validation of the whole system in that we can decide to model a subcomponent of which the behaviour is well known through a formal analysis, whereas we can have a detailed low level and time-consuming simulation component modelling for other components. We described how the simulation models can be coupled with the formal analysis framework and showed the applicability of the approach using case studies.

2.2 Current Results

2.2.1 Technical Achievements / Outcomes / Difficulties encountered

Timing Analysis of the Flexray Protocol (University Linköping)

In the second year the Linköping group has continued the work regarding analysis and optimization of distributed embedded real-time systems, with application in automotive electronics. The main goal is to develop models and tools for the analysis and optimization of such communication-intensive systems. Emphasis is placed on the analysis of timing properties, considering the heterogeneous nature of such systems and the particularities of the various communication protocols. In the most recent research the analysis of mixed static/dynamic protocols, such as FlexRay, has been performed [PPE+06]. FlexRay is likely to become a standard for certain automotive applications and the elaboration of the first timing analysis approach for distributed systems built on FlexRay is of importance for our industrial partners. On top of these timing analysis approaches, various system-level optimization tools have been built, performing application mapping, communication synthesis, priority assignment, etc. The Linköping group has closely collaborated with our industrial partners at Volvo as well as with the Braunschweig group. The developed analysis approaches are under integration in the Symta/S environment developed at Braunschweig.

Fault Tolerance (University Linköping)

One other issue that has been explored by the Linköping group, in the same context of distributed communication-intensive real-time systems, is that of fault tolerance and, in particular, the issue of transient faults. There are two main aspects of interest here:

(1) Analysis of timing properties in the presence of faults and possible guarantees regarding worst case behaviour

(2) System optimization, such that timing and fault tolerance requirements are satisfied given a certain, limited amount of resources.

An approach for scheduling and worst case analysis with fault tolerance has been developed [IPE+06]. On top of this analysis approach, an optimization technique for task mapping and fault tolerance policy assignment has been elaborated and implemented.

Combination of performance analysis methods: SymTA/S and MPA (ETH Zürich)

Collaboration with Arne Hamann, University of Braunschweig

This new collaboration is based on collaborations between the two institutions from previous years, where we tried to identify the similarities and differences of the performance evaluation methods developed (a) at TU Braunschweig integrated in the SymTA/S tool, and (b) at ETH Zurich implemented as toolbox for modular performance analysis (MPA). With this analysis of the weaknesses and strengths of the various methods in mind, we believe that a combination of the methods leads to a significant improvement of analysis results. Especially for systems in which not all parts of the system can be analysed using a single technique due to limitations of the methods, we see the possibility to apply a combined approach which leads to good analysis results. After the analysis of the individual techniques, we are now looking at a common basic for such a combination, and analyse the implementation effort needed for a tool that supports both analysis techniques. The plan for the next months is to implement the changes needed for a combination and analyse an example application to show the strength of the new approach. These steps should also result into a joint publication of the results.

To achieve this, we intend to (1) apply the changes in the tools at each of the partner's sites, (2) organise an integration week where the two parts should be combined to form a single tool, (3) perform the analysis of an example system.

Performance Analysis of an In-Car Radio Navigation System (ETH Zürich)

Collaboration with Marcel Verhoef at Chess Information Technology, Embedded Systems Institute Eindhoven and Radboud University Nijmegen, and with Paul Lieverse at Siemens VDO
In this activity, we investigated an in-car radio navigation system that was specified in UML. Modular Performance Analysis with Real-Time Calculus was used to evaluate and compare 5 different potential system architectures, and sensitivity analysis was applied to all architectures to identify their robustness and potential bottlenecks. For the architecture that is actually used in the commercial implementation of the case study system, the robustness and the bottlenecks could be identified correctly using the above methods. First results on this research were published at the First International Symposium on Leveraging Applications of Formal Methods [WTVL06]. After this symposium, we refined the analysis of the case study system. Based on the case study system, we also compared a number of different performance analysis and simulation methods. Currently, a hardware test bed is implemented to compare the analysis results with measured results in different system architectures.

The results of the refined analysis, together with a thorough description of the applied analysis methods were published this year in a journal article [WTVL06]. The results of the analysis methods comparison and of the comparison to the measurements will be published in a future joint publication.

Sureal-Project: Hierarchical Event Models (TU Braunschweig)

The main goal of the Sureal Project is to define an integrated development process for distributed embedded real-time Systems, especially regarding real-time aspect in all phases of the development. This includes the integration of different techniques for describing, analysing and modelling real-time aspects. To be able to use different tools specialized in handling real-time aspects in different phases of the system development interfaces must be defined for them to efficiently work together.

Also the early prediction of the timing behaviour, the sensitivity and optimizing possibilities of the architecture play a very important role in such an integrated development process. The tool SymTA/S is capable of analysing such aspects but the underlying methods still have some limitations regarding specific system setups. Up to date, only task sets, which consist of tasks that are activated according to a standard event model can be analysed appropriately. To lift

this limitation, first steps towards exploring hierarchical event models are taken. Future Results will be integrated into SymTA/S to further enhance its applicability.

Power Optimization under Timing Constraints (TU Braunschweig)

Cooperation with Sharon Hu and Bren Mochocki from University of Notre Dame

Based on the power analysis extension to SymTA/S which was realized in cooperation with Bren Mochocki during the first project year, TU Braunschweig and University of Notre Dame implemented heuristic and stochastic power optimization algorithms using DVS and SVS (Dynamic/Static Voltage Scaling). The presented algorithms are applicable to complex distributed systems with complex timing constraints (maximum jitter, end-to-end deadlines, etc.), and are capable of determining Pareto-optimal design trade-offs between system power consumption and timing properties.

The heuristic power optimization approach is based on research of TU Braunschweig related to sensitivity analysis [RHE06], whereas the stochastic algorithms utilize the compositional SymTA/S design space exploration framework [HRJ+06].

The results of this activity lead to a joint publication at the International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES) [RHE+06].

Robustness Optimization for Distributed Embedded Systems (TU Braunschweig)

Based on the results achieved in the domain of sensitivity analysis [RHE06], TU Braunschweig developed techniques for optimizing the robustness of embedded real-time systems with respect to variations of system properties like worst-case execution/communication times, bus bandwidth, CPU clock rate, input data rate, etc. Reasons for such variation during the design process or in the field include updates, bug fixes, late feature requests, and product variants.

The developed algorithms consider hard-real time constraints and are capable of optimizing a given system for static and dynamic design robustness. Thereby, the static design robustness optimization approach is applicable to the design scenario where system parameters are fixed early in the design process, whereas dynamic design robustness optimization approach includes possible counteractions to unforeseen system property changes, and is thus applicable to reconfigurable systems.

The results of this research will be published at the International Conference on Hardware - Software Codesign and System Synthesis 2006 (CODES) [HRE06].

Flex Film: High-resolution Real-time Digital Film Applications (TU Braunschweig)

In the context of the FlexFilm project, TU Braunschweig developed a multi-board, multi-FPGA hardware/software architecture, for computation intensive, high resolution (2048x2048 pixels), real-time (24 frames per second) digital film processing. The architecture reaches record performance running a complex noise reduction algorithm (used both as example and proof of concept) including a 2.5 dimensions DWT and a full 16x16 motion estimation at 24 fps requiring a total of 203 Gops/s net computing performance and a total of 28 Gbit/s DDR-SDRAM frame memory bandwidth. This design was awarded with the "DATE2006 Design Record" distinction [LHR+06].

Simulation-based analysis of SoC interconnection architectures (University of Bologna)

Industrial MPSoC platforms exhibit increasing communication needs while not yet reverting to revolutionary solutions such as networks-on-chip. The limited scalability of shared busses is being overcome by means of multi-layer communication architectures. However, the complex interaction among system components and the dependency of macroscopic performance metrics on fine-grain protocol features stress the importance of highly accurate modelling and analysis tools. The work in this area has focused on developing

accurate functional model of multi-node on-chip interconnects, as they are currently deployed in high-complexity SoCs today.

Network-on-chip architectures (Technical University of Denmark)

In the second year the group at the Technical University of Denmark has further developed the NoC architecture called MANGO (*Message-passing Asynchronous Network-on-Chip providing Guaranteed services over OCP interfaces*). In particular the network core, i.e. the routers and links. MANGO is based on clockless circuit techniques, and thus inherently supports a GALS (*Globally Asynchronous Locally Synchronous*) type design flow. This is an advantage in large scale SoC design, since the distribution of a global clock is becomming increasingly difficult. MANGO employs virtual channels to provide connection-less best-effort routing as well as connection-oriented virtual circuits, for which service guarantees can be given. The predictability of guaranteed services is a way to promote system-level integrity. The MANGO architecture has been demonstrated through a circuit-level design of a 5x5 router using a 0.13 μm CMOS standard cell library from STMicroelectronics. Netlist simulations showed a performance of 650 Mflits/s under typical timing conditions [BS06]. Three patents [BS05] on the MANGO technology have been filed and a startup company, called Teklatech (www.teklatech.com), was formed as a spin-off from this research. Teklatech is developing a one-step EDA solution to achieving timing closure in large scale, globally synchronous, deep submicron ASIC designs.

Distributed wireless sensor networks (Technical University of Denmark)

Besides the further development for extending the capabilities of the ARTS system-level modelling framework towards the modelling of wireless sensor networks (reported under the System Modelling Infrastructure action), a sensor node development platform [VLMB05] has been developed, implemented and build. The aim of the platform is to explore hardware/software tradeoffs when designing the node behavior and to calibrate the developed system-level models with real design implementations. In order to efficiently utilize the limited resources available on a sensor node, key design parameters needs to be optimized which is only possible by making system-level design decisions about its hardware and software (operating system and applications) architecture.

Simulation-based analysis of SoC interconnection traffic (Technical University of Denmark and University of Bologna)

In Multi-Processor System-on-Chip (MPSoC) design stages, accurate modeling of IP behaviour is crucial to analyze interconnect effectiveness. However, parallel development of components may cause IP core models to be still unavailable when tuning communication performance. Traditionally, synthetic traffic generators have been used to overcome such an issue. However, target applications increasingly present non-trivial execution flows and synchronization patterns, especially in presence of underlying operating systems and when exploiting interrupt facilities. This property makes it very difficult to generate realistic test traffic. Technical University of Denmark and University of Bologna have jointly developed a reactive traffic generator device [MAMBS05] capable of correctly replicating complex software behaviours in the MPSoC design phase. The approach has been validated by showing cycle-accurate reproduction of a previously traced application flow. Even when tested under complex synchronization scenarios, including asynchronous interrupts involving OS interaction in a multiprocessor environment, the proposed traffic generator is able to reproduce IP traffic with full capability to express the application flow.

2.2.2 Publications Resulting from these Achievements

[PPE+06] Timing Analysis of the FlexRay Communication Protocol, Traian Pop, Paul Pop, Petru Eles, Zebo Peng, Alexandru Andrei. 18th Euromicro Conference on Real-Time Systems (ECRTS 06), Dresden, Germany, July 5-7, 2006, pp. 203-213

[IPE+06] Synthesis of Fault-Tolerant Schedules with Transparency/Performance Trade-offs for Distributed Embedded Systems, Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng. Design Automation and Test in Europe Conference (DATE 2006), Munich, Germany, March 6-10, 2006, pp. 706-711

[MBT+06] Clemens Moser, Davide Brunelli, Lothar Thiele, Luca Benini, Real-Time Scheduling with Regenerative Energy, 8th Euromicro Conference on Real-Time Systems (ECRTS 06), Dresden, Germany, July, 2006.

[WTVL06] Ernesto Wandeler, Lothar Thiele, Marcel Verhoef and Paul Lieverse: System Architecture Evaluation Using Modular Performance Analysis -- A Case Study. Software Tools for Technology Transfer (STTT), Springer, pages to appear, 2006.
[WTVL06] Ernesto Wandeler, Lothar Thiele, Marcel Verhoef and Paul Lieverse: System Architecture Evaluation Using Modular Performance Analysis -- A Case Study, 1st International Symposium on Leveraging Applications of Formal Methods (ISoLA), Paphos, Cyprus, October, 2004

[Pera06] Simon Perathoner, Evaluation and Comparison of Performance Analysis Methods for Distributed Embedded Systems, Masters Thesis, Computer Engineering and Networks Laboratory, ETH Zurich

[RHE06] Razvan Racu, Arne Hamann, Rolf Ernst, A Formal Approach to Multi-Dimensional Sensitivity Analysis of Embedded Real-Time Systems. In Proc. of the 18th Euromicro Conference on Real-Time Systems (ECRTS), Dresden, Germany, July 2006

[RHE+06] Razvan Racu, Arne Hamann, Rolf Ernst, Bren Mochocki, Sharon Hu, Methods for Power Optimization in Distributed Embedded Systems with Real-Time Requirements, In Proc. International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES), Seoul, Korea, October 2006

[HJR+06] Arne Hamann, Marek Jersak, Kai Richter, Rolf Ernst, A framework for modular analysis and exploration of heterogeneous embedded systems, Real-Time Systems, volume 33, pages 101-137, July 2006

[HRE06] Arne Hamann, Razvan Racu, Rolf Ernst, A formal approach to robustness maximization of complex heterogeneous embedded systems, In Proc. International Conference on Hardware/Software Codesign and System Synthesis (CODES), Seoul, Korea, October 2006

[LHR+06] Amilcar do Carmo Lucas, Sven Heithecker, Peter Rüffer, Rolf Ernst, Holger Rückert, Gerhard Wischermann, Karin Gebel, Reinhard Fach, Wolfgang Huther, Stefan Eichner, Gunter Scheller, A reconfigurable HW/SW platform for computation intensive high-resolution real-time digital film applications, In Proc. Design Automation and Test in Europe Conference (DATE), Munich, Germany, March 2006

[VLMB05] Virk, K., Leopold, M., Madsen, J., Bonnet, P., Hansen, M., *Design of A Development Platform for HW/SW Codesign of Wireless Integrated Sensor Nodes*, EUROMICRO Symposium on DIGITAL SYSTEM DESIGN, 2005.

[MAMBS05] Mahadevan, S., Angiolini, F., Madsen, J., Benini, L., Sparsø, J., *Realistically Rendering SoC Traffic Patterns with Interrupt Awareness*, in the proceedings of the IFIP International Conference on Very Large Scale Integration (VLSI-SoC), 2005.

[BS06] T. Bjerregaard and J. Sparsø. Implementation of Guaranteed Services in the MANGO Clockless Network-on-Chip. *IEE Proceedings: Computing and Digital Techniques*, Vol. 153 no. 4, July, 2006, pp 217 - 229.

[BS05] T. Bjerregaard and J. Sparsø. A network, a system and a node for use in the network or system, 2005. DK and US patents submitted, DK serial no. PA 2005 00306 and US no. 60/656,375.

2.2.3 Keynotes, Workshops, Tutorials

Workshop: Workshop on Distributed Embedded Systems

Leiden, Netherlands, November 2005

Collaboration with various research groups in the area of performance analysis of embedded systems.
There exist almost no results on comparisons of system level performance estimation and analysis methods for embedded systems in literature. One of the main problems that prevents such results is that there exists no consensus on how these methods should be compared. To overcome this problem, we co-organized an international workshop on distributed embedded systems. The workshop aimed to achieve three goals: first to identify issues and trends of system level performance estimation and analysis of distributed embedded systems, secondly to learn about existing system level performance estimation and analysis methods for embedded systems, and thirdly to establish a set of benchmark applications that can serve as basis for future methods comparisons.

To achieve these three goals, the workshop was split into three modules. During the first two days, a set of presentations from various researches served as basis for discussions on issues and trends of system level performance estimation and analysis of distributed embedded systems. On the third day, a number of existing analysis and estimation methods were discussed. Also on the third day, all attendees were invited to propose benchmark applications for method comparisons. Discussions on these applications led to a set of benchmark applications that were then published on a webpage. The fourth day was dedicated to experimenting with the various methods, and to obtaining first results on the set of benchmark applications.

After the workshop, we compared five existing performance estimation and analysis methods and tools, based on a part of the benchmark application set. These methods and tools were: Modular Performance Analysis with Real-Time Calculus, SymTA/S, MAST, Timed Automata with UppAal, and SystemC simulation. The results of this comparison were published in a Masters Thesis [Pera06]. In future, we plan to publish an article on the methods comparison, together with Rolf Ernst from TU Braunschweig.

http://www.tik.ee.ethz.ch/~leiden05/

Workshop: Design Issues in Distributed, Communication-Centric Systems

DATE Conference, Munich, Germany, 10.3.2006

Organisers: Bruno Bouyssounouse, Rolf Ernst, Lothar Thiele

The workshop presented relevant, innovative, and holistic topics in communication-centric systems, sensor networks, dynamic real-time architecture, distributed computing, minimal operating systems, and self-organisation.

http://date.eda-online.co.uk/2006/prog/index.php?id=42

Workshop: New approaches to WCET analysis

York, England 30.7.-5.8.2006

Organisers: Jan Staschulat, Technical University of Braunschweig, Guillem Bernat Rapita Systems.

The workshop was set up to discuss new approaches to WCET analysis. In particular synergy effects between the SymTA/P and the RapiTime approach were examined.

Workshop: Robustness Optimization and Scheduling Anomalies

Linköping, Sweden, August 2006

Organisers: Petru Eles, Arne Hamann, Razvan Racu

During the workshop recent results of TU Braunschweig concerning system robustness optimization and the detection of scheduling anomalies were presented and discussed. Additionally, a cooperation in the field of simulation pattern generation based on the scheduling anomalies detection algorithms was discussed.

Tutorial: Introduction to Sensor Networks
ARTIST2 PhD Course, University of Linkoping, Sweden, May 2006

Speaker: Jan Madsen and Srdjan Capkun from DTU.

Phd course on wireless sensor networks. Organized in cooperation between DTU and Linkoping. Participant were from both academia and industry, mainly from Sweeden.

Sensor networks have become more and more popular as a solution to various large scale networked applications in very diverse areas. This course is an introduction to the problematic of sensor networks. The course addresses issues such as deployment and localization, routing protocols and operating systems for wireless sensor networks, design methodologies and security issues.

http://www.ida.liu.se/~petel/SN/

Tutorial: Supporting Predictable Design Using Formal Analysis Techniques
ARTES Summer School, Nässlingen, Sweden – August, 2006

ARTES is a Swedish network for real-time research and graduate education, which annually organizes a summer school for leading researchers and graduate students in real-time systems.

The tutorial presented the state of the art in formal performance verification (task and system level), and explained how these techniques can be used to design predictable systems using sensitivity analysis and robustness optimization algorithms.

http://www.artes.uu.se/events/summer06/

Tutorial : Frameworks for System-Level Analysis of Real-Time Systems - Symta/S and MPA
Real-Time and Embedded Technology and Applications Symposium (RTAS), *San Jose, USA – April, 2006*

RTAS is the leading international conference in real-time applications and is co-located with the Embedded Systems Conference.

System-level timing, performance, and power become increasingly intractable as the interactions between system parts introduce complex dynamic behaviour that can not be fully overseen by anyone in a design team. It is agreed that appropriate analysis tools are urgently needed. However, today's dynamic design processes require flexible and extensible tool suites that can cope with and be adapted to changed objectives and new requirements. Furthermore, the trend towards IP reuse and black-box integration introduces another type of complexity as it requires clear interfaces and must cope with only partially available information.

The tutorial addressed recent research on composable and extensible analysis methods, and tools that demonstrate the application in practice. The tutorial was targeted to embedded system architects, component designers, and integrators as well as researchers in these fields.

http://www.rtas.org/rtas2006/workshop.htm/

Mini-Keynote: Modular Communication-Centric MPSoC Architectures
MpSoC Summer school, Estes Park, Colorado, August 2006

Speaker: Rolf Ernst

The keynote presented distributed memory access analysis techniques for MPSoC modelling and analysis to leading researchers and industrial managers in System-on-Chip design.

http://tima.imag.fr/mpsoc/

3. Future Work and Evolution

3.1 Problem to be Tackled over the next 18 months (Sept 2006 – Feb 2008)

TU Braunschweig and ETH Zürich

The plan for the next months is to implement the changes needed for a combination and analyse an example application to show the strength of the new approach. These steps should also result into a joint publication of the results.

ESLAB Linköping

1. Further development of optimization approaches for systems built on heterogeneous communication protocols, in particular, Flexray.
2. Further development of the analysis and optimization techniques for fault-tolerant distributed systems.

These techniques will be incorporated into the tools developed by the various partners, in particular, Symta/S in Braunschweig.

TU Braunschweig

1. Further research in the extension of the SymTA/S model with hierarchical event models.
2. Development of advanced techniques for system robustness optimization. This would leverage the applicability of the SymTA/S methodology for reliable and predictable embedded system design.
3. Development of mapping optimization approaches with automatic communication synthesis.
4. Refinement and further development of semantical extensions for formal analysis of MPSoCs with focus on shared memory accesses. This includes the coupling of the tools SymTA/S und SymTA/P (both developed at TU Braunschweig). This activity could profit from synergy effects with 1.

University of Bologna

1. Network-on-chip architecture exploration: a more modular and scalable system-inteconnect architecture development approach will be studied in details, along with cross-benchmarking against traditional system interconnects

Technical University of Denmark

1. Further development of network-on-chip architectures and exploration at both circuit and system level. Development of NoC benchmarks and conducting comparative NoC studies.
2. Further development of communication models for distributed embedded systems, in particular wireless sensor networks and fault-tolerant distributed systems.
3. Development of mapping approaches which explores optimized communication architectures in terms of metrics like performance, power consumption, cost and fault-tolerance.

3.2 Current and Future Milestones

- ETH Zürich and Technical University of Braunschweig will pursue their efforts for creating a mixed performance analysis approach using SymTA/S and Real-Time Calculus. Final objective is the creation of a real-time calculus based library for SymTA/S allowing a per component analysis of heterogeneous distributed systems (i.e. parts of the system are evaluated using real-time calculus, whereas others are evaluated using SymTA/S). This requires interfaces between the two methods.

  Further discussions were performed during the last month and the interfaces required for coupling the two methods are currently refined in an iterative process. Until the end of this year ETH Zurich and TU Braunschweig will organize an integration week to finish the coupling process.

- ETH Zürich and Embedded Systems Institute Eindhoven will further investigate strengths and weaknesses of different performance analysis methods in the system design process.

  ETH Zurich and ESI Eindhoven successfully demonstrated in a case study how performance analysis techniques can be utilized in the development process of realistic embedded systems. The results of this case-study were published in [WTVL06] (see Section 2.2.1).

  Additionally, ETH Zurich published a master thesis (as a result of the Workshop on Distributed Embedded Systems in Leiden, November 2005) comparing strength and weaknesses of leading performance estimation and analysis methods [Pera06] (see Section 2.2.1). Currently, ETH Zurich and TU Braunschweig plan to publish an article on the method comparison results.

- Technical University of Braunschweig and University of Notre Dame will extend the existing power analysis to more detailed processor models and arbitrary scheduling policies and create power optimization methods (stochastic and heuristic) based on these models.

  TU Braunschweig and University of Notre Dame extended the power analysis and processor models and successfully developed two power optimization techniques for distributed embedded systems with complex timing constraints. The results of this research will be published in [RHE+06] (see section 2.2.1).

- University of Linköping will investigate analysis and optimization techniques for distributed embedded systems with fault tolerance constraints. Therefore, systems in the presence of transient faults will be considered to address the following issues:
  - Scheduling with the requirement that deadlines are satisfied even in the presence of transient faults.
  - Task mapping and optimisation of checkpoints.
  - Study of various trade-offs, such as transparency vs. schedule length.

  University Linköping developed an approach for scheduling and worst-case analysis with fault tolerance. Additionally, University Linköping developed and implemented an optimization technique for task mapping and fault tolerance policy assignment. The results of this work were published in [IPE06] (see Section 2.2.1).

- University of Linköping will continue their work in analysis and optimization of communication protocols from the automotive industry. In particular the emerging Flexray protocol will be considered.
  University Linköping developed a formal analysis technique for the Flexray communication protocol. The results were published in [PPE+06] (see Section 2.2.1).

- Technical University of Denmark and University of Bologna will continue their integration work combining ARTS and MPARM for NoC exploration.

Technical University of Denmark and University of Bologna have jointly developed a reactive traffic generator device capable of correctly replicating complex software behaviours in the MPSoC design phase. The results of this work were published in [MAMBS05] (see Section 2.2.1).Furthermore, two joint journal publications have been submitted and are currently under review

- ETH Zürich and University of Bologna will continue their work unifying analytic methods and simulation (hybrid performance evaluation approach). They will also investigate energy driven scheduling policies in the context of sensor networks.

  ETH Zürich and University of Bologna worked on efficient scheduling algorithms for sensor networks with regenerative energy sources. First results of this work were published in [MBT+06] (see Section 2.2.1).

- University of Bologna will perform a crossbenchmarking of the Xpipes architecture with state-of-the-art interconnects, considering performance, area and power. Based on the obtained results the Xpipes architecture will be tuned to improve weaknesses and to allow an industrial deployment.
- In the context of the effort spent on the high-level modelling of system interconnects, University Bologna will augment the underlying methods to account for variable voltage/frequency processor cores. The main intention of this refinement is the determination of optimal voltage and frequency assignments for system power minimization.

3.3 Indicators for Integration

As a result, we will have developed an important prerequisite for the design of embedded systems, namely analytic methods to estimate system properties. In particular, the approaches followed so far in the context of Hard Real Time and Embedded System Design Communities will be integrated and related to each other.

3.4 Main Funding

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- BMBF (Bundesministerium für Bildung und Forschung)