ARTIST 2
Network of Excellence

IST-004527 ARTIST2:
Embedded Systems Design

Activity Progress Report for Year 2

JPRA-Cluster Integration
Design for Low Power

Clusters:

Execution Platforms

Activity Leader:

Luca Benini (DEIS Università di Bologna)
http://www-micrel.deis.unibo.it

Policy Objective (abstract)

Power dissipation has become one of the most serious obstacles in the evolution of electronic systems. Historically, the transition from one CMOS technology generation to the next has been accompanied by a jump in power density, as well as increased active-state and stand-by power consumption. Furthermore, mainstream architectural design is moving towards energy-hungry programmable/configurable architecture meeting ever-increasing performance requirements. It is the objective of this activity to develop, promote and integrate methods that address power and energy issues across several layers of abstraction.

Table of Contents

1. Overview of the Activity 3
1.1 ARTIST2 Participants: Expertise and Roles 3
1.2 Affiliated Participants: Expertise and Roles 3
1.3 Starting Date, and Expected Ending Date 3
1.4 Baseline 4
1.5 1.1 Problem Tackled in Year2 4

2. Summary of Activity Progress 6
2.1 Previous Work 6
2.2 Current Results 7
2.2.1 Technical Achievements / Outcomes / Difficulties encountered 7
2.2.2 Publications Resulting from these Achievements 11
2.2.3 Keynotes, Workshops, Tutorials 12

3. Future Work and Evolution 14
3.1 Problem to be tackled over the next 18 months (Sept 2006 – Feb 2008) 14
3.2 Current and Future Milestones 14
3.3 Indicators for Integration 15
3.4 Main Funding 16
3.5 Internal Reviewers 16

1. Overview of the Activity

1.1 ARTIST2 Participants: Expertise and Roles

Team Leader: Luca Benini - University of Bologna (Italy)

(i) development of power modeling and estimation framework for systems-on-chip.
(ii) Development of optimal allocation and scheduling techniques for energy-efficient mapping of multi-task applications onto multi-processor systems-on-chips.
(iii) Development of energy-scavenging techniques for ultra-low power sensor network platforms.

Team leader: Petru Eles – Linköping University (Sweden)

development of optimization approaches for energy efficient, time constrained embedded systems; communication synthesis for energy-efficient real-time and fault-tolerant applications implemented on SoC; low power scheduling with voltage scaling and body biasing.

Team Leader: Jan Madsen - Technical University of Denmark (Denmark)

(i) *development of low-power asynchronous circuit design, in particular for efficient Network-on-Chip structures,*
(ii) development of multi-objective optimization approaches for exploring the mapping of multitask applications onto multiprocessor System-on-Chip,
(iii) experience in design and modeling of wireless sensor network platforms.

Team Leader: Lothar Thiele – ETH Zurich (Switzerland)

(i) *Combining scheduling methods with energy constraints,*
(ii) extensive experience in performance analysis for real-time embedded systems and interface-based approaches,
(iii) experience in building and deploying sensor network platforms.

1.2 Affiliated Participants: Expertise and Roles

Team Leader: Roberto Zafalon – STMicroelectronics (Italy)

(i) Provides an up-to-date view on industrial requirements for low-power system-on-chip platforms.
(ii) Makes available to the activity's participants up-to-date information on the power dissipated in current and up-coming advanced CMOS technologies, as developed by STMicroelectronics.
(iii) Provides information on applications and architecture trends in the market of consume multimedia silicon platforms.

Team Leader: Salvatore Carta – Università di Cagliari (Italy)

(i) *Cooperates with the cluster's participant on the development of power analysis and modeling techniques for on-chip interconnects (networks-on-chip).*
(ii) Provides competences and reference flows for back-end design issues (power issues arising from low-level design – logic design, placement, routing, etc.)

1.3 Starting Date, and Expected Ending Date

Starting date: September 1st, 2004.

Ending date: the activity will span the duration of the project, and continue beyond the end of the project. This is because all current trends indicate that low power design will increasingly

become a primary concern and focus of action for researchers, designers and developers working on embedded systems.

Moreover, the integration achieved by this activity is creating the know-how and the skills required for the definition of new research and development initiatives. As a result, all partners are already actively involved in long term funded research programs in low power design, whose end-date is beyond the duration of ARTIST2.

1.4 Baseline

The group of Luca Benini at the **University of Bologna** (UoB) is one of the leading centers in low power design, focusing on system level power management both from the architectural and from the software viewpoint. In this area, the group has produced a large number of contributions on OS-Based-dynamic power management, memory and communication architecture optimization for low power consumption, low power circuit design, battery-driven power management.

One of the baselines contributions of UoB to the project is a complete power modeling infrastructure both for all components of current MPSoC Platforms and for future Network-on-Chip-based platform.

More recently, UoB has focused on power optimization techniques for multi-processor systems on chip, with special emphasis on static and dynamic power management through voltage and frequency setting.

The group of Jan Madsen at the **Technical University of Denmark** (DTU) aims at low-power techniques for wireless sensor networks, and it brings significant experience on low-power asynchronous circuit design, as well as analytic and stochastic modeling of power consumption and battery usage. They have developed exploration methods for mapping applications onto heterogeneous multiprocessor platforms based on a multi-objective optimization framework from ETH Zurich, where one of the objectives is power consumption.

The group of Petru Eles at **Linkoeping University** (LIU) has given important contributions on high-level system modeling of both power and reliability, and on optimization techniques for energy efficient mapping of applications on execution platforms. They have developed approaches for energy efficient implementation of both hard and soft real-time systems.

The group of Lothar Thiele at **ETH Zurich** (ETHZ) has a long standing experience in the area of sensor networks. In particular, a low power platform including hardware, operating system, middleware and various applications has been developed (BTnode). It is used by many research groups worldwide. Together with the experience in real-time systems and scheduling, this is the basis for the joint effort in the design of low power massively distributed systems.

1.5 Problem Tackled in Year2

The high-level objective of the activity is the investigation of a comprehensive hardware-software power analysis and optimization approach for single and multi-processor embedded systems.

More specifically, in Year2 several relevant issues in this domain have been tackled:

(1) Power modeling for complex SoC platforms. The main objective here is to develop power models that provide a high-level view of the power consumed by a complex SoC platform to both the hardware architect and the software developer. In this area, the

most critical challenge is to provide reasonably accurate power and energy consumption information at the high level of abstraction typically adopted during architecture and software design. In Year1 the basic elements for a system-level power estimation framework have been integrated. In Year2, the focus has been on modeling system components at different level of abstraction and on improving the generality of the power modeling framework to support more complex platforms with multi-hop interconnects and multiple frequency and power domains.

(2) Power optimization via system-level resource allocation and scheduling. The main objective here is to develop techniques for optimally mapping multi-task (parallel) applications onto System-on-chip (SoC) platforms with multiple processors (MP-SoCs). This is an industry-relevant problem, as most high-end embedded computing platforms in a number of target markets (automotive, multimedia, networking) are evolving toward multi-core architectures. The most critical challenge in this area is the complexity of the problem of optimally mapping tasks onto cores (and storage resources), while selecting frequency and voltage assignments for the various cores. The focus in Year2 has been on a “static allocation” approach that assumes the knowledge of application workload requirements. The issue of both hard and soft real-time systems has been addressed.

(3) Scheduling based energy optimization for energy-scavenging wireless sensor networks. Sensor networks are an increasingly important class of distributed embedded systems. Wireless sensor networks are strategic enablers for a number of “ambient intelligence” applications, such as environmental monitoring, monitoring of body functions, tracking of people and objects. The main objective tackled here is the development of novel techniques for scheduling activities on sensor network nodes depending on the availability of environmental energy. The end goal is to enable sustainable environmentally powered operation for sensor networks. In year two, the main focus has been on the new class of energy-harvesting devices. In this case, the available energy is replenished, e.g. by the use of solar cells or other harvesting devices. In year 2, we have been investigating the (optimal) task scheduling problem under the energy-harvesting model. Here, the expertise of the research groups in Bologna and ETH Zurich has been combined towards the first result in this quickly growing area.

2. Summary of Activity Progress

2.1 Previous Work

Work performed in months 1-6

Bologna University has worked on interconnect optimization techniques for low power. Several schemes have been developed to instantiate application (platform) specific interconnect architectures for minimum energy consumption. An algorithm for automatic instantiation of multi-hop busses which includes topology generation and bus frequency assignment has been developed in collaboration with Penn State University. Additionally several extensions to the power modeling infrastructure in the MPARM virtual platform simulators have been developed, including the model for variable frequency and variable voltage cores, as well as a prototype model for estimating the power consumption of IOs and external memories (this work has been performed in cooperation with associate partner STMicroelectronics)

Linkoeping University has developed a technique for static routing on NoC, with guaranteed delays and arrival probabilities in the presence of transient faults. The approach is based on schedulability analysis of tasks and messages with priority based arbitration. For fault-tolerance, a combination of spatial and temporal redundancy is considered. Reduced communication energy is one of the goals. More recently the analysis of the worst-case buffer space needed has been performed. Based on this analysis, it is possible to develop an approach to buffer space minimization in the context described above.

Technical University of Denmark has started the development of a generic sensor network platform (Hogthrob project) which allows to tradeoff hardware and software implementations of the various components of the platform. So far, the focus has been on: (1) Processor design: Low-power design techniques have been investigated, included low-power synthesis (e.g., clock-gating), power modes and de-synchronizing in the context of the OpenCores AVR core (2) Power modeling: Simulation-based power modeling and estimation techniques have been investigated. This involves analytic and stochastic modeling of batteries and investigation into the macromodeling of various hardware components.

Work Performed in Months 7-12

Bologna University has started a research effort on energy aware mapping of multi-task applications on multi-processor SoC execution platforms. The approach is based on variable-voltage processors where execution speed and voltage supply can be independently adapted to the processor's workload. The first result of this effort has been a design space exploration technique that automatically finds Pareto points in the power vs. throughput design space. The technique has been tested on streaming-like signal processing applications.

Linkoeping University's most recent efforts are aiming at a more accurate modeling of actual communication and memory techniques used in MP SoC. Such an accurate modeling is needed in order for a system level analysis and optimization to produce useful results. Thus, work is concentrating on: (1) Capturing the background communication due to cache misses in system level models. (2) Capturing the bus load due to system-wide synchronization. Once these modeling issues are solved, different optimization techniques can be used for e.g. task mapping and scheduling, as well as voltage selection. Results can be validated using accurate and fast simulation in the environment developed at Bologna. Another issue which has been tackled is that of efficient optimization techniques based on advanced constraint solving and mathematical programming techniques. This work has been performed in cooperation with the group at University of Bologna.

In the framework of the research on low power wireless sensor networks (Hogthrob Project), the focus of the Technical University of Denmark has been on: (1) Processor design: DTU is currently investigating architectures for bit compression and bit-serial computation in the context of the BitSNAP core. (2) Power modeling: development of a sensor network power model within the UppAal model checking environment which allows for a formal analysis of power consumption within the network. (3) Empirical power estimation: Based on the prototype sensor network platform developed within Hogthrob, various testbench programs have been run on an AVR core synthesized on the FPGA and a number of physical measurements have been conducted. Finally, DTU has initiated the investigation on how the power modeling and the sensor network modeling can be captured within the multiprocessor simulation environment, ARTS, developed at DTU.

2.2 Current Results

2.2.1 Technical Achievements / Outcomes / Difficulties encountered

Power modeling for complex SoC platforms

The activity has focused on extending system-level energy analysis to highly integrated MPSoC platforms with segmented bus architectures, where the efficiency of bridges and protocol/frequency/size converters comes into play to determine the performance of the system interconnect. We leveraged a close cooperation with associate member STMicroelectronics which provided the models, traffic generators, system specifications and performance requirements. Platforms based on the on-chip communication protocols STBus, AMBA AHB, AMBA AXI-have been modeled and simulated at a very high level of accuracy (cycle-accuracy and bus-signal-accuracy), and compared with mixed AHB/AXI platforms

The original MPARM platform allowed the modeling and simulation of single-node

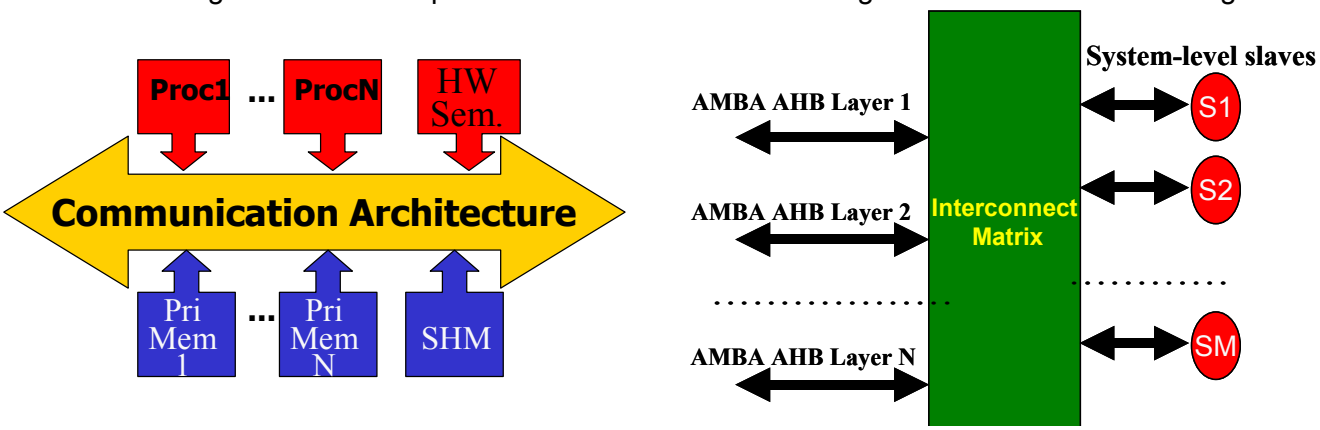

Fig 1 (a) Baseline single-node shared bus platform (b) advanced multi-layer interconnects

communication architectures (as depicted in Fig.1a). The platform was enhanced with the possibility to extend the modeling capability to a multi-layer architecture, as illustrated in Fig.1b. The first scenario corresponds to low-end real-life platforms, where AMBA AHB, AMBA AXI or STBus are the architectures of choice to accommodate on-chip communication. The MPARM platform can also instantiate a NoC as the communication fabric, by wrapping the masters and slaves with the proper network interfaces. In general, all cores can be wrapped with the native

bus interface. More complex MPSoC platforms adopt the communication architecture depicted in Fig.1b. It is a hierarchical infrastructure, where communication takes place at a first level of the hierarchy in the local AMBA AHB layers, and at a second level with the system-level slaves. The AMBA Multi-Layer specification introduced the notion of the interconnect matrix first, by envisioning point-arbitration at the destination slaves. This solution is quite interesting, since it allows a larger scalability than single-node solutions. Unfortunately, fabrication problems arise when the number of input layers increases a lot, since the implementation of the interconnect matrix is mostly combinational. This gives rise to clock frequency limitations and to layout unpredictability. As the level of integration of MPSoCs increases, the illustrated structures cannot satisfy communication requirements any more.

A further increase in communication scalability is exposed by segmented architectures, where a number of busses are interconnected with each other by means of bridges. In this case, the congestion on each bus is greatly decreased, thus favoring lower bus access times, but the latency of bus transactions can be seriously increased because of the multiple steps needed to reach a slave located on a different bus. Bridge traversal latency can significantly contribute to overall communication latency. Similarly, the use of bridges raises power concerns. The use of bridges helps to relieve the scalability limitations of traditional communication architectures, however the associated cost consists of the design of a complex IP block (the bridge itself) which is far from trivial and which can significantly affect system performance and energy. Many times, bridges do not perform only protocol conversion, but also size and frequency conversion. In fact, cores with homogeneous characteristics (i.e., clock frequency, data and address bus width) are typically grouped in the same node, therefore each “segment” of the global communication architecture turns out to be a domain with distinctive features. This obviously increases the bridging cost, since up/down size conversions or frequency conversions all take clock cycles to be carried out.

Another issue concerned the porting of traffic generators in order to make the simulation of complex systems in reasonable time possible. Moreover, this allowed overcoming confidentiality problems related to the intellectual property of communicating actors. STMicroelectronics made available its traffic generators for audio and video IP blocks, allowing us to reproduce on the MPSIM environment the traffic patterns of real-life set-top-box platforms with a high level of accuracy.

Another effect of the joint work on traffic generators between Technical university of Denmark and University of Bologna was the development of the necessary infra-structure to co-simulate modules of the abstract system-level MPSoC ARTS frameworks (DTU) with modules available in the cycle-true MPARM framework. The motivation of the work is to investigate MPSoC instances at mixed-levels of abstraction. A simple system where two ARTS IP cores were connected through a MPARM AMBA-AHB bus was successfully implemented and co-simulated.

Finally, a significant modeling effort was required also for the memory controller. In fact, MPSIM has traditionally simulated MPSoC systems with on-chip memories only; therefore we needed to model real-life memory controllers for I/O. We got the LMI specification from STMicroelectronics, and developed a SystemC model which was accurately (cycle-by-cycle) validated against the behavior of the real LMI. Such powerful model allows us to interface our MPSoC with SDR and DDR SDRAMs, and more interestingly to model I/O access latency of real systems. Finally, we retain the capability to model an on-chip shared memory in place of the off-chip SDRAM, thus being able to differentiate system performance and power in presence of a slow off-chip memory vs. a fast on-chip memory. Optimizations for access to the off-chip memory can also be analyzed with this platform.

Outcome
The outcomes of this activity are: the development of a virtual platform for power modeling of complex multi-core systems on chip. This platform will facilitate further integration among partners and associates, thanks to is flexibility and generality.

Difficulty
The main difficulty encountered was in the definition of meaningful traffic patterns, based on applications running on a real platform as specified by the associated industrial partner, without disclosing detailed functional models of the applications running on the platform (that are highly confidential). This difficulty was overcome through the use of traffic generators allowing definition of abstract traffic patterns which do not disclose confidential information on applications, while being accurate in terms of workload on interconnects and memory system.

Power optimization via system-level resource allocation and scheduling

In this activity, the focus is on addressing resource allocation problems in Multi-Processor Systems-on-Chip (MPSoCs). An important instance of this problem is when have to allocate and schedule a given task graph (representing a functional abstraction of a multi-task application) on a target multi core platform while choosing the frequency (and voltage) at which each task will be executed. Since hardware platforms and applications are extremely complex, it becomes thus important not only to measure the optimizer efficiency as done in general in the optimization area, but also to verify if the optimization model is accurate through a validation step performed via simulation on a virtual platform.

Allocation, scheduling and discrete voltage selection problem for variable voltage/ frequency MPSoCs, minimizing the system energy dissipation and the overhead for frequency switching, are clearly NP-hard problems. Only incomplete approaches have been proposed to solve these problems in the system design community. In this activity we have investigated a hybrid methodology based both on Constraint Programming (CP) and Integer Programming (IP) that splits the overall problem in two subproblems, the first being the allocation of tasks to processors and frequencies to tasks and the second being the scheduling. Our methodology derives static allocation, scheduling and frequency setting; therefore it targets applications with design-time predictable behavior.

In order to solve the problem to optimality without incurring accuracy limitations, we applied the concept behind the *logic-based Benders decomposition technique* to this new application problem. Bender decomposition can be summarized as follows. A complex optimization problem is decomposed in two parts: the first, called Master Problem, is the allocation of processors and frequencies to tasks and the second, called Subproblem, is the scheduling of tasks given the static allocation and frequency assignments provided by the master. The master problem is tackled by an Integer Programming solver while the subproblem through a Constraint Programming solver. The two solvers interact via generation of no-goods (constraints on acceptable solutions for the CP solver) and cutting planes (constraints on acceptable values of the integer variables for the IP solver) generation. The solution of the master is passed to the subproblem in an iterative procedure that is proved to converge to the optimal solution.

The methodology has been tested on a variety of realistic instances. In addition, we test the accuracy of the solutions provided by the optimizer simulating them on an MPSoC virtual platform. In particular, we have used two demonstrators (GSM and JPEG) to prove the applicability of the developed methodology to real-life embedded applications scenarios.

In a parallel, but strongly related activity, we have also addressed the specific problems of soft real-time systems. In this case, certain tasks are allowed to miss their deadlines. This however, negatively affects the delivered QoS. The goal is to maximize the QoS with a limited energy budget or to achieve a certain level of QoS with as low energy consumption as possible. We

have developed heuristics which determine the system schedule and voltage levels of tasks in such a system.

Finally, DTU has experimented with the use of meta-heuristics to solve the mapping a set of task graphs onto a heterogeneous multiprocessor platform. The objective is to meet all real-time deadlines subject to minimizing system cost and power consumption, while staying within bounds on local memory sizes and interface buffer sizes. Our approach allows for mapping onto a fixed platform or onto a flexible platform where architectural changes are explored during the mapping. The approach uses multi-objective evolutionary algorithms and is based on the PISA framework for multi-objective optimization developed at ETH Zurich. We demonstrate the approach through an exploration of a smart phone, where five task graphs with a total of 530 tasks after hyper period extension are mapped onto a multiprocessor platform. The results show four non-inferior solutions out of 10.000 explored solutions, which tradeoffs the various objectives.

Outcome
The outcome of this activity is the development of a methodology for design-time allocation, scheduling, frequency and voltage setting for multi-task applications onto MPSoC platforms. This outcome is a starting point for follow-up integration activities aiming at the extension of the methodology to more dynamic problems, where run-time decisions will be required

Difficulty
No major difficulties were encountered

Scheduling based energy optimization for energy-scavenging wireless sensor networks

Wireless sensor networks – consisting of numerous tiny sensors that are unobtrusively embedded in their environment – have been the subject of intensive research. As for many other battery-operated embedded systems, a sensor's operating time is a crucial design parameter. As electronic systems continue to shrink, however, less energy is storable on-board. Research continues to develop higher energy-density batteries and supercapacitors, but the amount of energy available still severely limits the system's lifespan. As a result, size and weight of most existing sensor nodes are largely dominated by their batteries.

On the other hand, one of the main advantages of wireless sensor networks is their independence of pre-established infrastructure. That is, in most common scenarios, recharging or replacing nodes' batteries is not practical due to (a) inaccessibility and/or (b) sheer number of the sensor nodes. In order for sensor networks to become a ubiquitous part of our environment, alternative power sources should be employed. Therefore, environmental energy harvesting is deemed a promising approach: If nodes are equipped with energy transducers like e.g. solar cells, the generated energy may increase the autonomy of the nodes significantly. Several technologies have been discussed how, e.g., solar, thermal, kinetic or vibrational energy may be extracted from a node's physical environment. Moreover, several prototypes have been presented which demonstrate both feasibility and usefulness of sensors nodes which are powered by solar or vibrational energy.

The focus of this activity is on sensor nodes with energy-scavenging features. In general our results apply for all kind of energy harvesting systems which must schedule processes under deadline constraints. For these systems, new scheduling disciplines must be tailored to the energy-driven nature of the problem. This insight originates from the fact, that energy – contrary to the computation resource "time" – is storable. As a consequence, every time we withdraw energy from the battery to execute a task, we change the state of our scheduling system. That is, after having scheduled a first task the next task will encounter a lower energy

level in the system which in turn will affect its own execution. This is not the case in conventional real-time scheduling where time just elapses either used or unused.

The main developments obtained in this activity can be summarized as follows

(a) We studied an energy-driven scheduling scenario for a system whose energy storage is recharged by an environmental source. For this scenario, we developed an optimal online algorithm that dynamically assigns power to arriving tasks. These algorithms are “energy-clairvoyant”, i.e., scheduling decisions are driven by the knowledge of the future incoming energy.

(b) We developed an admittance test that decides, whether a set of tasks can be scheduled with the energy produced by the harvesting unit, taking into account both energy and time constraints. For this purpose, we introduced the concept of energy variability characterization curves (EVCC).

(c) In addition, a comparison to earliest-deadline first (EDF) by means of simulation, demonstrated that significant capacity savings can be achieved by our approach, when compared to the classical EDF algorithm.

Outcome
The outcome of this work is a novel scheduling strategy (called lazy scheduling) that is well suited to energy-harvesting systems operating under real-time constraints. It is the first result of this kind in this quickly growing research area and received a lot of attention in the scientific community. Two joint publications have been written.

Difficulty
No major difficulties were encountered

2.2.2 Publications Resulting from these Achievements

Power modelling for complex SoC platforms

- S. Murali, T. Theocharides, N. Vijaykrishnan, M.J. Irwin, L. Benini, G. De Micheli, *Analysis of error recovery schemes for networks on chips*, IEEE Design & Test of Computers, Vol. 22, no. 5, Sept.-Oct. 2005, pp. 434 – 442.
- F. Angiolini, S. Mahadevan, J. Madsen, L. Benini, J. Sparsø, *Realistically Rendering SoC Traffic Patterns with Interrupt Awareness*, IFIP VLSI-SOC Conference, Oct 17-19, 2005, pp. 211-216.
- F. Angiolini, P. Meloni, S. Carta, L. Benini, L. Raffo, *Contrasting a NoC and a Traditional Interconnect Fabric with Layout Awareness*, Design, Automation and Test in Europe, 06-10 March 2006, vol. 1, pp.115– 121.
- G. Paci, P. Marchal, F. Poletti, L. Benini, *Exploring “temperature-aware” design in low-power MPSoCs*, IEEE/ACM Design, Automation and Test in Europe, 06-10 March 2006. vol. 1, pp. 255-260.
- L. Benini, *Application Specific NoC Design*, Design, Automation and Test in Europe, 06-10 March 2006, vol. 1, pp.318-422.
- Paolo Meloni, Salvatore Carta, Roberto Argiolas, Luigi Raffo and Federico Angiolini, "Area and Power Modeling Methodologies for Networks-on-Chip", Nano-Net 2006, Sept. 14-16.
- T. Bjerregaard, J. Sparsø, *A Scheduling Discipline for Latency and Bandwidth Guarantees in Asynchronous Network-on-Chip*, Proceedings of the 11th IEEE

International Symposium on Asynchronous Circuits and Systems (ASYNC'05), pp. 34-43, IEEE Computer Society, 2005.

- T. Bjerregaard, S. Mahadevan, R. G. Olsen, J. Sparsø, *An OCP Compliant Network Adapter for GALS-based SoC Design Using the MANGO Network-on-Chip*, Proceedings of the International Symposium on System-on-Chip (SoC'05), pp. 171-174, IEEE, 2005

Power optimization via system-level resource allocation and scheduling

- M. Ruggiero, M.; A. Acquaviva, D. Bertozzi, L. Benini, *Application-specific power-aware workload allocation for voltage scalable MPSoC platforms* IEEE International Conference on Computer Design, 2-5 Oct. 2005, pp. 87–93.
- L.Benini, D. Bertozzi, A. Guerri, M.Milano, *Allocation and Scheduling for MPSoCs via decomposition and no-good generation* International Joint Conference on Artificial Intelligence, IJCAI2005, poster version. Extended version in International Conference of Principle and Practice of Constraint Programming, CP2005
- L. A. Cortes, P. Eles, Z. Peng, *Quasi-Static Assignment of Voltages and Optional Cycles in Imprecise-Computation Systems with Energy Considerations*, IEEE Trans. on Very Large Scale Integration Systems (to be published).
- L. A. Cortes, P. Eles, Z. Peng, *A Quasi-Static Approach to Minimizing Energy Consumption in Real-Time Systems under Reward Constraints*, Intl. Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA), August 16-18, 2006.
- L.Benini, D. Bertozzi, A. Guerri, M.Milano, *Allocation, Scheduling and Voltage Scaling for Energy Aware MPSOCs*, International Conference on the Integration of Artificial Intelligence and Operations Research in Constraint Programming for Combinatorial Optimization, CPAIOR2006 LNCS 3990, Springer Verlag 2006.

Scheduling based energy optimization for energy-scavenging wireless sensor networks

- C. Moser, L. Thiele, L. Benini, D. Brunelli, Real-*Time Scheduling with Regenerative Energy* IEEE/Euromicro Conference Real-Time Systems, 05-07 July 2006, pp. 261–270.
- C. Moser, D. Brunelli, L. Thiele, and L. Benini, "Lazy scheduling for energy harvesting sensor nodes.", The Fifth IFIP Working Conference on Distributed and Parallel Embedded Systems (DIPES 2006), Braga, Portugal, October 13-15, 2006.

2.2.3 Keynotes, Workshops, Tutorials

Invited Presentation: Luca Benini - Application Specific NoC Design
Design Automation & Test in Europe Conference & Exhibition
Munich, Germany – 06-10 March, 2006.
http://www.date-conference.com

Keynote: Luca Benini - NoCs: Vision, Reality, Trends
Special Workshop: on Future Inteconnects and Networks on Chip
Munich, Germany – 10 March, 2006.
http://async.org.uk/noc2006

Tutorial: Luca Benini – Dynamic Power management
SBCCI: Symposium on Integratedi Circuits and Systems Design
Florianopolis, Brazil – 5 September 2005.

Tutorial: Lothar Thiele – Sensor Networks
Design Automation & Test in Europe Conference & Exhibition
Munich, Germany – 06-10 March, 2006.
http://www.date-conference.com

Invited Presentation: Tobias Bjerregaard – Modular SoC-Design using the MANGO clockless NoC
International Conference on Parallel Computing (PARCO'05)
Malaga, Spain – 13-16 September, 2005.
http://www.parco.org

Workshop : Artist2 Cluster meeting
Bologna, 22-23 May, 2006**.**
http://www-micrel.deis.unibo.it/Artist2/artist2.html

3. Future Work and Evolution

3.1 Problem to be tackled over the next 18 months (Sept 2006 – Feb 2008)

Power optimization via system-level resource allocation and scheduling

Linkoeping and Bologna will continue cooperation on this topic, and we will explore the possibility of including the evolutionary exploration from DTU. Our main goal for the coming period is to consolidate the results regarding the optimization of energy-efficient time constrained multiprocessor systems. The main directions are the following:

- improve and refine the task-based application models as well as the architecture models, in order to make them as realistic as possible, in the context of current execution platforms and target applications;
- explore more efficient design space exploration approaches based on mathematical programming or heuristics, e.g. evolutionary algorithms;
- extend the approaches to on-line voltage scaling, such that dynamic slack can be exploited; the problem is particularly interesting in the context of multiprocessors;
- Explore interaction and tradeoffs between energy efficiency and fault tolerance.

Scheduling based energy optimization for energy-scavenging wireless sensor networks
ETHZ and Bologna will continue to work on low power sensor network design. In particular, the results so far will be extended towards application-level decisions.

- To this end, on-line control strategies need to be developed that change the state of the application depending on the current systems state, e.g. the amount of local data stored, and on the estimation of the future energy flow. The approach will be based on the experience in UoB on building energy-harvesting nodes and on convex optimization from ETHZ. Both theoretical and practical aspects of the problem will be investigated. The feasibility of implementation of advanced on-line control strategies on tightly constrained sensor network hardware platforms will be explored. This activity will leverage the experience on ETHZ and UoB on the hardware-software design of wireless sensor nodes.

UoB and ETHZ are actively developing a joint prototype sensor node which is powered by solar energy. To this end, a BTnode - originally developed at ETH Zurich - has been transferred to Bologna. Equipped with solar panels and supercapacitors for energy storage, measurements on this prototype will illuminate the practical relevance of our theoretical results.

3.2 Current and Future Milestones

The main milestone set forth in the 18 month workplan for Year 2 was **"Component models will be investigated that model power dissipation of system components**".

This milestone has been achieved in a very general sense:

1. *Simulation models have been extended and generalized in activity "Power modeling for complex SoC platforms". The models have also being integrated in a common virtual platform environment*

2. *Static, abstract models for power consumption (e.g. energy consumed per task, energy per memory access) of system components have been developed and utilized in the optimal allocation and mapping techniques investigated in the activity "Power optimization via system-level resource allocation and scheduling" as well as in the activity "Scheduling based energy optimization for energy-scavenging wireless sensor networks"*

The models will be refined in the continuation of the work, and the matching between simulation models and static models will be verified in the continuation of these activities.

Year 3 milestones will be mostly in the area of power control (leveraging the models developed in the first two years:

1. **In the area of allocation and scheduling the milestone will be a demonstration of power savings achieved through optimal allocation and scheduling for a realistic MPSoC platform model, and a realistic applications from the multi-media and wireless communication domain.**

2. **In the area of sensor networks, there will be a method available to control the activities of a sensor node based on the current state and the expected future energy input. The off-line optimization as the on-line control strategy will be implemented on a jointly developed sensor network platform.**

3.3 Indicators for Integration

Consistent progress has been reported with respect to the integration indicators. Active and productive cooperation between has been further developed:

- The Linköping group has integrated the Bologna simulation platform for both research and education purposes. Several applications have been implemented and research results have been successfully validated. The platform is also used as part of a master-level course for design space exploration projects. The two groups have successfully cooperated with good synergy effect, resulted in research results on system level optimization, new ideas in system modeling, and common publication. This work has required frequent communications between graduate students and a visit of Linkoeping researchers to Bologna
- DTU and UoB have worked closely on the integration of traffic generators in the MPARM simulation platform, and they also achieved the integration of the high-level systemC models of task execution developed in the ARTS framework, into the MPARM cycle accurate simulation platform. This work has required several weeks of visits of a graduate student form DTU to the University of Bologna. The cooperation has resulted in joint publications.
- ETHZ and bologna have worked in close cooperation on energy conservation and energy scavenging for wireless sensor networks. This cooperation has been based on a 6-months stay of a graduate student from Bologna in ETHZ. Moreover, there has been a visit of the primary investigator from bologna to ETHZ. Several joint publications have been produced.

From the technical viewpoint, several new problems have been identified, and will be jointly researched by the partners. The research approach strongly leverages synergies between the partners, by integrating different levels of system abstraction (from scheduling via operating

systems to system design). The successful technical cooperation is demonstrated by several joint publications.

3.4 Main Funding

Bologna University:

- STMicroelectronics industrial grant, Freescale semiconductor industrial grant

Linkoeping University:

- Swedish Foundation for Strategic Research (SSF)

Technical University of Denmark

- Hogthrob, The Technical Research Council of Denmark (STVF)

ETH Zurich

- Siemens Building Technology Industrial Grant, National Project MICS (Mobile Information and Communication Systems).

3.5 Internal Reviewers

Davide Bertozzi – Università di Ferrara ITALY

Josè Ayala - Universidad Politécnica de Madrid SPAIN