

ARTIST 2

Network of Excellence

IST-004527 ARTIST2:
Embedded Systems Design

Cluster Progress Report for Year 2

Cluster:
Execution Platforms

Cluster Leader:

Prof. Dr. Lothar Thiele (ETH Zurich)
<http://www.tik.ee.ethz.ch>

Policy Objective (abstract)

This topic is strongly linked to the compilation and implementation of embedded systems. For a given application, it is important to have the technology, methods and tools to make rational choices about the platform and the design used, before proceeding to final implementation. Research in Execution Platforms targets the development of the theoretical and practical tools for modelling the dynamic behaviour of application software for a given platform. This is a new area of research, which will allow greater flexibility in designing optimal embedded systems.

Table of Contents

1. Overview	4
1.1 High-Level Objectives.....	4
1.1.1 <i>System Modelling Infrastructure</i>	4
1.1.2 <i>Communication-Centric Systems</i>	5
1.1.3 <i>Low-Power Design</i>	5
1.1.4 <i>Resource-Aware Design</i>	6
1.2 Industrial Sectors.....	6
1.2.1 <i>Automotive Industry</i>	6
1.2.2 <i>Mechatronic Industry</i>	7
1.2.3 <i>Information Technology</i>	7
1.3 Main Research Trends	8
2. State of the Integration in Europe	10
2.1 Other Research Teams	10
2.2 Interaction of the Cluster with Other Communities	11
2.3 Main Aims for Integration and Building Excellence through Artist2	14
3. Overall Technical View.....	15
3.1 Brief State of the Art	15
3.1.1 <i>Communication-Centric Systems</i>	15
3.1.2 <i>Resource-Aware Design</i>	17
3.1.3 <i>Simulation and Performance Analysis</i>	18
3.2 Ongoing Work in the Partner Institutions.....	19
3.3 Interaction and Building Excellence between Partners.....	22
3.3.1 <i>Integration Activities within the Cluster</i>	22
3.3.2 <i>List of Joint Publications</i>	24
4. Overall Assessment and Vision for the Cluster.....	27
4.1 Assessment.....	27
4.2 Vision and Long Term Goals	27
4.3 Future Work and Evolution	27
4.3.1 <i>Technical Description</i>	27
4.3.2 <i>Current and Future Milestones</i>	29
5. Cluster Participants.....	32
5.1 Core Partners	32



5.2	Affiliated Industrial Partners.....	38
5.3	Affiliated Academic Partners.....	39
5.4	Affiliated International Partners.....	39

1. Overview

In relation to the ARTIST2 network, it is the overall goal of the topic on execution platforms to extend the current state in composability towards issues like modeling of non-functional constraints, power and energy, end-to-end real-time behavior, timing and performance analysis and heterogeneous models of computation.

One of the most critical issues to be faced in the research on execution platform is their rapidly growing complexity. Complexity increase is pushed by Moore's law, and by the ever-increasing demand for high performance computing. In addition, the boundaries between hardware and software domains are getting more blurred (dynamically re-configurable hardware, adaptable embedded systems, breakthrough in power consumption and performance) and challenging questions are at the border (trade-offs in mapping applications to hardware and software components, re-configurable hardware, WCET, performance of distributed computer and communication systems).

The cluster attempts to combine the diverse knowledge and to integrate different approaches approaches in the area of execution platforms for embedded systems available in Europe and beyond.

1.1 High-Level Objectives

The workplan of the platform can be partitioned into System Modelling Infrastructure, Communication-Centric Systems, Low-Power Design and Resource-Aware Design.

1.1.1 System Modelling Infrastructure

The aim is to provide a scalable and realistic modelling platform which is abstract enough to provide complete system representations and some form of non-functional models even for billion-transistor future systems, while at the same time providing the needed flexibility for modelling a number of different embodiments (e.g. multi-processors, homogeneous and heterogeneous, reconfigurable, etc.).

In the first 12 months the focus has been on assessing the state-of-the-art within the two different modelling approaches, simulation- and formal-based. In the next 18 months (from which 12 months passed now) the integration within simulation- and formal-based modelling was further researched and in particular modelling extensions which allow combinations of simulation- and formal-based modelling approaches.

These objectives have been achieved. For the formal-based modelling approaches, the real-time calculus from ETH Zurich has been linked to SymTA/S from TU Braunschweig. Furthermore, the real-time calculus has been embedded into the SymTA/S front-end, allowing designers to express both models within the same environment. Within the simulation-based modelling approaches, ARTS from DTU and MPARM from University of Bologna have been linked through OCP interfaces, making it possible to simulate an MPSoC platform modelled at a mixture of abstraction levels. For the integration of mixed formal- and simulation-based modelling approaches, MPARM and the real-time calculus have been connected through the use of traffic generators; ARTS has been re-modelled using the timed automaton semantics of UPPAAL from Aalborg University and Uppsala University; finally, ARTS has been extended by Linköping University to support distributed embedded automotive systems with the aim to evaluate the degree of pessimism as expressed by formal models, in particular the holistic approach from Linköping University.

1.1.2 *Communication-Centric Systems*

The work aims at new best-case/worst-case models for hard real-time systems and at combined statistical and interval models for QoS applications in multi-media. These models will combine communication and computation, different models of computation, event models and scheduling policies.

In the first 12 month the state-of-the-art in models was assessed taking into consideration the particularities of various (quasi)standard communication protocols during system analysis and scheduling. The second 18 month will extend the modelling scope to emerging hierarchical protocols such as FlexRay, and include the new aspect of fault tolerant systems.

While at end of the first 12 month, a report was produced unifying and relating the different approaches to communication-centric systems and low power design, the second 18 month will combine statistical timing models, interval models and simulation to handle complex QoS requirements. The power models for scheduling will be extended, and the simulation platforms for communication centric systems, MPARM and ARTS will be integrated. New approaches to fault tolerance in heterogeneous embedded systems will be provided.

The objectives have been met in joint efforts by the respective teams. Feedback from first practical application of the research work has shown that design predictability can be drastically increased but some complex dependencies and protocols require additional research work (e.g. FlexRay). Therefore, research has focused on such protocols while statistical models have been postponed.

1.1.3 *Low-Power Design*

The high-level objectives are in two directions: strengthening integration and making inroads in effective techniques for system-level power optimization.

Strengthening integration: work will be performed aiming at defining abstractions and models suitable for very-high-level system power estimation, both for localized and distributed platforms. Example platforms will be used to drive the integration effort, in the domain of multi-processor-systems on chip (leveraging the MPARM infrastructure) and in the domain of distributed sensor networks (leveraging the ARTS simulation model and the prototype sensor networks).

System-level power optimization: in this area, the interaction between resource allocation and scheduling and power optimization will be explored both for localized and distributed systems. Furthermore, the interplay between power and other cost metrics (reliability, performance) will be explored.

These objectives are actively pushed, and several milestones have been achieved leveraging the cooperation of the groups involved in the activity. More specifically: simulation-based power estimation, based on the MPARM infrastructure has been considerably strengthened. Power models for interconnect fabrics and on-chip memories have been developed and extended to account for the characteristics of deep submicron technologies (leakage effects, variable voltage supply support). From the point of view of power-aware allocation and scheduling, significant progress has been made both in considering complex and realistic platform models (multi-core architectures, with variable frequency, shutdown support), and in the development of aggressive strategies to find optimal allocation and mappings of task-based parallel applications.

1.1.4 *Resource-Aware Design*

The goal is to provide, through the integration of research activities of many participants a viable path for resource-aware software and hardware development. The final objective is to achieve integration of research activities in a concrete deliverable:

A set of tools that can interact and work together and demonstrate the achievable optimizations on a particular hardware platform.

A methodology that enables the design of predictable embedded systems with a special focus on issues that cut several layers of abstraction, such as hardware and compiler design is to be found.

Significant progress toward reaching these objectives has been made, especially on the front of the integration between research infrastructures. Important milestones achieved in this area are: (i) the construction of a common simulation-based infrastructure for modelling, analysis and design space exploration of heterogeneous multi-core architecture. This milestone has been reached through the integration work performed by UNIBO and AACHEN that have developed a common virtual platform where application-specific processor models, generated through the LISATEK suite can be embedded in the system simulator MPARM. (ii) the integration of an optimizing compiler infrastructure (developed in UDORTMUND) with the virtual platform developed in UNIBO. This work opens the way for a wide range of joint research and integration activities, where synergies between optimizing compilers and architecture in multi-core systems can be explored.

1.2 **Industrial Sectors**

1.2.1 *Automotive Industry*

The automotive industry is currently in a fast and spectacular evolution towards the intelligent, safe, environmental, interconnected, and economic car. Electronics is at the basis of most of this development. New features such as automatic intelligent parking assist, blind-spot information system, navigation computers with real-time traffic updates, not to mention electronically controlled brakes or electronic power steering, are out and running in most recent high-end cars. This development is going to continue with new functionality being adopted not only in premium cars but also in the mass-market. This, of course, comes at a cost. Automotive electronics, currently accounts for 22% of a vehicle's cost and is predicted to increase to 40% by 2010 (www.altera.com).

This evolution brings a series of challenges in all steps of the development cycle. How to specify and model such a complex system? There is a need for a component based modelling, analysis, and synthesis approach in which independently designed hardware and software components can safely be combined into a working system. How to achieve the ever increasing demand on functionality and safety, at an affordable cost? Modern automotive electronic systems are highly distributed networks with components interacting over various infrastructures. How to achieve a safe and predictable system at such a huge level of complexity and heterogeneity? A well defined methodology is needed for mapping the complex functionalities on predefined distributed automotive platforms. This assumes well defined standards, middleware layers, analysis tools, software generation tools, design exploration and optimisation approaches.

Due to ARTIST2 activities, (e.g. the ARTIST workshop "Beyond AUTOSAR" in Innsbruck) several technical meetings between TU Braunschweig and leading automotive suppliers in the AUTOSAR context held place. As a main topic it was discussed how compositional performance verification methods can be utilized in the automotive design process to facilitate

the network integration problem. TU Braunschweig was invited to the SAE world congress 2007 in Detroit to present recent results in compositional performance verification.

1.2.2 *Mechatronic Industry*

Traditionally, the development of mechatronic systems was a rather sequential process. First the mechanical part was designed, next the hardware infrastructure was fixed, and finally the embedded software was developed. Typically, this led to many problems at systems engineering, because only then the interference of design decisions from the disciplines became visible. To improve this process and to shorten the time-to-market, there is a clear trend towards concurrent engineering. To be able to detect problems earlier in the development cycle, there is a strong need for high-level models that allow early analysis of system-level design decisions. Moreover, there is an increasing interest in the use of models to improve the early testing process; for instance, one would like to test the embedded software before its environment is available.

Concerning the execution platforms used, one can observe the need for a flexible process where one can easily switch between various solutions, such as the amount of distribution, the topology used, the communication infrastructure, and the operating system. Often in a first release of a high-tech system the execution platform is overdimensioned. For instance, one might choose a highly distributed architecture to avoid scheduling problems. In a later version, a strong cost reduction has to be achieved by combining more functionality on a single node. One major problem is to foresee at an early stage of the design whether a particular hardware platform is feasible for a given software system. Hence there is a strong need for methods that can help engineers to make a well-founded choice for an execution platform. Another important problem companies have to deal with is incomprehensive, far too detailed and inconsistent documentation. This creates a gap between the application domain and the implementation. To address this problem, systematic approaches are needed to refine high-level models into working implementation in a predictable way.

1.2.3 *Information Technology*

Microelectronic technology is continuing to grow according to Moore's law. However, the need for computation power in industry is growing even faster. This is the case with traditional areas such as technical/scientific computation, and, more recently, modern applications, for instance interactive multimedia, high bandwidth communication, or speech recognition. Many of these applications are running on mobile a computer, which makes issues even more complicated: an unprecedented amount of computation power has to be delivered with very low energy consumption. So, instead of just running after high performance, industry is out after a good performance - energy product. These unprecedented performance/energy requirements cannot be achieved by further pushing processor technology along the traditional Pentium lines. New architectures are needed in which several lower performance (and less energy hungry) computation nodes are cooperating in order to globally achieve the expected performance. Modern MPSoC and NoC architectures are developed along these lines.

Another clear trend is towards reconfigurable architectures, in general, and configurable processors, in particular. The generic goal is to achieve a high degree of flexibility (traditionally available only with software implementation) at a power consumption which is much lower than achievable with a traditional software implementation using general purpose processors.

The emerging trend for multimedia applications on mobile terminals, combined with a decreasing time-to-market and a multitude of standards have created the need for flexible and scalable computing platforms that are capable of providing considerable (application specific) computational performance at a low cost and a low energy budget.

Hence, in recent years, the first multiprocessor System-on-Chip components have emerged (like e.g. TI OMAP, ST Nomadik, Philips Nexperia, IBM/Toshiba/Sonys CELL). These platforms contain multiple heterogeneous, flexible processing elements, a memory hierarchy and I/O components. All these components are linked to each other by a flexible on-chip interconnect structure. These architectures meet the performance needs of multimedia applications, while limiting the power consumption.

1.3 Main Research Trends

Many embedded system applications are implemented today using distributed architectures, consisting of several hardware nodes interconnected in a network. Each hardware node can consist of a processor, memory, interfaces to I/O and to the network. The networks are using specialized communication protocols, depending on the application area. For example, in the automotive electronics area communication protocols such as CAN, FlexRay and TTP are used.

As the complexity of the functionality increases, the way it is distributed has changed. If we take as an example the automotive applications, initially, each function was running on a dedicated hardware node, allowing the system integrators to purchase nodes implementing required functions from different vendors, and to integrate them into their system. Currently, number of such nodes has reached more than 100 in a high-end car, which can lead to large cost and performance penalties.

Not only the number of nodes has increased, but the resulting solutions based on dedicated hardware nodes do not use the available resources efficiently in order to reduce costs. For example, it should be possible to move functionality from one node to another node where there are enough resources (e.g., memory) available. Moreover, emerging functionality, such as brake-by-wire, is inherently distributed, and achieving an efficient fault-tolerant implementation is very difficult in the current setting.

Moreover, as the communications become a critical component, new protocols are needed that can cope with the high bandwidth and predictability required. The trend is towards hybrid communication protocols, such as the FlexRay protocol, which allows the sharing of the bus by event-driven and time-driven messages. Time-triggered protocols have the advantage of simplicity and predictability, while event-triggered protocols are flexible and have low cost. A hybrid communication protocol like FlexRay offers some of the advantages of both worlds.

With growing embedded system complexity more and more parts of a system are reused or supplied, often from external sources. These parts range from single hardware components or software processes to hardware-software (HW-SW) subsystems. They must cooperate and share resources with newly developed parts such that the design constraints are met. There are many software interface standards such as CORBA, COM or DCOM, to name just a few examples that are specifically designed for that task. Nevertheless in practice, software integration is not a solved but a growing problem.

New design optimization tools are needed to handle the increasing complexity of such systems, and their competing requirements in terms of performance, reliability, low power consumption, cost, time-to-market, etc. As the complexity of the systems continues to increase, the development time lengthens dramatically, and the manufacturing costs become prohibitively high. To cope with this complexity, it is necessary to reuse as much as possible at all levels of the design process, and to work at higher and higher abstraction levels.

One of the most significant achievements in the cultural landscape of low-power embedded systems design is the consensus on the strategic role of power management technology. It is now widely acknowledged that resource usage in embedded system platforms depends on application workload characteristics, desired quality of service and environmental conditions.

System workload is highly non-stationary due to the heterogeneous nature of information content. Quality of service depends on user requirements, which may change over time. In addition, both can be affected by environmental conditions such as network congestion and wireless link quality.

Power management is viewed as a strategic technology both for integrated and distributed embedded systems. In the first area, the trend is toward supporting power management in multi-core architectures, with a large number of power-manageable resources. Silicon technology is rapidly evolving to provide an increased level of control of on-chip power resources. Technologies such as multiple power distribution regions, multiple power-gating circuits for partial shutdown, multiple variable-voltage supply circuits are now commonplace. In the area of distributed low-power systems, wireless sensor networks are the key technology drivers, given their tightly power-constrained nature. One important trend in this area is toward “battery free” operation. This can be achieved through energy storage devices (e.g. super-capacitors) coupled with additional devices capable of harvesting energy from environmental sources (e.g. solar energy, vibrational energy). Battery-free operation requires carefully balancing harvested energy and stored energy against the energy consumed by the system, in a compromise between quality of service and sustainable lifetime.

2. State of the Integration in Europe

2.1 Other Research Teams

It appears that main research groups in Europe dealing with execution platforms for embedded systems are in the ARTIST2 network, either as full or as affiliated partners. There are some exceptions though, caused by the fact that not all are accepting a European network of Excellence as a viable funding instrument. In the following, some of these groups are listed together with their relation to ARTIST2.

TIMA/Ahmed Jerraya: The TIMA Laboratory on System Level Synthesis that is headed by Ahmed Jerraya does is specialized on multiprocessor SoC design. They are particularly well known for Hardware/Software design flow based on a unified HW/SW interface model. In particular, they are dealing with topics like multiple and mixed-level specification of heterogeneous systems, multiprocessor System-on-Chip, concurrent hardware & software design, HW/SW interfaces modeling and design, memory design for multiprocessor Systems-on-Chip and reconfigurable prototyping platform for multiprocessor SoC. The work of the research group is taken into account via various links to researchers in ARTIST2, namely a common EU IP project (SHAPES) in which Lothar Thiele and Rainer Leupers are participating.

IMEC's MPSoC research team. The MPSoC research team focus on platforms containing multiple heterogeneous, flexible processing elements, a memory hierarchy and I/O components. All these components are linked to each other by a flexible on-chip interconnect structure. The main focus of the team is to develop architectures which can meet the performance needs of multimedia applications, while limiting the power consumption. They are dealing with topics like design-time application exploration and optimization, platform architecture and runtime management. Close interaction, both at design time and at runtime, between these three topics creates a global solution that meets the MPSoC environment needs. In particular the work on the ADRES core, a platform containing a coarse-grained reconfigurable array, has been explored in a cooperation with researchers in ARTIST2, in which Jan Madsen, DTU, has participated.

The University of North Carolina at Chapel Hill, Sanjoy Baruah and Jim Anderson. Sanjoy Baruah and Jim Anderson are known in particular for their research in the domain of multiprocessor real-time scheduling.

University of Dresden, Hermann Härtig. Hermann Härtig is a leading researcher in the domain of micro-kernel based real-time operating systems.

Low power embedded systems design: In the area of low power embedded systems design, several new and relevant research themes are explored by other teams, not included in the ARTIST2 network. In particular research groups in the USA have a long tradition of excellence in low power research. We can mention the group lead by prof. Jan Rabaey in UC Berkeley, which is carrying out ground-breaking work on hardware platforms for wireless sensor networks. In the same area, several other groups are performing top-level research, e.g. Anantha Chandrakasan's group at MIT and David Blaauw's group at University of Michigan. Low power execution platforms are not relevant only for wireless sensor network, but also for mobile computing and even for servers and traditional computing infrastructure (e.g. servers). In these areas, the groups lead by Profs. Vijaykrishnan Narayanan, Mahmut Kandemir and Mary Jane Irwin at Penn State University, has produced a large number of interesting results in the last few years. We mention in particular their work on power issues for 3D integration and their analysis of power vs. reliability tradeoffs in high-performance computing. In this area, very interesting work is also performed by the group of prof. Kevin Skadron. The focus of this group is on thermal issues, which are very significant for high-performance system.

Universita degli Studi di Verona/Electronic Design Automation (EDA) group, Prof. Franco Fummi. Main research activities of the EDA group concern system verification, system synthesis and optimization, hardware description languages, power consumption, language abstraction, and system testing. Interactions with members of the execution platforms cluster are, for example, by participation in European projects (e.g. the STRP “Vertigo”) together with the Linköping group.

University of Southampton,/Electronic Systems Design Group, Prof. Bashir Al Hashimi. The Electronic Systems Design (ESD) Research Group is internationally recognized in two main areas - the development of novel algorithms and methodologies for Electronic Design Automation to support the design and test of large systems, and for intelligent sensor micro-systems. The group is working in the areas of system modeling, simulation, and synthesis, SoC design and testing, as well as smart sensors. Several cooperation projects have been undertaken, in particular with the Linköping group.

Carnegie Mellon University/System Level Design Group/Prof. Radu Marculescu. The System Level Design group performs research on formal methods for system-level design of embedded applications. They, in particular, focus on fast methods for power and performance analysis that can guide the design process of portable information systems. Important results have been obtained with regard to the communication-centric SOC design, providing formal support for analysis and optimization of novel on-chip communication architectures. In particular, this work addresses fundamental research problems for defining scalable and flexible communication schemes via the Network-on-Chip (NoC) approach. Interaction has been by, for example, PhD student exchanges with the Linköping group.

2.2 Interaction of the Cluster with Other Communities

Two members of the cluster on Execution Platforms are giving part of a summer school/advanced course on ADVANCED DIGITAL SYSTEMS DESIGN in September, Lausanne, Switzerland. The participants are from industry and university. This way, results from the integrated view of embedded system design will be brought to a much larger community.

The cluster organized a large ARTIST2 Workshop on Distributed Embedded Systems, Leiden, The Netherlands, in November 2005. The purpose was to bring different communities together that are dealing with the design and analysis of distributed embedded systems, see <http://www.tik.ee.ethz.ch/~leiden05/>. Many research groups not present in the ARTIST2 network participated and helped to come up with a set of Benchmark problems for performance analysis. This set of carefully selected problems that have been proposed and discussed during the workshop appear to be an excellent instrument to compare and integrated different approaches for the analysis of distributed embedded systems. There have been already publications and further thesis work based on the results presented here.

Lothar Thiele has been a lecturer at the ARTIST2 / UNU-IIST Spring School in China on Models, Methods and Tools for Embedded Systems The School offered a 2-week course consisting of four tutorials on state-of-the-art techniques for the design and analysis of embedded systems given by leading scientific experts. The aim was to provide a forum for young professors, lecturers, researchers, postgraduates (advanced master and PhD students) working in the fields of modelling, design, implementation, validation and performance analysis of embedded systems as well as engineers from industry with practical background with the development of embedded systems.

Ernesto Wandeler from the research group of Lothar Thiele has been given a tutorial on Frameworks for System-Level Analysis of Real-Time Systems - SymTA/S and MPA together with members of the affiliated company SymtaVision. This tutorial was part of the RTAS

conference in San Jose, USA. The aim of this spreading excellence activity was to make a closer link between the work done in the area of distributed embedded systems (by the execution platform cluster) and the classical real-time community. The methods are different and there is still a lack in understanding the different scopes and capabilities of these approaches.

Ernesto Wandeler from the EP cluster has been participating in the ARTIST Workshop on Design Issues in Distributed, Communication-Centric Systems at DATE, Munich, Germany and presenting methods for the performance analysis of communication-centric systems. This way, the unified view that has been reached by the participants of the cluster has been spread among a much wider research community.

Jan Madsen from the EP cluster has been participating in the ARTIST Workshop on Design Issues in Distributed, Communication-Centric Systems at DATE, Munich, Germany and presenting a modelling approach for networked embedded systems covering systems from multiprocessor system-on-chip to wireless sensor networks. The aim was to spread the simulation based system model, ARTS, of ARTIST2 to a much broad research community.

Shankar Mahadevan and Kashif Virk from the research group of Jan Madsen have been given demonstrations of the ARTS modelling framework at the University booth at DATE, Munich, Germany. At that occasion the ARTS framework were made public available (<http://www.imm.dtu.dk/arts>).

Jan Madsen has given a mini-keynote on multiprocessor design space exploration based on the ARTS modelling framework at the 6th International Symposium on Multi-Processor System-on-Chip, Estes Park, Colorado, USA. The aim was to initiate discussions of a more systematic approach for exploring architectural alternatives of multiprocessor system-on-chip platforms which today largely are based on ad-hoc approaches.

Jan Madsen and Srdjan Capkun from DTU have been lecturers at the ARTIST2 Phd course on wireless sensor networks given at Linkoping Technical University. Participant were from both academia and industry, mainly from Sweden. The aim of this spreading excellence activity was to disseminate knowledge and creating awareness of the emergent field of wireless sensor networks.

Jan Madsen presented the Execution Platform cluster at the Scandinavian ARTIST2 Seminar on Embedded Systems Design, the SNART Seminar 2006. The theme of this spreading excellence activity was a pro-active approach to strengthen Scandinavia's position in Embedded Systems - with an emphasis on topics covered by the ARTIST2 EU/IST Network of Excellence on Embedded Systems Design.

Marcel Verhoef, who works at ESI on the comparison of performance analysis techniques, collaborated with Martijn Hendriks of the Radboud University Nijmegen on the use of the timed automata tool Uppaal. The results of this work have been presented at the WPDRTS workshop of the International Parallel and Distributed Processing Symposium 2006, Greece. A general overview of this comparison, based on a car radio-navigation systems of Siemens VDO has been presented at a recent Dagstuhl seminar bij Jozef Hooman of ESI. This includes a large number of methods, such as MPA, SymTA/S, POOSL, QOSA, and extended VDM++.

Jeroen Voeten and colleagues, who work on system-level modeling and design techniques at the ESI and at the Electronic Systems group of the TU/e, have given two tutorials (at the FDL and the DSD) on system-level performance modeling. The tutorial presented a methodology for predicting performance properties of industrial-sized embedded systems. Starting from UML specifications, the methodology derives formal executable performance models expressed in POOSL, which are transformed into Markov chains to support both analytical and simulation-based performance evaluation. Participants were invited to experiment with the supporting tools by modeling and analyzing a multi-media streaming application.

A plenary special session on performance modeling for system-level design was organized at the FDL last year by Jeroen Voeten (ESI, TU/e), Lothar Thiele and Wolfgang Rosenstiel (University of Tübingen). The special session focused on state-of-the-art system-level methodologies (languages, analysis techniques, tools and methods) for predicting performance characteristics in the very early stages of the design process. Emphasis was on methods and approaches that scale to industrial-sized embedded systems.

The ESI organized a special session devoted to system level performance modeling. The session was organized for a representative group of system architects and system designers in the Netherlands. Among others, the performance modeling of a real-time distributed subsystem of a wafer scanner carried out at ASML was discussed by Jeroen Voeten (ESI). A comparison of different performance modeling techniques was made by Marcel Verhoef (ESI).

Razvan Racu and Arne Hamann from the research Group of Rolf Ernst, TU Braunschweig, have given a tutorial at the ARTES Summerschool in Sweden. ARTES is a Swedish network for real-time research and graduate education, which annually organizes a summer school for leading researchers and graduate students in real-time systems. The tutorial provided the Swedish real-time community with a close look into state-of-the-art performance verification methods and their applicability to the design of robust and predictable embedded real-time systems.

Jan Staschulat spent two weeks in York to exchange recent results in WCET analysis with Guillem Bernat from Rapita Systems (Adaptive Real-Time Cluster), one of the leading industrial tool suppliers for WCET analysis. The aim of the meeting was to discuss synergy effect between formal and probabilistic WCET analysis techniques.

Prof. Ernst gave a keynote speech at the MPSoC Summerschool in Estes Park, Colorado. The keynote presented distributed memory access analysis techniques for MPSoC modelling and analysis to leading researchers and industrial managers in System-on-Chip design.

Luca Benini and members of his group in UNIBO have given a number of tutorial and invited presentations on low-power design and the design of communication-centric integrated systems. Prof. Benini has given an invited presentation in official invited lecturer programs in Philips research laboratories, Eindhoven. He has given presentations in several large semiconductor companies: Freescale Semiconductors, Samsung Electronics, STMicroelectronics. He also has given tutorial presentations in international events organized in South America (SBCCI – Brazil), Asia (VLSI Conference, Kolkata, SNU-Kaist distinguished lecturer program Korea) and in the USA (Invited presentations at Stanford University). The group of UNIBO is active in the working groups of the ARTEMIS platform, and it is participating to the IST-CLEAN project, one of the key IPs of the 6FP in the area of low-power design.

Members of the Linköping group have given several presentations, regarding research results and prospective projects, for industrial partners and institutes, such as Volvo (Gothenburg), IMEC (Leuven), Philips (Eindhoven), Guangzhou Radio Group (Guangzhou, China).

As part of the ACM-SIGDA Multimedia Monograph Series (Volume 12), a DVD with four video-presentations on “Novel Paradigms in System-Level Design” has been published. Among them is the talk “Analysis and Optimisation of Distributed Real-Time Embedded Systems”, given by Petru Eles.

2.3 Main Aims for Integration and Building Excellence through Artist2

Following the activities presented in the previous section, the cluster on execution platforms follows the following strategy and uses the following mechanisms to spread the knowledge and integration achieved so far:

- Summer Schools and Training Activities to distribute the knowledge acquired in ARTIST2 to (a) other countries, (b) other communities and (c) young researchers.
- Tutorials at major conferences to reach new and larger research communities.
- Common publications between partners which not only show the integration within the cluster but are an excellent instrument to disseminate the integration results.
- New research projects with industrial partners which allow us to apply the obtained results at an industrial scale. This way, we also receive feedback and ideas for new research directions.
- Cooperation with other research groups, especially outside the EU (mostly USA and Asia). In this case, spreading excellence is not the only objective. The cluster participants can be exposed to new research problems and new approaches, that can be then explored and improved within the cluster.

3. Overall Technical View

3.1 *Brief State of the Art*

3.1.1 *Communication-Centric Systems*

With growing embedded system complexity more and more parts of a system are reused or supplied, often from external sources. These parts range from single hardware components or software processes to hardware-software (HW-SW) subsystems. They must cooperate and share resources with newly developed parts such that the design constraints are met. There are many software interface standards such as CORBA, COM or DCOM, to name just a few examples that are specifically designed for that task. Nevertheless in practice, software integration is not a solved but a growing problem. In a recent interview with the German weekly Magazine "Der Spiegel", Jürgen Schrempp (DER SPIEGEL 14/2005, 02.04.2005), CEO DaimlerChrysler, has explained that systems integration was a key problem in the recent series of call backs of Mercedes cars.

Software and communication layers together with interface standards increase software portability but they do not yet solve some of the key embedded systems challenges, (1) integration verification and (2) the control of performance and other not functional constraints, such as power consumption or dependability. Integration verification is a general systems design problem that deserves much attention but is not the focus of the activity. Performance problems originate in the fact that platform components have limited performance and memory resources. Sharing resources introduces additional, not functional dependencies. Such dependencies slow down communication or processing and increase event jitter potentially leading to buffer over- or underflows and lost messages or system failures. Such failures are difficult to identify, because many of them appear as timing anomalies that are not discovered using the typical component test patterns.

There are several approaches to cope with large systems integration. Frequently, designers use simulation or test and add some design rules of thumb for uncovered cases. An example is to limit the load on a prioritized bus to 30 or 60% of the maximum bus load. This rule has a realistic formal background and can be backed by a proof by Liu and Layland for periodic systems that hold under certain circumstances on a single processor or bus. However, these approaches do not apply to multi-hop networked systems.

A more general approach is a conservative design style that decouples the integrated components and subsystems by assigning them a fixed share of the resources. This sharing uses a TDMA technique (Time Division Multiple Access) where fixed time slots are assigned to processes or communication. Unlike round-robin scheduling, unused time slots stay empty avoiding possible buffer overflow due to extra resource shares that speed up processing or communication. In essence, TDMA reaches a complete decoupling at the cost of sub optimal resource, and possibly energy, utilization. The TDMA technique can be extended all the way to software development, where the elegantly simple mathematical formulation describing TDMA performance can be used for a system wide performance analysis and control, such as in the Giotto tool of UC Berkeley.

Such a conservative design style is typical for the aircraft industry which uses bus protocols such as TTP. TTP has additional synchronization functions that support fault detection and fault tolerance. Recently, TTP has also been introduced to the automotive mass market where it shall replace the fixed priority CAN bus in the mid term. Audi is considering TTP as their future automotive bus standard while the majority of automotive companies have committed to FlexRay which uses a TDMA protocol as a basis and runs a dynamic "mini slot" protocol in one

of the time slots. This hierarchy offers the rigorous conservative design style for part of the automotive functions and a dynamic schedule with higher resource utilization but complex non functional dependencies for other functions that are less time critical. The practical impact of the relatively complex FlexRay protocol will be seen soon when the first automotive system developments will use this bus. But even when commercial tools for FlexRay will be available in the future, they will fall short in evaluating general multi-hop networks as they appear today, from automotive to MpSoC.

Another approach is formal timing analysis. The scheduling effects of fixed priority scheduling, such as used for CAN buses, are well understood and formal analysis has found its way into commercial tools, such as the Volcano software and tool set. For a while, these techniques were sufficient for fixed priority scheduling approaches used in many of the bus protocols and real-time operating systems. With the advent of more complex networks including bridges, "local" analysis techniques that look at a single bus or processor only are not sufficient any more. This development can be observed from distributed real-time systems down to the level of an individual chip where several different buses are combined today. On the chip-level, the problem is even more complicated due to the introduction of caches (see roadmap). At the same time, the individual bus protocol becomes more complicated as visible in the transition from the CAN to the FlexRay protocol. Hence, embedded real-time system design is approaching a new level of complexity for which the current tools and formalisms are not appropriate any more.

There are proposals combining few different scheduling strategies, e.g. RMS on a processor and TDMA on the bus. These are called holistic approaches and were introduced by Tindell. A very good recent example that shows the power of this „holistic“ approach is the work in ARTIST NoE by the group of Eles. This work covers many different scheduling techniques and can be considered as defining the state of the art in holistic analysis. Other work by Palencia and Harbor, again in ARTIST, is leading in holistic analysis of systems with task dependencies. In general, it appears more efficient to identify solutions that encompass the whole system than to consider local scheduling individually.

On the other hand, there is an apparent scalability problem when considering the huge number of potential subsystem combinations that require adapted holistic scheduling. An alternative is a modular analysis technique that combines local analysis of individual components using event models as interfaces. Local analysis and event model propagation are iterated for a global analysis. ARTIST is the center of gravity for the development of this composition technique with the two cooperating groups from ETH Zürich and TU Braunschweig working on different versions of this approach.

Better modeling, analysis, and optimization are only part of the solution to master communication-centric systems. Networked systems based on the extension of conventional communication networks suffer from increasingly complex and decreasingly predictable real-time behavior. Therefore, the second focus of this ARTIST 2 activity is the development of new predictable and scalable networks with an emphasis on networks-on-chip. This is the interest of DTU and University of Bologna.

Recently, there has been a substantial interest in the area of massively distributed embedded systems that are used for communication, sensing and actuating. These sensor networks appear in many different application domains such as environmental monitoring, disaster management, distributed large scale control, building automation, elderly care and logistics. This quickly emerging research area is closely related to the subjects of the cluster on execution platforms. In particular, we are faced with resource constraints in terms of power and energy, computing, memory and communication. In addition, some of the potential application areas are characterized by (hard) real-time requirements. The necessary design and analysis methods clearly ask for an integrated view of the whole distributed systems, i.e. taking into account hardware and software, a cross-layer view on the different protocols and algorithms,

and new concepts for application specification, middleware and operating systems. It is not possible to describe in a few sentences the major challenges in this new kind of systems. Please find below an incomplete set specific to the area of execution platforms:

- Deployment of large distributed networks with limited communication and computation resources.
- Low energy computation and communication.
- Fault tolerance and reliability.

Currently, it is not clear whether this kind of new embedded systems is finding wide acceptance in industry. Nevertheless, there are already first projects in Europe that attempt to do a technology transfer from academia to industry, e.g. a safety network for building applications (Siemens, ETH Zurich).

3.1.2 *Resource-Aware Design*

While microelectronic technology is continuing to provide growth according to Moore's law, our need for computation power is growing even faster. Therefore, although, they have unprecedented computation and memory resources at their disposal, designers of embedded systems have to be increasingly aware of the fact that, in order to achieve the requirements of novel applications, these resources have to be used in the most efficient way.

A particular dimension of this problem is that of power consumption, since energy is one of the dominating constraints, especially, but not only, in the case of mobile applications. Reducing energy consumption is one of the major concerns of the research and design community, from circuit designers to embedded software developers. However, integrated system-level approaches which allow for an energy efficient mapping of an application on a customized platform are still lacking. What the research community is currently looking after are accurate system-level energy models, power estimation and analysis tools, functionality mapping and scheduling techniques, energy efficient communication synthesis and memory hierarchy optimization, as well as energy aware software compilation techniques. Hardware components that must be efficiently utilized include processors and memories. Highly optimized and low-cost processors can be designed with tools that support the creation of tuned micro-architectures and tool chains for application-specific instruction set processors. Moreover, highly efficient use of memories is increasing critical, both because the speed gap between processors and memories widens, and because the power consumed in memory systems is rapidly increasing.

Real-time applications, hard or soft, are raising the challenge of predictability. This is an extremely difficult problem in the context of modern, dynamic, multiprocessor platforms which, while providing potentially high performance, make the task of timing predictability extremely difficult (if at all solvable without drastically limiting the spectrum of applicable architectures). . With the growing software content in embedded systems and the diffusion of highly programmable and re-configurable platforms, software is given an unprecedented degree of control on resource utilization. Software generation and performance evaluation tools have to be made aware of the particularities of a certain memory hierarchy, or the dynamic features of the processor micro-architecture, such as to be able to both generate efficient code and accurately predict performance numbers. The basic dilemma which researchers still face is how much to compromise predictability in order to improve average performance? Or how much can cost and average performance be affected in order to achieve a predictable system with good worst case behaviour? This always increasing inter-dependence between hardware and software layers can be used to perform aggressive optimizations that can be achieved only by a synergistic approach that combines the advantages of static and dynamic techniques.

3.1.3 *Simulation and Performance Analysis*

The success of such new design methods depends on the availability of analysis techniques, beyond those corresponding to the state-of-the-art. Today, manufacturers and suppliers still rely only on extensive simulation to determine if the timing constraints are satisfied. However, simulations are very time consuming and provide no guarantees that imposed requirements are met.

There is a large quantity of research related to scheduling and schedulability analysis, with results having been incorporated in analysis tools available on the market. However, the existing approaches and tools address the schedulability of processes mapped on a single processor, or the schedulability of messages exchanged over a given communication protocol.

Several research groups have provided analyses that bound the communication delay for a given communication protocol, and extended the uni-processor analysis to handle distributed systems. However, none of the existing approaches offers an analysis that can handle applications distributed across different types of networks (e.g., CAN, FlexRay, TTP) consisting of nodes that may use different scheduling policies (e.g., static cyclic scheduling, fixed-priority preemptive scheduling, earliest deadline first).

Current modeling and design approaches often dimension systems for the worst case. However, embedded systems are growing more complex and dynamic than they used to be. E.g. in multi-media embedded systems, bit rates and encoding effort may vary by orders of magnitude depending on the complexity of the audio or video being played out, the complexity of the compression and on the required quality. Additionally, the embedded devices and application's functionality increases and they become more open to interaction with their environments. E.g. users may issue requests to the applications to change the resolution or frame rate. High-quality multimedia delivery on affordable embedded system's hardware requires cost-efficient realization of high throughput processing that is guaranteed to deliver the required performance. The platform needs to have sufficient resources to process the stream, even under the highest load conditions. Yet, it should not waste too many available resources when complexity of the stream is less. Current design approaches for multimedia embedded systems cannot deal appropriately with the increasing dynamism inside applications and the dynamically changing set of running applications. Often design approaches are based on worst-case analysis, resulting in over-dimensioned systems.

In order to (automatically) take informed design decisions, accurate analysis techniques are needed to:

- handle distributed applications, data and control dependencies;
- accurately take into account the details of the communication protocols;
- handle heterogeneous scheduling policies;
- take into account the fault-tolerance techniques used for dependability;
- capture the integration of control models and streaming models to understand the effects of sporadic events interfering with ongoing dataflow computations;
- efficiently use platform resources through statistical multiplexing based on a combination of worst-case and stochastic techniques.

3.2 Ongoing Work in the Partner Institutions

ETH Zurich

At the computer engineering institute of ETH Zurich there are several projects associated to ARTIST2. Two examples are given here:

The research group is part of the Swiss Competence Center on Mobile Information and Communication Systems. We investigate an extreme area in the design space of communicating objects: the area of low energy, small size, and large population. In particular, we approach research problem in the design, implementation and deployment of wireless ad-hoc networks. We are developing an autonomous wireless communication and computing platform based on a Bluetooth radio. The BTnode has been jointly developed at ETH Zurich by the Computer Engineering and Networks Laboratory (TIK) and the Research Group for Distributed Systems. In addition, the aim of the research project is to investigate composable platforms for wireless sensor and actuator networks. Its expected outcomes are a software and hardware methodology that enables modular composition and configuration of sensor/actuator nodes. Together with Siemens Building Technologies, we are investigating and developing a large wireless sensor network product for safety and security applications in buildings.

The research group at ETH is part of the EU IP project SHAPES. It is based on a specific hardware/software architecture paradigm: A heterogeneous tile is composed of a VLIW floating-point DSP, a RISC, on chip memory, and a network interface. It includes a few million gates, for optimal balance among parallelism, local memory, and IP reuse on future technologies. The software challenge is to provide a simple and efficient programming environment. Here, we will investigate a layered system software, which does not destroy algorithmic and distribution info provided by the programmer and is fully aware of the hardware paradigm. For efficiency and quality of service, the system software manages intra-tile and inter-tile latencies, bandwidths, computing resources, using static and dynamic profiling. The software accesses the on-chip and off-chip networks through a homogeneous interface. Generation after generation, the number of tiles on a single-chip will grow, but the application will be portable.

University Bologna

The research group at UNIBO is involved in a wide range of research activities within the scope of the ARTIST2 consortium,

Industrial cooperations. UNIBO has active funded research agreements with two major silicon vendors, namely STmicroelectronics and Freescale. Cooperation with STmicroelectronics focuses on Multi-processor systems on chip design methodologies and energy efficient MPSoC architectures. In this cooperation, UNIBO is co-developing low-power system interconnects, as well as energy-efficient level-one memory architectures for on-chip processor tiles. In the cooperation with Freescale, UNIBO is developing a complete software infrastructure for power management within the Linux operating system. The goal of the project called "extreme energy conservation", is to co-develop with Freescale the next-generation energy-aware operating system. The research prototypes developed within this cooperation are now being migrated into platform support software marketed by Freescale.

Research cooperation in EU-funded projects. In this area, UNIBO is participating to the CLEAN research project, an Integrated Project in the IST area. The goal of the project is to develop and demonstrate design tools for power optimization that can be used for advanced technology nodes (65nm and future nodes). The work of UNIBO is focused on power modelling at the platform level, integrating power models with a cycle-accurate virtual platform. Moreover, UNIBO is actively developing strategies for power minimization in execution platforms based on power gating. These strategies will require a synergistic hardware software infrastructure, as

well as cooperative dynamic resource management strategies. The project involves a number of industrial and academic partners, such as Politecnico di Torino, CEA-LETI, STMicroelectronics and several EDA SMEs.

DTU

At the department of Informatics and Mathematical Modelling at DTU, there are several projects associated to ARTIST2. Among these are:

The research group on Embedded Systems Engineering at IMM/ DTU is heading the Hogthrob project funded by the Danish Research Council. The aim of the project is to monitor sows in the farm by the use of wireless sensor networks. In particular, to be able to detect the heat period of the sows. We are investigating and developing a wireless sensor network platform with emphasis on low power hardware design and efficient embedded software development. We are developing a set of detection algorithms to detect abnormal behavior of the sows, like being in heat. These algorithms are developed from actually carrying out field experiments where sensor readings are correlated with video streams and traditional manual measurements for detecting heat. The aim is to build a power efficient sensor node for this detection. We are also investigating models of the individual sensor nodes as well as the entire sensor network, with the aim to develop a model-based development methodology for wireless sensor networks.

The research group is part of the Danish Strategic Research Councils project on model driven development of intelligent embedded systems (MODES). Modern embedded systems typically involve the monitoring and control of complex physical objects using a number of hardware and software components. The physical environment, the software and the hardware have to work harmoniously together in order for the embedded system to provide its desired functionality. These three system aspects constitute well established research areas with their own set of concepts, models, tools, and research agenda. The aim of the MoDES project is to improve the development process by adjusting and combining the models and tools from each research area into a coherent tool chain. The development process will be validated based on industrial case studies linking fundamental concepts and models to final products, via tools and enabling technologies. Hence, MoDES are involving some of the major Danish companies working on embedded systems. Both Danish research groups from ARTIST2; execution platforms (DTU) and test and verification (Aalborg), are partners in the project. A more strategic goal of the project is to strengthen and increase the research and development of embedded systems within Denmark.

The same group of Danish researchers from ARTIST2 are in the process of setting up a large national research project aimed at coordinating the national activities within embedded system design in order to strengthen the industrial development and innovation, the research fields and the PhD education. A major goal is to position Denmark for the coming EU (FP7) platform on embedded systems, ARTEMIS.

Embedded Systems Institute (ESI)

At the Embedded Systems Institute (ESI), especially the work in the Boderc project is relevant for the Execution Platforms cluster. This project aims at performance improvements of mechatronic systems. This includes several activities such as a comparison of performance analysis methods, models to predict the performance of real-time control software on various execution platforms, and new control strategies to improve performance. Measurements have been carried out to increase the insight in the relation between hardware parameters (such as cache sizes and memory speed) and software performance. Control strategies have been developed that take software and communication delays into account. To be able to make

explicit trade-offs between controller performance, software load and hardware costs, new control strategies have been developed that are based on event-driven control instead of conventional time-driven control strategies. For these new and emerging control strategies, analysis methods are being developed and validated on test set-ups.

In the Trader project at ESI, the emphasis is on improving the reliability of consumer electronics. In this project IMEC participates with techniques to dynamically reconfigure video processing tasks, for instance when low-quality input requires more error correction. Moreover, there is a collaboration with Leiden University on improving state observability of components.

In the ESI Ideals project, model-driven engineering techniques are developed for real-time distributed embedded systems. Models are used both for analysis purposes, in order to take well-founded design decisions, but also as a formal starting point to systematically derive hardware/software implementations in a predictable way. This is done through formal model transformations. The techniques are developed in the context of high-tech systems, where wafer scanners form the driving applications.

Linköping University

The ARTIST2 related activity in ESLAB, Linköping University, is to a large extent focused on the issue of distributed real-time systems with applications in automotive systems. This work is conducted in interaction with our industrial partners at Volvo. Our main goal is to develop models and tools for the analysis and optimisation of such systems. Emphasis is placed on the analysis of timing properties, considering the heterogeneous nature of such systems and the particularities of the various communication protocols. In our most recent research we have also considered the analysis of mixed static/dynamic protocols, such as Flexrey, which is likely to become a standard for certain automotive applications. On top of these timing analysis approaches we are building various system-level optimisation tools for application mapping, communication synthesis, priority assignment, etc.

One other issue we are exploring, in the same context of distributed real-time systems, is that of fault tolerance and, in particular, the issue of transient faults. There are two main aspects of interest here: (1) analysis of timing properties in the presence of faults and possible guarantees regarding worst case behaviour; (2) system optimisation, such that timing and fault tolerance requirements are satisfied given a certain, limited amount of resources.

Another research direction at ESLAB/Linköping University, of interest in the context of ARTIST2, is that of multiprocessor systems on chip. One of the main issues is energy efficient implementation of time-constrained and communication intensive systems. We are looking at energy vs. performance trade-offs in the context of voltage/frequency scaling and dynamic body biasing. Another issue is that of the interaction between communication mapping, energy consumption, and fault tolerance in complex systems on chip.

Besides being energy efficient and high performance, for many applications it is needed that multiprocessor SoC implementations are highly predictable with regard to their timing behaviour. While this issue has been investigated in the context of mono-processor systems, available results are inapplicable to modern multiprocessor architectures in which, for example, due to the shared access to sophisticated memory hierarchies, the individual WCETs of tasks are depending on the global system schedule. This is one of the issues we are currently investigating.

TU Braunschweig

In the context of the Soreal Project, TU Braunschweig defines an integrated development process for distributed embedded real-time systems, especially regarding real-time aspect in all phases of the development. This includes the integration of different techniques for describing, analysing and modelling real-time aspects. To be able to use different tools specialized in handling real-time aspects in different phases of the system development interfaces must be defined for them to efficiently work together.

In cooperation with Sharon Hu and Bren Mochocki from University of Notre Dame, TU Braunschweig works on power analysis techniques and heuristic and stochastic power optimization algorithms using DVS and SVS (Dynamic/Static Voltage Scaling). The so far developed algorithms are applicable to complex distributed systems with complex timing constraints (maximum jitter, end-to-end deadlines, etc.), and are capable of determining Pareto-optimal design trade-offs between system power consumption and timing properties.

TU Braunschweig develops techniques for optimizing the robustness of embedded real-time systems with respect to variations of system properties like worst-case execution/communication times, bus bandwidth, CPU clock rate, input data rate, etc. Reasons for such variation during the design process or in the field include updates, bug fixes, late feature requests, and product variants. The developed algorithms consider hard-real time constraints and are capable of optimizing a given system for static and dynamic design robustness. Thereby, the static design robustness optimization approach is applicable to the design scenario where system parameters are fixed early in the design process, whereas dynamic design robustness optimization approach includes possible counteractions to unforeseen system property changes, and is thus applicable to reconfigurable systems.

TU Braunschweig has continued to investigate design paradigms of MPSoC architectures. As opposed to distributed systems, a common feature here is the use of a shared memory that is accessed from each processor, introducing conflicts on the memory and interconnects. System designers often implement latency-hiding techniques to reduce the effect of waiting for data, by allowing frequent context switches to tasks that are ready. In ongoing research dependencies in such systems that have an influence on design properties such as end-to-end delays are systematically identified. Additionally, the timing of multiple coinciding memory accesses are investigated. Previous approaches had to assume a worst-case timing for each individual memory access. Due to large timing variations, this leads to a large deviation of analysis result and actual behaviour.

3.3 Interaction and Building Excellence between Partners

3.3.1 Integration Activities within the Cluster

The following list summarizes the integration activities within the cluster on execution platforms:

- *ETHZ*: Organization of an ARTIST2 Workshop on Distributed Embedded Systems, Leiden, The Netherlands, in November 2005. *Results*: (1) Understanding the different concepts and views of the design of distributed embedded systems by selected presentations. (2) Providing a set of benchmark problems for testing and comparing different approaches, see <http://www.tik.ee.ethz.ch/~leiden05/>.
- *SymtaVision - ETHZ*: Tutorial on Frameworks for System-Level Analysis of Real-Time Systems - SymTA/S and MPA, held at RTAS, San Jose, USA. *Results*: Combining the different approaches in terms of a common view on performance analysis and presenting the result at a major conference.

- *ETHZ – Embedded Systems Institute*: Applying the performance analysis method (MPA) at an industrial case study. *Result*: Joint publication at conference and in a journal [10].
- *ETHZ – Embedded Systems Institute – University of Nijmegen*: Using the benchmark problems defined at the workshop in Leiden to compare different approaches (MAP, SymTa/S, timed automata, MAST). *Result*: Master Thesis that compares the different approaches.
- *TU Braunschweig - ETHZ*: Combining the Symta/S tool with the implementation of the MAP performance analysis toolbox from ETHZ. *Result*: Concept for tool coupling and start of the implementation.
- *U Bologna – ETHZ*: Combining formal analysis and simulation in an integrated approach, several visits. *Result*: Tool coupling and a joint publication [11].
- *U Bologna – ETHZ*: Investigation of energy harvesting sensor nodes in terms of scheduling and energy consumption, PhD exchange (Davide Brunelli was for 7 months at ETHZ). *Results*: Two common publications [12, 13].
- *U Bologna – DTU*: Combining models for system-level simulation and cycle-true simulation in an integrated approach, visit of 3 weeks. *Result*: Tool coupling and a technical report, a joint publication is being considered.
- *U Bologna – DTU*: Extending the joint traffic generator to handle reactive behavior such as interrupts, visit of 1 week. *Result*: Tool development and two joint publications [3, 4]. Another two joint publications have been submitted.
- *DTU – TU Linköping*: A simulation environment for distributed real-time systems such as those used in automotive applications has been developed and implemented based on the ARTS environment, developed at DTU. *Result*: Tool transfer and extension.
- *Embedded Systems Institute – ETHZ - University of Tübingen*: Conference-wide special session on performance modeling for system-level design at the FDL conference in Lausanne.
- *TU Braunschweig – University of Notre Dame*: Refinement of previously developed power analysis and processor models. Realization of power optimization techniques for distributed real-time systems under timing constraints. *Results*: Two publications [14, 15].
- *TU Braunschweig – Syntavision GmbH*: Investigations how state-of-the art formal analysis techniques can be utilized in the industrial design process. *Results*: Several publications [16, 17, 18, 19, 20]
- *TU Braunschweig - ESLAB Linköping*: Razvan Racu and Arne Hamann held a workshop at ESLAB presenting recent research results of TU Braunschweig concerning system robustness optimization and the detection of scheduling anomalies. Additionally, a cooperation in the field of simulation pattern generation based on the scheduling anomalies detection algorithms was discussed.
- *U. Bologna - DTU*. Joint work on platform modelling both in terms of high-level traffic modelling for performance analysis, and in terms of building simulation infrastructure working at mixed abstraction levels. PhD Exchange students (Shankar Mahadevan from DTU was for 3 Months at UNIBO).
- *U. Bologna - Aachen*. Joint work on building a common simulation platform for ASIP integration in multi-core platforms (Students from UNIBO: Federico Angiolini and Francesco Poletti visited Aachen for one week).

- *U. Bologna – Dortmund*. Joint work on memory-aware compiler infrastructure for multi-core platform (Students from UNIBO: Federico Angiolini and Francesco Poletti visited Dortmund for 3 days).
- *U. Bologna – Linköping*. Joint work on scheduling and allocation for multi-processor platforms with power awareness (Students from Linköping visited unibo for several weeks).
- *Linköping U – Volvo*: Analysis of Distributed embedded systems with deadline and fault tolerance constraints; optimisation of soft real-time systems. Result: tool elaboration and joint publication [6, 21, 22, 23].
- *Linköping U – U Dortmund*: Extending current mono-processor techniques for on-line voltage/frequency scaling to multiprocessor on chip systems. Student mobility (Olivera Jovanovic, 7 months in Linköping). *Result*: Master thesis, tool implementation.
- *U Bologna – Linköping U*: Optimal mapping, scheduling and voltage scaling for time and energy constrained multiprocessors on chip, using Constraint Programming and ILP-based techniques. *Result*: implementation and common publication [24].
- *DTU – Linköping U*: Simulation environment for Distributed real-time embedded systems; extension of the ARTS modelling&simulation environment. *Result*: Tool development.
- *DTU – Linköping U*: PhD course at Linköping “Introduction to Sensor Networks”. Lectures at Linköping by Prof. Jan Madsen (DTU) and Ass. Prof. Srdjan Capkun (DTU).
- *Linköping U – TU Braunschweig*. Integration of analysis approaches for distributed real-time systems into the Symta/S environment. *Result*: tool integration.

3.3.2 List of Joint Publications

The following list contains publications, where authors are in different research sites which are participating in the ARTIST2 network and where at least one author is in the cluster on Execution Platforms. It clearly shows the degree of integration that has been achieved.

- [1] Lothar Thiele, Reinhard Wilhelm: Design for Timing Predictability. Dagstuhl Online, 2004.
- [2] Lothar Thiele, Reinhard Wilhelm: Design for Timing Predictability. Journal on Real Time Systems, 2004.
- [3] S. Mahadevan, F. Angiolini, M. Storgaard, R. G. Olsen, J. Sparsø, and J. Madsen. A network traffic generator model for fast network-on-chip simulation. In Proceedings of Design, Automation and Testing in Europe Conference 2005 (DATE05)
- [4] F. Angiolini, S. Mahadevan, J. Madsen, L. Benini, and J. Sparsø. Realistically rendering soc traffic patterns with interrupt awareness. In IFIP International Conference on Very Large Scale Integration (VLSI-SoC), September 2005.
- [5] Ernesto Wandeler, Lothar Thiele, Marcel Verhoef, Paul Lieverse: System Architecture Evaluation Using Modular Performance Analysis - A Case Study. Paphos, Cyprus, October, 2004.
- [6] Paul Pop, Petru Eles, Zebo Peng, Viacheslav Izosimov, Magnus Hellring, Olof Bridal: Design Optimization of Multi-Cluster Embedded Systems for Real-Time Applications. I Design, Automation and Test in Europe (DATE 2004).
- [7] M. Loghi, F. Angiolini, D. Bertozzi, L. Benini, R. Zafalon, "Analyzing on-chip communication in a MPSoC environment", IEEE/ACM Design, Automation and Test in Europe, Paris, France, Feb 2004.

-
- [8] Jan Staschulat, Rolf Ernst, Andreas Schulze, Fabian Wolf. Context Sensitive Performance Analysis of Automotive Applications. In Designer's Forum at Design, Automation and Test in Europe (DATE), 2005.
- [9] Bren C. Mochocki, Xiaobo S. Hu, Razvan Racu, Rolf Ernst. Dynamic Voltage Scaling for the Schedulability of Jitter-Constrained Real-Time Embedded Systems, ICCAD 2005.
- [10] E. Wandeler, L. Thiele, M. H. G. Verhoef, P. Lieverse. System Architecture Evaluation Using Modular Performance Analysis - A Case Study. Journal Software Tools for Technology Transfer (STTT), 2006.
- [11] Simon Künzli, Francesco Poletti, Luca Benini, Lothar Thiele: Combining Simulation and Formal Methods for System-Level Performance Analysis, IEEE Design Automation & Test in Europe (DATE), Munich, Germany, March 2006.
- [12] C. Moser, D. Brunelli, L. Thiele, and L. Benini, "Real-time scheduling with regenerative energy.", 18th Euromicro Conference on Real-Time Systems (ECRTS 2006), Dresden, Germany, July 5-7, 2006.
- [13] C. Moser, D. Brunelli, L. Thiele, and L. Benini, "Lazy scheduling for energy harvesting sensor nodes.", The Fifth IFIP Working Conference on Distributed and Parallel Embedded Systems (DIPES 2006), Braga, Portugal, October 13-15, 2006.
- [14] Bren Mochocki, Xiaobo Sharon Hu, Razvan Racu, Rolf Ernst. Dynamic Voltage Scaling for the Schedulability of Jitter-Constrained Real-Time Embedded Systems. In *International Conference on Computer Aided Design (ICCAD)*, San Jose, USA, November 2005.
- [15] Razvan Racu, Arne Hamann, Rolf Ernst, Bren Mochocki, Sharon Hu, Methods for Power Optimization in Distributed Embedded Systems with Real-Time Requirements, In Proc. International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES), Seoul, Korea, October 2006
- [16] Kai Richter, Marek Jersak, Rolf Ernst. How OEMs and suppliers can tackle the network dimensioning problem. *Embedded Real Time Software Congress (ERTS06)*, Toulouse, France, January 25-27, 2006.
- [17] Kai Richter, Rolf Ernst. Real-Time Analysis as a Quality Feature: Automotive Use-Cases and Applications, *Embedded World 2006 Fair and Conference*. Nuremberg, Germany - February 14-16, 2006.
- [18] Kai Richter, Marek Jersak, Rolf Ernst. How OEMs and suppliers can face the network dimensioning challenges. *Design, Automation and Test in Europe (DATE) Conference*, Special Track Automotive Designer's Forum, Munich, Germany, March, 2006.
- [19] Kai Richter, Rolf Ernst. Applying Real-Time Network Research in the Automotive Industry: Lessons Learned and Perspectives, *Euromicro Conference on Real-Time Systems (ECRTS)*, satellite workshop on Real Time Networks (RTN), Dresden, Germany, July 2006.
- [20] Kai Richter, Marek Jersak, Arne Hamann, Rolf Ernst. Scheduling Analysis in the Automotive Design Flow. *ARTIST2 Workshop at the International Conference on Embedded Software (EMSOFT)*, Seoul, Korea, October, 2006.
- [21] L. A. Cortes, P. Eles, Z. Peng, "Quasi-Static Scheduling for Multiprocessor Real-Time Systems with Hard and Soft Tasks", 11th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA'05), Hong Kong, 2005.
- [22] L. A. Cortes, P. Eles, Z. Peng, "A Quasi-Static Approach to Minimizing Energy Consumption in Real-Time Systems under Reward Constraints", 12th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA'06), Sydney, Australia, 2006.

- [23] L. A. Cortes, P. Eles, Z. Peng, "Quasi-Static Assignment of Voltages and Optional Cycles in Imprecise-Computation Systems with Energy Considerations", IEEE Transactions on VLSI Systems (accepted for publication)
- [24] M. Ruggiero, G. Pari, A. Guerri, M. Milano, D. Bertozzi, L. Benini, A. Andrei, "A Cooperative, accurate solving framework for optimal allocation, scheduling and frequency selection on energy-efficient MPSoCs", International Symposium on System-on-Chip, Tampere, Finland, 2006.

4. Overall Assessment and Vision for the Cluster

4.1 Assessment

There has been substantial progress in integrating different research directions and view points. Indicators that show this clearly are (a) the joint participation in summer schools, workshops and tutorials and (b) the number and quality of joint publications, and (c) the integration of tools.

4.2 Vision and Long Term Goals

The research in embedded systems still is fragmented. This not only is true within a single subject but also between several subdisciplines. Examples are the parallel efforts in real-time scheduling and real-time analysis in the area of 'Execution Platforms', 'Hard Real-Time Systems' and 'Software Components'. It is one of the major goals of the cluster on 'Execution Platforms' to establish closer links to the other communities and to take advantage of the scientific results and insights.

Cross-layer design is a key issue in embedded systems. The classical view of a strict layering according to chosen abstraction levels does not work any more because of the importance of non-functional constraints and limited resources. Therefore, completely new concepts are necessary that enable the integrated modelling and design under predictability AND efficiency constraints. It is expected that this move towards a resource-aware design trajectory involves all current layers and a breakthrough can be obtained by integration only.

4.3 Future Work and Evolution

4.3.1 Technical Description

System Modelling Infrastructure

Within the system modelling infrastructure ,we are planning the following activities within the next 18 months:

TU Linköping will further develop the simulation environment based on the ARTS environment from DTU, towards a simulation environment for distributed embedded systems. In particular, they will evaluate various protocols on worst case and average performance, evaluate the pessimism of various response time analysis approaches, and evaluate the impact on quality of control. Work on dependable systems, in particular for safety critical issues, will be done in cooperation with DTU.

TU Braunschweig will continue its work extending the semantic model of SymTA/S to efficiently cover MPSoC architectures. Additionally, TU Braunschweig will conduct further research in sensitivity analysis techniques and its application to predictable system design.

University of Bologna and DTU will consolidate their cooperation on model integration between MPARM and ARTS. Each partner will continue the development of their respective modelling environments.

DTU will continue research on the ARTS environment, extending the modelling capabilities toward lab-on-a-chip, in particular towards biochips, i.e. platforms which are able to move microfluidic droplets around within an array of cells in order to mix and analyse chemical liquids.

DTU will extend the research on the ARTS environment with modelling capabilities for dynamically reconfigurable architectures. This requires that not only the software can be moved and modified during platform execution, but also the hardware itself. The aim is to be able to model and analyse new architectures for reconfigurable computing. DTU will also continue the research on modelling wireless sensor networks.

DTU will continue the work on linking simulation models with formal models. In particular they will extend their effort in formalizing the ARTS model using timed automaton based on UPPAAL. This will allow the same platform model to be expressed as a simulation model and as a formal model. The work will be carried out in cooperation with the research group at CISS in Aalborg which is a partner in the cluster on test and verification.

Communication-Centric Systems

TU Braunschweig and ETH Zürich will implement the changes needed for a combination of the SymTA/S and the MPA frameworks. An example application will be analyzed to show the strength of the new combined approach. These steps should also result into a joint publication of the results.

ESLAB Linköping will further develop optimization approaches for systems built on heterogeneous communication protocols, in particular, Flexray.

ESLAB Linköping will multiply its research efforts in analysis and optimization techniques for fault-tolerant distributed systems. These techniques will be incorporated into the tools developed by the various partners, in particular, Symta/S in Braunschweig.

TU Braunschweig will conduct further research in the extension of the SymTA/S model with hierarchical event models.

TU Braunschweig will development advanced techniques for system robustness optimization. This will leverage the applicability of the SymTA/S methodology for reliable and predictable embedded system design.

TU Braunschweig will develop mapping optimization approaches with automatic communication synthesis.

TU Braunschweig will refine and further develop semantical extensions for formal analysis of MPSoC architectures with focus on shared memory accesses. This includes the coupling of the tools SymTA/S und SymTA/P (both developed at TU Braunschweig). This activity could profit from synergy effects with the work on hierarchical event models.

University of Bologna will focus on NoC architecture exploration. A more modular and scalable system-inteconnect architecture development approach will be studied in details, along with cross-benchmarking against traditional system interconnects.

DTU will focus on platform exploration covering the layers of application software, operating system and hardware platform, i.e. processing elements and interconnects. Special emphasis will be on the interconnect architectures of multiprocessor system-on-chip.

Low-Power Design

Future work in this activity will focus on two main areas:

Power-optimization for multi-core systems.

Work in this area, will explore in more depth the interaction between resource allocation and scheduling and power optimization. Consideration will be given to non-stationary and non-deterministic behaviour of applications. While in simpler models applications can be abstracted as stationary data-flow graphs, a more realistic model includes non-deterministic behaviour due to conditionals and due to data-dependent execution times. Moreover, task graphs are dynamical created and destroyed in real non-stationary applications. Research on these

issues will be carried out in cooperation between UNIBO and Linköping. Soft constraints and multi-objective optimization will be considered as well, in cooperation with DTU.

Power management for wireless sensor networks.

ETHZ and UNIBO will strengthen their cooperation on techniques for optimizing not only power consumption, but also usage of harvested energy in sensor networks capable of harvesting energy from the environment. The impact on scheduling decisions and on various quality of service metrics (e.g. rate of sensor processing) will be analyzed as well.

Resource-Aware Design

The future work in this activity will focus on the following areas:

Predictability issues on multiprocessors on-chip.

Linköping will continue work in this area by working toward an integrated environment for execution time analysis in multi-core architectures, including WCET estimation, system scheduling and optimisation, taking into account the system wide interactions. Furthermore, the cooperation of the Linköping group with Braunschweig on WCET analysis and Bologna on the hardware implementation will continue. Cooperation with Dortmund on frequency and voltage scaling will continue. The group at the University of Saarbrücken will extend its estimation techniques for WCET bounds towards more complex architectures.

Efficient utilization of memory hierarchies

Over the next reporting period, Dortmund will work on efficient utilization of memory hierarchies by multi-process applications. The group will extend the memory allocation approaches to improve the scratchpad utilization by multi-process applications comprising of periodic and aperiodic tasks. A further improvement of the proposed approaches will be achieved by supporting applications with cooperative multi-tasking. Memory allocation approaches will be considered as part of a compilation framework tightly integrated with the multi-processor SoC (MPARM) simulator from University of Bologna. The integration of the highly configurable memory hierarchy simulator developed at Dortmund into MPARM is also planned for the coming months. It is expected that these research efforts will further strengthen the cooperation between University of Dortmund and University of Bologna.

4.3.2 *Current and Future Milestones*

WP1 Platform: System Modelling Infrastructure

Activity Leader: Jan Madsen (Technical University of Denmark)

- Year2: Initial definition of the modelling platform (achieved). Several simulation- and formal-based models have been investigated and extended towards integration. Early integration of the simulation-based models, ARTS and MPARM, and of the formal-based models SymTA/S and Real-Time Calculus has been achieved. Initial linking between simulation- and formal-based models, MPARM and Real-Time Calculus has been investigated.
- Year3: Version 1 of the system modelling platform implementation. Due to the experience gained with the different modeling formalisms, it was found that rather than aiming for a single unified model, the focus should be on further exploration of the existing models and in particular their interaction. Therefore, the focus will be on linking and integrating different modeling formalisms and to extend the models to support analysis and exploration as needed by the other cluster activities.
- Year4: Integration of modelling formalisms covering different levels of abstraction. Effective strategies for selecting model formalisms. Refinement and dissemination of models.

WP3 NoE Integration: Resource-aware Design

Activity leaders: Luca Benini (University of Bologna) and Peter Marwedel (University Dortmund)

- Year2: A set of tools that can interact and work together and demonstrate the achievable optimizations on a particular hardware platform (achieved). Integration between AACHEN Lisa tools and Unibo's MPARM has been achieved. An early version of the memory aware compiler by Dortmund has been targeted to the MPARM platforms.
- Year3: Strengthening the integration between Dortmund and Bologna: development of a memory-aware compiler for parallel multi-task applications. Linkoepping will also work to an integrated execution analysis environment for multi-core systems.
- Year4: A methodology for the design of predictable embedded systems

WP8 Cluster Integration: Communication-centric systems

Activity leader: Rolf Ernst (TU Braunschweig)

- Year1 (achieved): Assess the state-of-the-art in models that take into consideration the particularities of various quasi-standard communication protocols during system analysis and scheduling
- Year2: New best-case/worst-case models for hard real-time systems and at combined statistical and interval models for QoS applications in multi-media. These models may combine communication and computation, different models of computation, event models and scheduling policies (achieved)

Due to the feedback of practical applications it was found that interval models cover a wide range of QoS application. Therefore, it was considered as more useful to extend work in this direction rather than starting a new work in the domain of combined statistical and interval models. This is subject to future work.

The following main results were achieved:

The industry increasingly applies hierarchical communication protocols, such as the automotive FlexRay Standard. New timing analysis techniques were developed to follow that trend. Since system dependability and flexibility are growing demands in embedded systems, techniques for fault tolerance and robustness measurement were developed and included in communication modelling and optimization. Additionally, case studies were performed to demonstrate the feasibility and practicability of the research results. Power optimization techniques were developed, since low power design is a new and urgent requirement in mobile and streaming applications.

- Year3: Analytic methods to estimate system properties
- Year4: Refinement and dissemination of these methods

WP8 Cluster Integration: Design for low power


Activity leader: Luca Benini (University of Bologna)

- Year2: Component models will be investigated that model power dissipation of system components (achieved)) this objective has been achieved: several extensions to the MPARM platform power modelling capabilities have been developed (multi-cluser systems, multi-frequency domains, multiple-voltage domains)


- Year3: Effective strategies for power management and power aware allocation and scheduling for both single-chip and distributed systems
- Year4: Integration of the different levels of abstraction - from scheduling via operating systems to system design - participating in low power design


5. Cluster Participants

5.1 Core Partners


Cluster Leader	
	Lothar Thiele (ETH Zurich)
Technical role(s) within Artist2	Main areas of research: Embedded Systems and Software Artist2 activities and role: Communication Centric Systems: Formal Performance Analysis, Linking Simulation and Verification, Design Space Exploration of Embedded Systems
Research interests	Research interests include models, methods and software tools for the design of embedded systems, embedded software and bioinspired optimization techniques.
Awards / Decorations	In 1986 he received the "Dissertation Award" of the Technical University of Munich, in 1987, the "Outstanding Young Author Award" of the IEEE Circuits and Systems Society, in 1988, the Browder J. Thompson Memorial Award of the IEEE, and in 2000-2001, the "IBM Faculty Partnership Award". In 2004, he joined the German Academy of Natural Scientists Leopoldina. In 2005-2006, he was the recipient of the Honorary Blaise Pascal Chair of University Leiden, The Netherlands.

Activity Leader for Cluster Integration: Design for Low Power Activity Leader for NoE Integration: Resource-aware Design	
	<p>Luca Benini (University of Bologna)</p>
<p>Technical role(s) within Artist2</p>	<p>Main areas of research: Execution platforms</p> <p>Other projects involved in: low power design, communication-centric architectures</p> <p>Artist2 activities and role: JPRA Communication centric Systems, JPRA Design for Low Power (activity leader), JPRA Resource-aware design (co-activity leader)</p>
<p>Research interests</p>	<p>Research interests are in computer architecture and computer-aided design of digital systems, with special emphasis on low-power applications and SoC design.</p>
<p>Notable past projects</p>	<p>IST-Clean Contributes to the development of low-power design technologies for deep submicron technologies</p> <p>http://clean.offis.de/</p> <p>MARM project A collaborative infrastructure for MPSOC research. Virtual simulation platform in SystemC, with a complete software environment</p> <p>http://www-micrel.deis.unibo.it/sitnew/research/marm.html</p>
<p>Awards / Decorations</p>	<p>IEEE Senior Member</p>
<p>Further Information</p>	<p>Visiting professor at EPFL</p>

Activity Leader for Cluster Integration: Communication-centric systems	
	Rolf Ernst (TU Braunschweig)
Technical role(s) within Artist2	Main areas of research: Embedded Systems Artist2 activities and role: Communication Centric Systems: Formal Performance Analysis, Design Space Exploration of Embedded Systems, Sensitivity Analysis of Embedded Systems. System modelling infrastructure: Flexibility Optimization of Embedded Systems.
Research interests	Research interests include embedded architectures, hardware-/software co-design, real-time systems, and embedded systems engineering.

Activity Leader for Platform: System Modelling Infrastructure	
	Jan Madsen (Technical University of Denmark)
Technical role(s) within Artist2	Main areas of research: Embedded Systems Design and Modeling Artist2 activities and role: System Modelling Infrastructure, Communication-Centric, Systems, Design for Low-Power
Research interests	Research interests include high-level synthesis, hardware/software codesign, System-on-Chip design methods, and system level modeling, integration and synthesis for embedded computer systems.
Role in leading conferences/journals/etc in the area	He is Program Chair for DATE07. He has been Tutorial Chair and Program Vice Chair for DATE06, Workshop Chair for CODES+ISSS'05, General Chair of CODES '01 and Program Chair of CODES '00. He is on the editorial board of the journal "IEE Proceedings – Computers and Digital Techniques"
Awards / Decorations	In 1995 he received the Jorck's Foundation Research Award for his research in hardware/software codesign

	<p>Petru Eles (Linköping University)</p>
<p>Technical role(s) within Artist2</p>	<p>Main areas of research: Embedded Systems Artist2 activities and role: Communication Centric Systems: analysis, optimisation. Low Power: modeling, optimisation, power management. System modeling infrastructure: modelling and simulation of distributed embedded systems.</p>
<p>Research interests</p>	<p>Research interests include electronic design automation, hardware/software co-design, real-time systems, design of embedded systems and design for testability.</p>
<p>Role in leading conferences/journals/etc in the area</p>	<ul style="list-style-type: none"> - Associate Editor, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems; - Associate Editor, IEE Proceedings - Computers and Digital Techniques; - TPC Chair and General Chair, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS). - Topic chair, Design Automation and Test in Europe (DATE). - Topic Chair, Int. Conference on Computer Aided Design (ICCAD). - Program chair of the Hw/Sw Codesign track, IEEE Real-Time Systems Symposium (RTSS).
<p>Awards / Decorations</p>	<ul style="list-style-type: none"> - Best paper award, European Design Automation Conference (EURO-DAC), 1992. - Best paper award, European Design Automation Conference (EURO-DAC), 1994. - Best paper award, Design Automation and Test in Europe (DATE), 2005. - Best presentation award, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS), 2003. - IEEE Circuits and Systems Society Distinguished Lecturer, for 2004 - 2005.

	<p>Jozef Hooman (Computing Science Department, Radboud University Nijmegen, Embedded Systems Institute, Eindhoven)</p>
<p>Technical role(s) within Artist2</p>	<p>Main areas of research: Development of Embedded Systems, Performance and Reliability of Software Artist2 activities and role: Performance Analysis in the System Design Process</p>
<p>Research interests</p>	<p>Research interests: formal specification and compositional verification of distributed real-time and fault-tolerant systems. Design of technical applications, e.g. using a combination of the UML and formal methods. Applications of the interactive theorem prover PVS.</p>

5.2 *Affiliated Industrial Partners*

	Magnus Hellring (Volvo Technology Corporation, Manager Systems and Architecture)
Technical role(s) within Artist2	Architecture and Design of Automotive Embedded Systems

	Roperto Zafalon (STM, Advanced System Technology – Research and Innovation, Manager Low Power System Design)
Technical role(s) within Artist2	Main areas of research: Low Power System Design Artist2 activities and role: JPRA design for low power, JPRA Resource-aware design

	Fabian Wolf (Volkswagen AG)
Technical role(s) within Artist2	Software and Hardware for Embedded Systems in Automotive Applications

	Kai Richter (SymTAVision GmbH)
Technical role(s) within Artist2	Formal Performance Analysis and Optimization of Embedded Systems, Reliable System Integration, Early Architecture Exploration

	Dirk Ziegenbein (Robert Bosch AG)
Technical role(s) within Artist2	Automotive Software Architectures

	Peter Mårtensson (Nokia Denmark)
Technical role(s) within Artist2	Platform architectures for mobile terminals

5.3 *Affiliated Academic Partners*

	Axel Jantsch (Royal Institute of Technology Stockholm)
Technical role(s) within Artist2	Design Methodology for Embedded Systems
	Giovanni DeMicheli (EPFL Lausanne)
Technical role(s) within Artist2	Main areas of research: Design Methodology for Embedded Systems, Low Power Design Artist2 activities and role: JPRA communication centric design
	Donatello Sciuto (Politecnico Di Milano)
Technical role(s) within Artist2	Design Methodology for Embedded Systems, Low Power Design
	Ed Deprettere (University Leiden, The Netherlands)
Technical role(s) within Artist2	Main areas of research: Design Methodology for Embedded Systems, Signal and Image Processing, Algorithm Design and Mapping Artist2 activities and role: Preparation of ARTIST2 Workshsop on Embedded Systems in Leiden, The Netherlands; Visists to Zurich in order to discuss on JPRA "Communication Centric Systems".
	Eugenio Villar, Pablo Sanchez (Universidad de Cantabria)
Technical role(s) within Artist2	Design and Implementation of Embedded H/S Systems
	Geert Deconinck (Katholiecke Universiteit Leuven)
Technical role(s) within Artist2	Dependability, embedded systems, control & automation, real-time, robust communication, interdependencies, critical information infrastructure protection
	Luciano Lavagno (Politecnico di Turino)
Technical role(s) within Artist2	Asynchronous Circuit Design and Testing, H/S Codesign

5.4 *Affiliated International Partners*

	Sharon Hu (University of Notre Dame)
Technical role(s) within Artist2	Design for Low Power