Year 2 Review
Paris, November 8th and 9th, 2006

Achievements and Perspectives :

Compilers and Timing Analysis

Cluster leader : Rainer Leupers

RWTH Aachen

High-Level Objectives

- Combine expertise of leading European research institutes and companies in selected areas of embedded compilers
  - Efficient machine code generation
  - Timing-aware compilation
  - Verification
- Build on common compiler platforms instead of pure in-house solutions
- ARITST2 as an infrastructure for networking, demonstration and dissemination of new technologies

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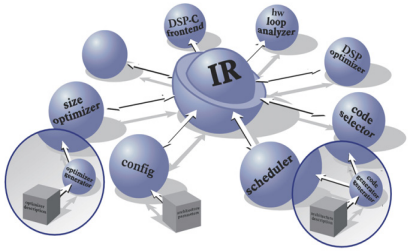
State of the Art

- Many compiler platforms scattered in academia and industry
  - Inefficient but difficult to overcome in practice
  - ARTIST2 focused primarily on CoSy (similar to e.g. use of gcc in HiPEAC)
- Embedded code quality is never "good enough"
  - New demanding applications, new advanced embedded processor architectures
- Compilers are generally not timing nor safety nor memory aware

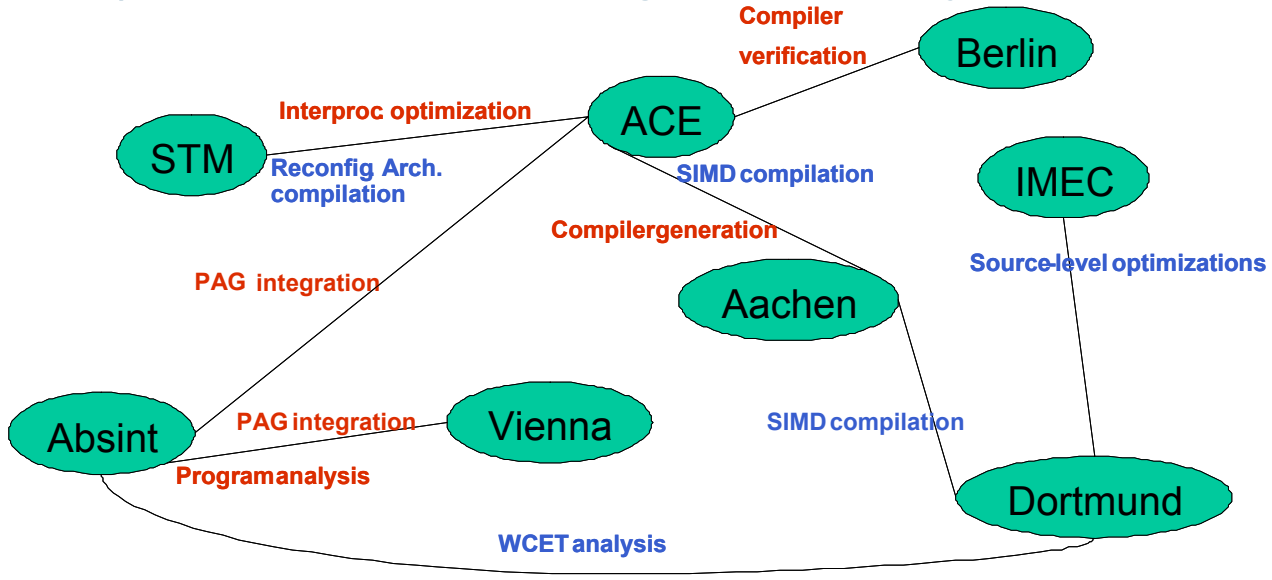


Research Trends

- Power/energy aware processor architectures and code generation
  - Battery powered embedded systems
- Source-level code optimizations
  - Complementing capabilities of traditional compilers
- Code optimization for new architectures
  - SIMD, scratchpad memory aware, …
- Dependability requirements
  - WCET aware compilation
  - Verification of optimizing compilers

Integration and Building Excellence

- Not all partners have the same research interests, therefore
  - 2 major activities: compiler platform (S. Glesner) and architecture aware compilation (R. Leupers)
  - 2 global cluster meetings per year
  - "Mini-cluster" structure for day-to-day cooperation, linked e.g. via common compiler platforms
  - Each partner himself has a large network beyond ARTIST2



Integration and Building Excellence

- Available results with ARTIST2 sponsoring include:
  - ACE CoSy academic workshop with ARTIST2 participants
  - ACE guest lectures in compiler classes at Aachen
  - IMEC training on DTSE methodology
  - Aachen/ACE code optimization engines in beta use in industry
  - Berlin/ACE: first code optimization verification in place
  - Vienna/Absint: PAG/ROSE infrastructure integration
  - Dortmund/Absint: WCET aware compiler tool chain
  - STM/ACE: retargetable compiler for reconfigurable processors
  - Many joint publications at leading conferences, e.g. DATE:
    - Dortmund/Bologna, Dortmund/Absint, IMEC/Bologna, Aachen/Bologna, Aachen/ACE, ...

Integration and Building Excellence

- Beyond compiler cluster:
  - Compiler/architecture interface:
    - Dortmund/Bologna: coherent memory aware compilation and simulation tool chain based on MPARM platform
    - Aachen/Bologna: MPARM/LISATek coupling
  - Industrial exploitation:
    - Dortmund: cooperation with Infineon on bit-true data flow analysis
    - IMEC: DTSE transfered via M4 project to semiconductor vendors
    - Absint: integration of results into commercial tool chain
    - ACE/Aachen/CoWare: LISATek Processor Designer product and code optimization engines

Integration and Building Excellence

- Dissemination with ARTIST2 sponsoring (short list):
  - SCOPES: leading European event in code generation for embedded systems (Dortmund, Aachen, ACE,...)
  - ESWeek/Seoul: leading international event on embedded software and EDA, incl. CASA workshop on SoC compilers
  - HiPEAC/ACACES: compiler courses for >100 students
  - Xian spring school: embedded systems course (P. Marwedel)
  - Nokia Compiler Workshop (P. Marwedel, R. Leupers, A. Krall)
  - SHAPES/CASTNESS: winter school involving IPs and ARTIST2 guest lecturers
  - ALARI: Master of ES design courses (P. Marwedel, R. Leupers)
  - EPFL: Advanced Digital Systems Design course for industry
  - COCV ETAPS 2007 Workshop (S. Glesner)

HiPEAC COMPILATION ARCHITECTURE

SCOPES 2007 Workshop on Software & Compilers for Embedded Systems

Università della Svizzera italiana

ALaRI Advanced Learning and Research Institute
Education for leading-edge information technologies in Embedded Systems Design

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Assessment at Y0+2

- What is going well
  - Participation of key industrial players (Absint, ACE)
  - Common compiler platform established
  - Mini-cluster structure is very effective
  - TU Berlin as new affiliate partner
  - Many visible results (integrated SW prototypes, successful meetings, staff mobility, joint papers, dissemination activities)
  - Reduced reporting overhead over Y1
- What is not going well
  - Very limited NoE funding per partner results in suboptimal motivation
  - NoE coordination needs improvements (e.g. need clear procedures in some financial management issues)
  - Splitting between two major activities (compiler platform + architecture aware compilation) has become artificial
  - Lack of resources for TU Berlin (compiler verification)

Structural changes

- After Y2, all compiler cluster activities are centered around platform based code generation
- Merge „compiler platform“ and „architecture aware compilation“ activities into one unified activity
  - *Platform based code optimization and verification*
- TU Berlin (Prof. Sabine Glesner) to take activity lead and to join ARTIST2 as a core partner from Y3 on
- Budget to be reallocated from STM budget

Future Work

- Visions:
  - Strengthen position of European compiler researchers, tool providers, and tool users in industry
  - Make industry aware of new research results (papers, courses, etc.), facilitate technology transfer
  - Exploit results in teaching (guest lectures, summer schools, etc.)
  - Establish and maintain stable network structure beyond ARTIST2 (spatially and temporally)

Specific future work (18 months)

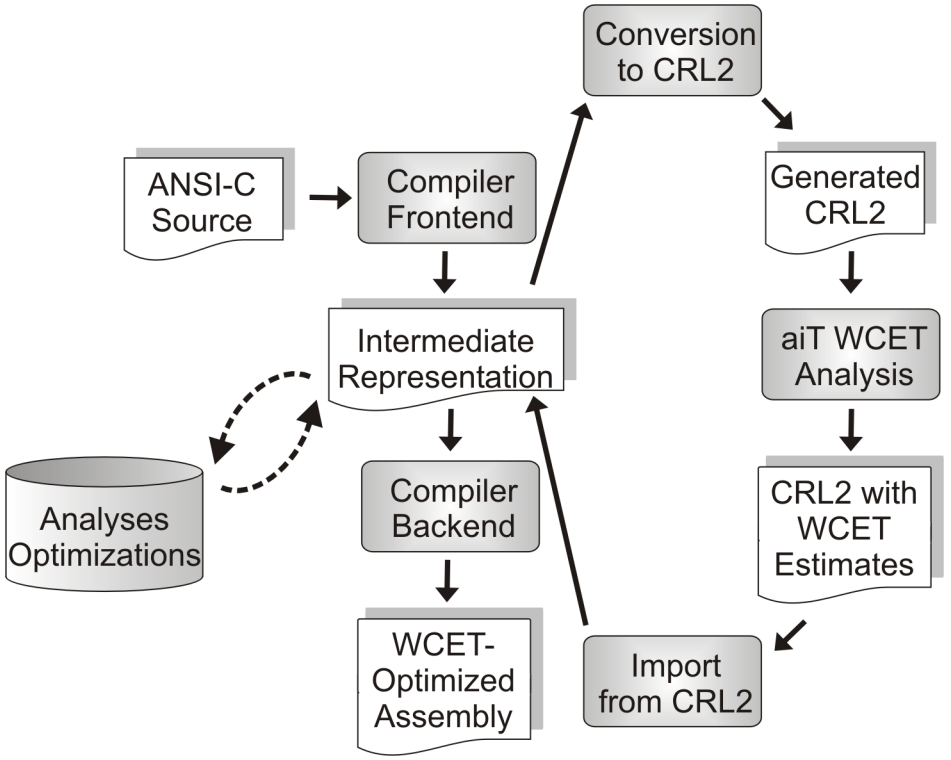
- Dortmund/IMEC: use of memory hierarchies for WCET minimization, source-to-source code optimization, ...
- Absint/USaar: ILP based register allocation
- ACE/Aachen: refinement of SIMD optimization
- Berlin/ACE: verification of compiler engines
- Vienna/Absint: ROSE/PAG coupling for whole program analysis
- Dissemination activities by all partners as in Y1, Y2

General Discussion on the Deliverables
D13-CTA-Y2: Architecture aware compilation

- *Report needs further elaboration. Is highly synthetic and does not go in sufficient detail. Is in contrast with similar reports from other clusters which are much more complete. It has 11 pages where all other reports go over 16.*
  - *Same page count as D15-CTA-Y2 (compilers platform)*
  - *Activity report partially contained in cluster progress report (32 pages)*
- *Chapter 2: publications: no links to conference websites or publications*
  - *Publications are correctly listed, hyperlinks required?*
- *Chapter 3 on Future Work and evolution: gives too roughly an overview in years. It does not go in detail of what the partners are going to do.*
  - *See also cluster progress report and compiler platform report*
  - *See "structural changes": merger of two activities from now on*

Scientific Highlights (arch. aware compilation)

- New direction in WCET aware compilation:
  - Compiler using Timing Model WCET Analysis
- Opportunities:
  - Precise WCET Information for Runtime Optimizations
  - Aggressive Optimizations, respecting WCET Constraints
  - Tighter WCET Bounds
  - Avoiding time-consuming Iterations by the Designer



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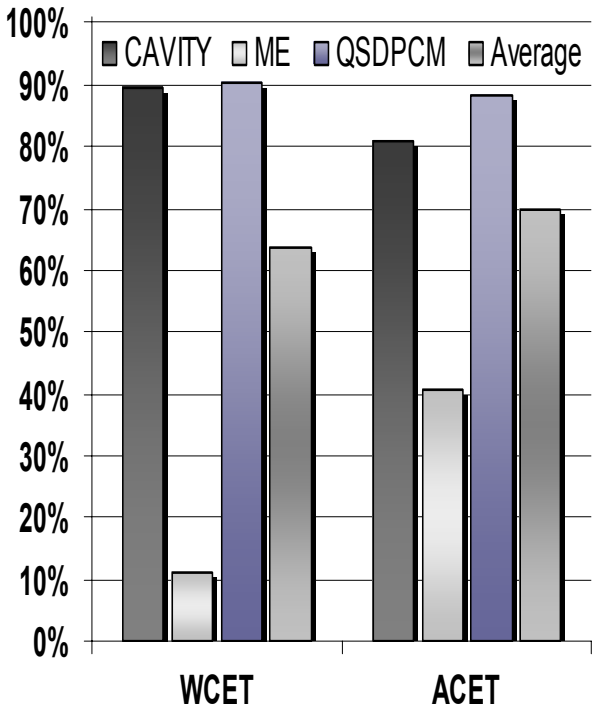
Scientific Highlights (arch. aware compilation)

- Impact of Source-Level Transformations on WCET
- Loop Nest Splitting (LNS):
  - Multimedia Applications (e.g. MPEG4): Irregular Control Flow
  - Poor Timing Predictability, Pipeline & Cache Behavior
  - LNS: Automated Analysis of Loops and If-Statements
  - Rewrites Source Codes to get Regular Control Flow
- Improves Average-Case Performance by 30%, but WCET by 38%.
- Fully compatible with IMEC's DTSE Data-Flow Transformations



ARM7 Thumb

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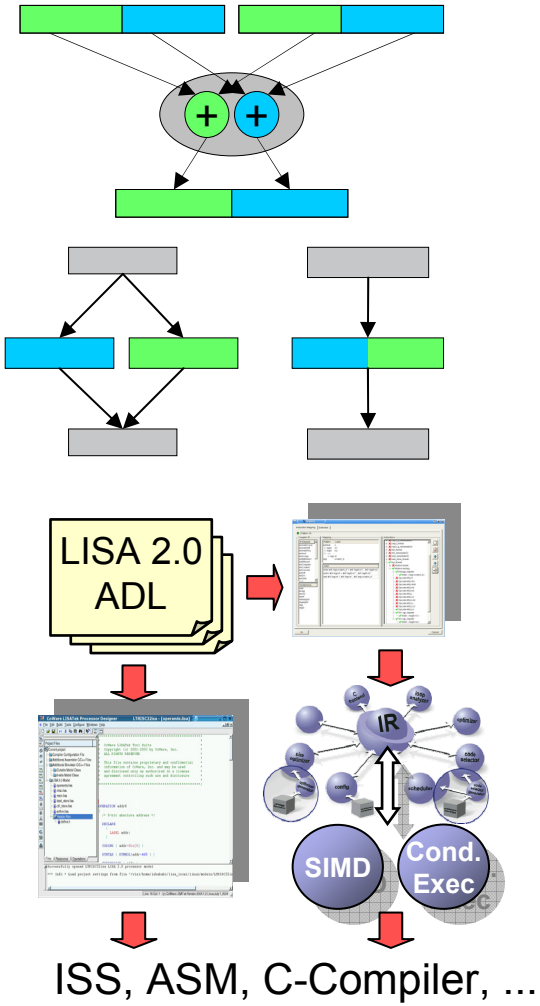
Scientific Highlights (arch. aware compilation)

- Retargetable code optimizations
  - Single Instruction Multiple Data (SIMD)
  - Conditional Execution
- Integrated into CoSy Platform
  - New optimization engines
  - Plug and play fashion
- Complete & retargetable path from ADL models to highly optimizing C-compilers
  - E.g. CoWare Processor Designer
- In beta use by industry partners
- Mobility funding from ARTIST2



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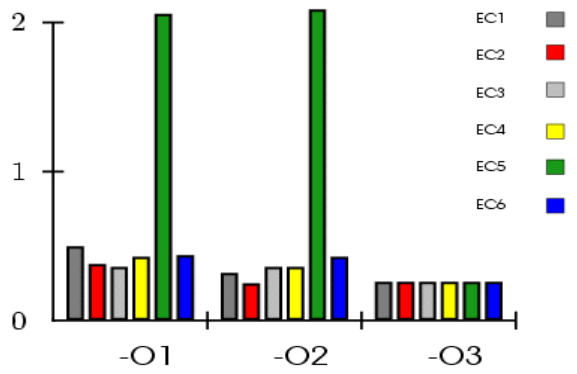
Scientific Highlights (arch. aware compilation)

- TU-Vienna determined high-level C++ programming styles suitable for programming DSPs with ROSE-PAG
- Evaluated 6 different levels of abstraction that give similar performance as low-level C code (GNU 4.0)
- The low-level C code is frequently found in DSP codes and benchmarks
- Vision: use safe HL-abstractions but get similar performance or code size



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Scientific Highlights (compiler platform)

- ACE CoSy as a common platform
- CoSy training to partners
- CoSy used for teaching (Aachen: compiler design course, master theses, ALARI (www.alari.ch), ...)

CoSy training, May '06

CoSy Community Gathering (CCG), AMS, Oct '06

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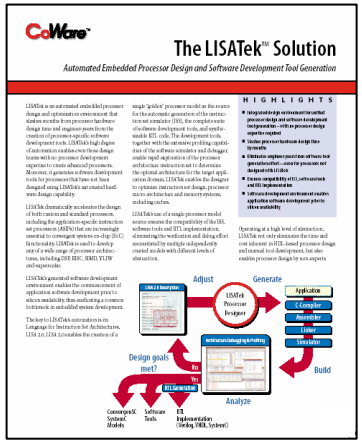
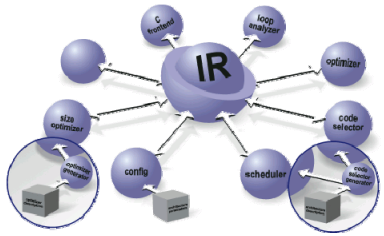
Scientific Highlights (compiler platform)

- Retargetable C-compiler generation based on
  - LISA 2.0 Architecture Description Language
  - CoSy Platform
- Fully integrated into an industry proven ASIP design platform
  - SW tools (C-Compiler, Simulator, ...)
  - HW models (VHDL, SystemC, ...)
- Commercially available from CoWare
  - LISATek Compiler Designer





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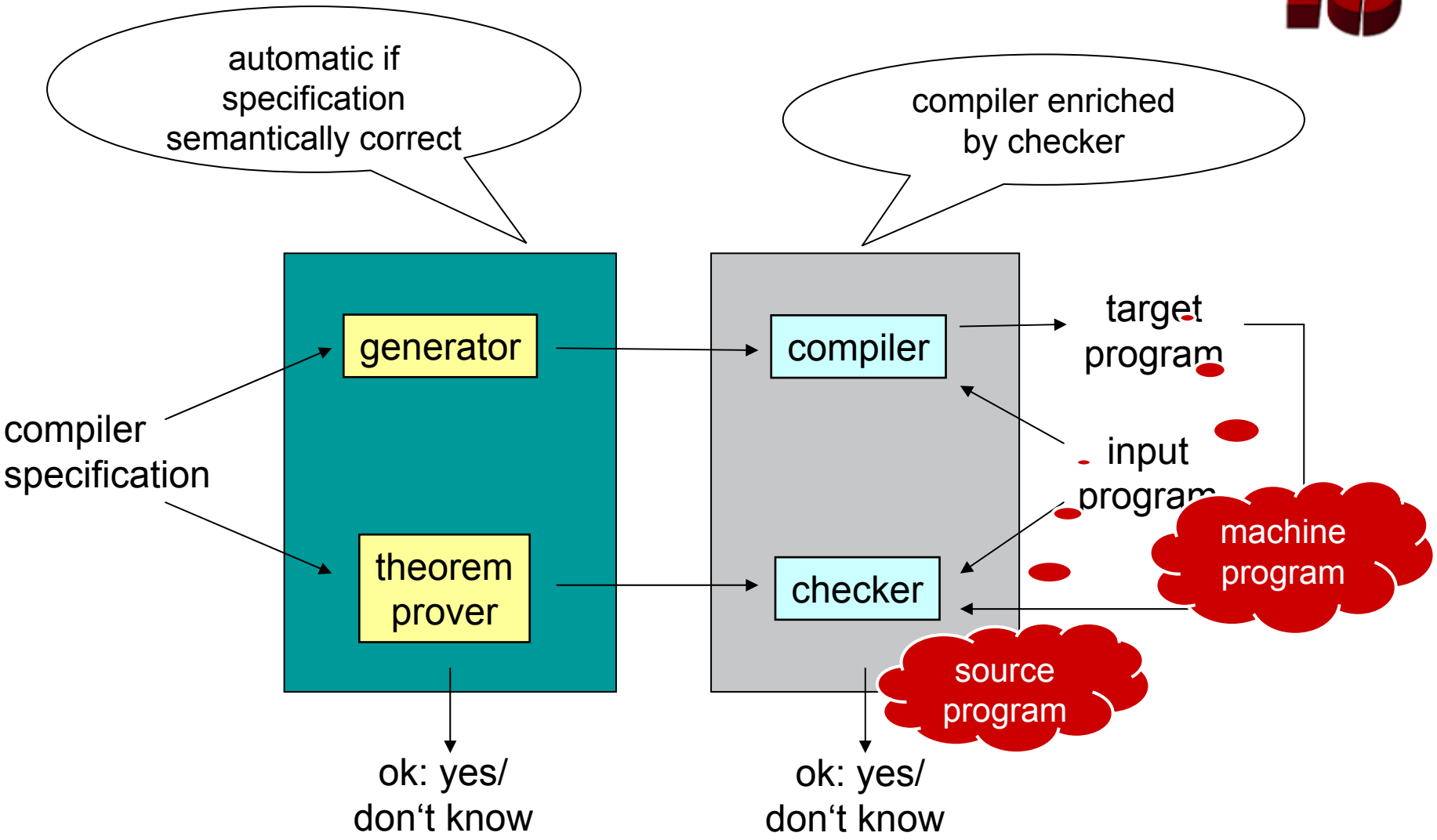
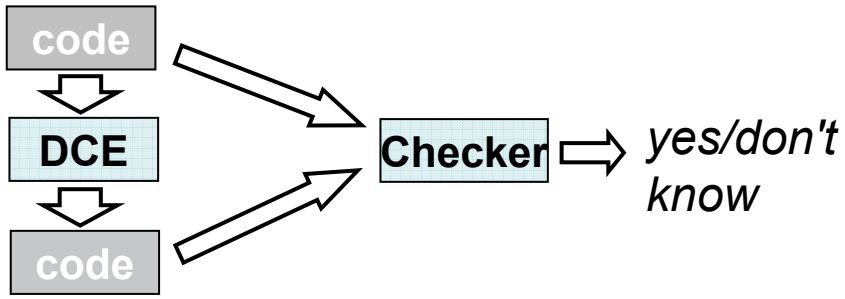
Verification Architecture



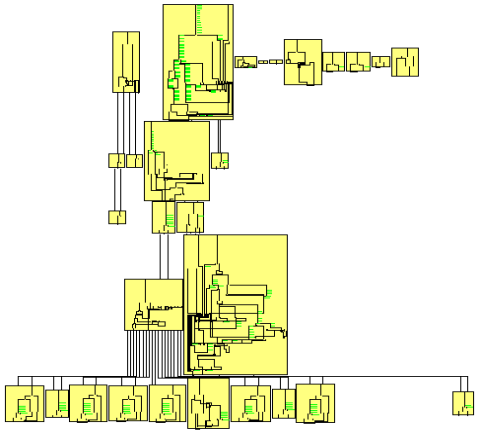
Scientific Highlights (compiler platform)
Verification of Dead Code Elimination

- Verification considers correctness of algorithm and correctness of implementation
- Correctness of algorithm verified within theorem prover Isabelle/HOL
  - Formal Semantics for Static Single Assignment (SSA) Form
  - Formalization of Dead Code Algorithm
- Correctness of Implementation
  - Checker approach
  - Implemented as CoSy Engine



Scientific Highlights (compiler platform)

- ROSE-PAG Integration
- Integrates ROSE and PAG for performing analysis and transformation of C/C++ apps
- Supports full C, object-oriented language features, and templates



- All language features of PAG specifications are supported and mapped to the ROSE C/C++ IR interface
- Also used for teaching optimizing compilers at TU-Vienna since October 2006
- Optimized C/C++ source code can be passed as input to ACE compiler for generating machine specific code

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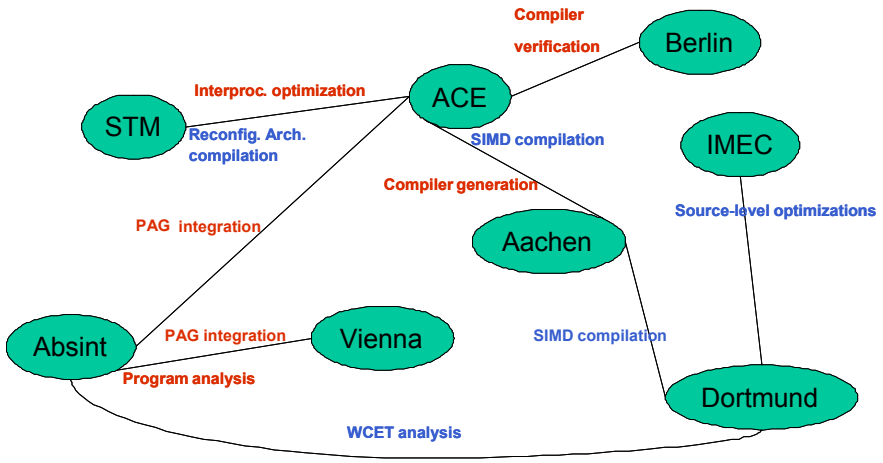
Thank you !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SIMD compilation
IMEC
Compiler generation
Source-level optimizations
PAG integration
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Vienna
SIMD compilation
Program analysis
Dortmund
WCET analysis