



Year 2 Review
Paris, November 8th and 9th, 2006

Scientific Highlights :

Communication Centric Systems

Activity leader : Rolf Ernst
Technical University of Braunschweig



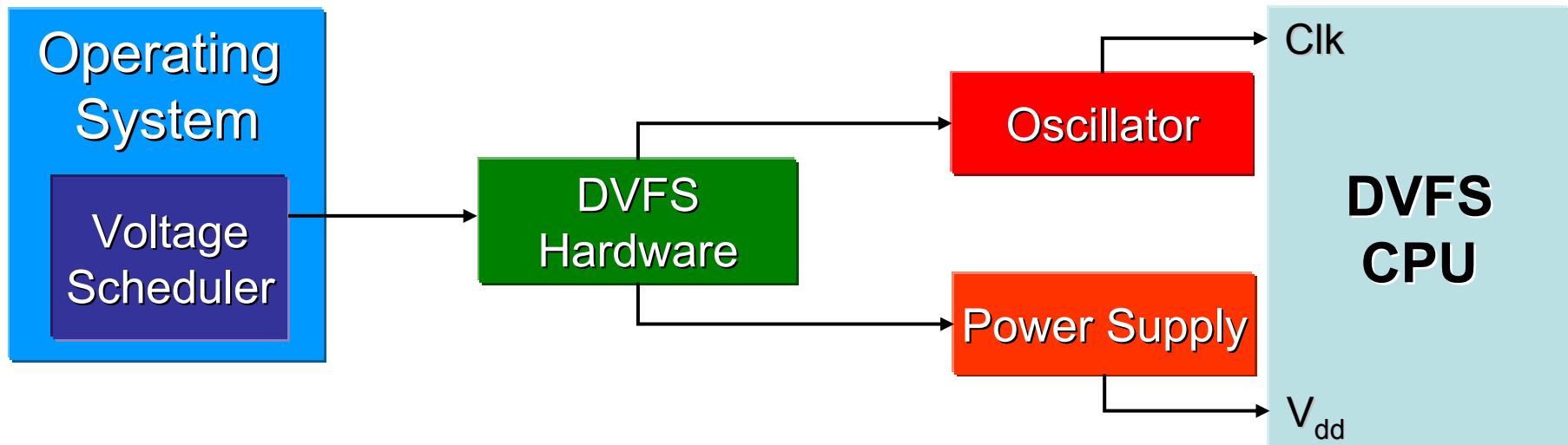
Outline

1. Power optimization under timing constraints
 - Collaboration ARTIST 2 - University of Notre Dame, USA
 - Tool coupling
 - Case study: Mobile gaming platform
2. Automotive platform design
 - Collaboration ARTIST 2 - Startup Syntavision GmbH
 - Application 1: Engine ECU analysis
 - Application 2: CAN bus with gateway

1. Power Optimization under Timing Constraints

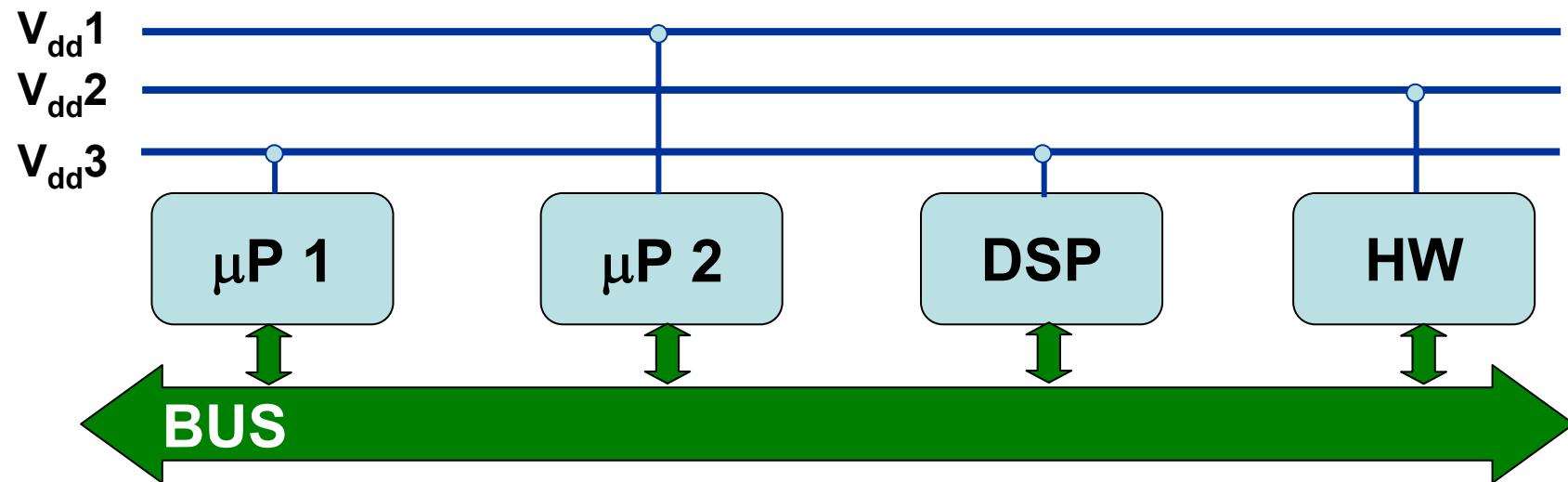
- Cooperation between University of Notre Dame and TU Braunschweig
- Two power optimization approaches
 - Given a set of tasks and their mapping to resources
 - Task level: determine the voltage/speed of each task that minimizes power (DVFS)
 - Resource level: determine the static voltage/speed of each resource that minimizes power (MV)
- Two optimization algorithms for each approach
 - Greedy Heuristic: uses sensitivity analysis of timing properties
 - Stochastic: uses evolutionary algorithms

Dynamic Voltage and Frequency Scaling (DVFS)



- Change the CPU supply voltage and speed **dynamically** during runtime
- Increase energy efficiency by matching the CPU performance to the current workload
- Need a “good” voltage scheduler
- Require additional energy and time for transitions

Multiple Supply Voltage (MV)



- Different supply voltages and operation modes
 - Each resource is assigned a **fixed** supply voltage and operation frequency at design time
 - Voltage selection according to performance requirement

Composition of timing and power analyses

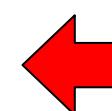
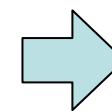
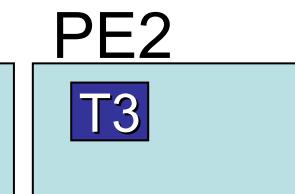
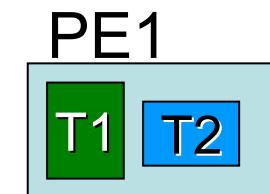
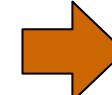
TU Braunschweig

SymTA/S

Univ. of Notre Dame

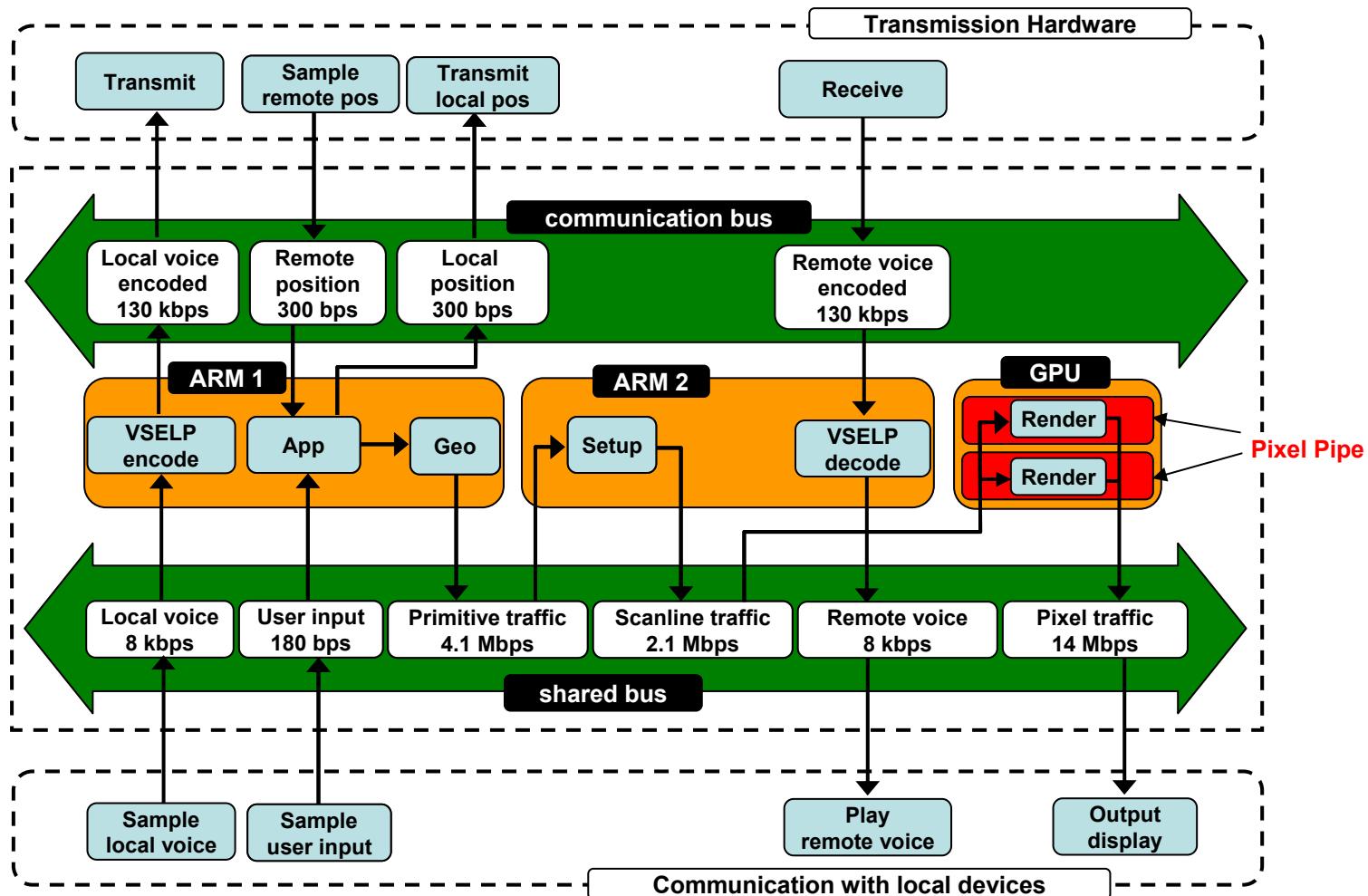
Power Analyzer

- **System setup**
 - Processor model selection
 - Task allocation + speed assignment
- **Send worst case load execution trace**
 - One trace per PE
 - One or more hyperperiods
- **Return avg. power est. for WC trace**
 - (Energy / Simulation time)



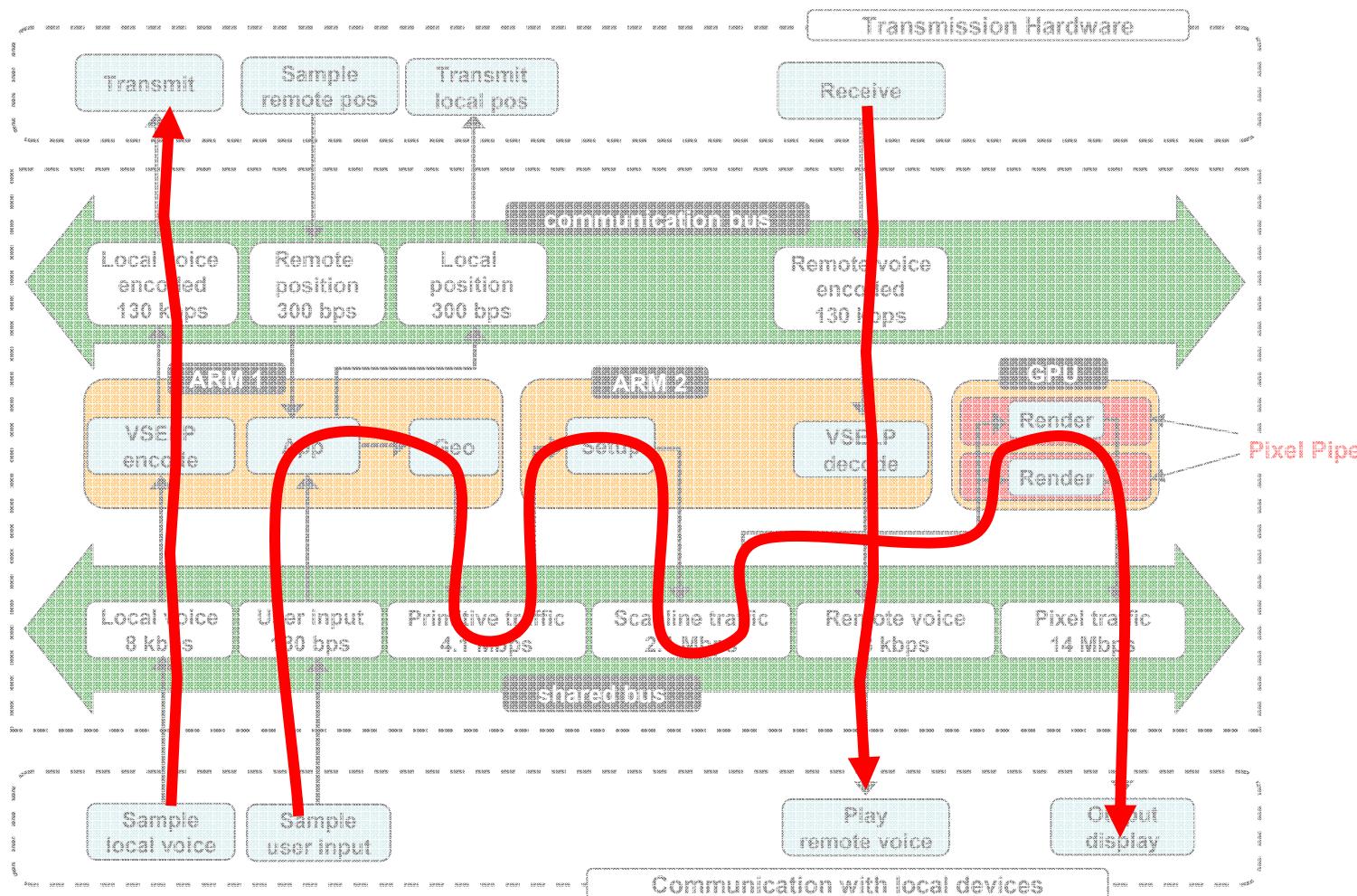
322.054 mW

Case study: Mobile Gaming SoC





Mobile Gaming SoC – Timing Constraints



Greedy Heuristic: Results

Task level (DVFS)

<i>Task</i>	sf_{init}	sf_{opt}	<i>Mapping</i>
VSELP_ENCODE	1.0	0.48	ARM1
SETUP	1.0	0.75	ARM2
RENDER2	1.0	0.61	PIXEL_PIPE2
3D_APP	1.0	0.65	ARM1
VSELP_DECODE	1.0	0.1	ARM2
RENDER1	1.0	0.61	PIXEL_PIPE1

<i>Resource</i>	E_{init}	E_{min}
ARM1	0.65	0.43
ARM2	0.5	0.26
PIXEL_PIPE1	1.0	0.23
PIXEL_PIPE2	1.0	0.23
COMM_BUS	0.08	0.08
SHARED_BUS	0.28	0.28
Total Power	3.51	1.51

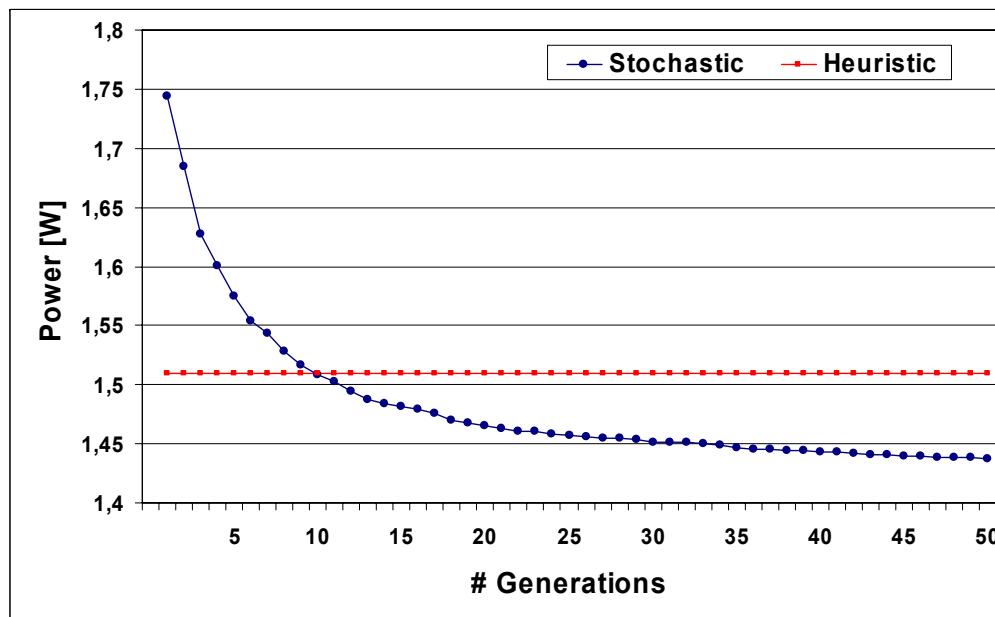
Resource level (MV)

<i>Resource</i>	sf_{init}	sf_{opt}	<i>Mapping</i>
ARM2	1.0	0.64	[SETUP, VSELP_DECODE]
PIXEL_PIPE1	1.0	0.61	[RENDER1]
PIXEL_PIPE2	1.0	0.61	[RENDER2]

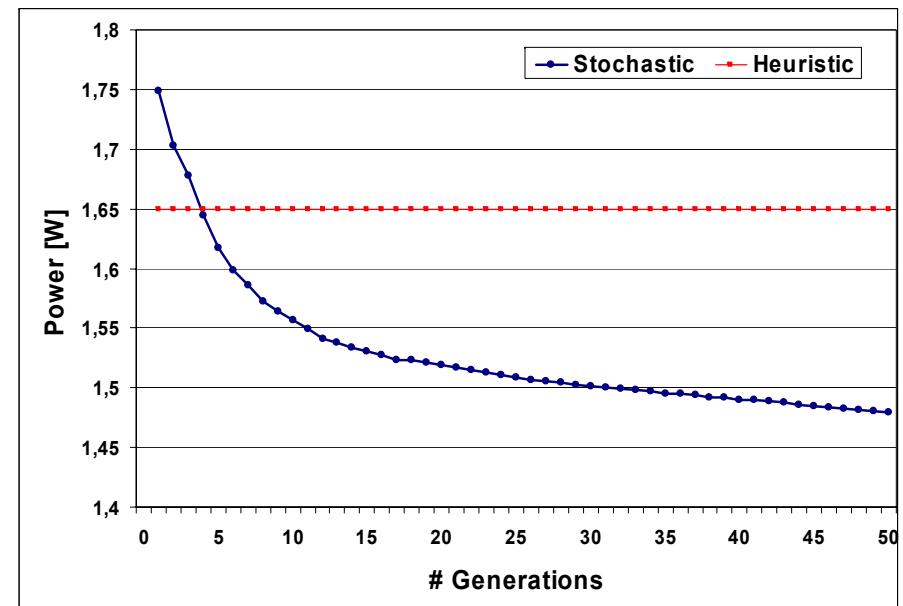
<i>Resource</i>	E_{init}	E_{min}
ARM1	0.65	0.65
ARM2	0.5	0.21
PIXEL_PIPE1	1.0	0.23
PIXEL_PIPE2	1.0	0.23
COMM_BUS	0.08	0.08
SHARED_BUS	0.28	0.25
Total Power	3.51	1.65

Heuristic vs. Stochastic Approach

Task level

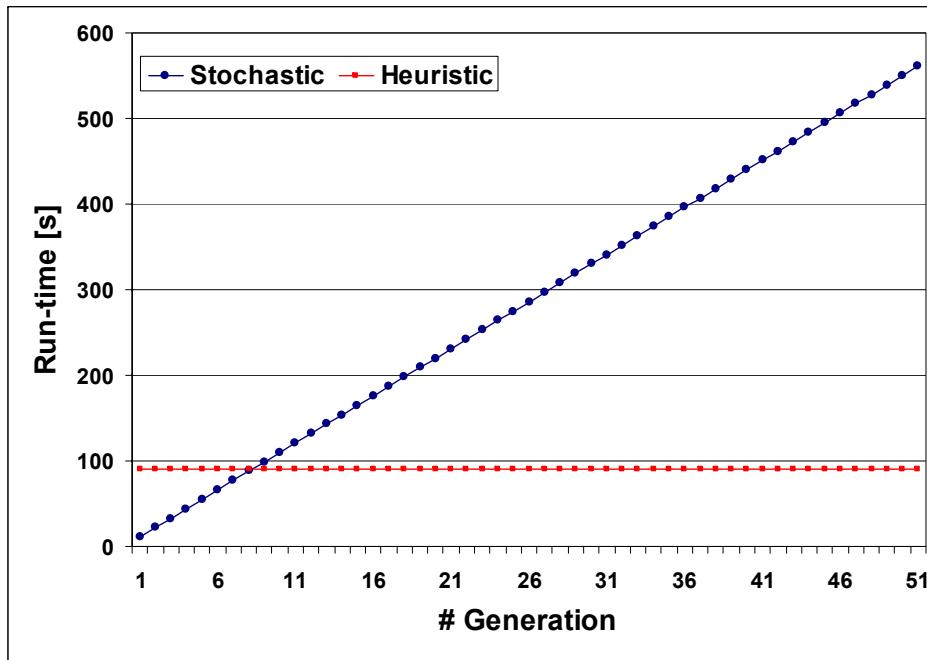


Resource level

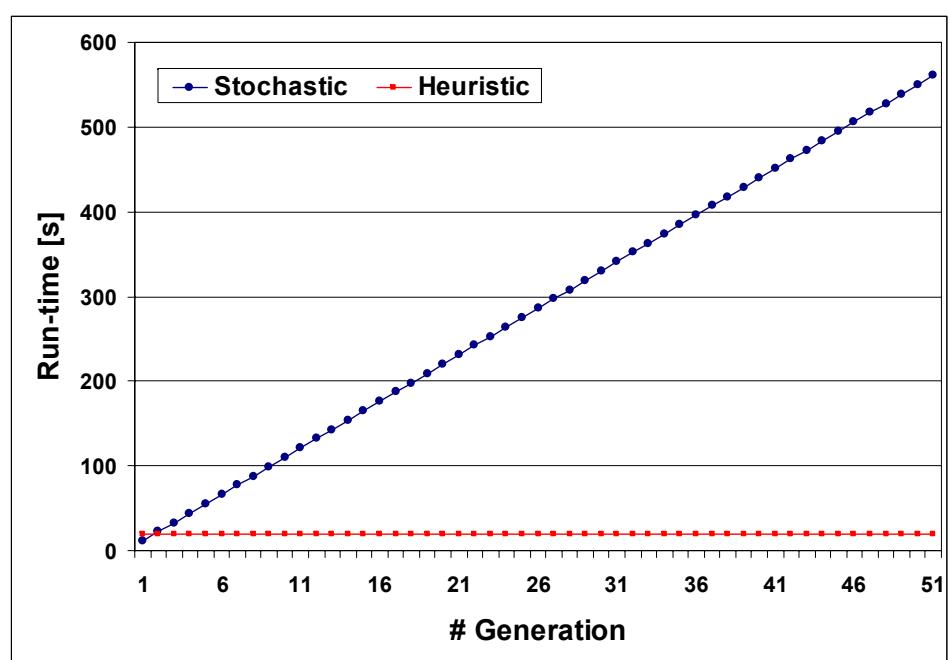


Run-time – Heuristic and Stochastic Approach

Task level



Resource level



Outline

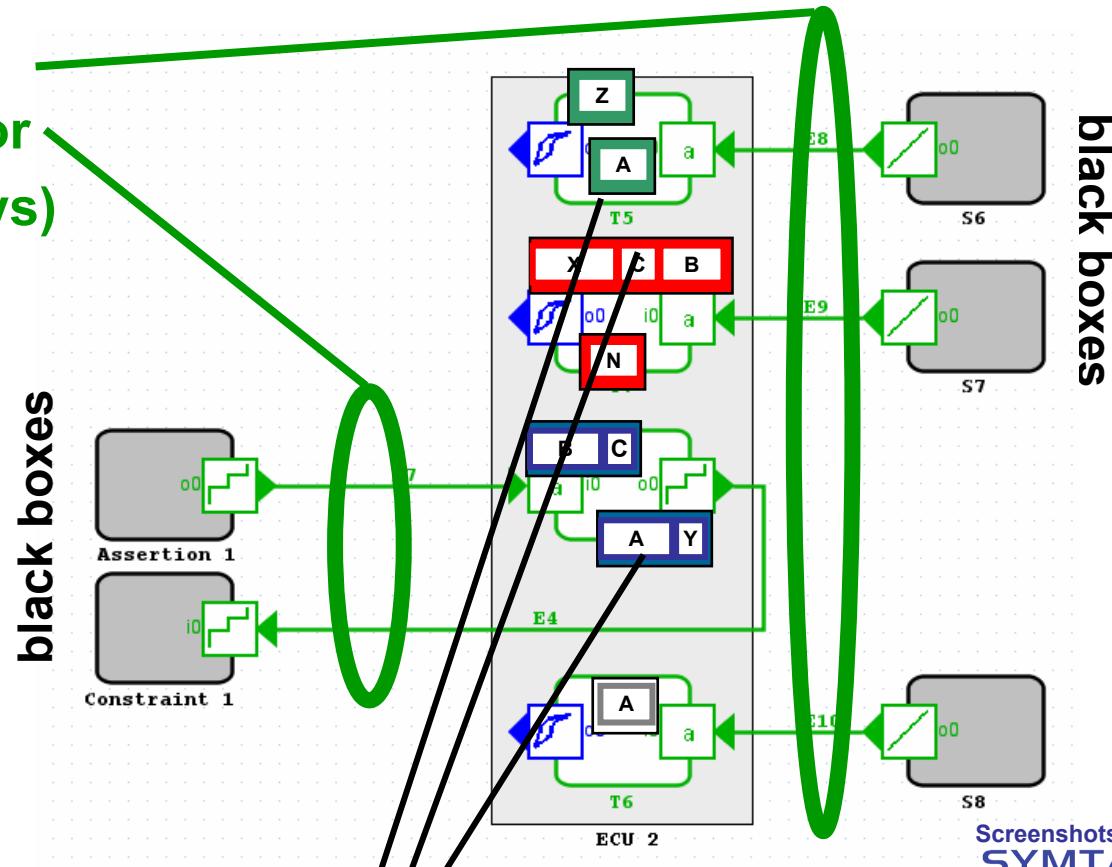
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2. Automotive Platform Design

- SymTA/S tool of TU Braunschweig was extended to cover automotive platform details
 - techniques to model activation phases such as generated by time table based activations
 - detailed automotive OS, bus, and gateway models
 - import/export of automotive design data (design process integration)
 - extension work mostly by Symtavision w partial support of public funding
 - discussions w ETH and Linköping U

Application 1 - Timing Analysis on ECU

**interface captures
dynamic I/O behavior
(jitter, min/max delays)**



**preemptive and
cooperative tasks**

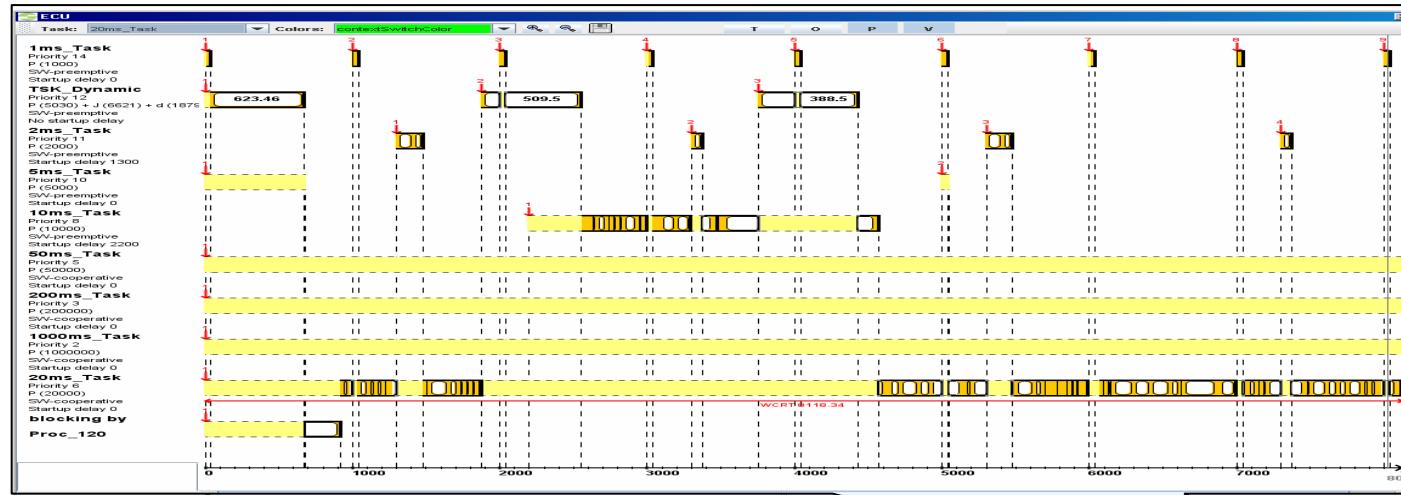
Screenshots by
SYMTA



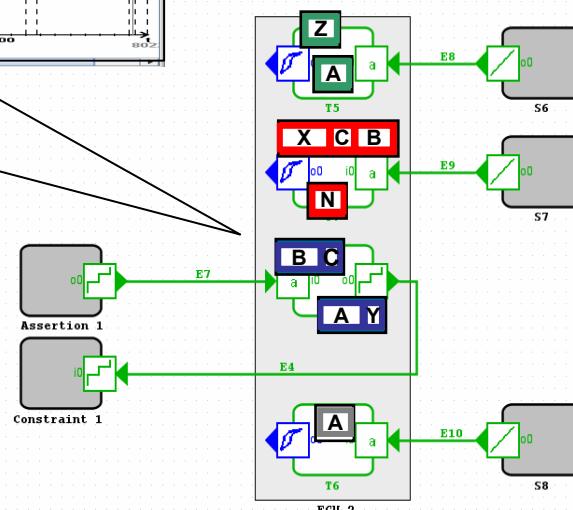
Information Society
Technologies



Analysis Challenges



- complicated preemption and cooperation scheme
- task chaining
- high accuracy



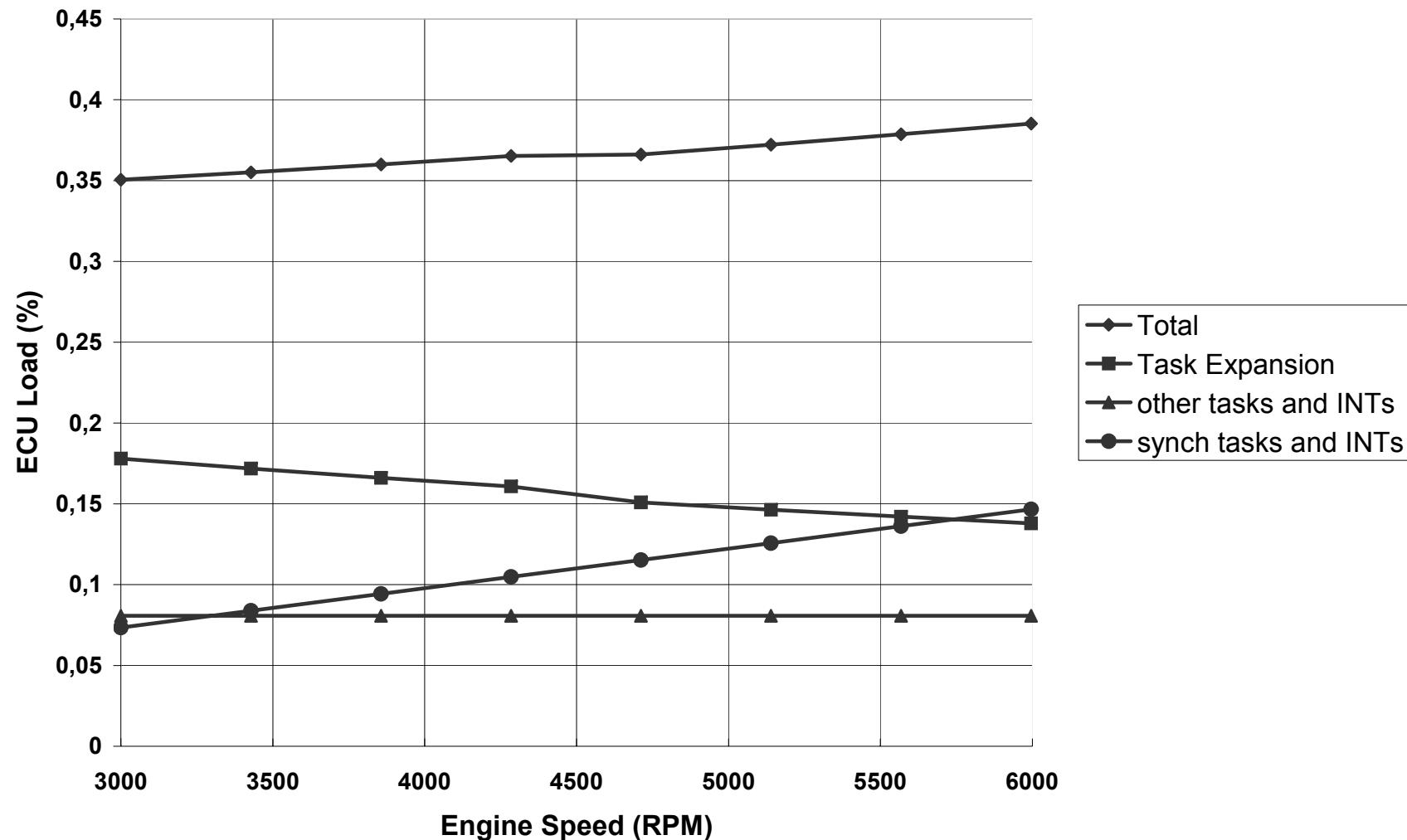
Design task

- Engine ECU with periodic and engine-synchronous tasks
- Specialties
 - load of engine-synch. tasks increases with engine speed
 - compensation by application level „task expansion“ mechanisms
- Accuracy issues
 - chained task activations w/ preemptive & cooperative tasks
 - alternating task executions (mutex)

Goals

- automatic analysis of multiple „points of interest“ (RPM curve)
- support test development by identifying corner cases
- consideration of platforms (4-, 6-, 8- cylinder engine)

Results I – Characteristic Load Curve

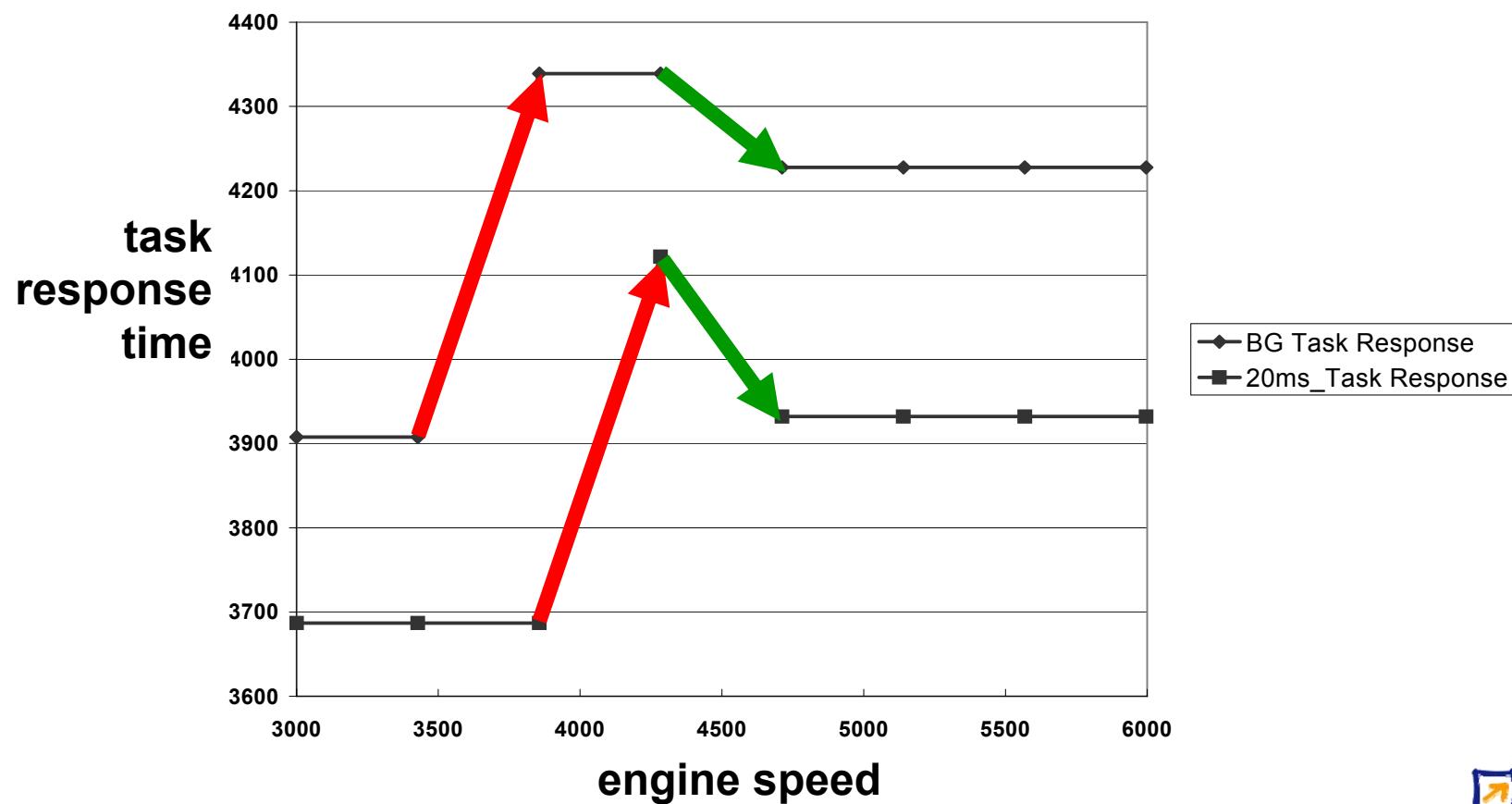




Results II – Detecting "Anomalies"

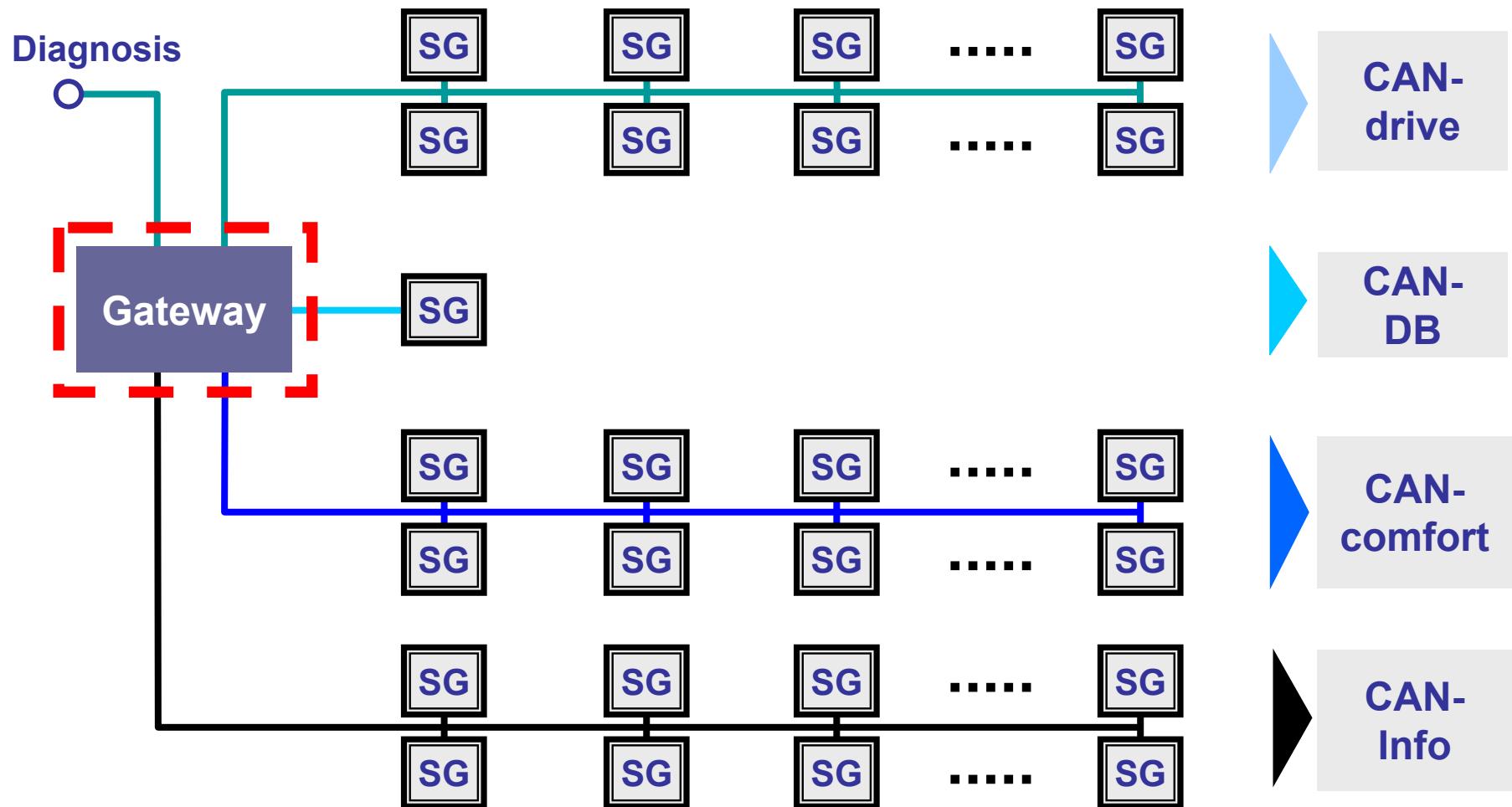
Additional preemption by
RPM-synchronous tasks
(increases task interference)

Task cut-off
(reduces core
execution time)



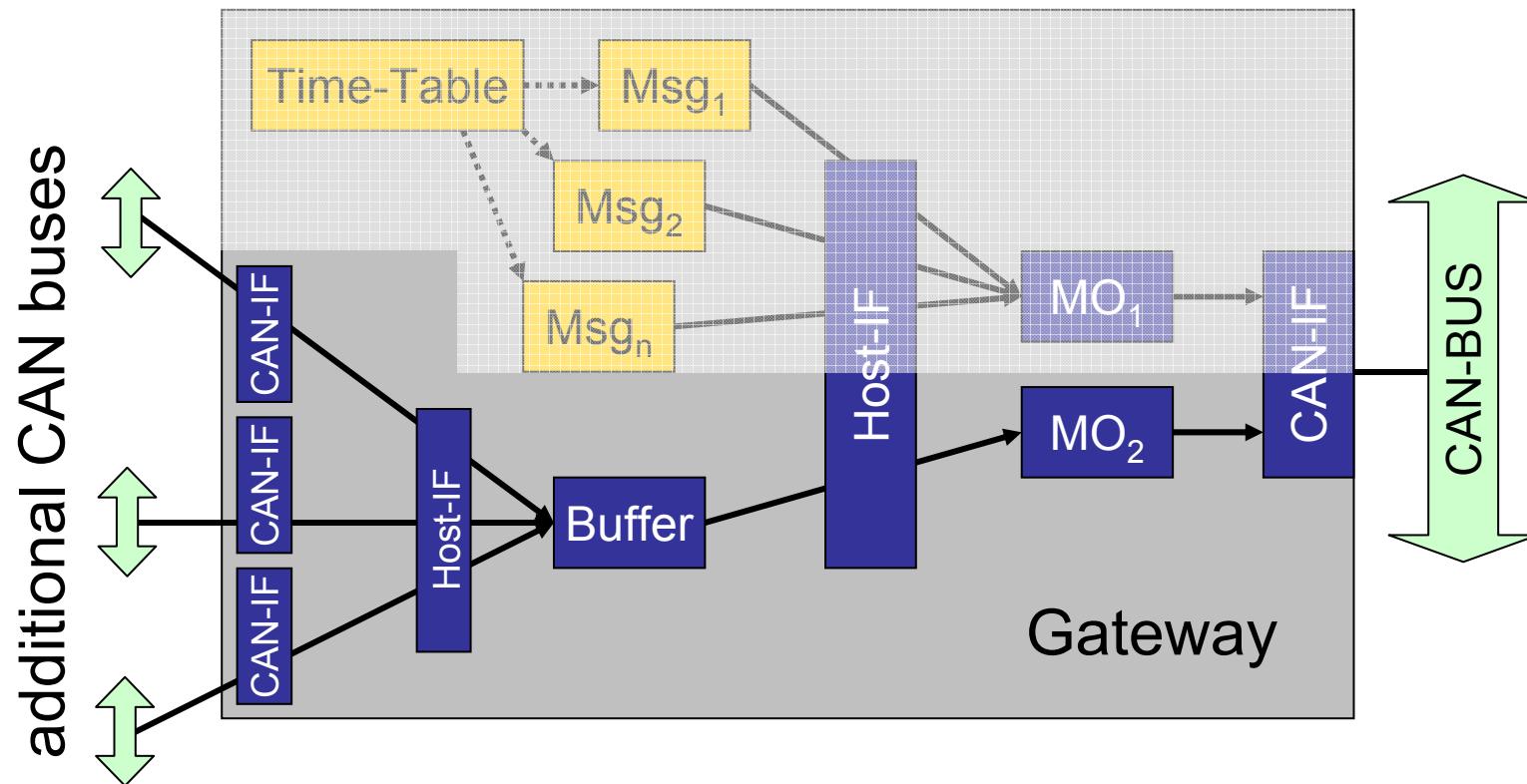


Application 2: CAN Bus with Gateway

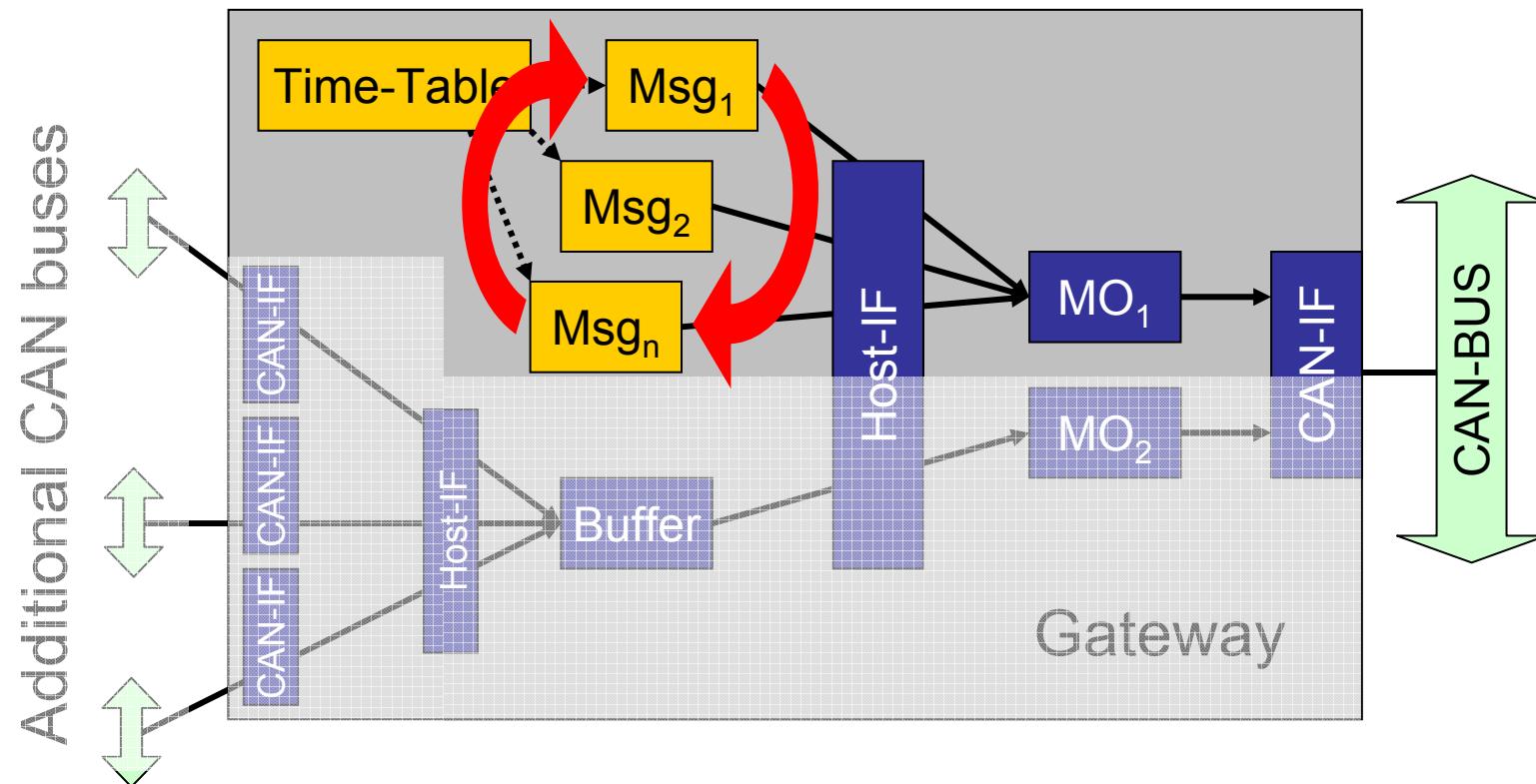




Gateway



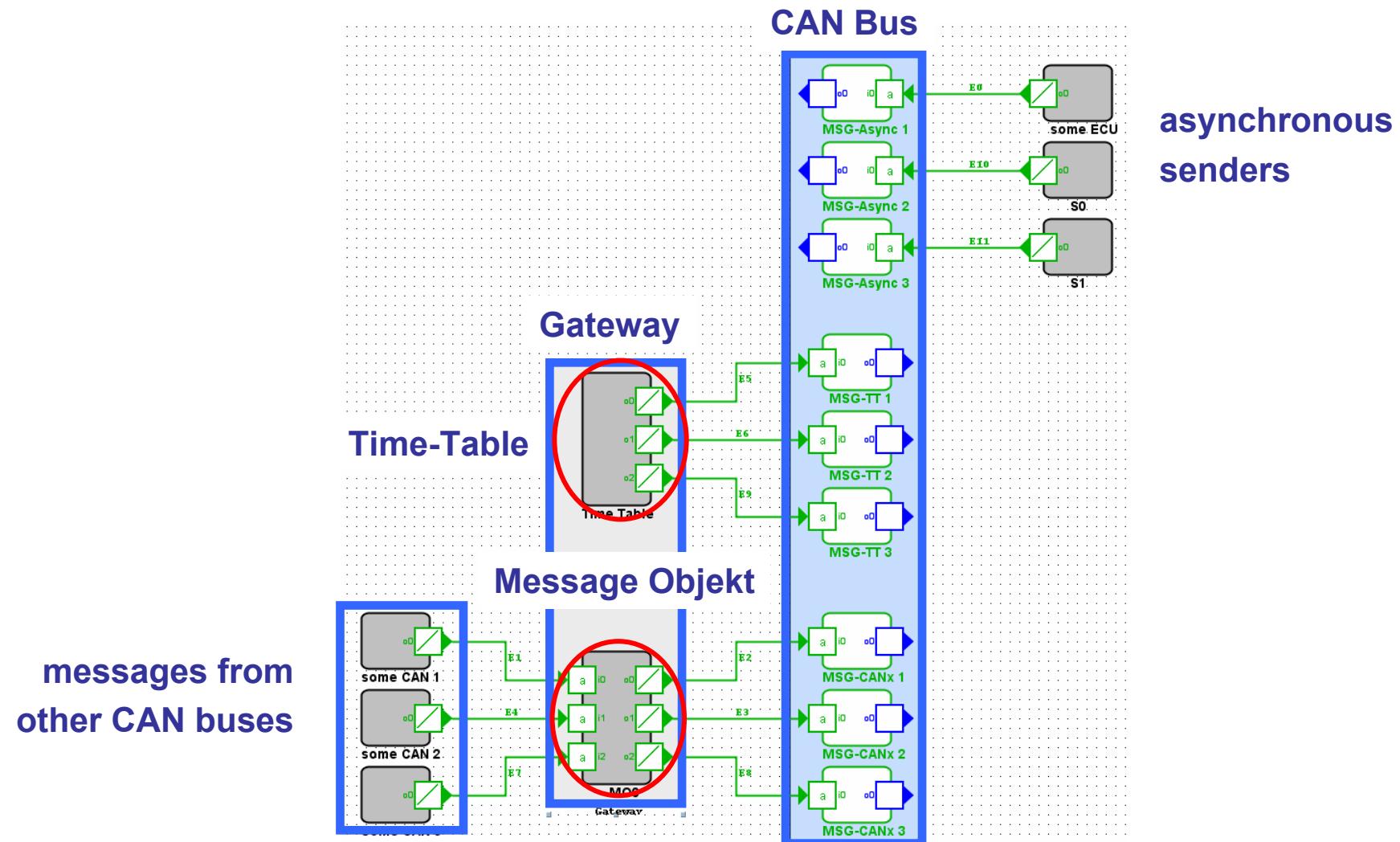
Time-Table Driven Messages



Analysis Challenges

- CAN-Bus
 - CAN protocol
 - Error models
- Gateway
 - Consideration of timing dependencies between time table generated messages (traffic shaping)
 - Shared, priority-ordered send buffer
 - Shared message objects (CAN Controller)

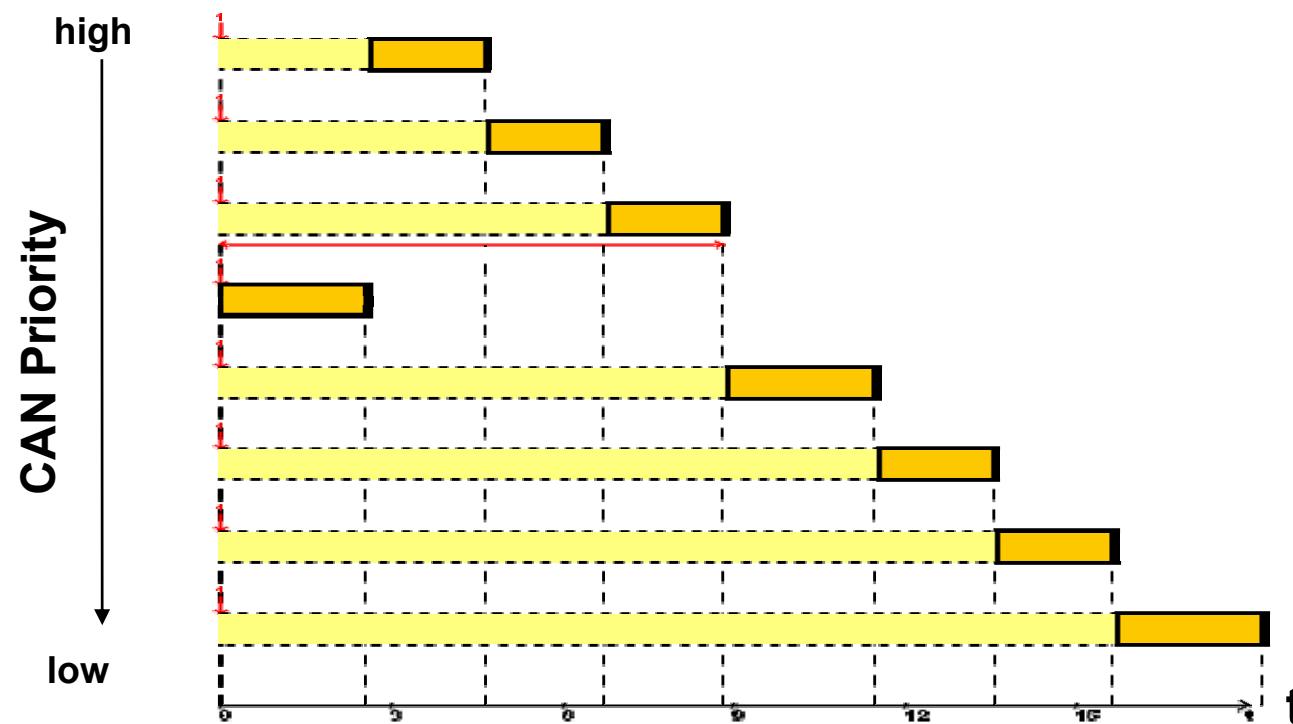
System Setup



Timing Influences I

Simplification: NO Time-Table and NO shared Message Object

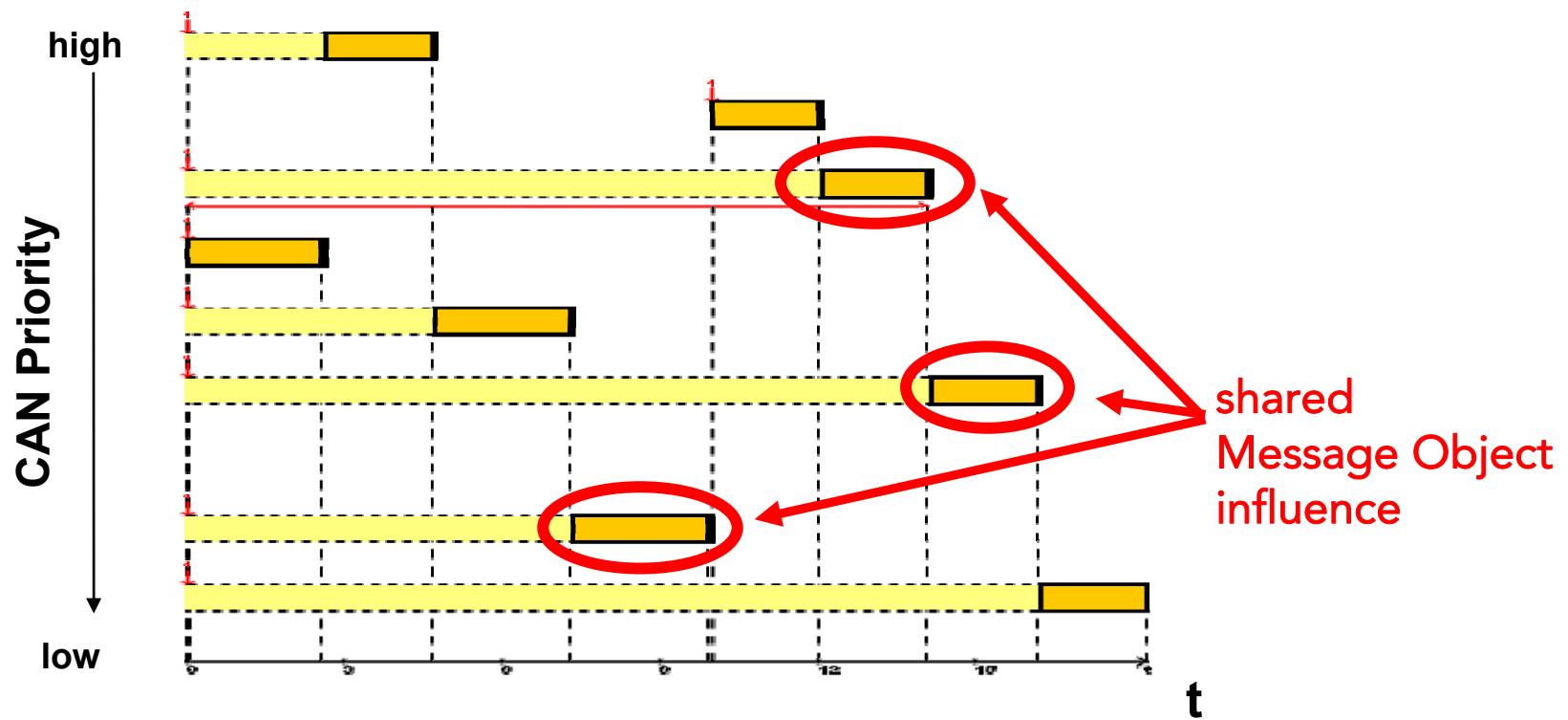
- Behavior according to message priorities with one blocking lower priority message in the worst-case
- Can be easily predicted



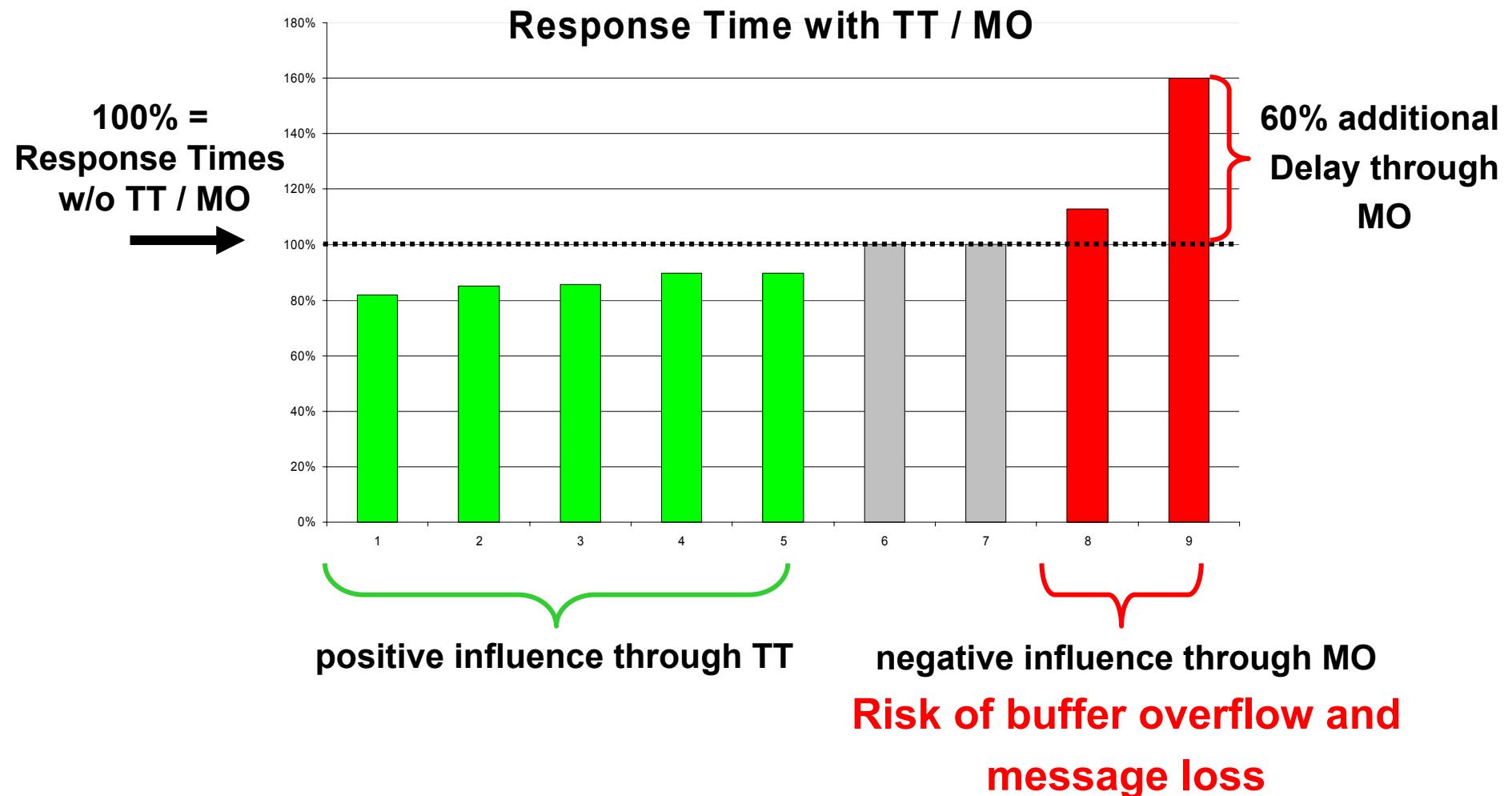
Timing Influences II

Detail: WITH Time-Table and WITH shared Message Object

- Complex, non-intuitive communication pattern
- Many blocking messages



Influence on Response Times



Conclusion

- collaboration of ARTIST 2 w international leading research institutions and industry leads to world leading practical solutions
- collaboration and meetings in ARTIST 2 instrumental for success
- tool status
 - evaluated and introduced by automotive manufacturers and suppliers world wide
 - already used for new car model design at one manufacturer – feedback with top quality ratings