Year 2 Review
Paris, November 8th and 9th, 2006

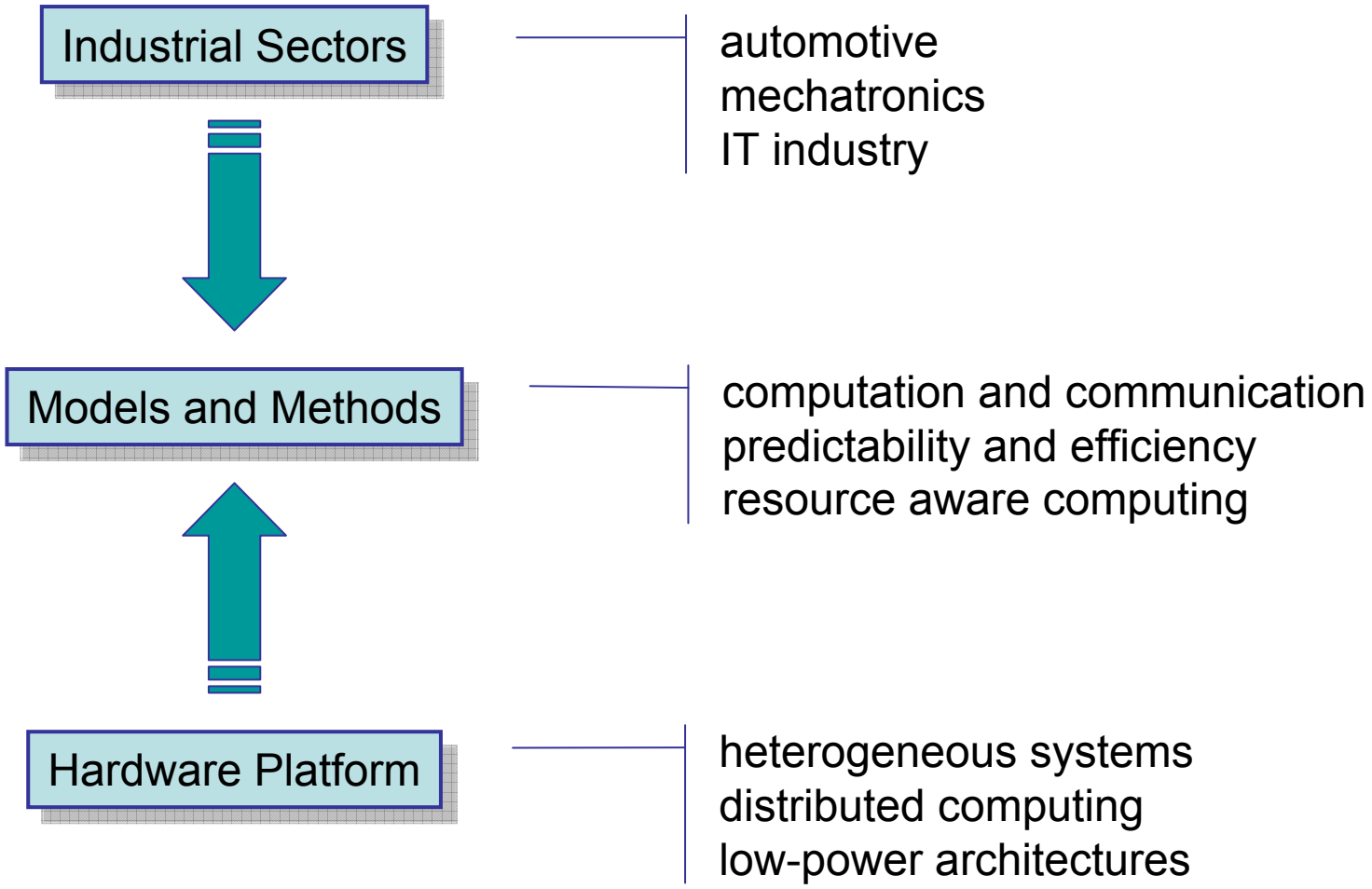
Achievements and Perspectives :

Execution Platforms

Cluster leader : Lothar Thiele

Swiss Federal Institute of Technology Zurich (ETHZ)

High-Level Objectives



High-Level Objectives

The cluster on execution platforms will consider

- the *hardware* architecture and *software* components in their *interaction*,
- investigate *models and methods* for accurate *estimation* of important properties (energy, timing),
- provide the designer with adequate support for *design space exploration* and *optimisation*.

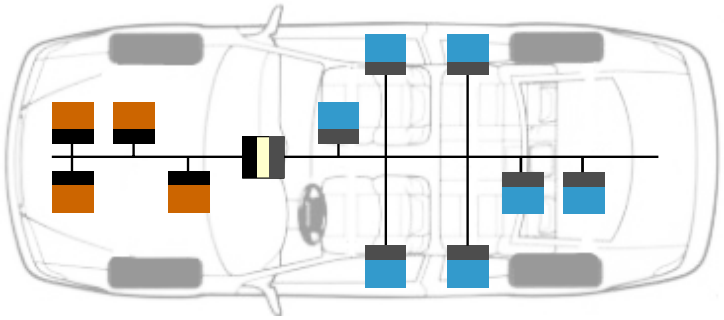
Challenges and Research Trends

- Resource Aware Computing
- Communication Centric Systems
- Predictability and Efficiency

Industrial Sectors and Needs

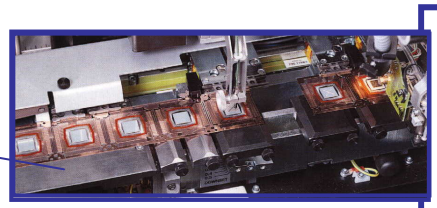
- Automotive (Volvo, Volkswagen)

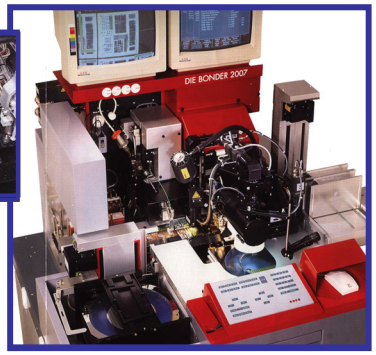
increasingly distributed
complex integration



- Mechatronics (Océ)

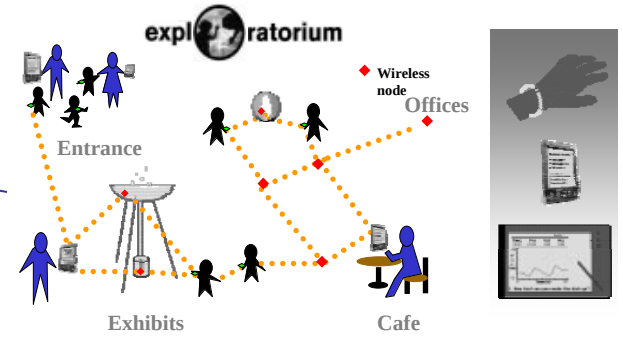
increasingly networked
predictability





- IT Industry (Siemens, STM)

resource awareness
short product cycles
distributed operation



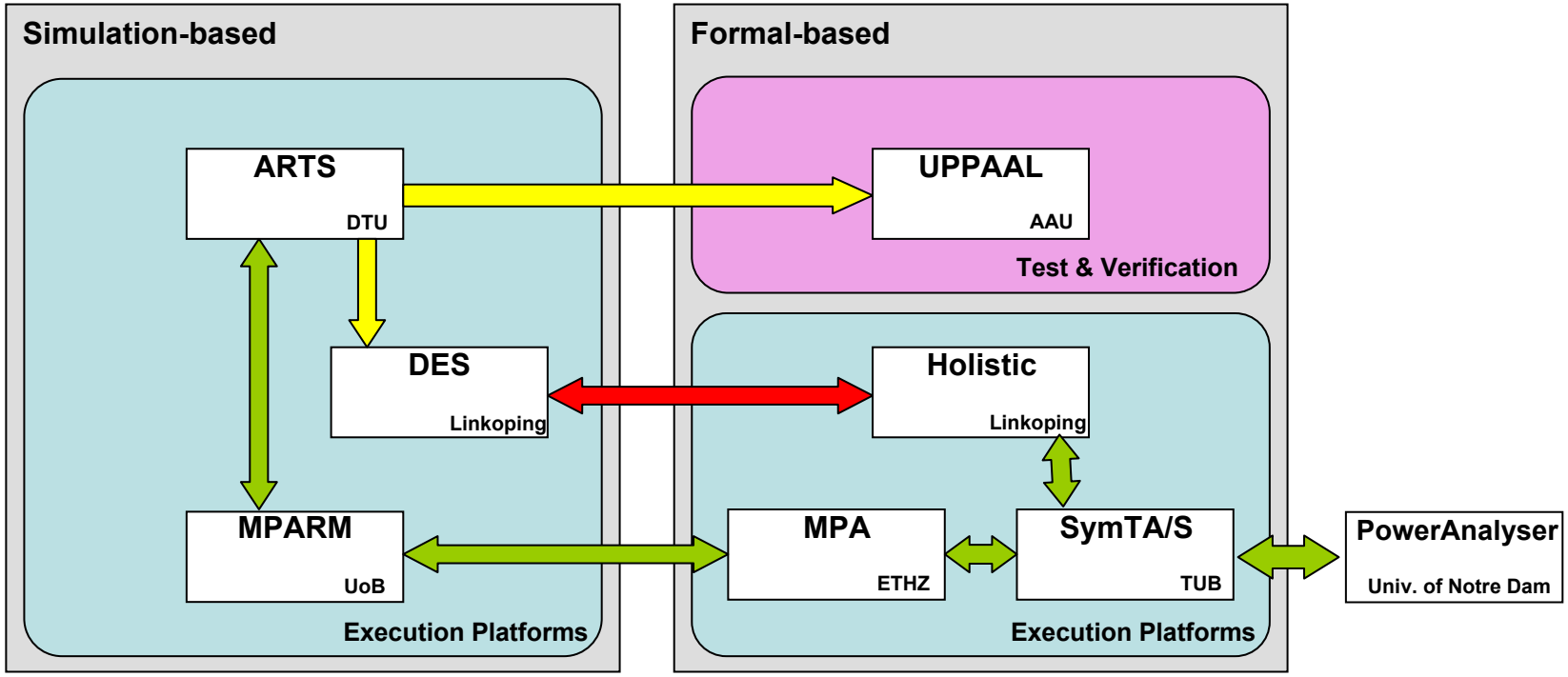
Collaboration with Industry

- **Communication-Centric Systems:**
  - **SymtaVision**: Integration of MPA into Symta/S, analysis of automotive gateway architectures, sensitivity analysis and robustness optimization
  - **Siemens**: Sensor Networks for Building Applications
  - **Atmel**: Hardware and Software for massively parallel embedded systems
  - **Volvo**: Safety Critical Distributed Systems for Automotive Applications
  - **Océ**: Used SymTA/S to model data path of printer/copier
  - **Volkswagen**: Modeling of automotive gateways
  - **Absint**: Coupling of WCET and system level analysis (supporting Symtavision) in the SuReal project
  - **Intel**: RT-analysis of multi-core multi-threaded network processor architectures for optical network applications
- **Resource-Aware Design:**
  - **STMicroelectronics**: Dynamic resource management energy-efficient MPSoC platforms
  - **Coware**: Virtual platform for resource constraint analysis for heterogeneous MPSoCs
  - **ETAS**: integration of model-based design tool with timing analyzer

Collaboration with Industry

- **Design for Low Power:**
  - **IO Technology**: sensor networks for sow monitoring
  - STMicroelectronics: Low power design of MPSoC platforms for multimedia
  - Freescale: OS-based dynamic power management for SoCs
  - Bulldast: Power consumption analysis for nanometer CMOS platforms
  - Siemens: Power optimization techniques for wireless sensor networks
- **New Start-ups:**
  - **Teklatech (2006):** one-step EDA solution to achieving timing closure in large scale, globally synchronous, deep submicron ASIC designs.
  - **SymtaVision (2006):** Timing Analysis of distributed real-time systems

Integration and Building Excellence



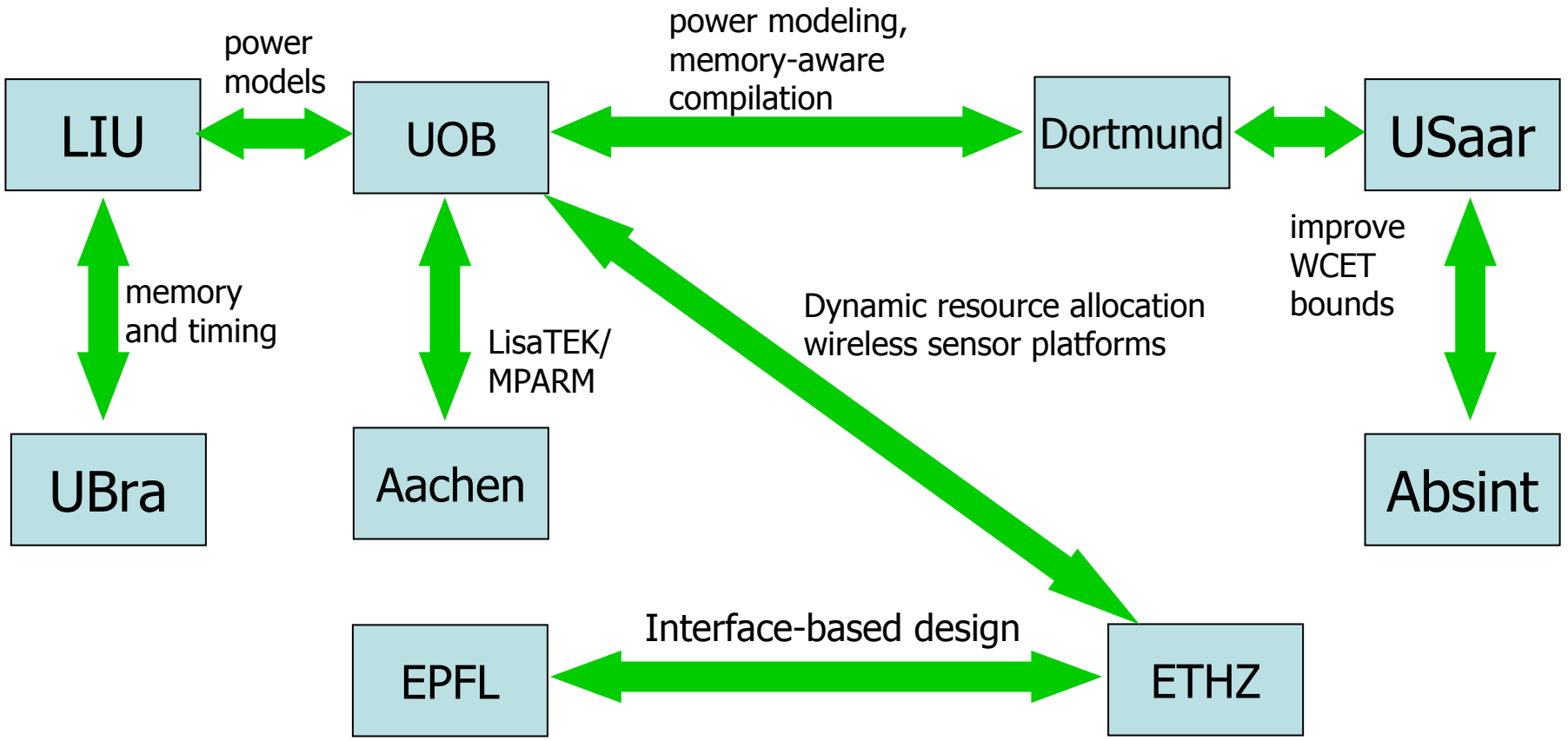
Implemented tool interconnect

Translation

Planned tool interconnect

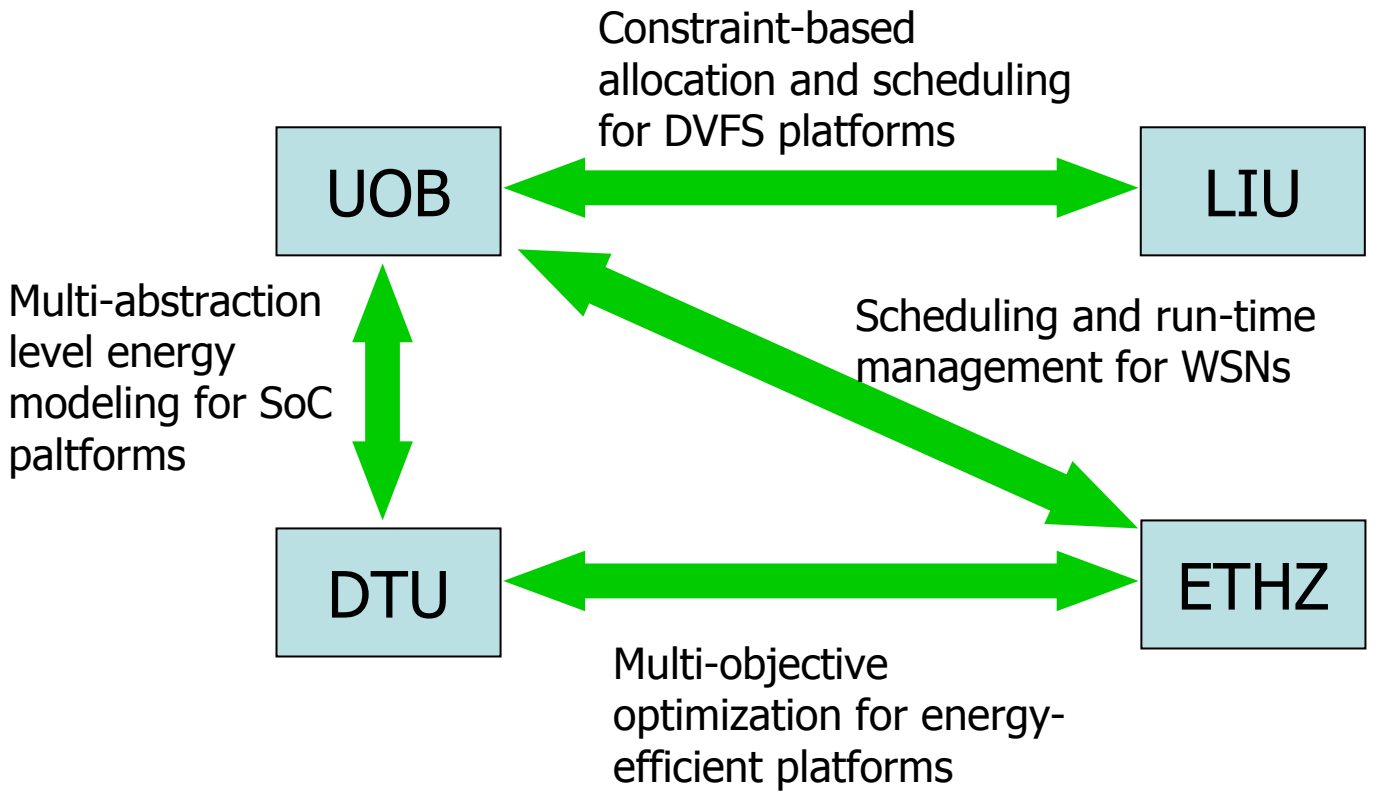
JPIA WP1: Platform System Modeling Infrastructure

Integration and Building Excellence



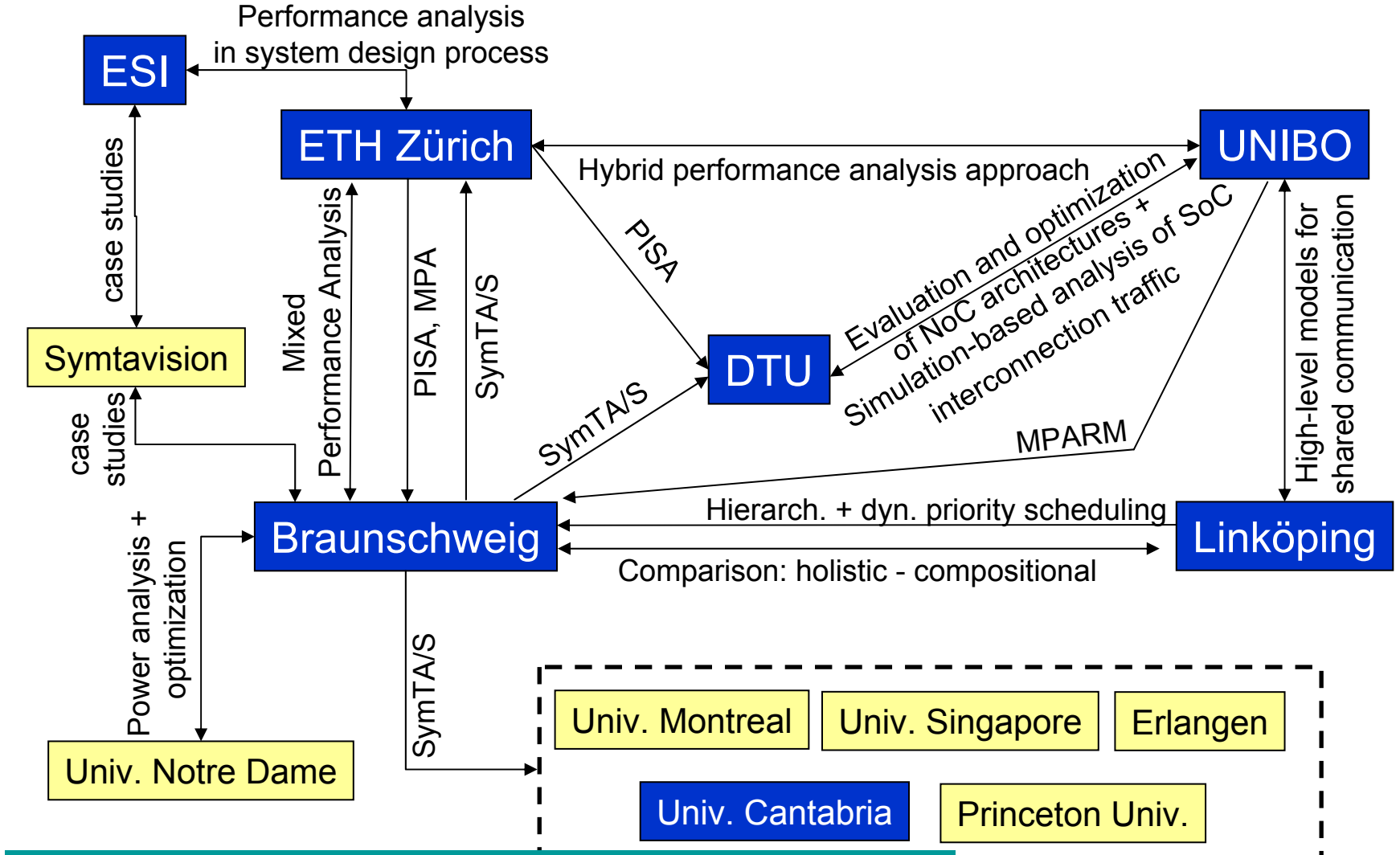
JPRA WP3: Resource-Aware Design

Integration and Building Excellence



JPRA WP8: Design for Low Power

Integration and Building Excellence



JPRA WP8: Communication-Centric Systems

Indicators of Success

- (Co-)Organization of Workshops and Tutorials
  - ARTIST2 Workshop on Distributed Embedded Systems, Leiden, Nov. 2005 (ETHZ)
  - ARTIST2 Workshop on Component Based Design, Seoul, Oct. 2006 (ETHZ, VERIMAG)
  - Tutorial on Frameworks for System-Level Analysis of Real-Time Systems, RTAS 2006, San Jose (ETHZ, SymtaVision)
  - ARTIST2 Workshop on Execution Platforms, March 2006, Bologna (UBologna)
  - ARTIST Workshop at DATE'06: W4 Design Issues in Distributed, Communication-Centric Systems, March 2006 (UBraunschweig).

Indicators of Success

- **Integration of Models, Methods and Tools**
  - Symta/S - Modular Performance Analysis (UBraunschweig – ETHZ)
  - MPARM – Real-Time Calculus (UBologna – ETHZ)
  - Symta/S – EDF scheduling analysis (UBraunschweig – Linköping)
  - MPARM – ARTS Cosimulation (UBologna – DTU)
  - ARTS – Resource Sharing Protocols (DTU – Linköping)
  - Comparison and cross-benchmarking of multiprocessor allocation and scheduling techniques (UNIBO – LIU)
  - Coupling of Performance Analysis and Design Space Exploration with Power Models and Analysis Techniques of (UBraunschweig - UNotre Dame)

NEW Joint Publications (2005-2006)

1. Jan Staschulat, Rolf Ernst, Andreas Schulze, Fabian Wolf. Context Sensitive Performance Analysis of Automotive Applications. In Designer's Forum at Design, Automation and Test in Europe (DATE), 2005.
2. Bren C. Mochocki, Xiaobo S. Hu, Razvan Racu, Rolf Ernst. Dynamic Voltage Scaling for the Schedulability of Jitter-Constrained Real-Time Embedded Systems, ICCAD 2005.
3. E. Wandeler, L. Thiele, M. H. G. Verhoef, P. Lieverse. System Architecture Evaluation Using Modular Performance Analysis - A Case Study. Journal Software Tools for Technology Transfer (STTT), 2006.
4. Simon Künzli, Francesco Poletti, Luca Benini, Lothar Thiele: Combining Simulation and Formal Methods for System-Level Performance Analysis, IEEE Design Automation & Test in Europe (DATE), Munich, Germany, March 2006.
5. C. Moser, D. Brunelli, L. Thiele, and L. Benini, “Real-time scheduling with regenerative energy.”, 18th Euromicro Conference on Real-Time Systems (ECRTS 2006), Dresden, Germany, July 5-7, 2006.
6. C. Moser, D. Brunelli, L. Thiele, and L. Benini, “Lazy scheduling for energy harvesting sensor nodes.”, The Fifth IFIP Working Conference on Distributed and Parallel Embedded Systems (DIPES 2006), Braga, Portugal, October 13-15, 2006.

NEW Joint Publications (2005-2006)

7. Bren Mochocki, Xiaobo Sharon Hu, Razvan Racu, Rolf Ernst. Dynamic Voltage Scaling for the Schedulability of Jitter-Constrained Real-Time Embedded Systems. In *International Conference on Computer Aided Design (ICCAD)*, San Jose, USA, November 2005.
8. Razvan Racu, Arne Hamann, Rolf Ernst, Bren Mochocki, Sharon Hu, Methods for Power Optimization in Distributed Embedded Systems with Real-Time Requirements, In Proc. International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES), Seoul, Korea, October 2006
9. Kai Richter, Marek Jersak, Rolf Ernst. How OEMs and suppliers can tackle the network dimensioning problem. *Embedded Real Time Software Congress (ERTS06)*, Toulouse, France, January 25-27, 2006.
10. Kai Richter, Rolf Ernst. Real-Time Analysis as a Quality Feature: Automotive Use-Cases and Applications, *Embedded World 2006 Fair and Conference*. Nuremberg, Germany - February 14-16, 2006.

NEW Joint Publications (2005-2006)

11. Kai Richter, Marek Jersak, Rolf Ernst. How OEMs and suppliers can face the network dimensioning challenges. *Design, Automation and Test in Europe (DATE) Conference,* Special Track Automotive Designer's Forum, Munich, Germany, March, 2006.
12. Kai Richter, Rolf Ernst. Applying Real-Time Network Research in the Automotive Industry: Lessons Learned and Perspectives, *Euromicro Conference on Real-Time Systems (ECRTS), s*atellite workshop on Real Time Networks (RTN), Dresden, Germany, July 2006.
13. Kai Richter, Marek Jersak, Arne Hamann, Rolf Ernst. Scheduling Analysis in the Automotive Design Flow. *ARTIST2 Workshop at the International Conference on Embedded Sofware (EMSOFT),* Seoul, Korea, October, 2006.
14. L. A. Cortes, P. Eles, Z. Peng, "Quasi-Static Scheduling for Multiprocessor Real-Time Systems with Hard and Soft Tasks", 11th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA'05), Hong Kong, 2005.

NEW Joint Publications (2005-2006)

15. L. A. Cortes, P. Eles, Z. Peng, "A Quasi-Static Approach to Minimizing Energy Consumption in Real-Time Systems under Reward Constraints", 12th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA'06), Sydney, Australia, 2006.
16. L. A. Cortes, P. Eles, Z. Peng, "Quasi-Static Assignment of Voltages and Optional Cycles in Imprecise-Computation Systems with Energy Considerations", IEEE Transactions on VLSI Systems (accepted for publication)
17. M. Ruggiero, G. Pari, A. Guerri, M.Milano, D. Bertozzi, L.Benini, A Andrei, "A Cooperative, accurate solving framework for optimal allocation, scheduling and frequency selection on energy-efficient MPSoCs", International Symposium on System-on-Chip, Tampere, Finland, 2006.

Assessment at Y0+2

- **Substantial progress in integration.** Indicators that show this clearly are
  - the joint organization of and participation in summer schools, workshops and tutorials
  - the number and quality of joint publications, and
  - the integration of tools.
- **Research is still fragmented: Real-time scheduling and real-time analysis in** 'Execution Platforms', 'Hard Real-Time Systems' and 'Software Components':
  - Workshop on Component Based Design in Seoul (Oct. 2006)
  - Workshop on Models of Computation in Zurich (Nov. 2006)

Organizational Change

Petru Eles (Linkoeping) will lead the activity

"Design for Low Power"

instead of Luca Benini (UBologna)

Future Work: System Modeling Infrastructure

- **Description:**
  - **Linköping – DTU**: Extend ARTS Simulation Environment towards average case and worst case analysis of distributed systems, evaluation of pessimism, dependable systems.
  - **UBraunschweig – DTU**: Combine Symta/S and ARTS in terms of *sensitivity analysis*.
  - **UBologna – DTU**: Combine MPARM (Bologna) and ARTS (DTU) by providing model adaptors; extend ARTS towards modeling dynamically reconfigurable FPGAs.
  - **DTU-CISS**: Combine ARTS (Simulation) with UPPAAL (*Formal Verification* of Timing Properties)

Future Work: System Modeling Infrastructure

- Milestones:
  - Year2: Initial definition of the modeling platform (achieved). Several simulation- and formal-based models have been investigated and extended towards integration. Early integration of the simulation-based models, ARTS and MPARM, and of the formal-based models SymTA/S and Real-Time Calculus has been achieved. Initial linking between simulation- and formal-based models, MPARM and Real-Time Calculus has been investigated.
  - Year3: Version 1 of the system modeling platform implementation. Due to the experience gained with the different modeling formalisms, it was found that rather than aiming for a single unified model, the focus should be on further exploration of the existing models and in particular their interaction. Therefore, the focus will be on linking and integrating different modeling formalisms and to extend the models to support analysis and exploration as needed by the other cluster activities.
  - Year4: Integration of modeling formalisms covering different levels of abstraction. Effective strategies for selecting model formalisms. Refinement and dissemination of models.

Future Work: Communication-Centric Systems

- **Description:**
  - **ETHZ – TUBraunschweig**: Link the Symta/S tool and the MPA (Modular Performance Analysis).
  - **Linköping-TUBraunschweig-ETHZ**: Extend analysis frameworks towards *fault-tolerance, robustness and sensitivity* issues. Integrate into existing analysis tools.
  - **Linköping-TUBraunschweig-ETHZ**: Work towards a common understanding of hierarchical scheduling, e.g. Flexray protocols.
  - **UBologna-DTU-UBraunschweig**: Work towards MPSoC architectures in terms of (a) memory access, (b) NoC exploration and (c) inclusion of several software layers.

Future Work: Communication-Centric Systems

- **Milestones:**
  - **Year2**: New best-case/worst-case models for hard real-time systems and at combined statistical and interval models for QoS applications in multi-media. These models may combine communication and computation, different models of computation, event models and scheduling policies (**achieved**).

    The following main results were achieved: The industry increasingly applies hierarchical communication protocols, such as the automotive FlexRay Standard. New timing analysis techniques were developed to follow that trend. Since system dependability and flexibility are growing demands in embedded systems, techniques for fault tolerance and robustness measurement were developed and included in communication modelling and optimization. Additionally, case studies were performed to demonstrate the feasibility and practicability of the research results. Power optimization techniques were developed, since low power design is a new and urgent requirement in mobile and streaming applications.
  - **Year3**: Analytic methods to estimate system properties.
  - **Year4**: Refinement and dissemination of these methods.

Future Work: Low Power Design

- **Description:**
  - **Linköping-DTU-UBologna**: *Power optimization for multi-core systems* (interaction between resource allocation and scheduling and power optimization, non-deterministic behavior due to conditionals and due to data-dependent execution times, task graphs are dynamically created).
  - **ETHZ – UBologna**: *Power management for wireless sensor networks* (optimizing not only power consumption, but also usage of harvested energy in sensor networks; impact on scheduling decisions and on various quality of service metrics).

Future Work: Low Power Design

- **Milestones:**
  - **Year2**: Component models will be investigated that model power dissipation of system components (achieved)) this objective has been achieved: several extensions to the MPARM platform power modelling capabilities have been developed (miulti-cluser systems, multi-frequency domains, multiple-voltage domains)
  - **Year3**: Effective strategies for power management and power aware allocation and scheduling for both single-chip and distributed systems
  - **Year4**: Integration of the different levels of abstraction - from scheduling via operating systems to system design - participating in low power design

Future Work: Resource-Aware Design

- **Description:**
  - **Dortmund-Saarbrücken-Linköping-Braunschweig**: *Predictability issues on multiprocessors on-chip* (WCET estimation and analysis vs. simulation results; influence of frequency and voltage scaling.)
  - **Dortmund-UBologna**: *Efficient utilization of memory hierarchies* (efficient utilization of memory hierarchies by multi-process applications, consider cooperative multi-tasking, combine with MPARM simulation environment of UBologna.)

Future Work: Resource-Aware Design

- **Milestones:**
  - **Year2**: A set of tools that can interact and work together and demonstrate the achievable optimizations on a particular hardware platform (achieved). Integration between AACHEN Lisa tools and Unibo's MPARM has been achieved. An early version of the memory aware compiler by Dortmund has been targeted to the MPARM platforms.
  - **Year3**: Strengthening the integration between Dortmund and Bologna: development of a memory-aware compiler for parallel multi-task applications. Linkoeping will also work to an integrated execution analysis environment for muilti-core systems.
  - **Year4**: A methodology for the design of predictable embedded systems

Forthcoming Events

- Models of Computation and Communication Workshop Zurich (MoCC), Nov. 16-17 (~40 participants).
- Architecture of Computing Systems Workshop Zurich (ARCS), March 2007 (~100 participants).
- Dagstuhl Workshop on 'Performance Analysis', March 2007.
- Co-organization Workshop on 'Predictability', 2007.
- Workshop Execution Platforms, Linköping, 2007.