Information Society Technologies

ARTIST2 – Cluster Meeting

Bologna, May 22nd, 2006

Activity *Execution Platforms*

System Modelling Infrastructure

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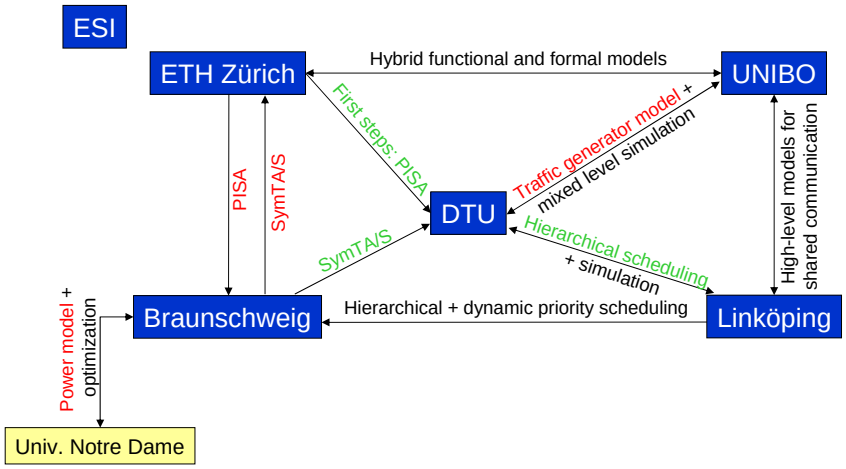
ARTIST2 Network of Excellence on Embedded Systems Design
cluster meeting –Bologna, May 22nd, 2006

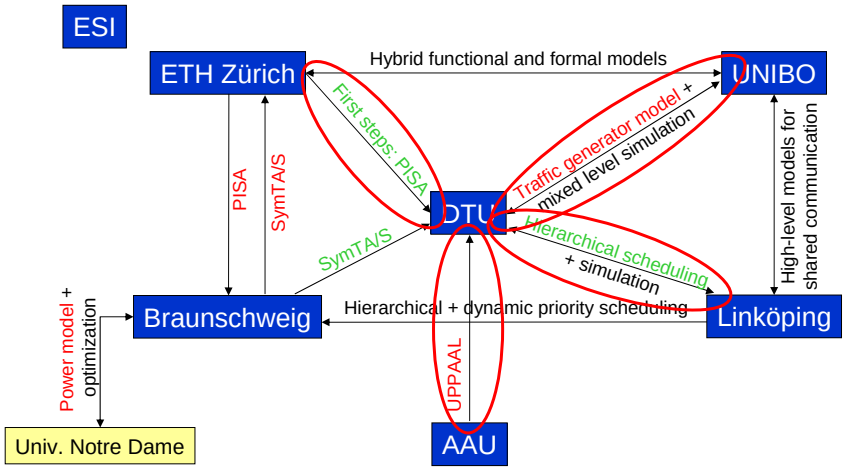
Year 1 activities

Achievements: Our integration work

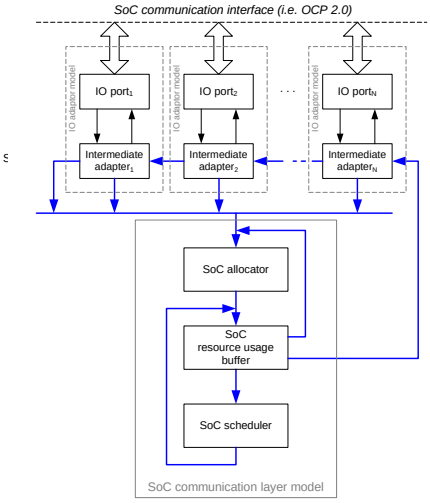


Year 2 activities

Research related to DTU



ARTS Framework



- **ARTS** Simulation framework based on SystemC
- **ARTS** PE module:
  - Application
  - OS
  - IO ports (OCP 2.0 interface)
  - IO device drivers
- **ARTS** Communication module:
  - Network topology and protocol
  - Network adapters
  - IO ports (OCP 2.0 interface)
- Applications of **ARTS**:
  - MPSoC (NoC exploration)
  - Wireless sensor networks
  - Automotive systems (TT vs. ET)
  - Dynamic reconfiguration

Outline of presentation

- ARTS / MPARM
- ARTS for automotive
- ARTS exploration using PISA/ETHZ
- ARTS UPPAAL

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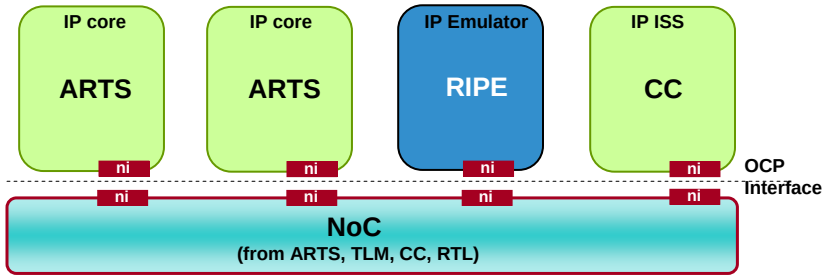
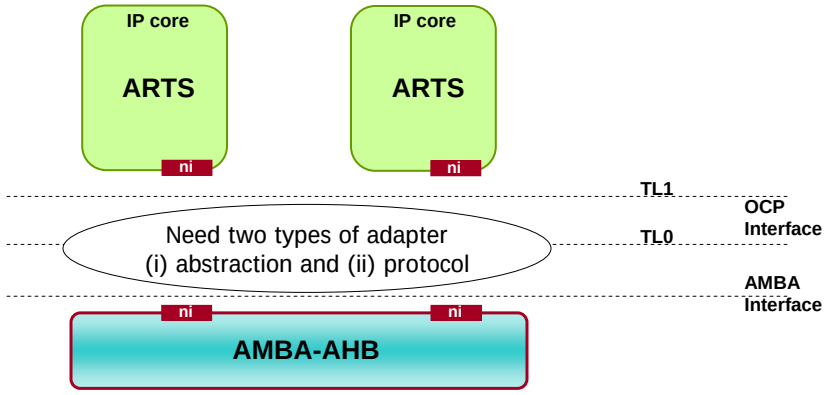
ARTS / MPARM

- Interactions between Univ. of Bologna and DTU
  - Traffic generators
  - ARTS – MPARM interaction for mixed level simulation

System Integration Overview



Exploration with AMBA-AHB



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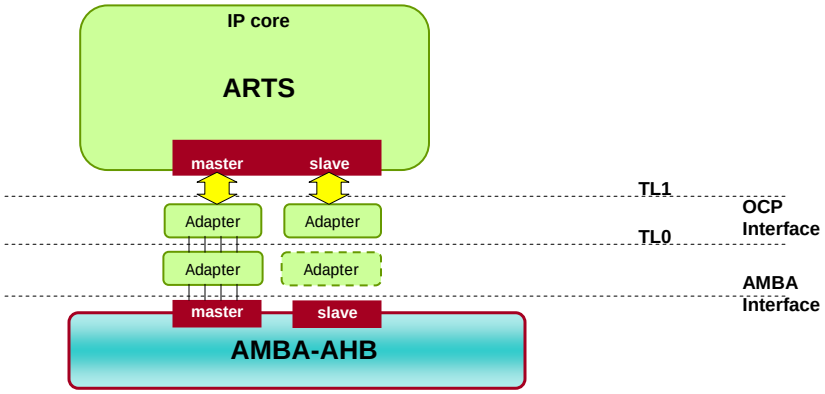
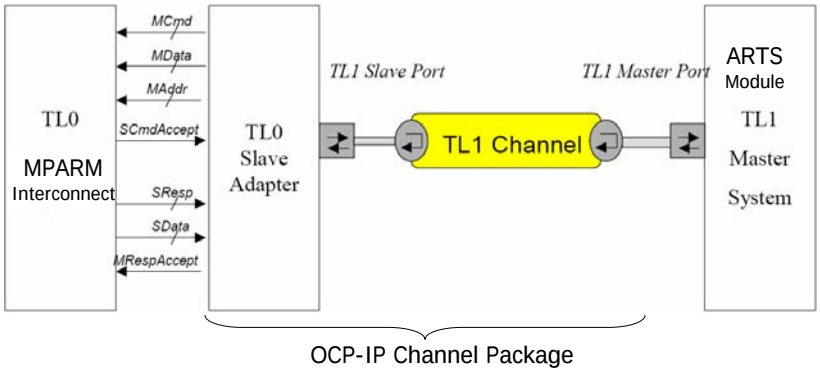
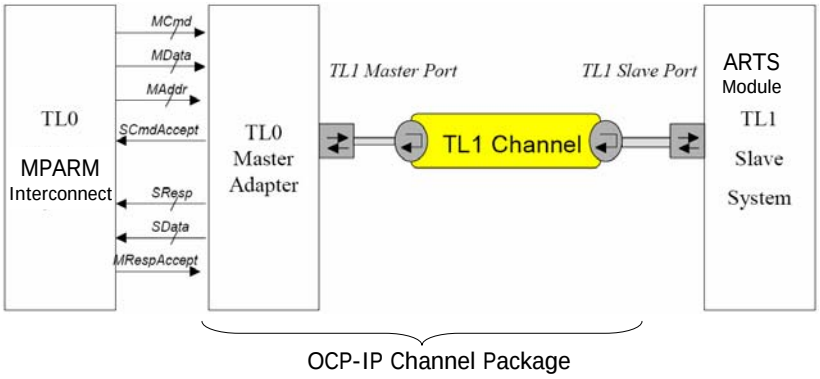


ARTS Master OCP Interface



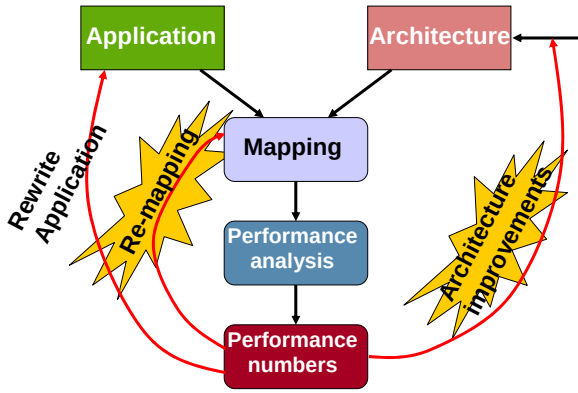
ARTS Slave OCP Interface



ARTS for automotive

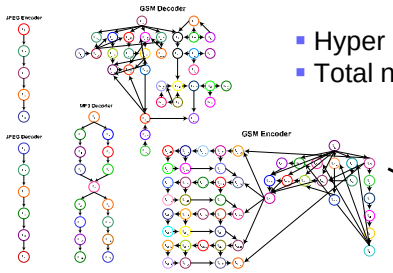
- TU Linkoping has extended ARTS
  - No global clock for time reference
  - Possible to execute real code
  - Implemented a number of automotive network protocols

ARTS exploration using PISA/ETHZ



- Multiobjective optimization problem
- Using the PISA framework from ETHZ (SPEA2)

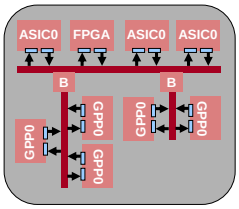
Design space exploration



- Hyper period
- Total number of tasks **530**

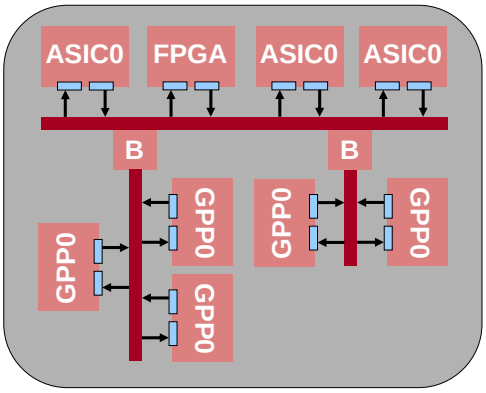
mapping

- Meet deadlines
- Min. power
- Min. buffer sizes
- Component cost



Static scheduling

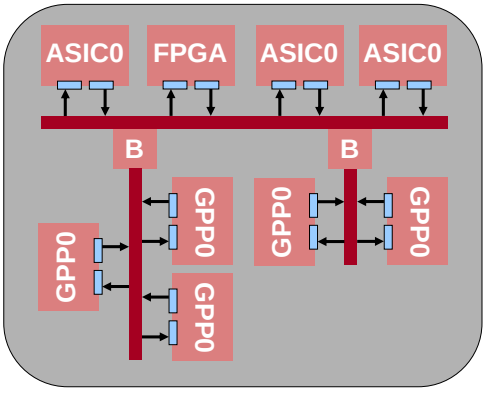
Scenarios



- Explore task mappings
  - No change in architecture
- Explore task mappings and architecture improvements
  - Number and types of cores buses and bus bridges

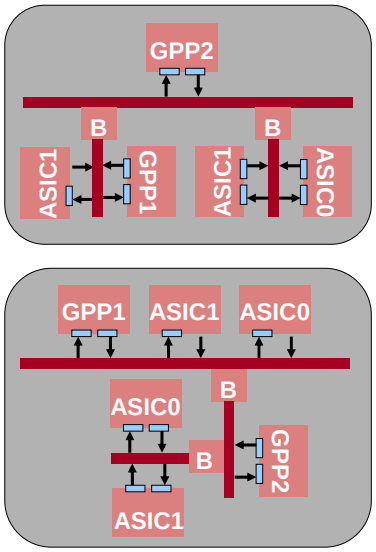
PE	GPP0	GPP1	GPP2	FPGA	ASIC0	ASIC1	BUS
Frequency (MHz)	25	10	6.6	2.5	2.5	2.5	66
Cost ($)	100	50	50	250	400	300	65

Exploring task mappings



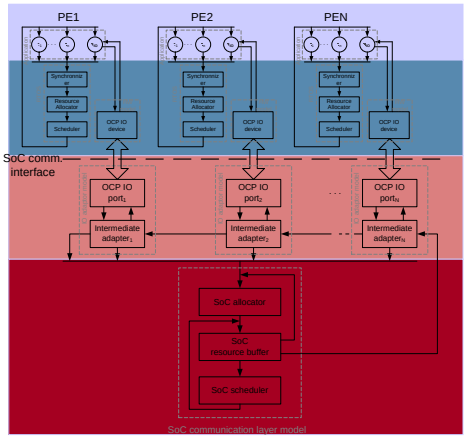
	A0	A1
Cores	8	8
Cost ($)	2045	2045
Energy (mJ)	3540	2649
Total buffer	29389	28036
Max buffer	9812	10366

+ Architecture improvements



	A1	A2	A3
Cores	8	5	6
Cost ($)	2045	1295	1695
Energy (mJ)	2649	817	789
Total buffer	28036	83260	40367
Max buffer	10366	14978	14978

ARTS UPPAAL



Application layer

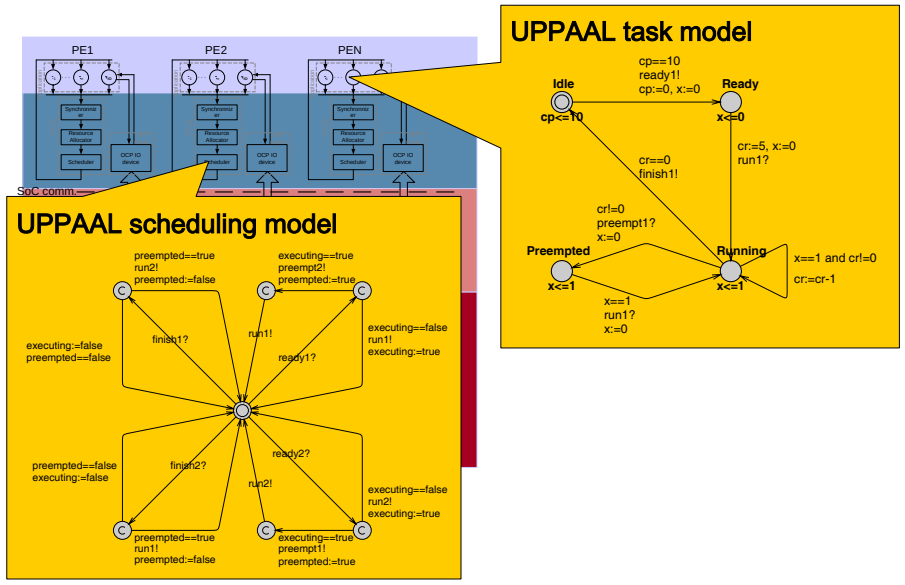
Middelware layer

Processing element layer

Network layer

A layered collection of event-triggered timed automatons

ARTS UPPAAL model



Preliminary results

- Task model
- Schedulers
  - RM
  - EDF
- Experiments
  - 2-8 tasks on 1-2 processor verified in 1-30 sec.

System Modelling Infrastructure

- Focus of year 2:
  - Integration of models
- Results:
  - MPARM and RT-Calculus using Trafficgenerators (DATE'06)
  - ARTS and UPPAAL
- More ?