# A Unified Graphical Representation and Tool for Design and Integration of Components in Heterogeneous Distributed Real-Time Systems

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National Instruments Corporation

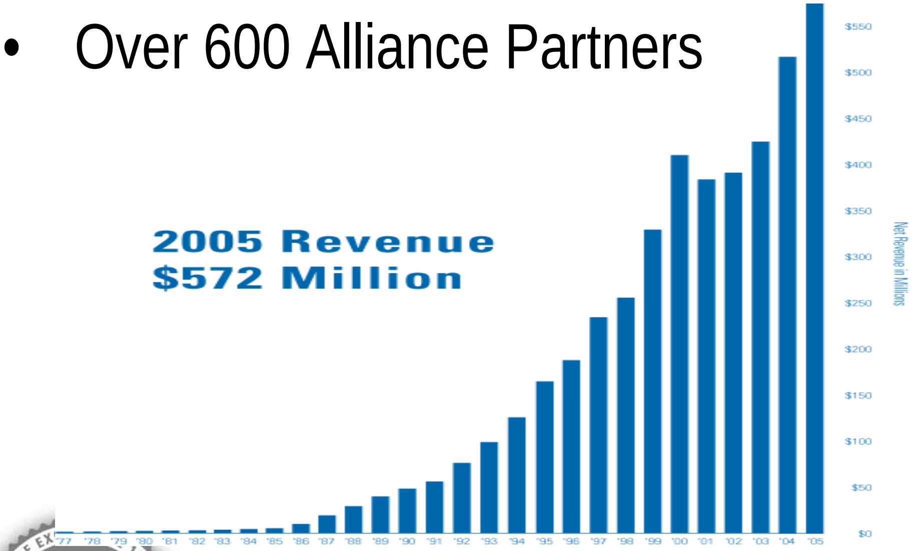
Austin, TX, USA

# National Instruments

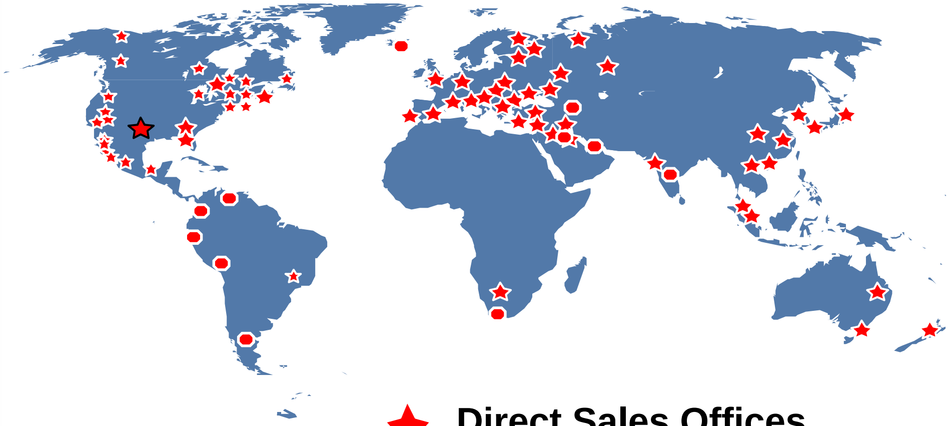
- 30 Year Leaders in Computer-Based Measurement and Automation
- 3800 Employees, 1,500 Engineers
- Corporate Headquarters in Austin, Texas
  - Direct Operations in 40 Countries
- Over 600 Alliance Partners

FORTUNE 100 BEST COMPANIES TO WORK FOR 2005

7 Years



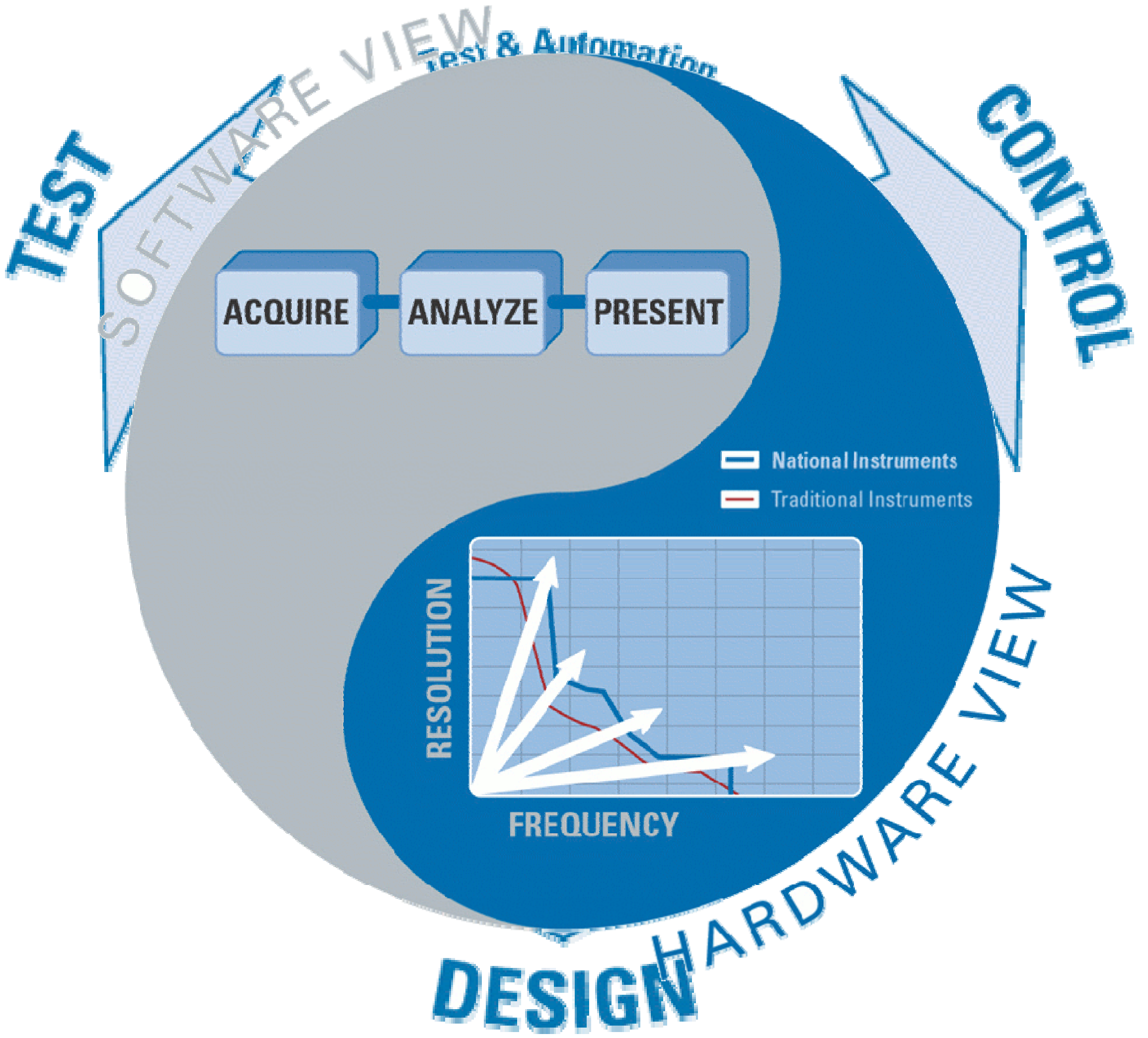
2005 Revenue $572 Million



★ Direct Sales Offices

● Distributors

# Virtual Instrumentation Vision



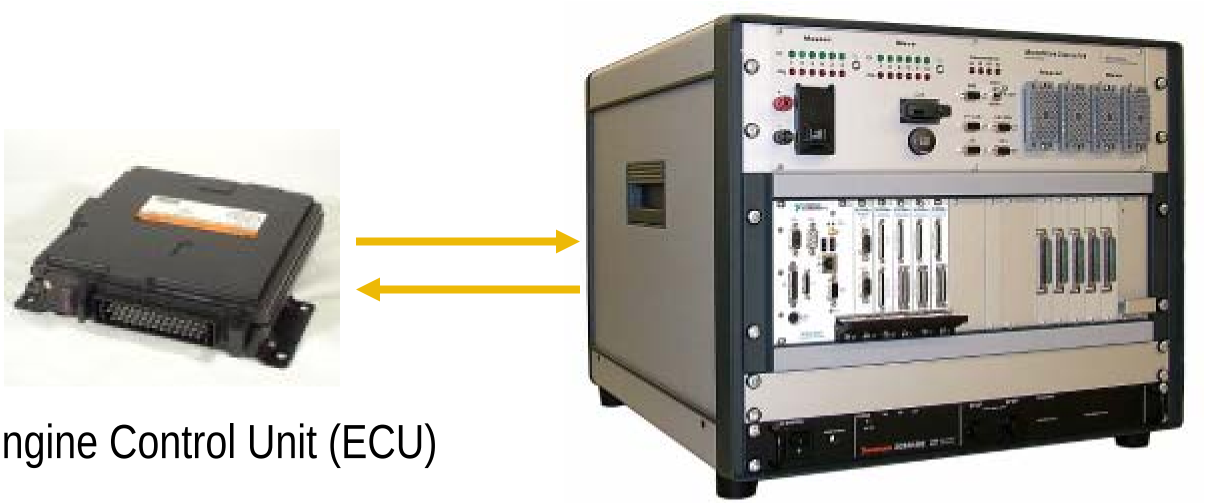
**“To do for test and measurement what the spreadsheet did for financial analysis.”**

# Use Case: Distributed Fly-by-Wire HIL Simulation

- Challenge
  - Integrate 10 distributed nodes executing device models
  - Share simulation data and I/O with low latency
- Solution
  - Implement simulation models on real-time platforms
  - Deterministic network used to share data

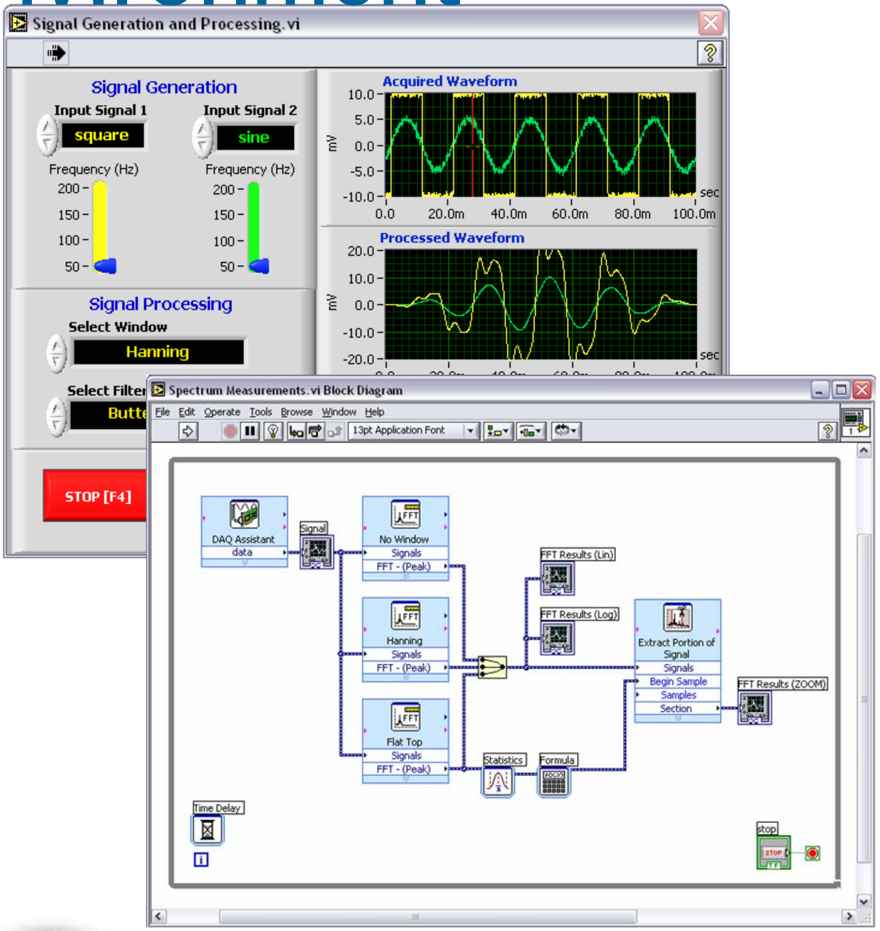
# Use Case: Engine HIL Simulation

- Challenge: Simulate a 12 cylinder hybrid engine to test control strategies
- Solution: Implement simulation model on real-time platform



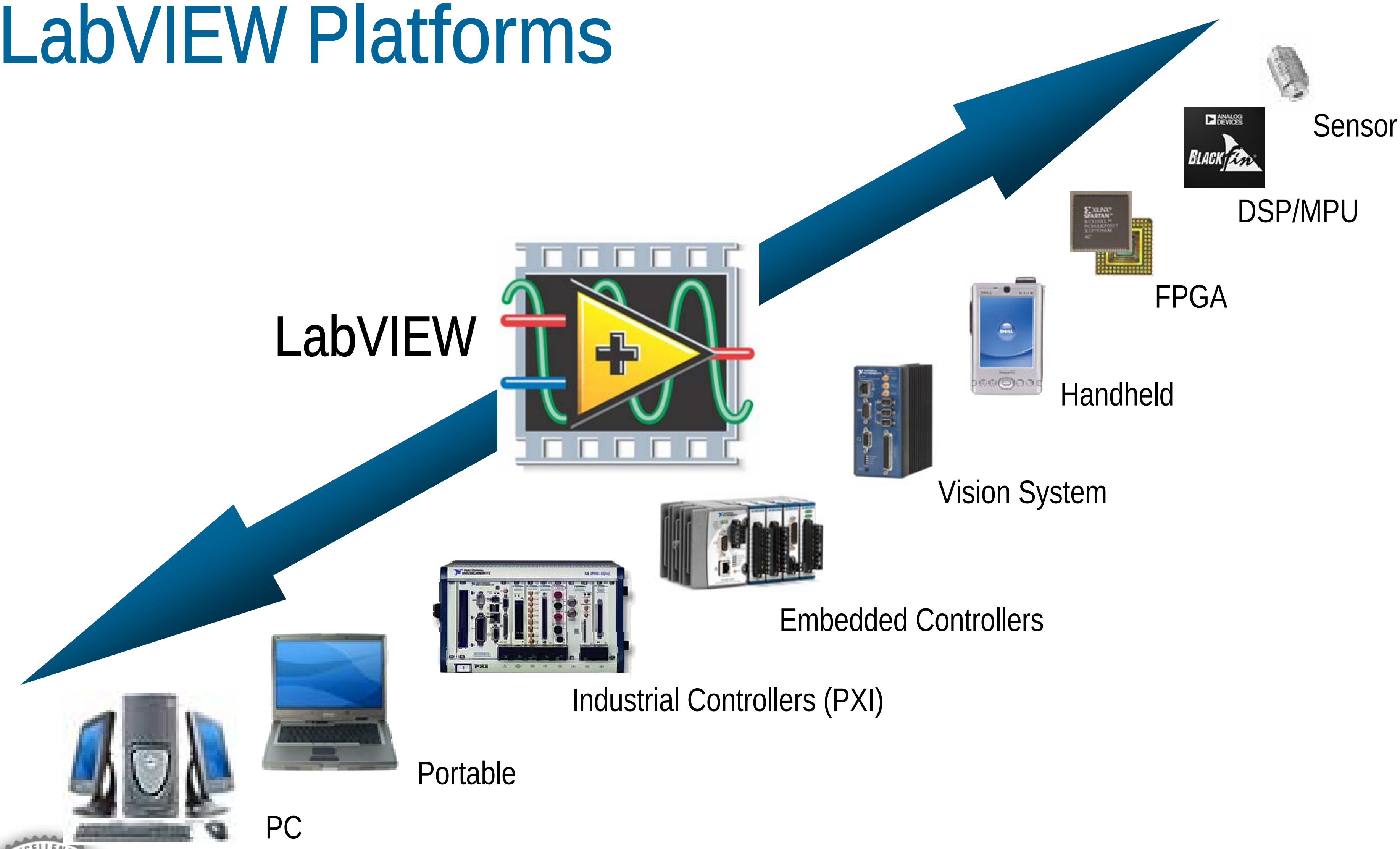
Engine Control Unit (ECU)

# LabVIEW Graphical Development Environment



- Structured data flow programming
- Compiled graphical development
- Target desktop, mobile, industrial, and embedded
- Thousands of out-of-the box mathematics and signal processing routines
- Seamless connectivity to millions of I/O devices

# LabVIEW Platforms



LabVIEW

Sensor

DSP/MPU

FPGA

Handheld

Vision System

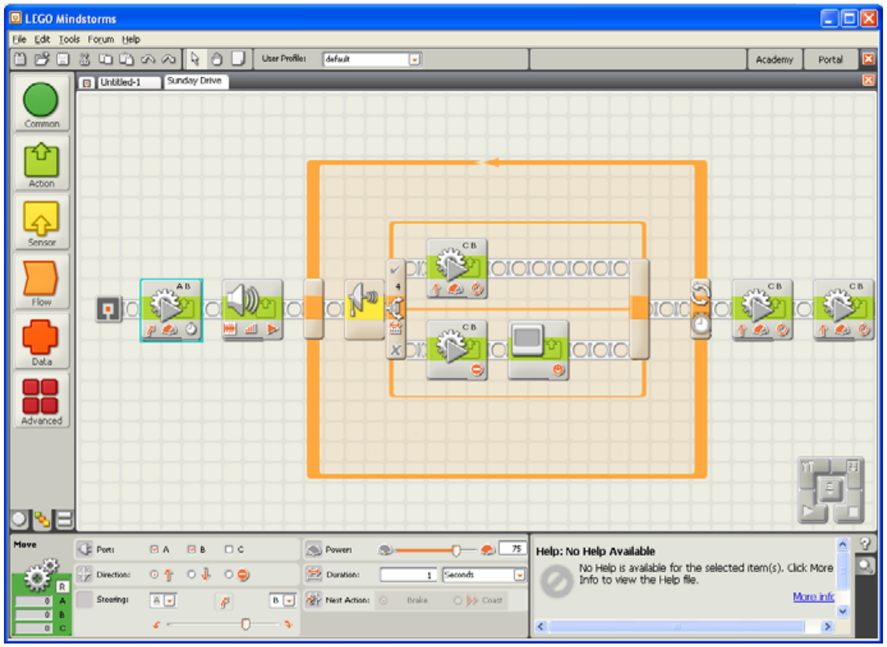
Embedded Controllers

Industrial Controllers (PXI)

Portable

PC

# LEGO mindstorms



Move

Port: ☑ A ☑ B □ C

Direction: ● ○ ○

Steering: A B

Power: 75

Duration: 1 Seconds

Next Action: ● Brake ○ Coast

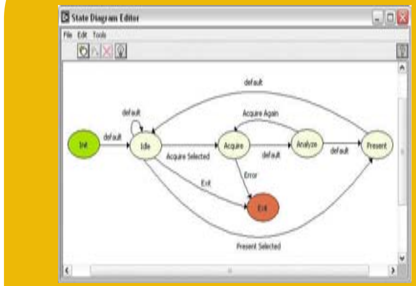
Help: No Help Available

No Help is available for the selected item(s). Click More Info to view the Help file.

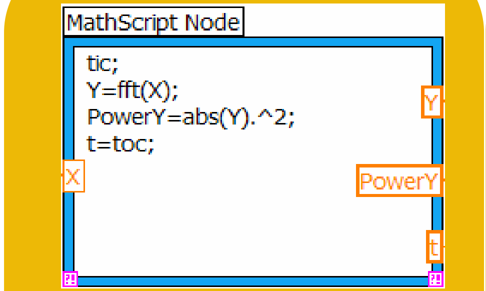
More info

POWERED BY

NATIONAL INSTRUMENTS™ LabVIEW™

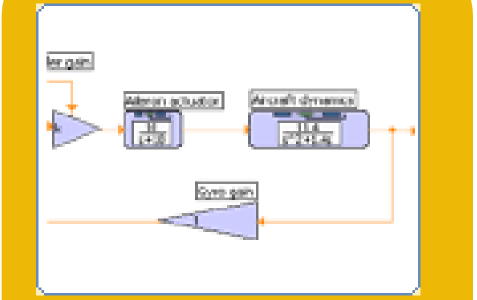


State Diagram

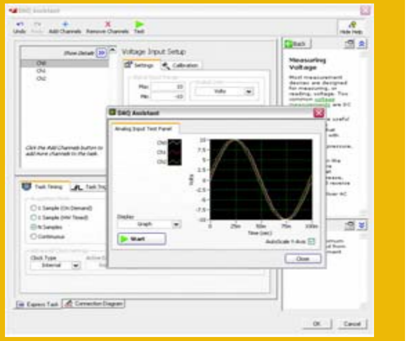


```
tic;
Y=fft(X);
PowerY=abs(Y).^2;
t=toc;
```

Textual Math



Simulation



Configuration

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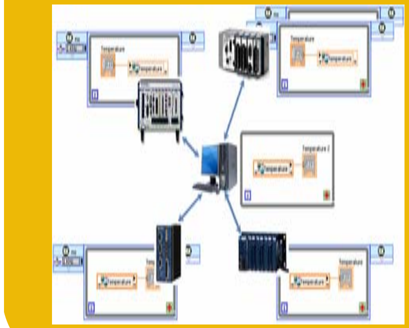
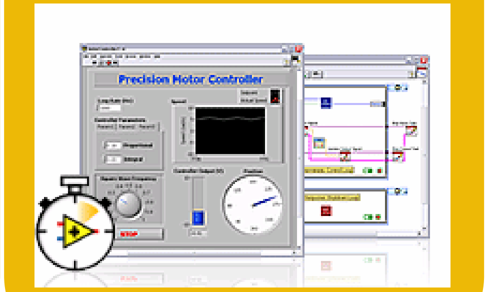
LabVIEW™

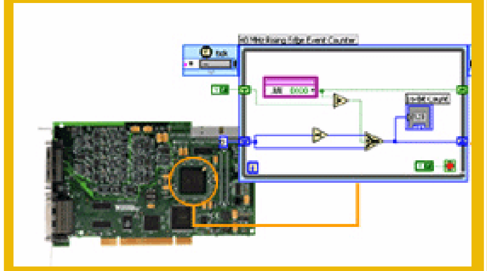
Distributed



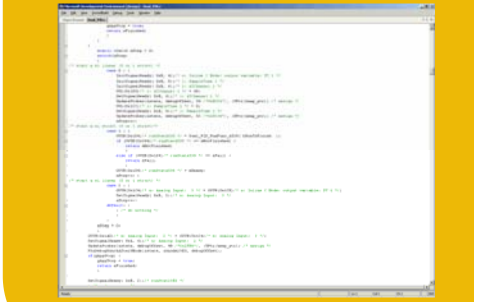
Real-Time



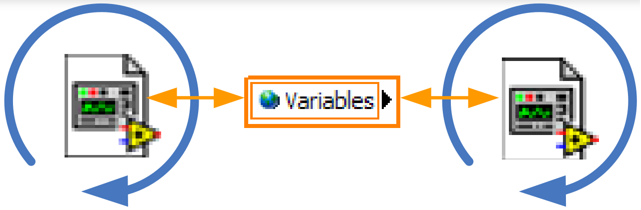
FPGA



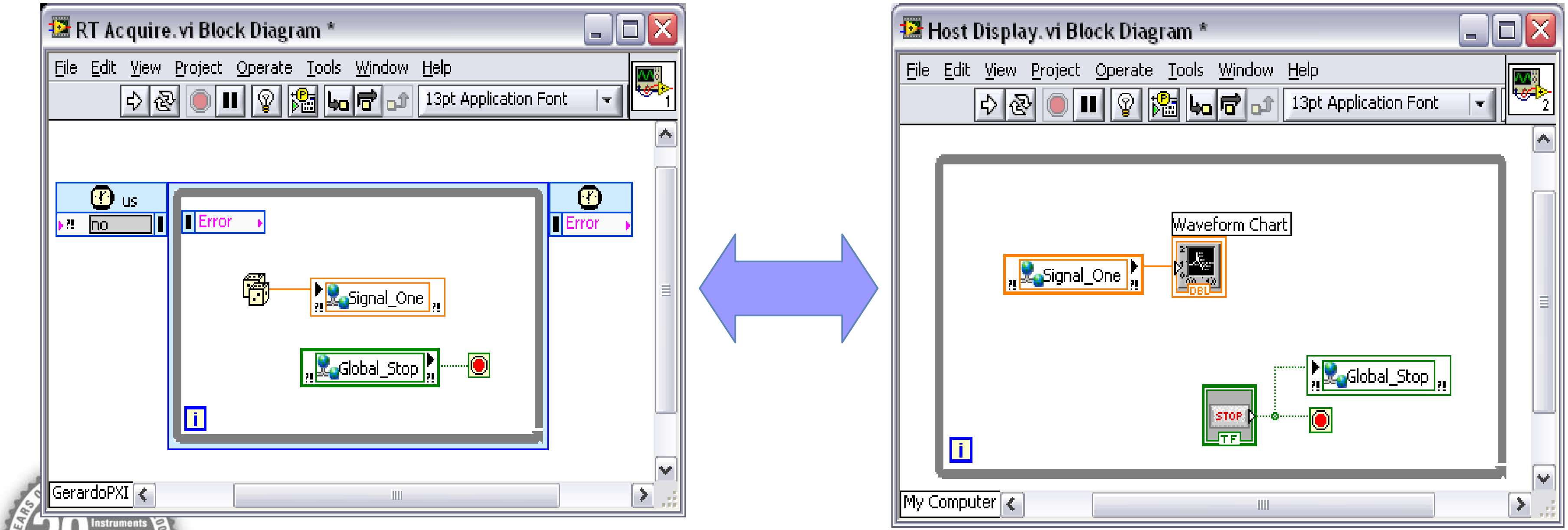
C Code Generation



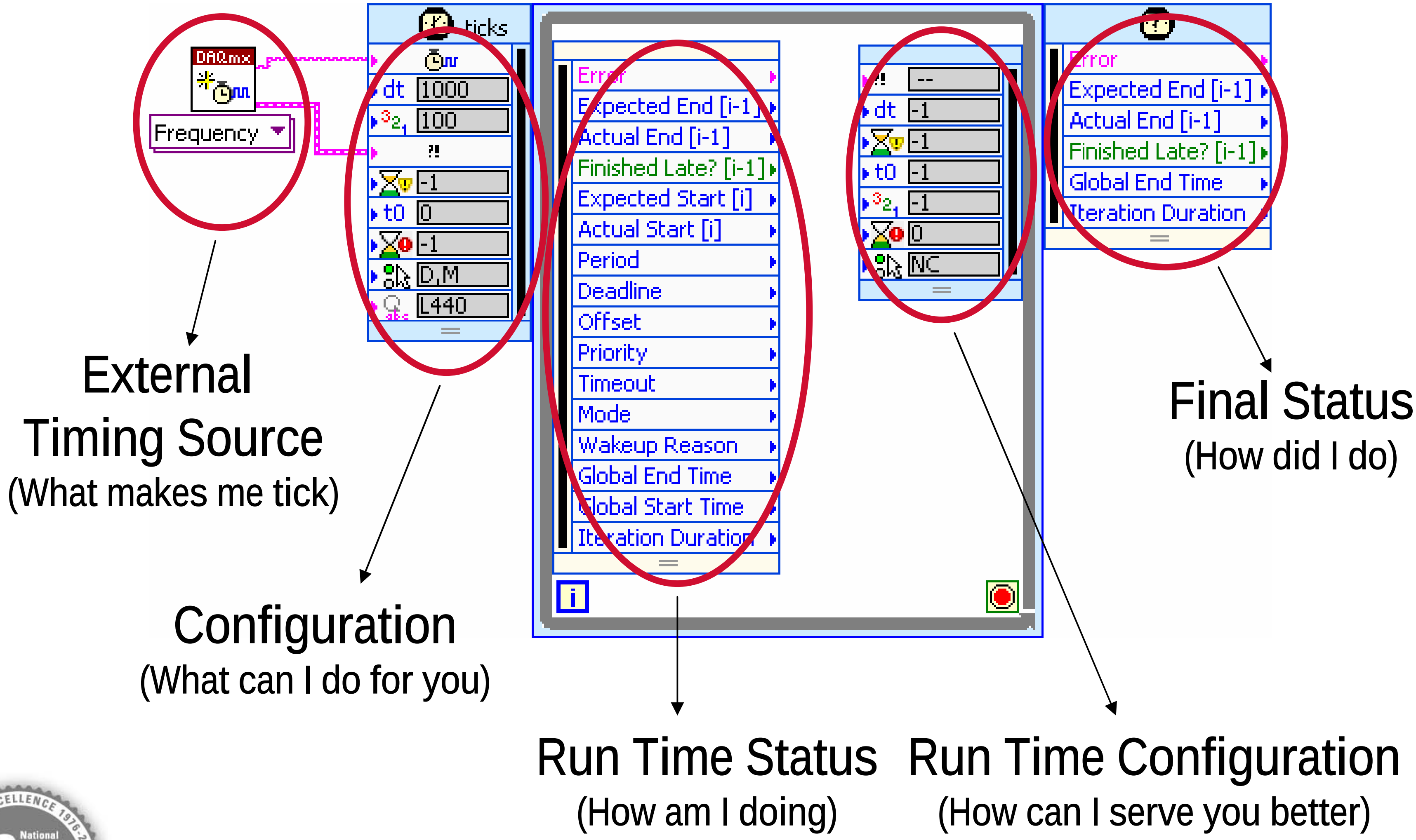
# LabVIEW Shared Variable



- Exchanging values when data flow is not appropriate
  - Loop to Loop
  - In a distributed setting
  - Utilize non-blocking buffers


RT Acquire.vi Block Diagram *
File Edit View Project Operate Tools Window Help
13pt Application Font
us
no
Error
Signal_One
Global_Stop
i
Error
GerardoPXI
Host Display.vi Block Diagram *
File Edit View Project Operate Tools Window Help
13pt Application Font
Waveform Chart
Signal_One
DBL
Global_Stop
STOP
TF
i
My Computer

# Timed Loop in LabVIEW: Specifying a Task



External Timing Source
(What makes me tick)

Configuration
(What can I do for you)

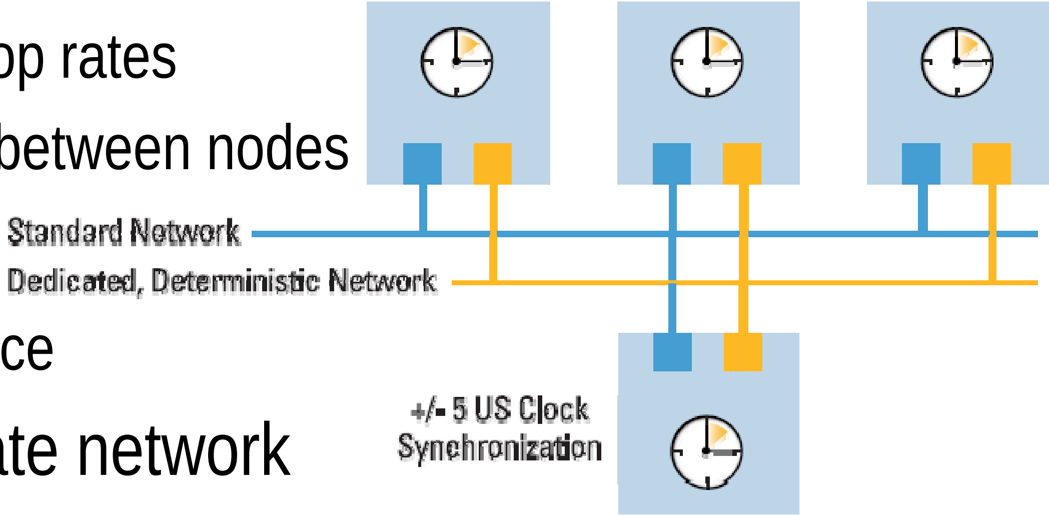
Run Time Status
(How am I doing)

Run Time Configuration
(How can I serve you better)

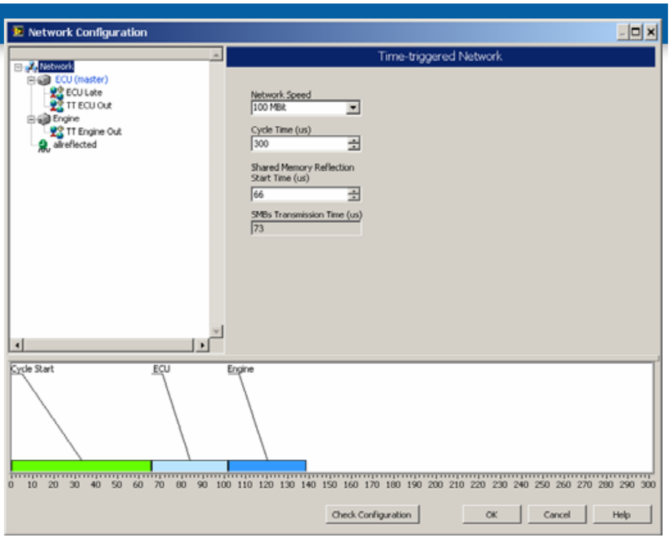
Final Status
(How did I do)

# National Instruments' Time-Triggered Network

- Deterministic communication
  - 100 µs to 100 ms network loop rates
  - ±5 µs clock synchronization between nodes
- Off-the-shelf hardware
  - Uses second Ethernet interface
- Communication across private network
  - Traffic is scheduled
- Similar to other time-triggered offerings
  - FlexRay, TTP, TTCAN, Ethernet PowerLink, …


Standard Network
Dedicated, Deterministic Network
+/- 5 US Clock Synchronization

# Using Deterministic Ethernet



Network Speed: 100 MBit

Cycle Time (us): 300

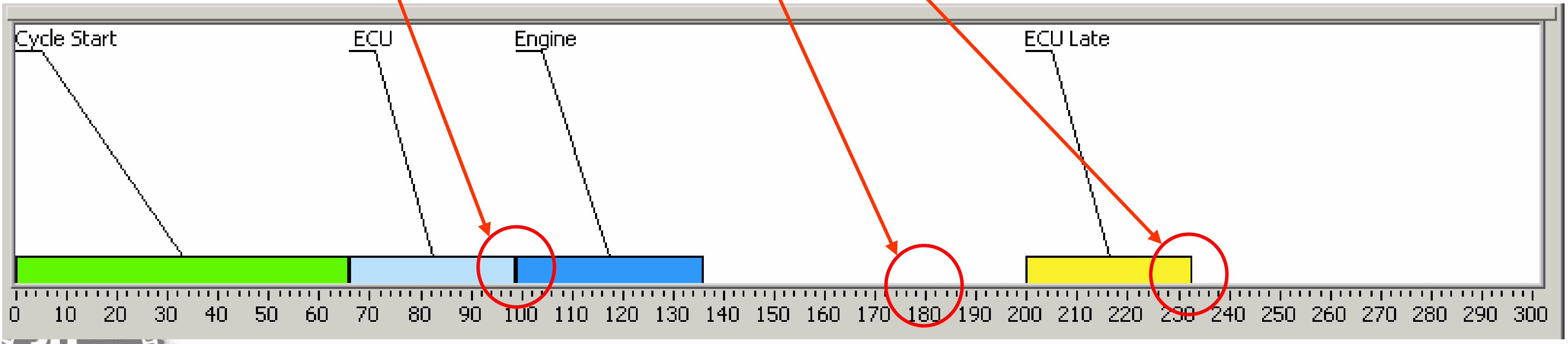
Shared Memory Reflection Start Time (us): 66

SMBs Transmission Time (us): 73

- User specifies a network cycle time
  - All traffic is repeated at this interval
- Time-triggered variables
  - Used on the diagram just like other variables in LabVIEW
    - Owning system is the only writer
  - Values are communicated during designated time slots within the network cycle

# Using Deterministic Ethernet

- Network timing sources
  - Fires the Timed Loop when the network event happens
  - Timing source types
    - Network synchronized microsecond
    - Shared memory block has been reflected
    - Slot based variable timing sources

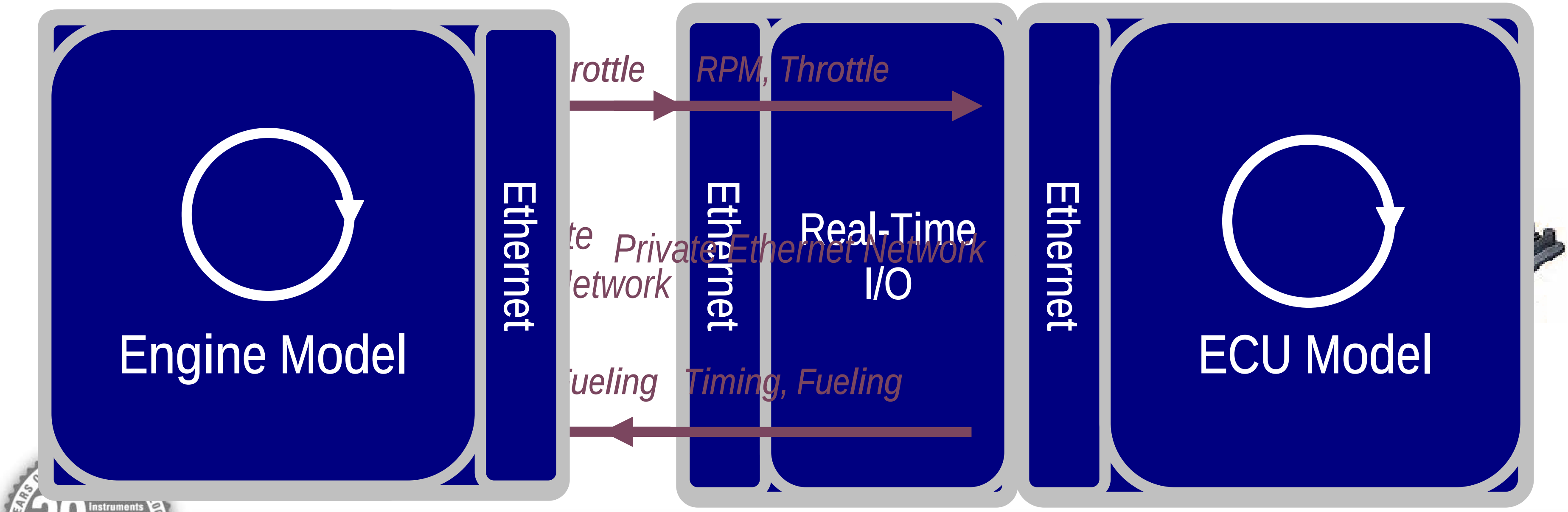


# Other uses of shared variable

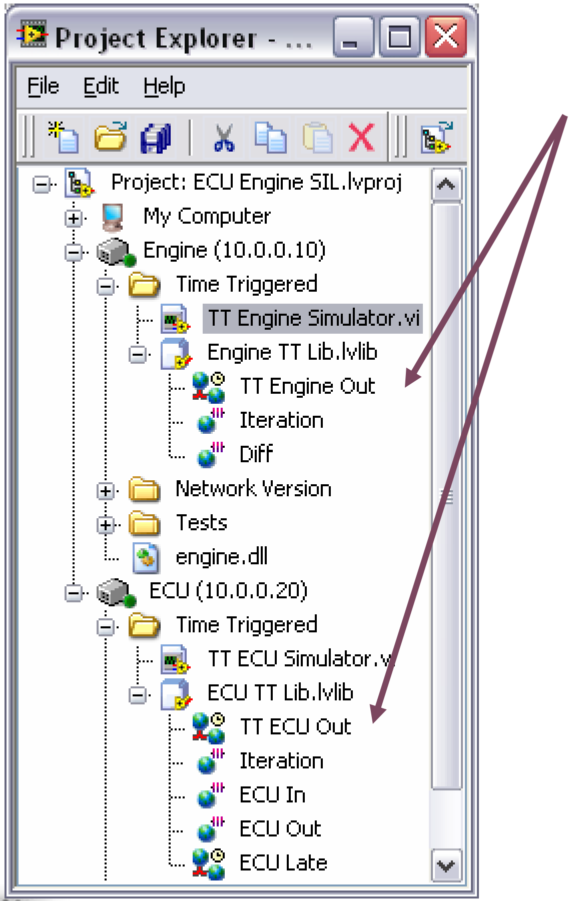
- Publish and subscribe
- Non-blocking FIFOs
- Streaming
- DMA transfers
- IO abstraction
- Can you change the model of computation just by changing variable types?
  - Without redrawing the diagram

# Time-Triggered Distributed Simulation Use Case

- Separate models for different system components
- Models execute in real-time with synchronized timing
- Capability to switch to real-world I/O

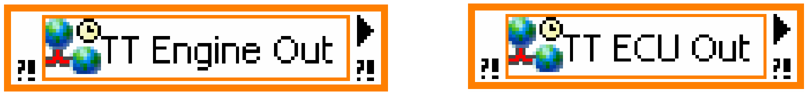


# Time-Triggered Distributed Simulation Example



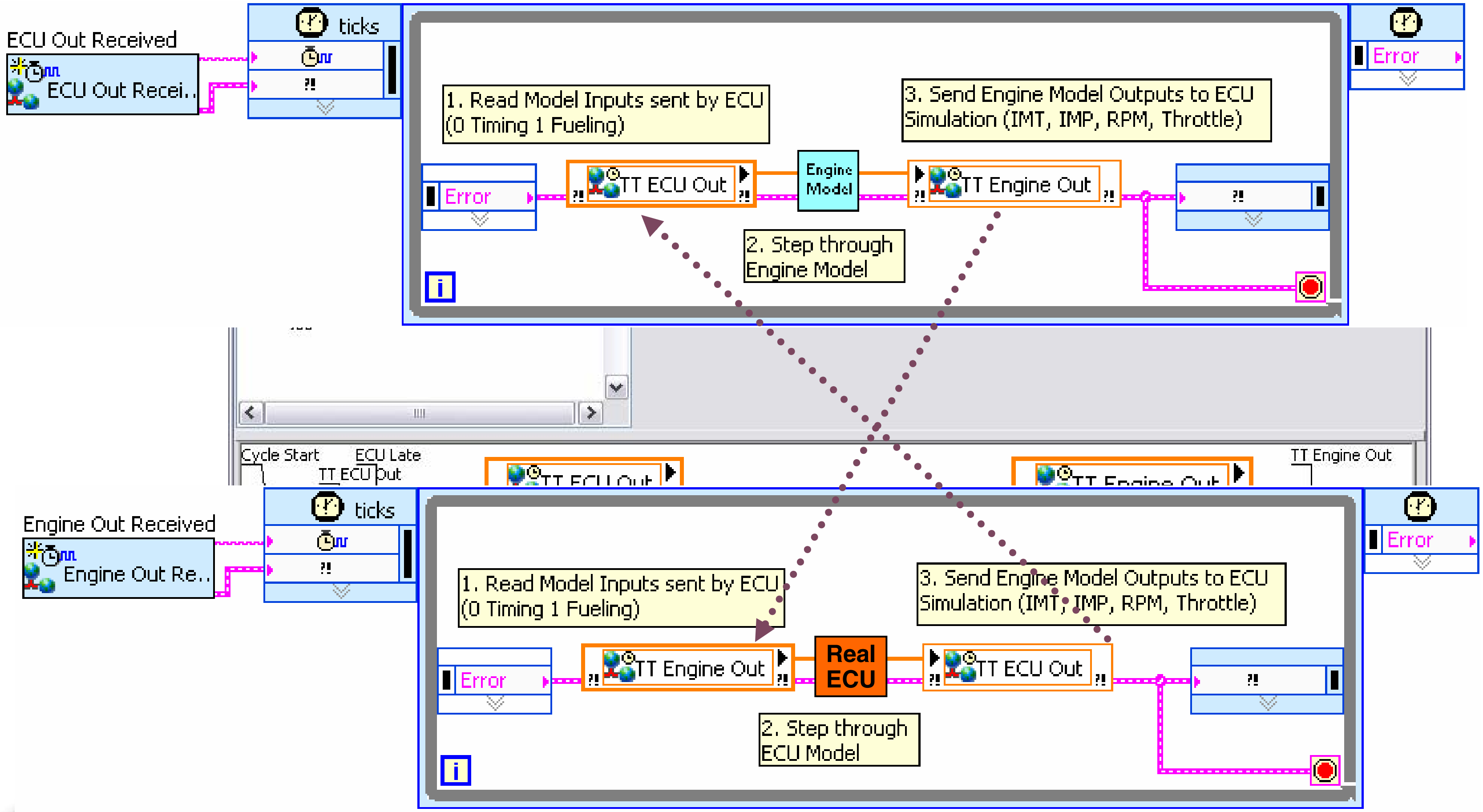
- Project: ECU Engine SIL.lvproj
  - My Computer
  - Engine (10.0.0.10)
    - Time Triggered
      - TT Engine Simulator.vi
      - Engine TT Lib.lvlib
        - TT Engine Out
        - Iteration
        - Diff
    - Network Version
    - Tests
    - engine.dll
  - ECU (10.0.0.20)
    - Time Triggered
      - TT ECU Simulator.vi
      - ECU TT Lib.lvlib
        - TT ECU Out
        - Iteration
        - ECU In
        - ECU Out
        - ECU Late

- Create Time-Triggered Shared Variables

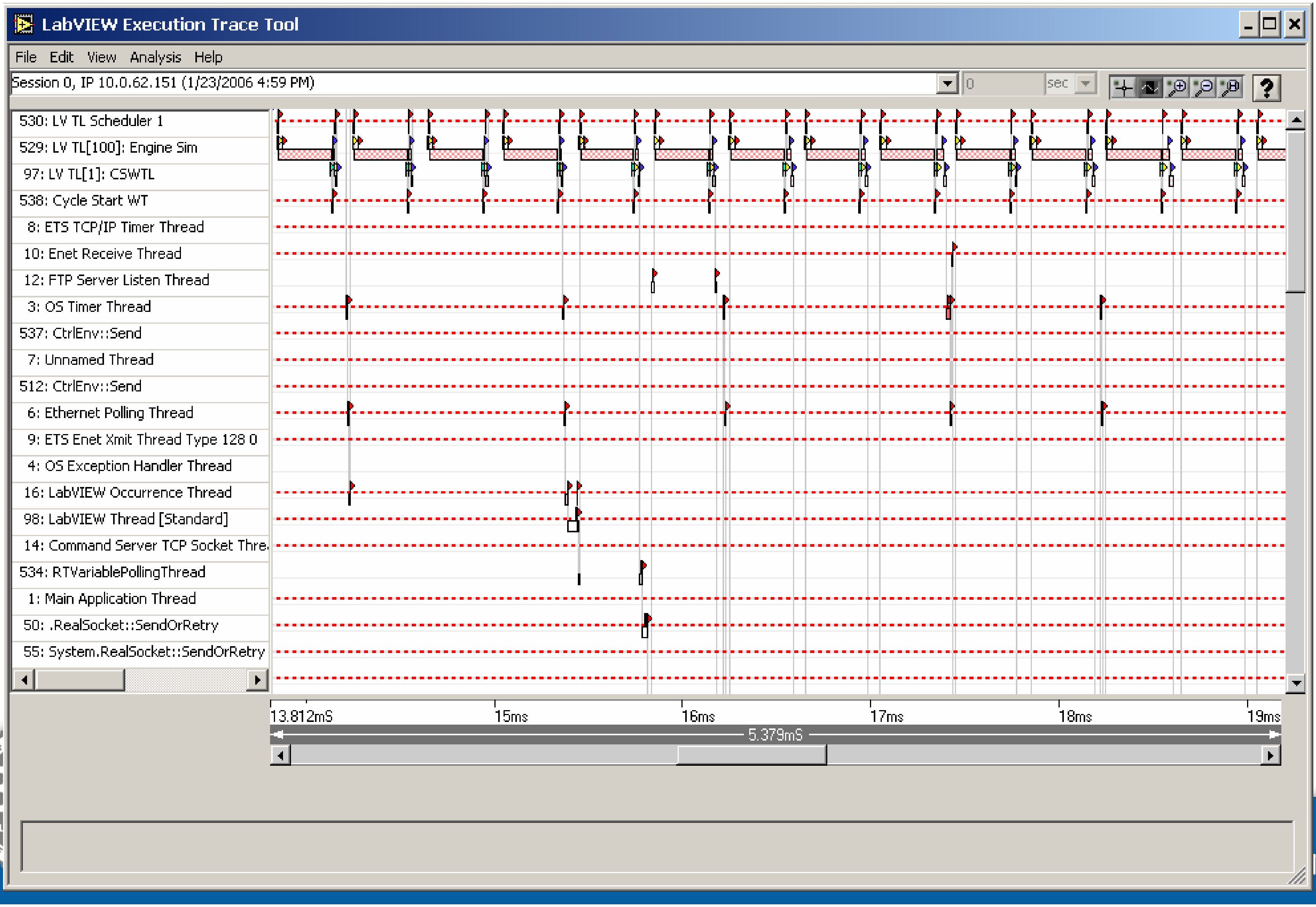


- Reserve time slots for variables in network configuration utility

# Time-Triggered Distributed Simulation Example


ECU Out Received
ECU Out Recei..
ticks
Error
1. Read Model Inputs sent by ECU (0 Timing 1 Fueling)
TT ECU Out
Engine Model
2. Step through Engine Model
3. Send Engine Model Outputs to ECU Simulation (IMT, IMP, RPM, Throttle)
TT Engine Out
i
Cycle Start
ECU Late
TT ECU Out
TT Engine Out
Engine Out Received
Engine Out Re..
ticks
Error
1. Read Model Inputs sent by ECU (0 Timing 1 Fueling)
TT Engine Out
Real ECU
2. Step through ECU Model
3. Send Engine Model Outputs to ECU Simulation (IMT, IMP, RPM, Throttle)
TT ECU Out
i

# Capturing the Real-time Behavior

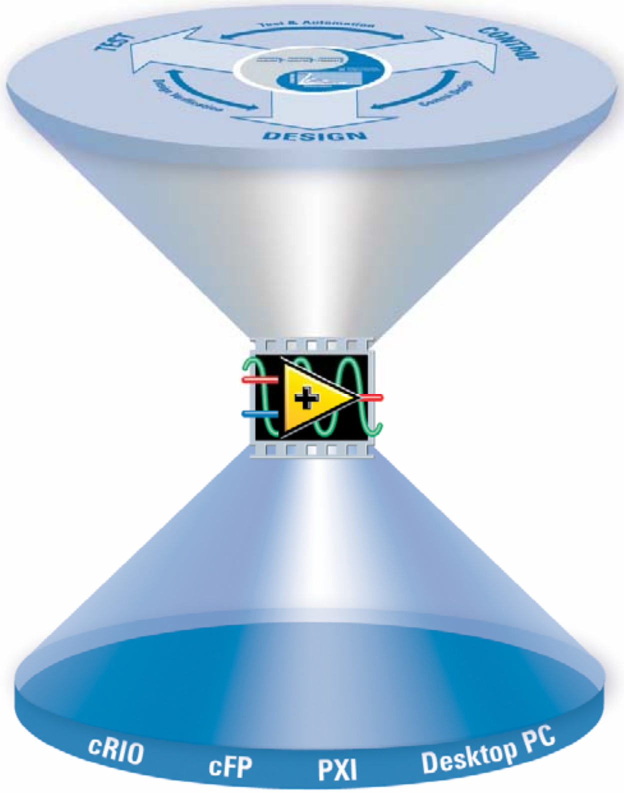


Session 0, IP 10.0.62.151 (1/23/2006 4:59 PM)

530: LV TL Scheduler 1
529: LV TL[100]: Engine Sim
97: LV TL[1]: CSWTL
538: Cycle Start WT
8: ETS TCP/IP Timer Thread
10: Enet Receive Thread
12: FTP Server Listen Thread
3: OS Timer Thread
537: CtrlEnv::Send
7: Unnamed Thread
512: CtrlEnv::Send
6: Ethernet Polling Thread
9: ETS Enet Xmit Thread Type 128 0
4: OS Exception Handler Thread
16: LabVIEW Occurrence Thread
98: LabVIEW Thread [Standard]
14: Command Server TCP Socket Thre
534: RTVariablePollingThread
1: Main Application Thread
50: .RealSocket::SendOrRetry
55: System.RealSocket::SendOrRetry

# Separation of Concerns

- Programming abstractions
  - Diagram describes (abstract) functionality
  - Variable describes communication style
  - Timing sources describes events
- System architecture
  - Platform/ hw architecture
    - Real-time, FPGA, Embedded, Desktop
  - Data transfer
  - Time, event, data triggering
  - HW/SW boundary



# Temporal Isolation

- Static schedule of communication
- Rigid temporal contract between programs and network
  - Between components
  - Network enforces the global schedule
    - If a program runs over, its values will not get communicated in this cycle

# Questions