







CPU vs. outside CPU

- · WCET Research too focused on modelling the CPU
- But systems have:
 - DMA, sharing same memory
 - DSP, sharing the same bus
 - Arbitration to access other devices
 - Memory management units
- Focus on the feature that have the largest impact, others can be "approximated".
 - Cache has by far the largest impact
 - Cache misses "looks" like HD Page faults!.
- Example (real HW):
 - Cache hit = 2 cycles
 - Cache miss = 40 cycles
 - Cache miss together at worst instant with DMA transfer = 80 cycles
 - But very unlikely to happen every time.

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WCET - Scheduling	
•	 Typical assumptions on WCET "task running in isolation, not interrupted, no preemptions" Typical schedulability analysis assumptions: (<i>possibly all wrong</i>) <i>Ci</i> : WCET is known, constant and accurate. <i>Ci</i> does not change over time Mode changes HW impact (interrupts/ preemptions/)
	 Actual execution time depends on schedule, circular dependency. Cooperative scheduling Cache Partitioning and Locking Locking interrupt code outside cache! Control of mode changes.
	 Strategies for scheduling: handle WCET overruns, Opportunities for gain time!!! LOTS (less on <i>slack time</i>) Careful with "Correlation" and dependencies Long execution times tend to happen together associated to single events. E.g. mode changes

Measured vs. Computed profiles

- Applicable to all resources
 - Execution time (WCET)
 - Cache misses
 - Number of accesses to external buses, and other HW features
 - Memory consumption
- "The best model of a system is the system itself"
 - Observational systems:
 - Trace Box
 - · CPU support for observing behaviour system
 - · CPU support for injecting HW test vectors

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