Modular Performance Analysis

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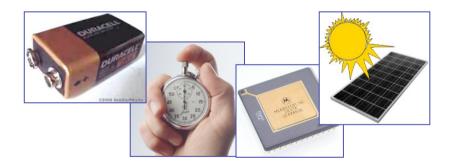
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Embedded Systems

Computation/Communication ⊕ Resource Interaction







Models of Computation

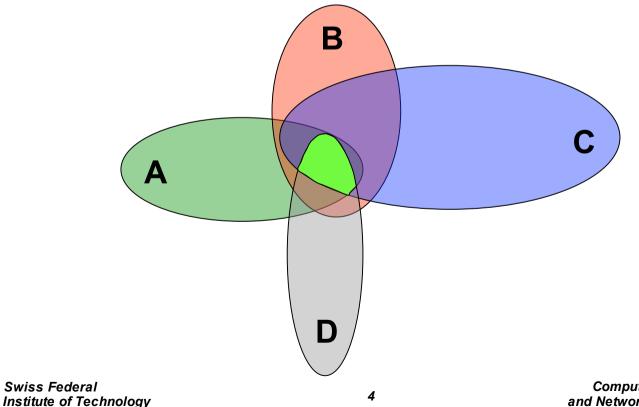
How can we classify and compare them?

stepwise refinement incremental design hierarchy concurrency safe modular beauty simple expressive formal accuracy tools compositional easy to use efficient executable implementation scope scalable



Why is it difficult ?

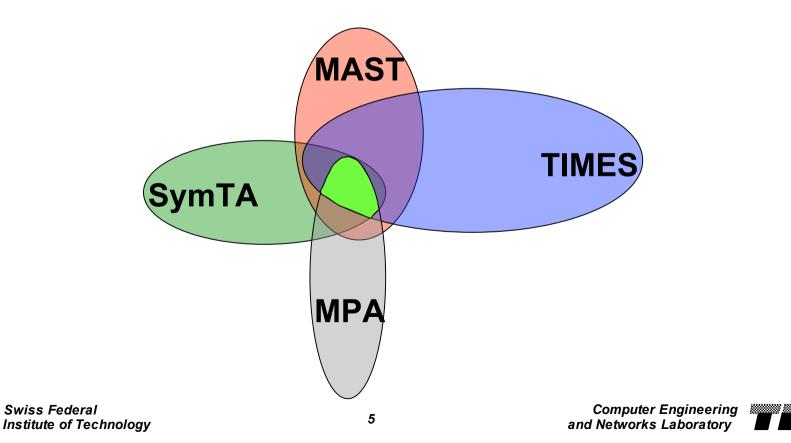
- Many aspects can not be quantified.
- Models cover different scenarios:





Intention

 Compare models and methods that analyze the timing properties of distributed systems.





Approach

- Define a set of benchmark examples that cover common area (*obligatory*)
 Define benchmark examples that show the power of each method (*free style*)
- Leiden Workshop on Distributed Embedded Systems: http://www.tik.ee.ethz.ch/~leiden05/

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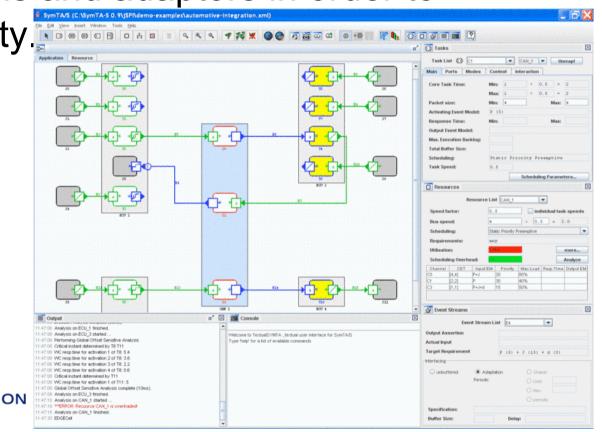
MAST

Wait another 20 minutes ...



SymTA/S

- Based on classical RT analysis (periodic, jitter).
- Simplified relations and adaptors in order to achieve modularity.
- Computation and Communication



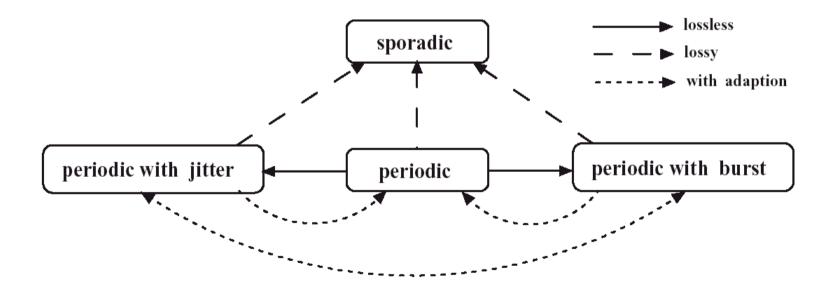






SymTA/S

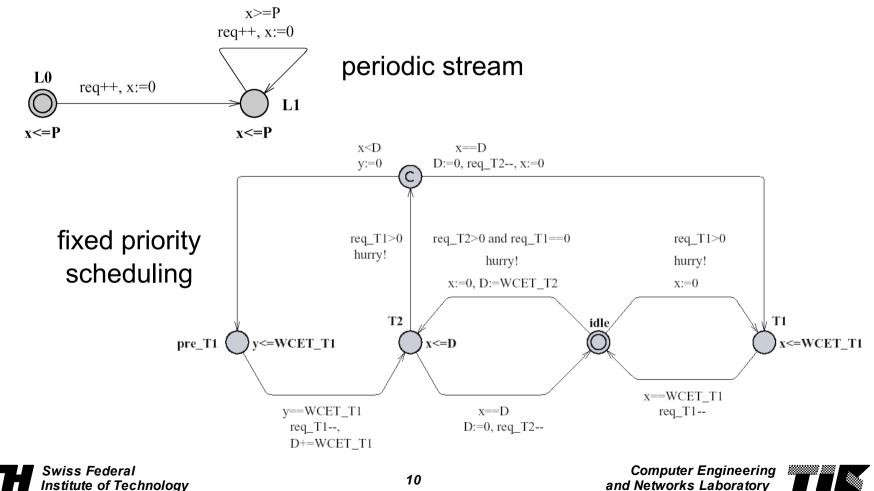
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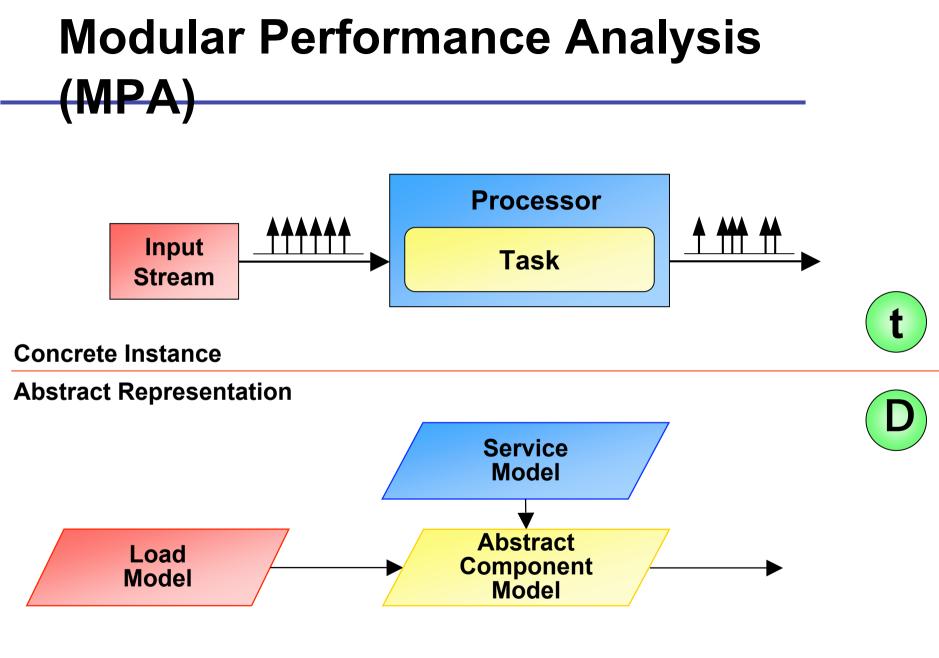




TIMES/UPPAAL

• Models are based on Timed Automata.



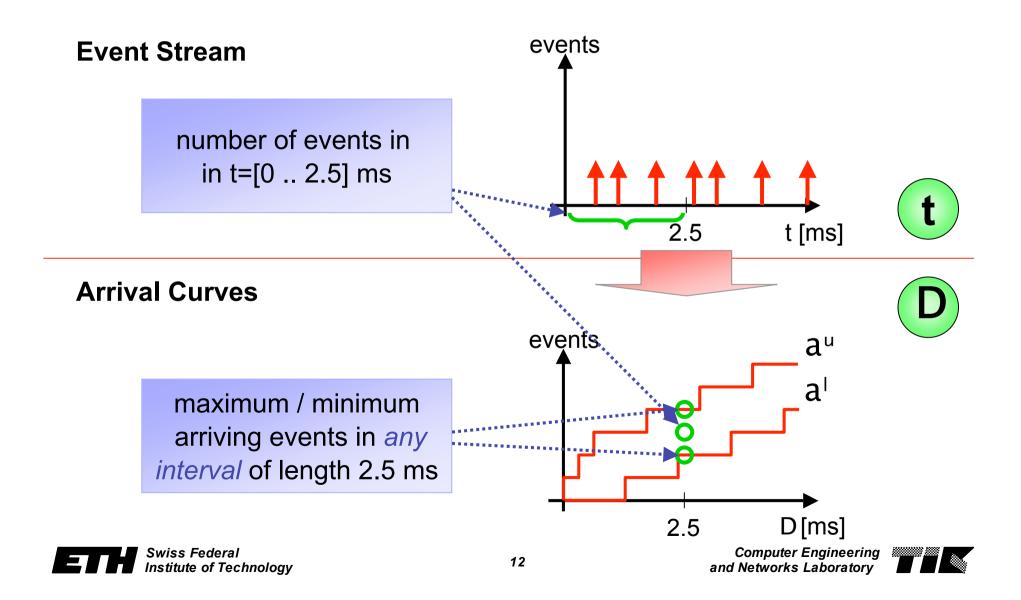


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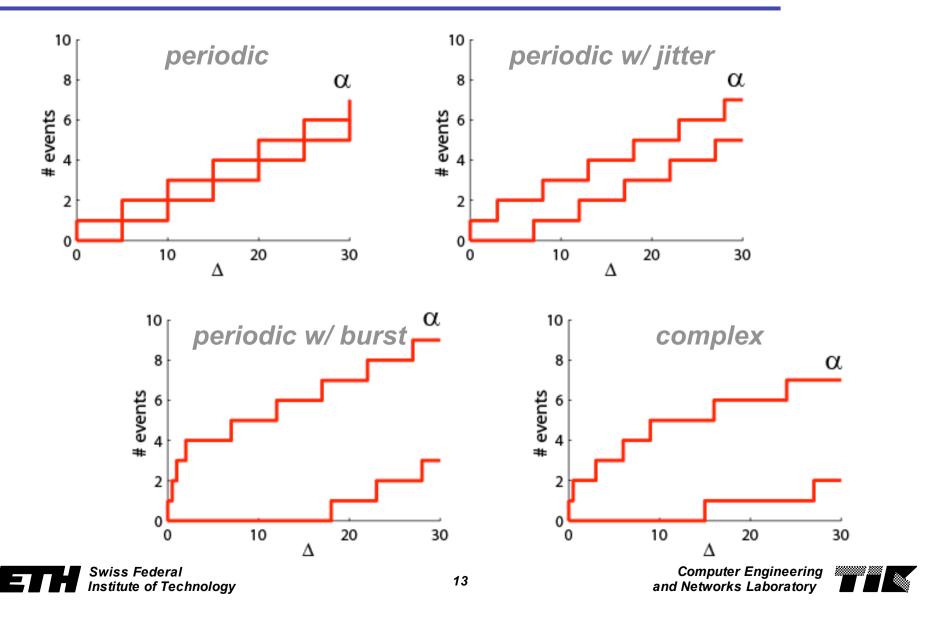
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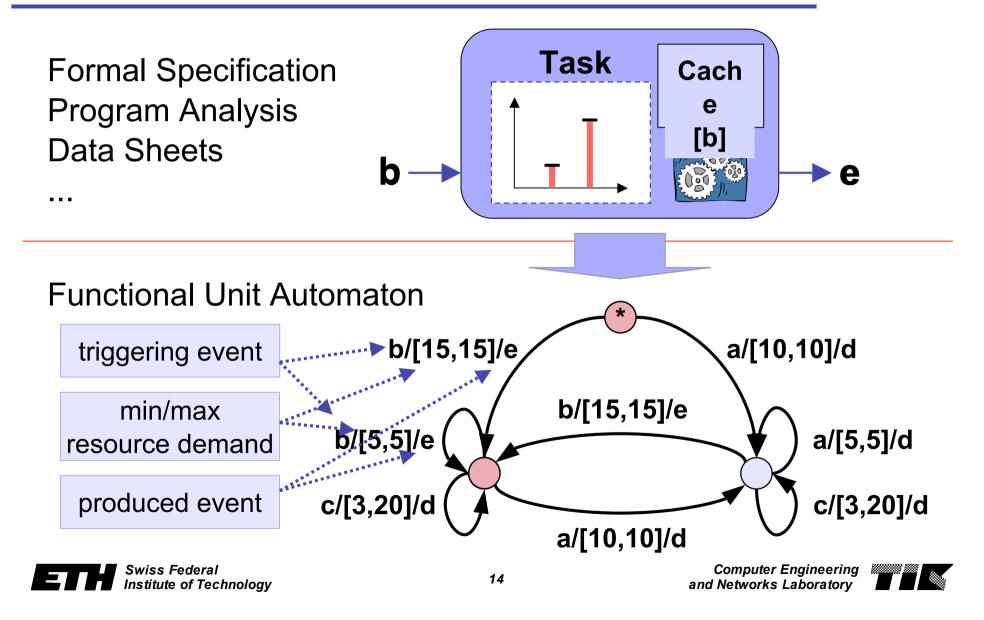
Abstract Stream Model



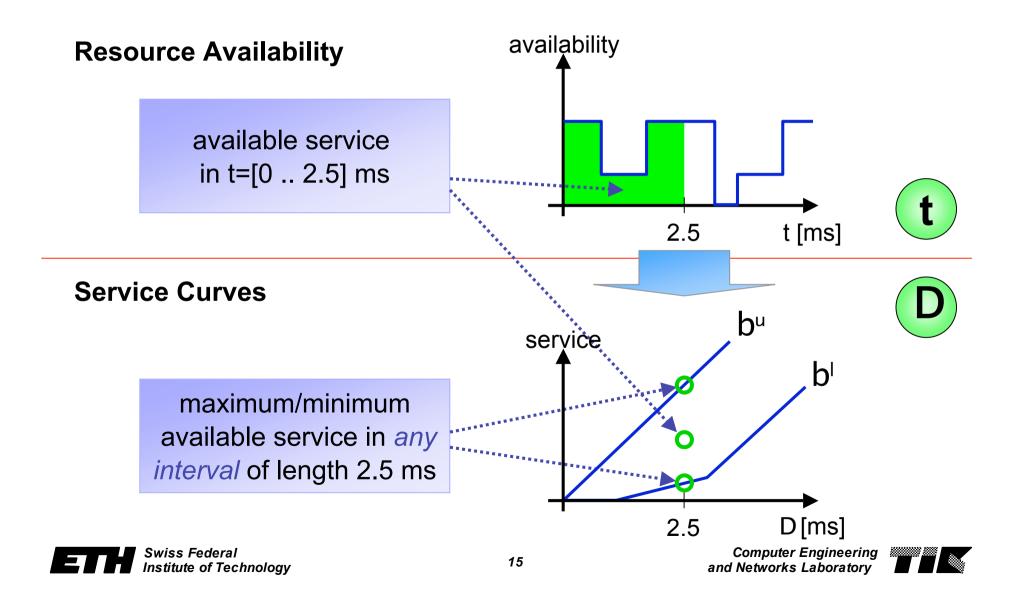
Load Model - Examples

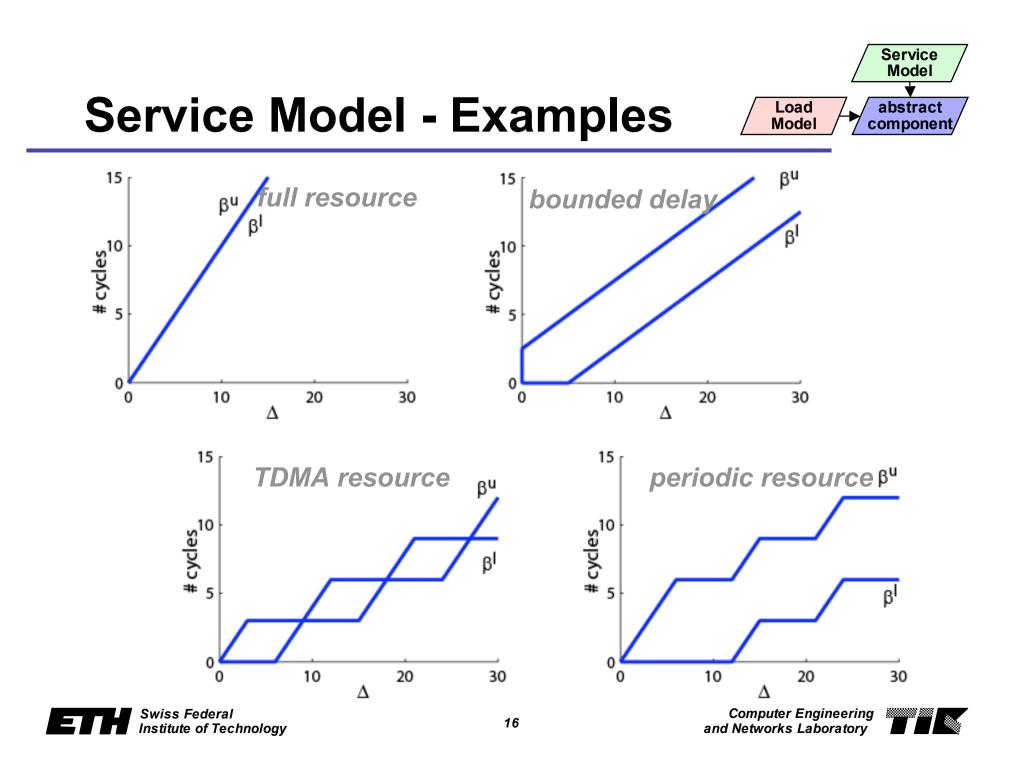


Process Abstraction



Service Model (Resources)





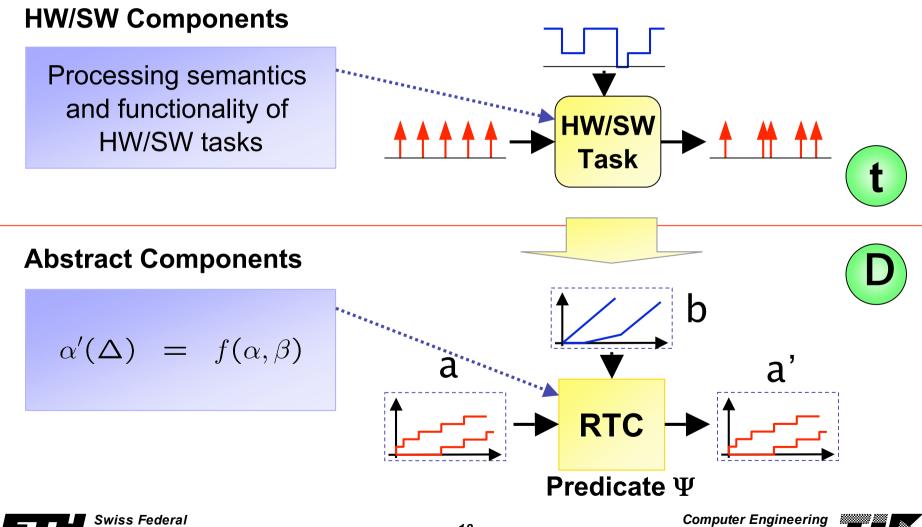
What kind of resources can be modeled?

- Memory (buffer space)
- Delay (end-to-end delay / processing and waiting)
- Computation
- Communication
- Energy





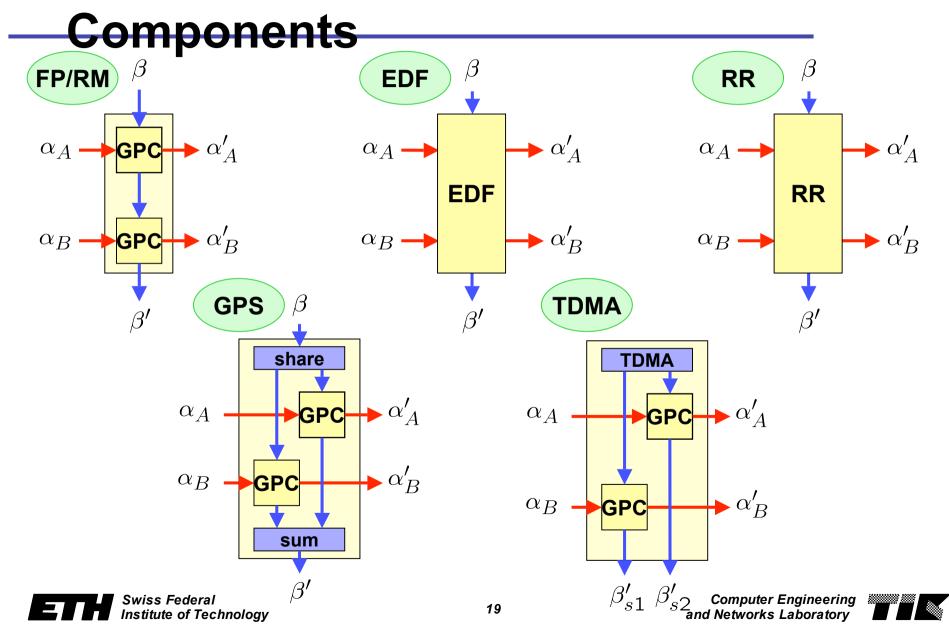
Processing Model (HW/SW)



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Scheduling and Arbitration



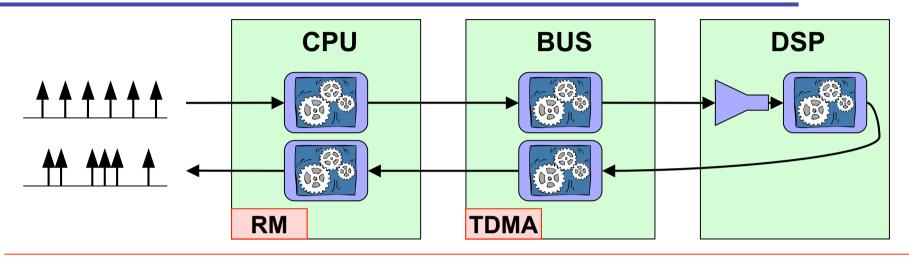
What kind of resource usage can be modeled?

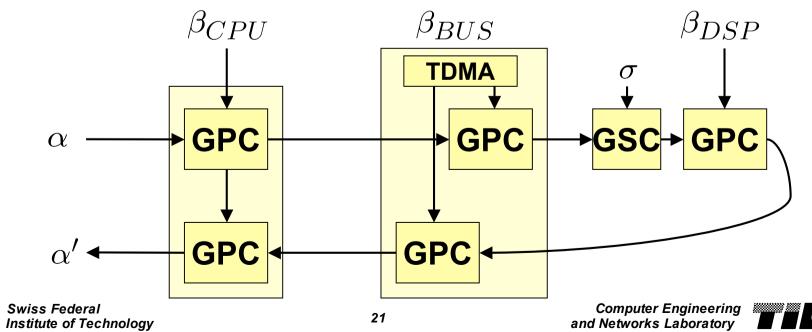
- Different resource sharing strategies
 - EDF
 - TDMA
 - Fixed Priority
 - GPS
- Different processing semantics
 - Greedy Processing
 - Greedy Shaper
 - Blocking

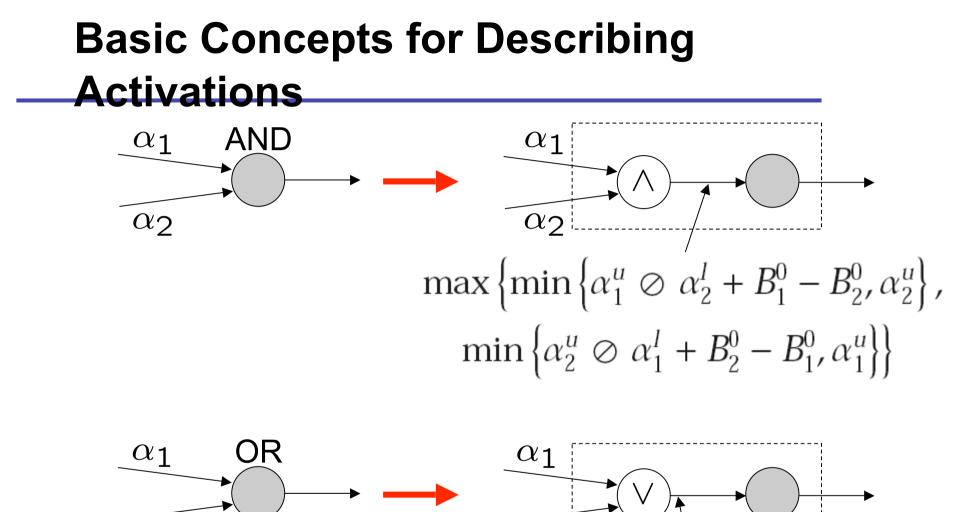




Complete System Composition





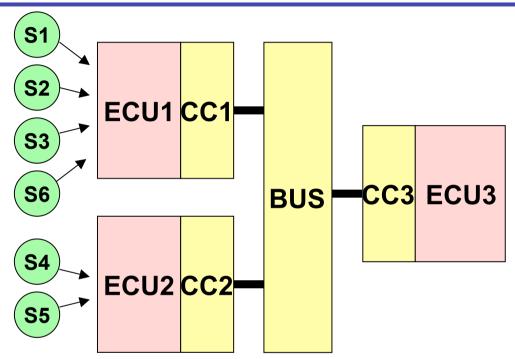








Free Style



Total Utilization:

- ECU1 59 %
- ECU2 87 %
- ECU3 67 %
- BUS 56 %

6 Real-Time Input Streams

- with jitter
- with bursts
- deadline > period
- 3 ECU's with own CC's

13 Tasks & 7 Messages

- with different WCED

2 Scheduling Policies

- Earliest Deadline First (ECU's)
- Fixed Priority (ECU's & CC's)

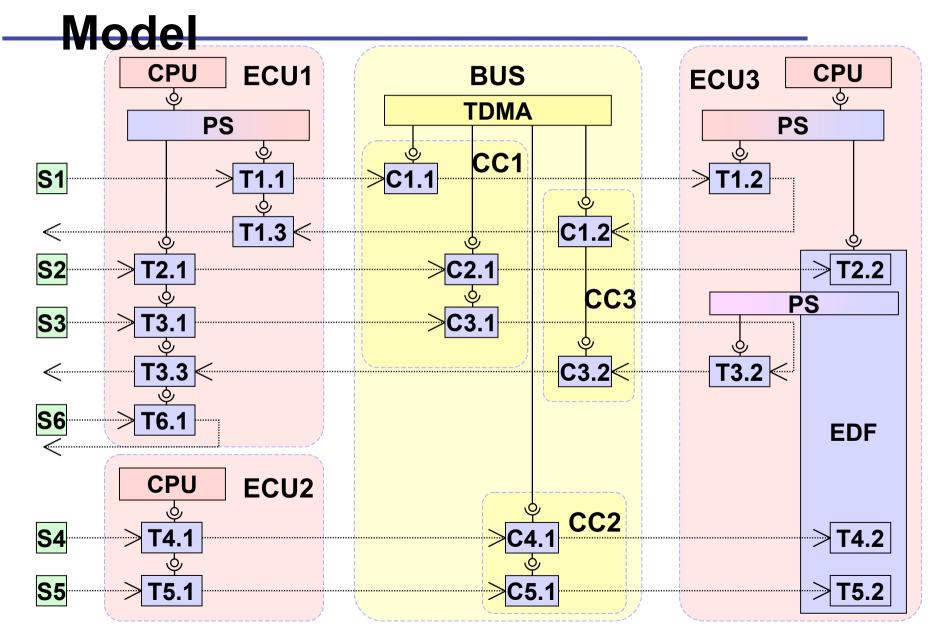
Hierarchical Scheduling

- Static & Dynamic Polling Servers

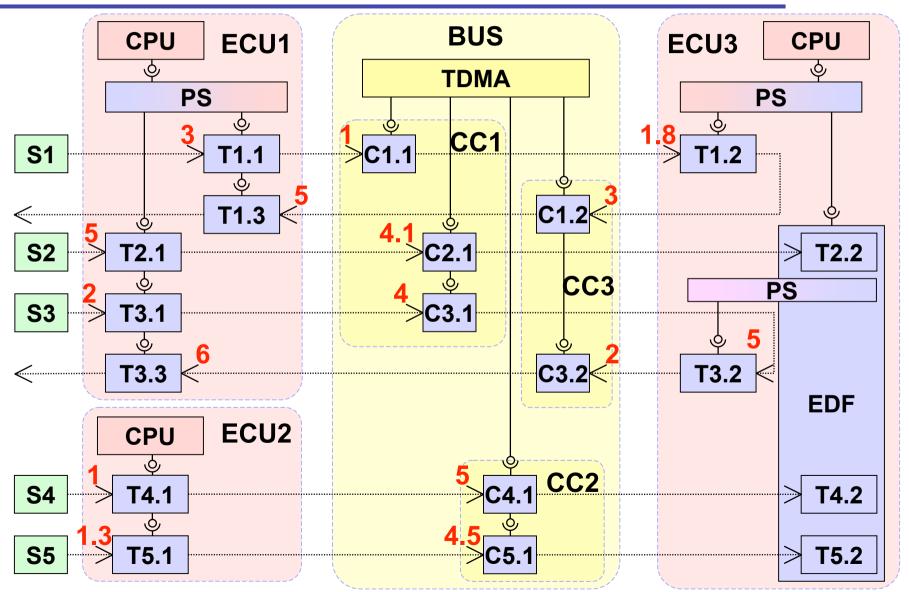
Bus with TDMA

- 4 time slots with different lengths (#1,#3 for CC1, #2 for CC3, #4 for CC3

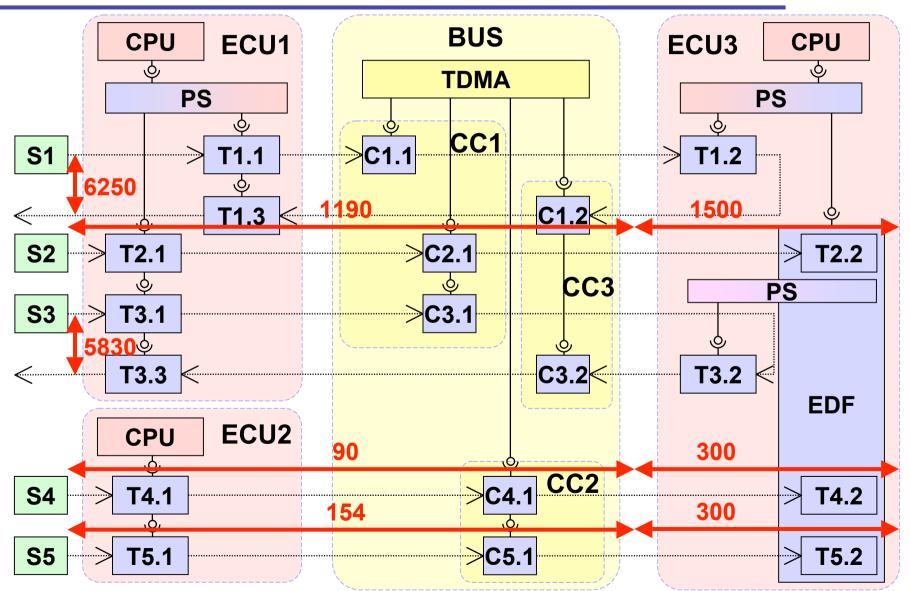
... and its Abstract Component



Buffer Requirements

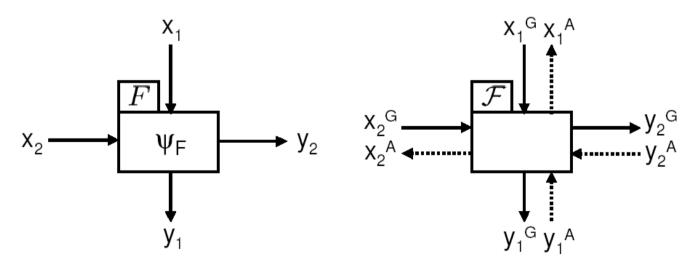


Delay Guarantees



Interface-Based Design

- MPA is suited for interface-based design
 - Stepwise refinement
 - Inverse relations because of min-+ algebra
 - Assume/Guarantee by means of partial order



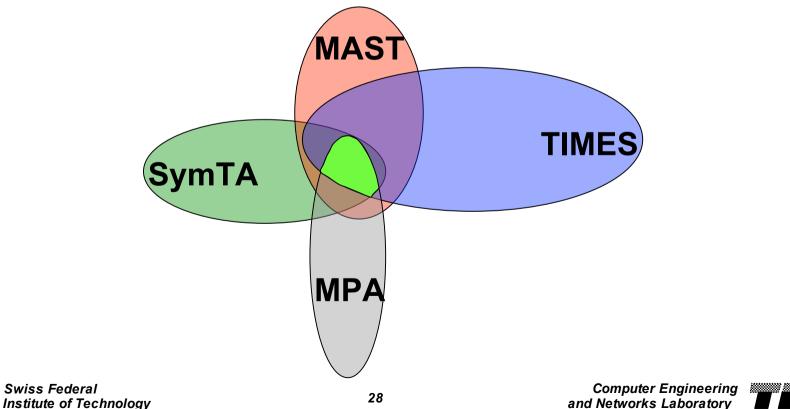




Intention

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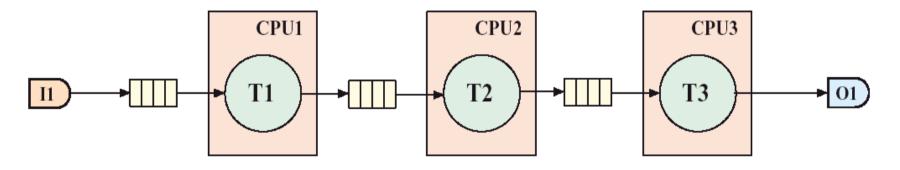




- Pay Burst Only Once
- Cyclic Dependencies
- Variable Feedback
- AND/OR task activation
- Intra-context information
- Workload Correlation
- Data Dependencies

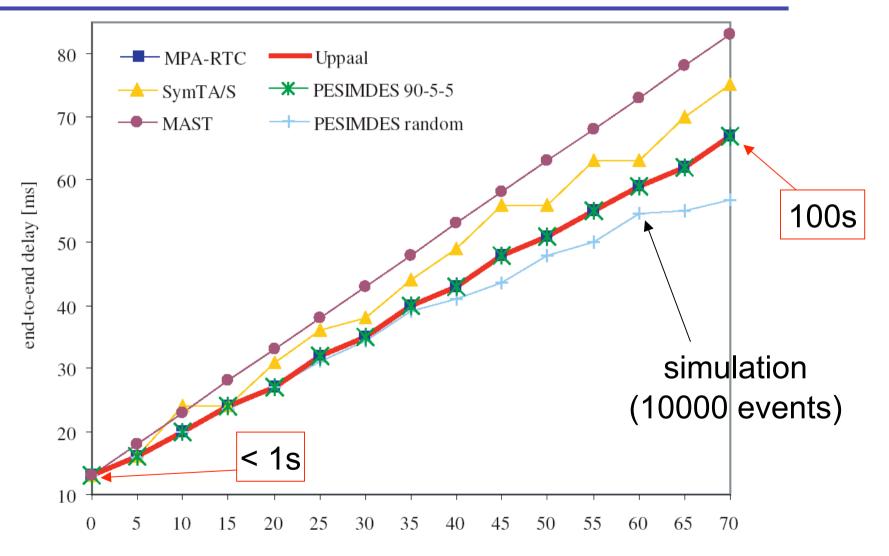


Pay Bursts Only Once



Input stream I1	periodic with burst (P=10ms, J=50ms, d=1ms) \mathbf{k}
Task WCETs	T1: 1ms, T2: 4ms, T3: 8ms
	0 ≤ J ≤ 70ms



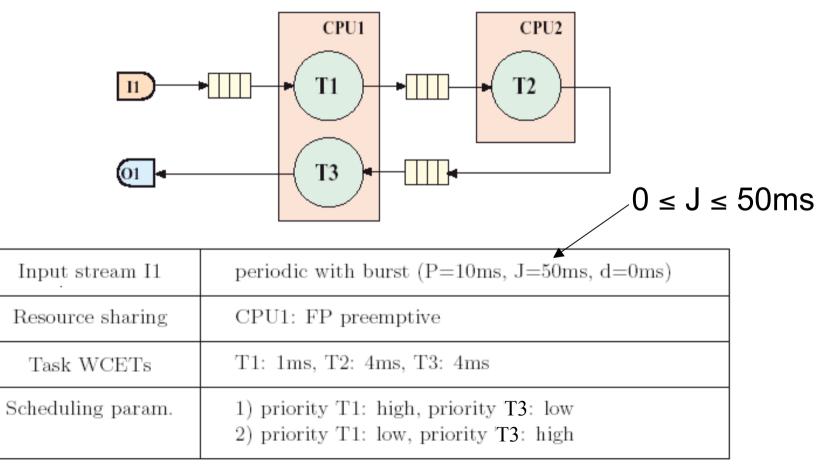




Computer Engineering

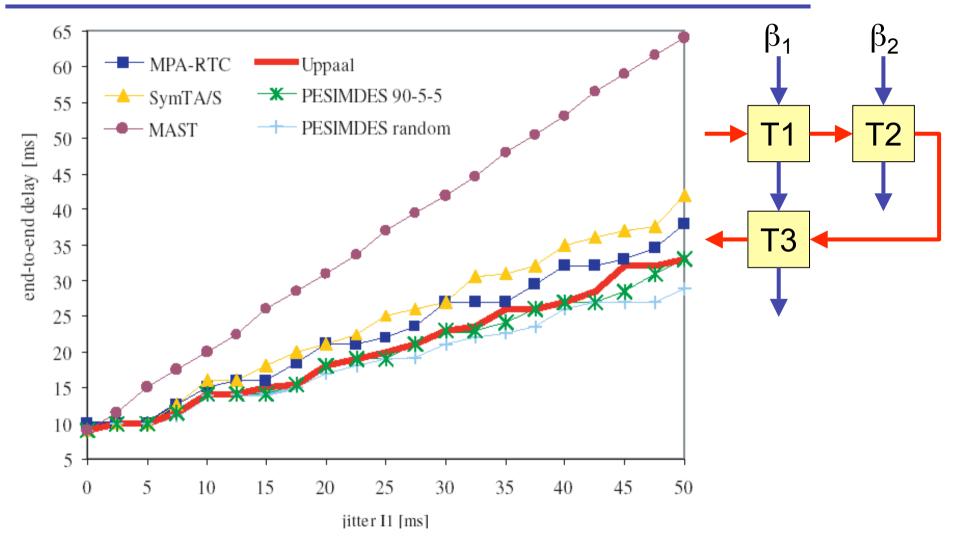


Cyclic Dependencies





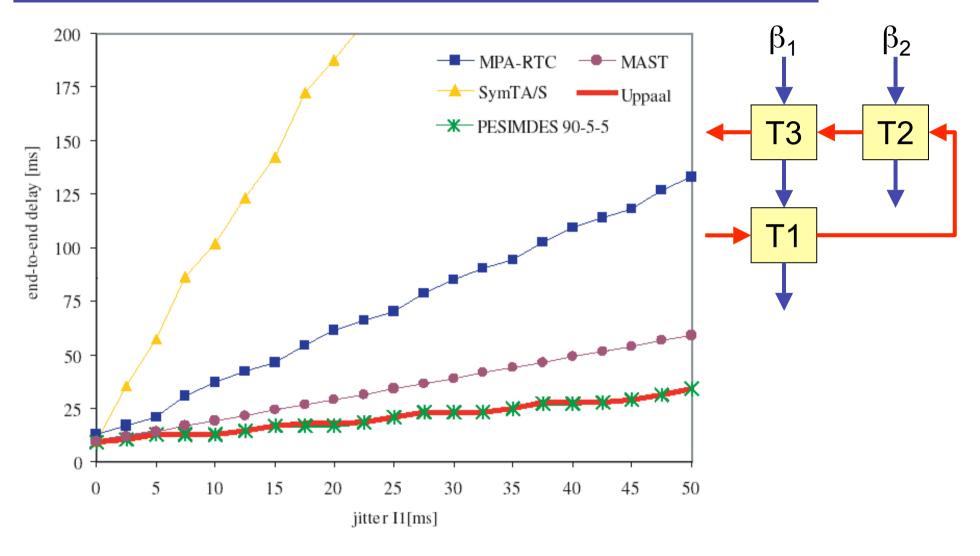
Benchmark 2-1 : T1 high







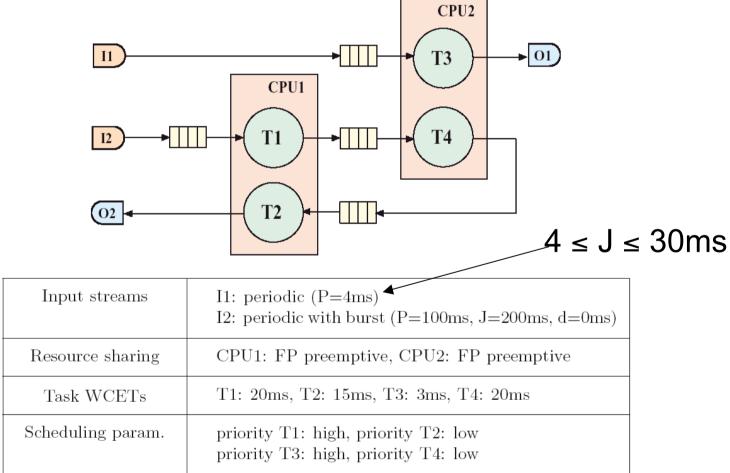
Benchmark 2-2 : T3 high



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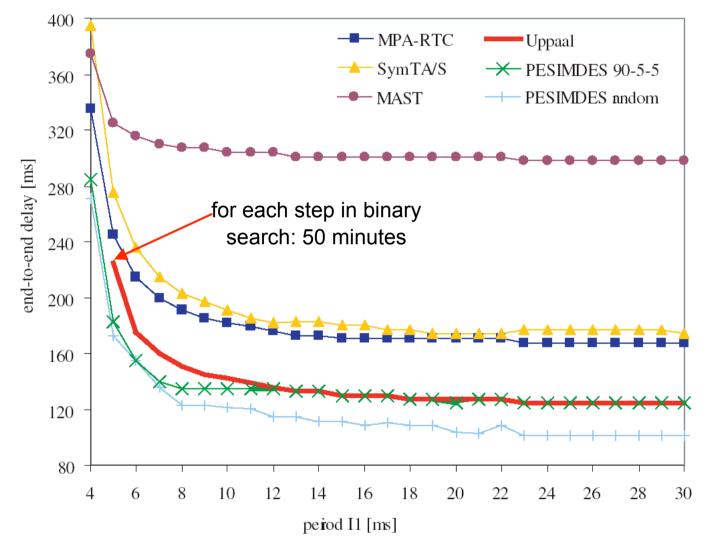


• Variable Feedback





Benchmark 3 : T1 high





(Expected) Results

- Understand the modeling power of different models and the relation between models and analysis accuracy.
- Improve methods by combining ideas and abstractions.
- Not: competition





In models for timed systems abstraction matters

Knowledge about MoCCs that (also) talk about resource usage are far less understood



