QUBE: A Practical Education Program for System LSI Designers

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https://qube.slrc.kyushu-u.ac.jp/
Outline

• QUBE (Q-shu University hardware/software Borderless system design Education program)

• Education Program for
  - SoC Engineers
  - System Designers
  - Hardware (Logic) Engineers
  - Embedded Software Engineers
  - Engineers in industry

• July, 2005 to March, 2010
• QUBE developed in 2005
  - A curriculum for SoC Designers
  - Exercise centric course materials
Motivation

• Difficult to design SoCs considering aspects of:
  - Hardware
  - Software
  - Whole of System
  - Business

• Universities dose not provide lectures to understand whole of system in Japan
  - individual technologies only

• Industries under heavy cost competitions cannot use big budgets for educating engineers

• It is not cost effective to develop course materials which should be improved in each industries or universities

• Technologies are improved very quickly.
Mission

• Educate SoC Designers
  – Hardware Engineers
  – Embedded Software Engineers
  – System (HW/SW codesign) Engineers

• QUBE provides practical classes:
  – invites top professors / industrial engineers of individual technical domain
  – Exercise Centric
QUBE System

- Funded by Ministry of Education, Culture, Sports, Science and Technology, Japan.
- A Curriculum Committee consists of All of Lecturers of QUBE.
- QUBE provides classes according to the curriculum committee's decision.
- QUBE obtains questionnaire from students and lecturers for feedback to the curriculum and classes.
QUBE System

• We have a plan to form a advisory committee
  – The curriculum committee is too big to discuss and revise the curriculum appropriately.
  – The advisory committee consists of someone from industries and someone from universities.
  – To obtain opinions from industries.
Curriculum

System LSI Design Training Program

- long-term class
- Project Based Learning

System LSI Design Course
- System LSI Design Training (2005 - )
- Software Product Lines Training (2006 - )
- Production Chip Evaluation (2006 - )

Advanced Design Technology Program

- Educating deeply professional design technologies
- short-term classes (average 2day)

Hardware Design Technology Course
- noise, power/signal integrity, RF, large-scaled design

Embedded Software Design Technology Course
- development methodologies, test, RTOS, middleware

HW/SW Co-Design Technology Course
- ASIP, C-based design and low-power design

Technology Management Knowledge Course
- intellectual properties, management of technology
SLD:
System LSI Design Training Class

• Motivation
  - Educate System LSI Design knowledge and skills to hardware, embedded software, and co-design engineers
  - Educate practical design and implementation skills

• Originally developed

• Party–Exercise:
  - Leader: HW/SW co-design architects (1 person)
  - hardware engineers (2 or more person)
  - embedded software engineers (2 or more person)
  - engineers who belong to different industry

• HW/SW Co–design:
  - Lectures
  - Tutorials
  - Exercise using processor embedded FPGA board
SLD: Course Plan

- Lecture (1st, 2nd day am)
  - What is System LSI?
  - Basics of HW/SW development
    - basics of hardware design for software engineers
    - basics of software development for hardware engineers
  - System LSI and Costs
  - HW/SW Co–Design
  - Low-power system development
- Tutorials (1st, 2nd day pm)
  - familiarize students with development environment and board
- Exercise (3rd – 8th day)
  - Gives a target system spec and some IPs.
  - A team designs:
    - HW/SW partitioning
    - write documents
  - A team implement a target system according to the documentations.
The Target System of Exercise

Multimedia (Sound & Whiteboard) Phone

Call Target List
1: xxxx-xxxx
2: yyyy-yyyy

Call Target List
1: zzzz-zzzz
2: xxxx-xxxx

Talk by Mic & Speaker

Whiteboard Sharing

Exchanger

Call Target Selection

Q-shu University hardware/software Borderless system design Education program
SLD: Environment

- Terminal Emulator
- RS-232
- PS/2
- Audio I/O
  - AC97 CODEC
  - VGA
- Ethernet hub
- Communication via Ethernet
- Service Discovery & Call Target Selection
- Talk
- White Board Sharing
- Multimedia Phone
- Other
- Xilinx XUP Virtex II Pro Board:
  - PowerPC 405 Core×2 + user logic
- development environment
  - Xilinx ISE & EDK
1st run at 1st – 10th, March 2006

• Students
  – 5 students from industry
    • CO: 1, HW: 2, SW: 2
  – 2 students from university
    • SW: 2, (HW: 1 from staff)

• Course
  – Lecture / Tutorials (2 days)
  – Design (2.5 days)
    • eUML
    • PLUS (Product Lines)
  – Implementation (3 days)
    • implement MMP in software only
  – Presentation (0.5 days)
    • Peer review

• Questionnaire
  – Industry wants system design courses.
  – They wants a course for newcomer (this course too difficult for newcomer)
  – too short to implement whole of system in 8 days
  – Development Methodologies

• Now, we tackles:
  – To develop course materials for beginner
  – To develop a course including development process
Project activities in 2005

- 16 classes (35 days) in 18 weeks
- 40 organizations / 106 registered applicants
- 149 applicants (8.3 per class)
- 80% applicants comes from industrial or research org
- Most of applicants comes from Fukuoka area

# of Applicants of each area
Project activities in 2005

• Most of motivations to take QUBE class is applicants’ wish

• Engineers in industry have motivations to educate themselves
Project activities in 2005

- Students feel good to our classes
- Publicity of the QUBE is not enough
  - But... applicants are registered half of capacity on average (8.3 applicants / class)

How was you satisfied with your prospect?

- 78% (very good + good)
However ...

- Pass ratio: Average: 74% (Non-students 82%, Students 38%)
  - 10% applicants canceled or absent classes due to business accident
  - Not passed: 34 students
    - 22 students attend but not submit their reports + absentee 12 students
  - Why they do not submit reports?
- Level of some classes is too high
  - pass ratio of some class is lower than 50%
  - Some students lack basic knowledge to understand lectures.
  - to improve pass ratio
    - We should show course required levels explicitly.
    - We should provide pre-learning materials in some course.
## Applicants’ Statistics of Classes in 2005

<table>
<thead>
<tr>
<th>Course Description</th>
<th>Total</th>
<th>Age</th>
<th>Passed</th>
<th>Pass Ratio</th>
<th>Questionnaire</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total</td>
<td>149</td>
<td>33.3</td>
<td>98</td>
<td>74%</td>
<td>109</td>
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<tr>
<td>SLD-HW: Hardware Design Training</td>
<td>3</td>
<td>2</td>
<td>2</td>
<td>2%</td>
<td></td>
</tr>
<tr>
<td>SLD-SW: Embedded Software Training</td>
<td>4</td>
<td>30.7</td>
<td>4</td>
<td>100%</td>
<td>3</td>
</tr>
<tr>
<td>SLD-CD: HW/SW Co-Design Training</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>100%</td>
<td></td>
</tr>
<tr>
<td>A-HW1: Noise problems in SoC</td>
<td>9</td>
<td>33.0</td>
<td>4</td>
<td>44%</td>
<td>7</td>
</tr>
<tr>
<td>A-HW2: A/D・D/A Converter in SoC</td>
<td>8</td>
<td>35.3</td>
<td>6</td>
<td>86%</td>
<td>6</td>
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<tr>
<td>A-HW3: EDA Algorithms</td>
<td>3</td>
<td>35.3</td>
<td>3</td>
<td>100%</td>
<td>3</td>
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<tr>
<td>A-HW4: Power/Signal Integrity Problems</td>
<td>14</td>
<td>31.1</td>
<td>7</td>
<td>58%</td>
<td>11</td>
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<tr>
<td>A-HW5: RF Analog Circuit Design for Wireless System</td>
<td>15</td>
<td>32.4</td>
<td>5</td>
<td>36%</td>
<td>9</td>
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<tr>
<td>A-HW6: Test Design for LSI</td>
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<td>29.5</td>
<td>4</td>
<td>100%</td>
<td>4</td>
</tr>
<tr>
<td>A-HW7: Large-Scaled High-Performance System LSI Design</td>
<td>4</td>
<td>30.7</td>
<td>3</td>
<td>100%</td>
<td>3</td>
</tr>
<tr>
<td>A-SW1: Embedded Software Development Methodology</td>
<td>9</td>
<td>32.7</td>
<td>7</td>
<td>78%</td>
<td>6</td>
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<tr>
<td>A-SW2: Software Test Methodology</td>
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<td>31.4</td>
<td>9</td>
<td>90%</td>
<td>7</td>
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<td>A-SW3: Realtime OS and Middleware</td>
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<td>31.8</td>
<td>7</td>
<td>88%</td>
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<tr>
<td>A-CD1: HW/SW Co-Design</td>
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<td>31.4</td>
<td>4</td>
<td>44%</td>
<td>6</td>
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<tr>
<td>A-CD2: LSI Design using C Language</td>
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<td>35.9</td>
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<td>57%</td>
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<tr>
<td>A-CD3: Low-Power Design</td>
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<td>31.1</td>
<td>8</td>
<td>89%</td>
<td>9</td>
</tr>
<tr>
<td>A-MG1: Intellectual Properties in Business</td>
<td>7</td>
<td>35.9</td>
<td>6</td>
<td>86%</td>
<td>6</td>
</tr>
<tr>
<td>A-MG2: Design Process and Management of Technologies</td>
<td>16</td>
<td>40.4</td>
<td>14</td>
<td>100%</td>
<td>12</td>
</tr>
</tbody>
</table>
Sumarry

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Thank you for your attention!