IST-004527 ARTIST2
Network of Excellence
on Embedded Systems Design

Activity Progress Report for Year 3

JPRA-Cluster Integration

Communication-centric Systems

Clusters:

Execution Platforms

Activity Leader:

Prof. Dr. Rolf Ernst (TU Braunschweig)
http://www.ida.ing.tu-bs.de/index.php?id=ernst

The activity assesses the state-of-the-art in models that take into consideration the particularities of various quasi-standard communication protocols during system analysis and scheduling. The communication infrastructure can be optimised in order to be adapted to the particularities of the implemented application. That meets a growing need in industry to consider formal techniques in embedded system design as a complement to traditional prototyping and simulation based approaches.

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1. Overview of the Activity

1.1 ARTIST Participants and Roles

Prof. Lothar Thiele – TIK, ETH Zürich (Switzerland)
Developing a calculus to describe the performance of communication-centric systems, unifying the models for computation and communication.
Prof. Petru Eles – ESLAB, Linköping University (Sweden)
Schedulability analysis for heterogeneous distributed systems, communication synthesis.
Prof. Rolf Ernst – IDA, TU Braunschweig (Germany)
Formal performance models for networks-on-chip.
Prof. Luca Benini – Micrel Lab, University of Bologna (Italy)
Analytic and simulation based models for performance, power and area of NoCs.
Prof. Jan Madsen – Technical University of Denmark (Denmark)
Power issues in network on chip architectures.

1.2 Affiliated Participants and Roles

Dr. Fabian Wolf – Volkswagen AG (Germany)
Software integration under real-time constraints
Dr. Magnus Hellring – Volvo (Sweden)
Requirements analysis
Dr. Kai Richter – Symtavision (Germany)
Performance analysis of complex distributed systems
Prof. Sharon Hu – University of Notre Dame (USA)
Power analysis and optimization

1.3 Starting Date, and Expected Ending Date

Starting date: September 1st, 2004
Ending date: when the different techniques for integration have been successfully combined

1.4 Baseline

Formal communication modelling has been investigated by Zebo Peng and Petru Eles at Linköping University, Lothar Thiele at ETH Zurich (ETHZ) and Rolf Ernst at Braunschweig. The ETH Zurich and Linköping University have outstanding expertise in modelling and analyzing packet flow communication and network processors (ETH) and conditional task graphs combined with statistical modelling. UoB is one of the most widely recognized centres of expertise in NoC design, analysis and road mapping. DTU has a long experience in asynchronous circuits design and in NoC design based on this technology. Embedded architectures and heterogeneous distributed embedded systems have grown to extremely complex computation and communication patterns. New performance models and a corresponding theory are urgently needed Europe needs to develop skills to safely design such systems.

1.5 Problem Tackled in Year 3

One purpose of this activity is to unify different approaches to communication-centric systems and low power design. In the first two years we coupled several tools to extend the analysis scope and accuracy of the individual approaches. In the third year we continued this work by coupling the system level analysis tools MPA and SymTA/S. Since system dependability and flexibility are growing demands in embedded systems, we addressed fault tolerance techniques as well as robustness evaluation and optimization approaches, including multi-core systems. Communication network simulation, such as found on multi-core systems suffers from long simulation times. A new approach compacting reactive behaviour of network clients was developed that drastically reduces simulation time.

The industry increasingly applies hierarchical communication protocols, such as the automotive FlexRay standard. In year three, the modelling scope was extended to cover emerging hierarchical protocols such as FlexRay in the automotive domain. Additionally, bus access optimization techniques for such hierarchical models were proposed.

1.6 Comments From Year 2 Review

1.6.1 Reviewers' Comments

"Generell comments apply"

1.6.2 How These Have Been Addressed

Since no particular comments related to this activity have been given, we have tried to follow the general comments given by the reviewers.

In particular, we have addressed the issue of fault tolerance in complex embedded systems, which was a general issue raised by the reviewers. In year four this aspect will be further strengthened.

2. Summary of Activity Progress

2.1 Previous Work in Year 1

Mixed Performance Analysis in Communication Centric Systems

In a first step, the SymTA/S tool framework that was initially designed to support only the evaluation methods designed at TU Braunschweig was extended with a dynamic library concept, such that different analytical libraries can be loaded into the tool to perform the system-level analysis of embedded systems. In a next step, at ETH Zürich, the formal analysis method Real-Time Calculus was implemented as a Java library that can be used from within the SymTA/S tool. This library was then integrated into the tool and can now be used for performance evaluation.

Hybrid Approach for Performance Analysis of Communication Centric Embedded Systems

After an initial meeting (3 days in Bologna) in March 2004 to discuss the possibilities for a joint effort towards this new approach and exchange the knowledge of the existing performance evaluation methods used, Simon Künzli spent 3 weeks in May 2005 in Bologna for the actual implementation of a case study using such a hybrid approach.
The existing simulation framework was extended by the interfaces needed for the proposed hybrid approach. Further, an example application was analyzed using the new approach. The hybrid analysis can be performed automated and exposes the expected speed-up for the simulation of embedded systems, with only a small deterioration of the accuracy of the results.

Performance Analysis in the System Design Process

In February 2004, Ernesto Wandeler spent 10 days at the ESI. During this time, an appropriate case-study system was identified and analyzed using a formal performance analysis method developed at TIK, ETH Zürich (Real-Time Calculus). Further, Ernesto Wandeler held 3 talks at ESI, to introduce people at ESI to the performance analysis research at TIK. In April 2005,
Marcel Verhoef spent 5 days at ETH. During this time, a journal paper was written, based on a former conference paper. Further, new potential case-study systems, as well as plans for a performance analysis tool were discussed.
As a first case study, an existing distributed in-car radio navigation system was chosen and was specified in UML. For this case study, Real-Time Calculus was used to evaluate and compare 5 different potential system architectures. Sensitivity analysis was applied to all architectures to identify their robustness and potential bottlenecks. For the architecture that is actually used in the commercial implementation of the case study system, the robustness and the bottlenecks could be identified correctly using formal performance analysis methods.

Optimization and analysis of distributed embedded systems

Prof. Eles and his research group, University Linköping, have continued their work in the context of optimization and analysis of distributed embedded systems. They have concentrated on the following issues:

- Analysis of hierarchically scheduled systems
- Timing analysis of distributed task sets communicating through the FlexRay protocol
- Analysis and optimization of distributed embedded systems with fault tolerance requirements

Power analysis and optimization

To initiate the joint activity, Bren Mochocki, University of Notre Dame, spent 2 month at TU Braunschweig. During this time, interfaces between the power analysis tools developed at University of Notre Dame and SymTA/S were created. Based on these interfaces SymTA/S

could be extended with an analysis technique to determine the power consumption of a given embedded system. Since then the power models and the interfaces were regularly extended and refined.

On-chip interconnections for single-chip execution platforms

The work on communication-centric systems by the group of Prof. Madsen, Technical University of Denmark (DTU), has focused on on-chip interconnections for single-chip execution platforms. The starting point for this work has been the development of a clock less NoC architecture (MANGO) and a system-level NoC model based on the multiprocessor simulation environment (ARTS) developed at DTU. The MANGO NoC architecture is based on asynchronous message-passing and provides guaranteed services. Its interface is based on the standard OCP interface protocol which makes the architecture very suited for a modular SoC design flow. The use of a clockless circuit technique has a number of advantages, among which are; inherent global timing closure, low forward latency in pipelines, and zero dynamic idle power consumption. The ARTS modelling framework, which is developed as part of the System Modelling Infrastructure activity of ARTIST2, was extended with capabilities to model interconnect structures. At the system-level, the details of the processing elements and the NoC need to be abstracted in a way that allows for an accurate modelling of the global performance of the system, including the interrelationships among the diverse processors, software processes and physical interfaces and interconnections. To support the designer of single-chip based embedded systems, which includes multi-processor platforms running dedicated RTOS's, with the ability to analyse effects of on-chip interconnect network, the ARTS framework was required to support the analysis of network performance under different traffic and load conditions. This was achieved by extending the model with capabilities for NoC modelling.

Highly scalable communication architectures

The design objective was to develop a NoC targeting heterogeneous systems and featuring support for customizable, domain-specific NoC realizations. This implies designing Xpipes network building blocks as soft cores and to arbitrarily instantiate these blocks so to obtain custom-tailored irregular topologies. All Xpipes components were modelled in SystemC at the cycle accurate level, and integrated in an overall system simulation environment. Network interface was designed with the objective to allow frequency decoupling and efficient protocol conversion between system cores domain and network domain. Moreover, a standard OCP interface protocol with the cores was implemented to increase portability across different platforms. Links design was characterized by the concern to avoid limiting effects of signal propagation time on overall system clock period. This was achieved by providing support for link pipelining and latency-insensitive design. Finally, switch modules design followed the following guidelines: latency minimization, minimum impact of routing logic, output buffering to avoid head-of-line blocking, and initial support for best-effort traffic only. Parameters that can be set at design time include number of switch input/output ports, buffer sizing, flit width, over clocking factor, etc.

High level modelling of system interconnects

High level models for system interconnects were at first derived for state-of-the-art busses, validated on a virtual platform and potentials for their deployment were explored. In particular, cooperation with Linköping University paved the way for exploring different high level models for shared communication resources and for exploiting them within theoretical frameworks for efficient allocation, mapping and scheduling of tasks onto MPSoC hardware platforms.
Specifically, we identified two modelling approaches to on-chip communication (additive models and coarse-grain modelling of communication tasks) and addressed the issue of modelling implicit communication in a predictive way (cache misses, semaphore polling). Then, we developed the theoretical framework taking the Benders Decomposition approach: an

Integer Programming model to assign tasks to computation and storage resources and a Constraint Programming model to schedule tasks onto processors. Non-feasible schedules generate a no-good for the IP problem, which is then re-iterated. The procedure is proved to converge to the optimum.

Hybrid system-level performance analysis approach
High level bus models can also be used for performance estimation. However, it is well known that formal models by themselves may turn out to be inaccurate for exploring the performance of complex multi-processor systems, because abstractions might fail to capture the system behaviour. Similarly, accurate simulation of the entire system might turn out to be infeasible due to the long simulation times. Therefore, we set up cooperation with ETH Zürich with the objective to assess the efficiency of a hybrid approach: combining simulation and formal methods for system-level performance analysis. This approach enables a faster validation of the whole system in that we can decide to model a subcomponent of which the behaviour is well known through a formal analysis, whereas we can have a detailed low level and timeconsuming simulation component modelling for other components. We described how the simulation models can be coupled with the formal analysis framework and showed the applicability of the approach using case studies.

2.2 Previous Work in Year 2

Timing Analysis of the Flexray Protocol
In the second year the Linköping group has continued the work regarding analysis and optimization of distributed embedded real-time systems, with application in automotive electronics. The main goal is to develop models and tools for the analysis and optimization of such communication-intensive systems. Emphasis is placed on the analysis of timing properties, considering the heterogeneous nature of such systems and the particularities of the various communication protocols. In the most recent research the analysis of mixed static/dynamic protocols, such as FlexRay, have been performed [PPE+06].
FlexRay is likely to become a standard for certain automotive applications and the elaboration of the first timing analysis approach for distributed systems built on FlexRay is of importance for our industrial partners. On top of these timing analysis approaches, various system-level optimization tools have been built, performing application mapping, communication synthesis, priority assignment, etc. The Linköping group has closely collaborated with our industrial partners at Volvo as well as with the Braunschweig group. The developed analysis approaches are under integration in the Symta/S environment developed at Braunschweig.

Fault Tolerance
One other issue that has been explored by the Linköping group, in the same context of distributed communication-intensive real-time systems, is that of fault tolerance and, in particular, the issue of transient faults. There are two main aspects of interest here:
(1) Analysis of timing properties in the presence of faults and possible guarantees regarding worst case behaviour
(2) System optimization, such that timing and fault tolerance requirements are satisfied given a certain, limited amount of resources.
An approach for scheduling and worst case analysis with fault tolerance has been developed [IPE+06]. On top of this analysis approach, an optimization technique for task mapping and fault tolerance policy assignment has been elaborated and implemented.

Combination of performance analysis methods: SymTA/S and MPA
This new collaboration is based on collaborations between the two institutions from previous years, where we tried to identify the similarities and differences of the performance evaluation

methods developed (a) at TU Braunschweig integrated in the SymTA/S tool, and (b) at ETH Zurich implemented as toolbox for modular performance analysis (MPA). With this analysis of the weaknesses and strengths of the various methods in mind, we believe that a combination of the methods leads to a significant improvement of analysis results. Especially for systems in which not all parts of the system can be analysed using a single technique due to limitations of the methods, we see the possibility to apply a combined approach which leads to good analysis results. After the analysis of the individual techniques, we are now looking at a common basic for such a combination, and analyse the implementation effort needed for a tool that supports both analysis techniques. The plan for the next months is to implement the changes needed for a combination and analyse an example application to show the strength of the new approach. These steps should also result into a joint publication of the results.
To achieve this, we intend to (1) apply the changes in the tools at each of the partner's sites, (2) organise an integration week where the two parts should be combined to form a single tool, (3) perform the analysis of an example system.

Performance Analysis of an In-Car Radio Navigation System
In this activity, we investigated an in-car radio navigation system that was specified in UML. Modular Performance Analysis with Real-Time Calculus was used to evaluate and compare 5 different potential system architectures, and sensitivity analysis was applied to all architectures to identify their robustness and potential bottlenecks. For the architecture that is actually used in the commercial implementation of the case study system, the robustness and the bottlenecks could be identified correctly using the above methods. First results on this research were published at the First International Symposium on Leveraging Applications of Formal Methods [WTVL06]. After this symposium, we refined the analysis of the case study system.
Based on the case study system, we also compared a number of different performance analysis and simulation methods. Currently, a hardware test bed is implemented to compare the analysis results with measured results in different system architectures.
The results of the refined analysis, together with a thorough description of the applied analysis methods were published this year in a journal article [WTVL06]. The results of the analysis methods comparison and of the comparison to the measurements will be published in a future joint publication.

Sureal-Project: Hierarchical Event Models
The main goal of the Sureal Project is to define an integrated development process for distributed embedded real-time Systems, especially regarding real-time aspect in all phases of the development. This includes the integration of different techniques for describing, analyzing and modelling real-time aspects. To be able to use different tools specialized in handling realtime aspects in different phases of the system development interfaces must be defined for them to efficiently work together.
Also the early prediction of the timing behaviour, the sensitivity and optimizing possibilities of the architecture play a very important role in such an integrated development process. The tool SymTA/S is capable of analysing such aspects but the underlying methods still have some limitations regarding specific system setups. Up to date, only task sets, which consist of tasks that are activated according to a standard event model can be analysed appropriately. To lift this limitation, first steps towards exploring hierarchical event models are taken. Future Results will be integrated into SymTA/S to further enhance its applicability.

Power Optimization under Timing Constraints
Based on the power analysis extension to SymTA/S which was realized in cooperation with Bren Mochocki during the first project year, TU Braunschweig and University of Notre Dame implemented heuristic and stochastic power optimization algorithms using DVS and SVS (Dynamic/Static Voltage Scaling). The presented algorithms are applicable to complex distributed systems with complex timing constraints (maximum jitter, end-to-end deadlines,

etc.), and are capable of determining Pareto-optimal design trade-offs between system power consumption and timing properties.
The heuristic power optimization approach is based on research of TU Braunschweig related to sensitivity analysis [RHE06], whereas the stochastic algorithms utilize the compositional SymTA/S design space exploration framework [HRJ+06].
The results of this activity lead to a joint publication at the International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES) [RHE+06].

Robustness Optimization for Distributed Embedded Systems
Based on the results achieved in the domain of sensitivity analysis [RHE06], TU Braunschweig developed techniques for optimizing the robustness of embedded real-time systems with respect to variations of system properties like worst-case execution/communication times, bus bandwidth, CPU clock rate, input data rate, etc. Reasons for such variation during the design process or in the field include updates, bug fixes, late feature requests, and product variants.
The developed algorithms consider hard-real time constraints and are capable of optimizing a given system for static and dynamic design robustness. Thereby, the static design robustness optimization approach is applicable to the design scenario where system parameters are fixed early in the design process, whereas dynamic design robustness optimization approach includes possible counteractions to unforeseen system property changes, and is thus applicable to reconfigurable systems.
The results of this research will be published at the International Conference on Hardware - Software Codesign and System Synthesis 2006 (CODES) [HRE06].

Flex Film: High-resolution Real-time Digital Film Applications
In the context of the FlexFilm project, TU Braunschweig developed a multi-board, multi-FPGA hardware/software architecture, for computation intensive, high resolution (2048x2048 pixels), real-time (24 frames per second) digital film processing. The architecture reaches record performance running a complex noise reduction algorithm (used both as example and proof of concept) including a 2.5 dimensions DWT and a full 16x16 motion estimation at 24 fps requiring a total of 203 Gops/s net computing performance and a total of 28 Gbit/s DDRSDRAM frame memory bandwidth. This design was awarded with the "DATE2006 Design Record" distinction [LHR+06].

Simulation-based analysis of SoC interconnection architectures
Industrial MPSoC platforms exhibit increasing communication needs while not yet reverting to revolutionary solutions such as networks-on-chip. The limited scalability of shared busses is being overcome by means of multi-layer communication architectures.
However, the complex interaction among system components and the dependency of macroscopic performance metrics on fine-grain protocol features stress the importance of highly accurate modelling and analysis tools. The work in this area has focused on developing accurate functional model of multi-node on-chip interconnects, as they are currently deployed in high-complexity SoCs today.

Network-on-chip architectures
In the second year the group at the Technical University of Denmark has further developed the NoC architecture called MANGO (*Message-passing Asynchronous Network-on-Chip providing Guaranteed services over OCP interfaces*). In particular the network core, i.e. the routers and links. MANGO is based on clockless circuit techniques, and thus inherently supports a GALS (*Globally Asynchronous Locally Synchronous*) type design flow. This is an advantage in large scale SoC design, since the distribution of a global clock is becomming increasingly difficult.
MANGO employs virtual channels to provide connection-less best-effort routing as well as connection-oriented virtual circuits, for which service guarantees can be given. The

predictability of guaranteed services is a way to promote system-level integrity. The MANGO architecture has been demonstrated through a circuit-level design of a 5x5 router using a 0.13 µm CMOS standard cell library from STMicroelectronics. Netlist simulations showed a performance of 650 Mflits/s under typical timing conditions [BS06]. Three patents [BS05] on the MANGO technology have been filed and a startup company, called Teklatech (www.teklatech.com), was formed as a spin-off from this research. Teklatech is developing a one-step EDA solution to achieving timing closure in large scale, globally synchronous, deep submicron ASIC designs.

Distributed wireless sensor networks
Besides the further development for extending the capabilities of the ARTS system-level modelling framework towards the modelling of wireless sensor networks (reported under the System Modelling Infrastructure action), a sensor node development platform [VLMB05] has been developed, implemented and build. The aim of the platform is to explore hardware/software tradeoffs when designing the node behavior and to calibrate the developed system-level models with real design implementations. In order to efficiently utilize the limited resources available on a sensor node, key design parameters needs to be optimized which is only possible by making system-level design decisions about its hardware and software (operating system and applications) architecture.

Simulation-based analysis of SoC interconnection traffic
In Multi-Processor System-on-Chip (MPSoC) design stages, accurate modeling of IP behavior is crucial to analyze interconnect effectiveness. However, parallel development of components may cause IP core models to be still unavailable when tuning communication performance.
Traditionally, synthetic traffic generators have been used to overcome such an issue. However, target applications increasingly present non-trivial execution flows and synchronization patterns, especially in presence of underlying operating systems and when exploiting interrupt facilities. This property makes it very difficult to generate realistic test traffic. Technical
University of Denmark and University of Bologna have jointly developed a reactive traffic generator device [MAMBS05] capable of correctly replicating complex software behaviours in the MPSoC design phase. The approach has been validated by showing cycle-accurate reproduction of a previously traced application flow. Even when tested under complex synchronization scenarios, including asynchronous interrupts involving OS interaction in a multiprocessor environment, the proposed traffic generator is able to reproduce IP traffic with full capability to express the application flow.

2.3 Current Results

2.3.1 Technical Achievements

Comparison of different performance analysis approaches (ETH Zurich)
ETHZ has been leading a major effort in comparing the modeling scope and accuracy of various performance analysis methods: MAST (Univ. Cantabria), Symta/S (TU Braunschweig), Timed Automata and Modular Performance Analysis (ETH Zurich). The results are based on a set of benchmarks that have been determined in a Workshop at Leiden, organized by ETH Zurich. The comparison showed interesting results that will be the basis for future work in this activity. In addition, a joined publication at EMSOFT 2007 [PWT+07] will describe the obtained results in detail. The results have been also presented at various occasions (Workshop on Models of Computation in Zurich, Seminar at EPF Lausanne).
http://www.tik.ee.ethz.ch/~leiden05/index2.html

Mixed performance analysis using MPA and SymTA/S (ETH Zurich, TU Braunschweig)

There has been an intensive cooperation between TU Braunschweit and ETH Zurich in terms of coupling their respective frameworks for performance analysis (Symta/S and MPA). As a result, one can now mix different model paradigms in a single analysis run and therefore, exploit the different modeling scopes and accuracies. The cooperation has led to a joint publication at CODES 2007 [KHE+07].

Advanced formal analysis features based on evolutionary search strategies (ETH Zurich, TU Braunschweig)

The PISA multi-objective framework from ETH Zurich has been successfully applied to a new system analysis methodology developed at TU Braunschweig: robustness optimization [HRE07a, HRE07b] and system sensitivity analysis [RHE06].

Analysis and optimization of communication-intensive systems (University of Linköping, DTU)

University of Linköping and DTU have continued the work regarding analysis and optimization of distributed embedded real-time systems, with application in automotive electronics. The main goal is to develop models and tools for the analysis and optimization of such communication-intensive systems. Emphasis is placed on the analysis of timing properties, considering the heterogeneous nature of such systems and the particularities of the various communication protocols.
In the most recent research the Technical University of Denmark (DTU) and Linkoeping University (LiU) have proposed an approach to the timing analysis of applications communicating over a FlexRay bus [PPE+06], taking into consideration the specific aspects of this protocol, including the dynamic segment. More exactly, they have proposed techniques for determining the timing properties of messages transmitted in the static and the dynamic segments of a FlexRay communication cycle. The analysis techniques for messages are integrated in the context of a holistic schedulability analysis algorithm that computes the worst-case response times of all the tasks and messages in the system.
This was the first step towards enabling the use of this protocol in a systematic way for time critical applications. As a second step, DTU and University of Linköping have proposed an optimization approach for determining a FlexRay bus configuration which is adapted to the particular features of an application and guarantees that all time constraints are satisfied [PPE+07b]. Heuristics for solving the bus access optimization problem with FlexRay have been proposed as part of this research. While the optimization techniques proposed by us can also be applied to other heterogeneous distributed applications, solving the particular problem of analysis and optimization of FlexRay-based systems is, today, of particular importance for the automotive industry.

Fault tolerance under energy constraints (University of Linköping, DTU)

One other issue that has been explored by the Linköping group, in cooperation with the group at DTU, is that of fault tolerance and, in particular, the issue of transient faults. During the last year, efforts were concentrated on achieving a certain, required degree of fault tolerance with minimal energy consumption [PPI+07].

Analysis of shared memory accesses in MPSoC architectures (University of Linköping)

The Linkoping group has investigated the impact of memory access over shared buses on the global predictability of real-time systems implemented on multiprocessor SoC architectures.

We have elaborated an approach [RAE+07] to system level scheduling and bus access which provides predictable implementations in the context of potential bus conflicts. Bus traffic taken into consideration is not only that for inter-task communication but also that caused by regular memory access in the case of cache misses. The basic WCET analysis used as part of the proposed systems is based on the Symta/P tool from Braunschweig.

Network-on-chip architectures (DTU)

The Technical University of Denmark (DTU) has continued its research in Network on Chip architectures as described in the following. Work on the MANGO NoC (reported in last year) has addressed the design of the network adapters [BS06b]. One of the experiences from the MANGO NoC is that circuit complexity and power consumption can be quite large. From related work on NoC architectures, it is clear that this is generally the case. For this reason DTU have been studying more "leight-weight" NoC architectures as well as more efficient clock-distribution methods [SBS06], [BSS07]. Finally work has been started on: (1) automatically generating efficient NOC topologies, (2) programming models for NoC-based systems, and (3) combining circuit switching and packet switching in reconfigurable NoC structures.

Simulation-based analysis of SoC interconnection traffic (DTU, University of Bologna)

The Technical University of Denmark and University of Bologna have completed their joint development of a reactive traffic generator device through 3 additional joint publications [MAS07a], [MAS07b], and [MAS07c]. The reactive traffic generator is capable of correctly replicating complex software behaviours in the MPSoC design phase. The developed approach has been validated by showing cycle-accurate reproduction of a previously traced application flow. Even when tested under complex synchronization scenarios, including asynchronous interrupts involving OS interaction in a multiprocessor environment, the proposed traffic generator is able to reproduce IP traffic with full capability to express the application flow.

Fault tolerance and robustness of autonomous systems (TU Braunschweig)

The AIS project ('Autonomous Integrated Systems') is a research cooperation involving several universities. The aim is to research new system design methodologies which enable MpSoCs to realize autonomous behaviour in case of faults and modifications in the environment. This includes self-healing and self-configuration properties on hardware layer due to specially designed components as well as on software layer. The measures on software layer range from an offline design space exploration at early design stages to the adoption of an autonomous operating system, which supports dynamic reconfiguration mechanism at runtime. Our main research interest focuses on the determination of the performance of such systems under real-time conditions. Therefore we consider two generally different types of failures. Transient errors have a bounded duration, and they are countered usually with one-time actions. Examples of transient errors are single event upsets or timing failures due to the difficulty of accurate prediction of transistor behaviour. In contrast permanent errors have a potentially unbounded duration, and mostly they affect complete function units or processors. A defect during manufacturing process causing a processor breakdown as well as a permanent performance reduction due to heat fluctuations are exemplary situations for permanent errors. We implemented algorithms to capture the consequences of this kind of failures and to explore several countermeasures. In this context we developed an approach to analyse the sensitivity of system against performance fluctuations up to complete processor breakdowns. Furthermore possible task migrations have been explored to make the system more robust against errors by remapping functionality within the system in error case. Currently, the system

properties during the occurrence of transient errors are investigated, including a derivation of deadline miss probabilities. All analysis algorithms are based on the SymTA/S tool for performance analysis in complex real-time systems.
http://www.edacentrum.de/ais

Online performance analysis of distributed embedded systems (TU Braunschweig)

In order to perform online performance analysis in distributed embedded real-time systems, we implemented a framework for distributed analysis of a formal system model [SHE06a, SHE06b]. We based our work on the compositional performance verification approach of Richter et al. as implemented in the tool SymTA/S. A prototype implementation extending the tool has already been tested.
Online Performance control is achieved by using this framework to continuously evaluate the current state an embedded system. For this, applications entering the system must enter a service contract, stating the computational and communication needs, which are integrated in the current system model. If the resulting system does not violate any constraints, the new application can be accepted into the system. Watchdogs will ensure that no application breaks its service contract. At this time, the concept has been finalized and a prototype has been implemented on a standard PC running parallel processes.
The framework will also be used for optimization of the current system configuration. Heuristic optimization algorithms can perform what-if analyses to continously improve i.e. the robustness of the system. Similar strategies can be applied to deal with faulty hardware, such as degrading processors or if applications break their service contract in order to remain in a feasable system state.

Integrated development process for distributed embedded systems (TU Braunschweig)

Within the SuReal Project, the sureal-process model was defined, which describes the different steps that have to be undertaken for an integrated development process for embedded real-time systems, taking real-time aspects into account. More importantly, it associates the different steps with the different tools defining the interfaces that must be established between them. For the system level timing analysis tool SymTA/S, two interfaces were defined: one between SymTA/S and the UML-tool Ameos from Scopeset and another between SymTA/S and the execution time analyser aiT from AbsInt. The interface between SymTA/S and aiT has already been prototypically implemented using an XML based exchange format. This interface enables SymTA/S to request the execution times of tasks from aiT and incorporate the obtained analysis results from aiT directly into SymTA/S.

Effect of COM-Layers on the communication timing (TU Braunschweig)

In order consider the effects modern COM-Layers have on the communication timing it is necessary to appropriately capture the event stream hierarchies which arise, e.g. when several signals are packed in the same packet. Therefore hierarchical event models, representing these hierarchies, were defined. They not only enable a more accurate description of the timing of the packets transporting the signals, but they also conserve the models describing the inner event streams. This in turn permits to unpack the inner event streams on the receiving side, which can significantly reduce overestimation compared to using non hierarchical event models, e.g. standard event models.

High Speed DDR-SDRAM Memory Controller for the MORPHEUS platform (TU Braunschweig)

Applications designed for the MORPHEUS platform may require a massive amount of memory, as well as sufficient bandwidth, to fully demonstrate MORPHEUS's potential as a high-performance reconfigurable architecture. For example, the film grain noise reduction application requires massive amounts of bandwidth due to its real-time requirements. To meet these constraints and to eliminate external memory bottlenecks, a high-bandwidth DDR-SDRAM memory controller has been designed for use with the MORPHEUS platform. Using a bandwidth-optimizing two-stage buffered access scheduler, bank interleaving and request bundling, the controller achieves read and write throughput levels up to 2 GiB/s.

Real-time Digital Film Noise Reduction (TU Braunschweig)

A real-time film grain noise reduction algorithm, originally developed for the FlexFilm project to process digital film in real time, has been chosen as an appropriate algorithm to be implemented on the MORPHEUS platform. Film grain reduction is actually itself a combination of different image processing algorithms or tasks, each with massive memory bandwidth requirements.
The following two-phase approach was chosen for implementation. In Phase 1, the film grain noise reduction has been implemented on an existing reconfigurable platform board based on several state of the art FPGAs (FlexFilm board) to closely match the future implementation for the MORPHEUS SoC. Rough estimates show that real time implementation will only be possible for a frame format of about 2 KiPixels x 1.5 KiPixels, which is a widely used digital film format. In Phase 2, which begins in the coming months, the full scale film grain application will be implemented on the MORPHEUS SoC.

2.3.2 Individual Publications Resulting from these Achievements

TU Braunschweig (TUBS)

[RHE06] Razvan Racu, Arne Hamann, Rolf Ernst, A Formal Approach to Multi-Dimensional Sensitivity Analysis of Embedded Real-Time Systems. In Proc. of the 18th Euromicro Conference on Real-Time Systems (ECRTS), Dresden, Germany, July 2006

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2.3.3 Interaction and Building Excellence between Partners

TU Braunschweig – ETHZ:

- Model and tool integration between MPA from ETHZ and SymTa/S from TU Braunschweig. The results are published in 1 joint paper [KHE+07]
- Application of the PISA framework of ETHZ for the development of sensitivity and robustness optimization techniques at TU Braunschweig. The results are published in 3 individual publications by TU Braunschweig [RHE06, HRE07a, HRE07b].
- TU Braunschweig participated in the initiative of ETHZ with the aim to evaluate and compare different performance analysis methods. The results were published in 1 joint paper [PWT+07]

University Linköping – DTU:

- University of Linköping and DTU cooperated to develop analysis and optimization techniques for hierarchically scheduled multi-processor systems. Thereby, in particular the Flexray communication protocol was considered. The results were published in 2 joint papers [PPE+07, PPE+07b].
- University of Linköping and DTU developed techniques to ensure fault tolerance in energy constrained embedded systems. The results were published in 1 joint paper [PPI+07].

DTU – University of Bologna

- In a joint effort, DTU and University of Bologna developed a reactive traffic generator device. The results are published in 3 joint publications [MAS07a], [MAS07b], and [MAS07c].

2.3.4 Joint Publications Resulting from these Achievements

[PWT+07] S. Perathoner, E. Wandeler, L. Thiele, A. Hamann, S. Schliecker, R. Henia, R. Racu, R. Ernst, M. González Harbour. Influence of Different System Abstractions on the Performance Analysis of Distributed Real-Time Systems. In Proc. of the ACM Conference on Embedded Systems Software (EMSOFT), Salzburg, Austria, October, 2007.

[KHE+07] Simon Künzli, Arne Hamann, Rolf Ernst, Lothar Thiele. Combined Approach to System Level Performance Analysis of Embedded Systems. In Proc. of the IEEE Conference on Hardware/Software Codesign and System Sythesis (CODES/ISSS), Salzburg, Austria, 2007.

[PPE+07] Traian Pop, Paul Pop, Petru Eles, Zebo Peng. Analysis and Optimisation of Hierarchically Scheduled Multiprocessor Embedded Systems, Intl. Journal of Parallel Programming, 2007 (to be published).

[PPI+07] Kare Poulsen, Paul Pop, Viacheslav Izosimov, Petru Eles. Scheduling and Voltage Scaling for Energy/Reliability Trade-offs in Fault-Tolerant Time-Triggered Embedded Systems, Intl. Conf. on Hardware/Software Codesign and System Synthesis (CODES+ISSS), Salzburg, 2007.

[PPE+07b] Traian Pop, Paul Pop, Petru Eles, Zebo Peng. Bus Access Optimisation for FlexRay-based Distributed Embedded Systems, Design, Automation, and Test in Europe Conference (DATE'07), Nice, France, April 2007.

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[MAS07c] S. Mahadevan, F. Angiolini, J. Sparsø, M. Storgaard, J. Madsen, A Network Traffic Generator Model for Fast Network-on-Chip Simulation. In R. Lauwereins, J. Madsen, editors, *Design, Automation, and Test in Europe: The Most Influential Papers of 10 Years DATE*. Springer, 2007

2.3.5 Keynotes, Workshops, Tutorials

Workshop: Models of Computation and Communication
Zurich, Switzerland – November 16-17, 2006
A Workshop Models of Computation and Communication has been taken place at ETH Zurich November 16th and 17th 2006. It brought together scientists from various areas, i.e. formal methods, hardware design and software architecture, see http://www.artist-embedded.org/artist/MoCC-06.html.

Workshop and Tutorial: Computing Architectures and SW Tools for Numerical Embedded Scalable Systems
Rom, Italy – January 15-17, 2007
ETH Zurich has been organizing and participating in the CASTNESS Workshop. The workhop put together the expertise of various EU projects such as ARTIST2, SHAPES, AETHER. In addition, ETH Zurich has been given a tutorial on issues that have been investigated in the ARTIST2 context: Analytic Performance Estimation, Mapping Algorithms to Architectures,

Scalable SW Construction. The workshop has been sponsored by ARTIST2 and took place 15.-17th of January 2007.
www.casteness.org

Tutorial: Advanced Digital System Design
Lausanne, Switzerland – September 25-29, 2006
Two members of the cluster on Execution Platforms have been given part of a summer school advanced course on ADVANCED DIGITAL SYSTEMS DESIGN on 25.-29th September, Lausanne, Switzerland. The participants are from industry and university. This way, results from the integrated view of embedded system design will be brought to a much larger community.

Workshop and Tutorial: Foundations and Applications of Component-based Design
Embedded Systems Week (ESWEEK)
Seoul, Korea – October 26, 2006
ETH Zurich has been organizing a Workshop at a major conference in the area of Embedded Software (EMSOFT): „Foundations and Applications of Component-based Design“, October 26th 2006, Seoul. The workshop has been organized in the framework of the Embedded Systems Week, which federates CODES/ISSS, EmSoft, and CASES.
http://www.esweek.org/

Seminar: Quantitative Apects of Embedded Systems
Schloss Dagstuhl, Germany – March 4-9, 2007
ETH Zurich has been organizing the Dagstuhl seminar: „Quantitative Aspects of Embedded Systems“. The purpose was to connect the results on performance analysis in ARTIST2 with the community dealing with statistical and stochastic methods. Therefore, organizers of this workshop have been B. Haverkort (Univ. of Twente, NL), J.-P. Katoen (RWTH Aachen, DE), L. Thiele (ETH Zürich, CH).
http://kathrin.dagstuhl.de/07101/.

Conference: Architecture of Computing Systems (ARCS) 2007
ETH Zurch, Switzerland – March 12-15, 2007
ETH Zurich has been the general chair of the ARTIST2-sponsored conference ARCS'07: „Architecture of Computing Systems“, that took place at the Swiss Federal Institute of Technology (ETH) Zurich, Switzerland, March 12-15, 2007. Here, a broad audience was present which allowed disseminating results on embedded system design methods to a larger community.
http://arcs07.ethz.ch/

Tutorial: Analysis and Optimization of Real-Time Distributed Embedded Systems
International Workshop on Embedded Systems
Seoul, Korea – October, 2006
Petru Eles has given a tutorial at the “International Workshop on Embedded Systems", Seoul October 2006. With this occasion several results obtained in the ARTIST context have been made accessible to an international audience.

Tutorial: Extensible Frameworks for System-Level Analysis of Real-Time Systems
Real-Time and Embedded Technology and Applications Symposium (RTAS)
San Jose, USA – April 4, 2006
TU Braunschweig has organized together with ETH Zürich and University of Notre Dame the tutorial "Extensible Frameworks for System-Level Analysis of Real-Time Systems" at the Real-

Time and Embedded Technology and Applications Symposium (RTAS). The tutorial took place April 4, 2006.

Worshop: Models and Analysis for Automotive Systems
Real-Time Systems Symposium (RTSS)
Rio de Janeiro, Brasil – December 5, 2006
TU Braunschweig participated in the "Workshop on Models and Analysis for Automotive Systems" at the Real-Time Systems Symposium (RTSS). The talk was named and discusses "The Need of a Timing Model for the AUTOSAR Software Standard". The workshop took place December 5, 2006.

Conference: Design Automation and Test in Europe (DATE) 2007
Nice, France – April 16-20, 2007
TU Braunschweig has been organizing the Embedded Software Track at the major European conference on design automation DATE (Design Automation and Test in Europe) that took place April 16-20, 2007. The track was devoted to modelling, analysis, design and deployment of embedded software, including formal methods, tools, methodologies and development environments. Thereby, the emphasis was on embedded software platforms, software integration and portability issues.

Tutorial: Supporting Predictable Design Using Formal Analysis Techniques
Näsślingen, Sweden– August 23, 2006
TU Braunschweig has given a lecture with the title "Supporting Predictable Design Using Formal Analysis Techniques" at the ARTES summerschool (A Network for Real-Time Research and Graduate Education in Sweden) that took place in Näsślingen, Sweden, August 23, 2006. The audience consisted of Phd Students from the field of real-time research, which allowed disseminating recent results in embedded system design to related research teams (mainly) in Scandinavia.

Special session: Virtual Automotive Platforms
Design Automation Conference (DAC)
San Diego, USA – June 6, 2007
TU Braunschweig was invited to participate in the special session on "Virtual Automotive Platforms" at the renowned Design Automation Conference (DAC). The talk "Automotive Software Integration" showed how formal techniques can be applied to solve performance related integration problems in the design process of complex modern automotive systems. The special session took place June 6, 2007.

Workshop: Tool Platforms for Modelling, Analysis and Validation of Embedded Systems
Conference on Computer Aided Verification (CAV)
Berlin, Germany – July 1-2, 2007
TU Braunschweig was invited to participate in the ARTIST workshop on "Tool Platforms for Modelling, Analysis and Validation of Embedded Systems" at the conference on Computer Aided Verification (CAV).The talk "SymTA/S - Modeling system timing using abstract event streams" allowed disseminating results in the field of compositional performance verification techniques to a larger community. The workshop took place July 1-2, 2007.

3. Future Work and Evolution

3.1 Problem to be Tackled over the next 12 months (Sept 2007 – Aug 2008)

ETH Zurich plans to build on the results of the previous year in terms of comparing different analysis methods in terms of scope and accuracy. As a result, we expect to combine even more different formalisms, e.g. timed automata, and to improve the properties of our own method, Modular Performance Analysis.

The Linköping group will continue further development of the analysis and optimization techniques for fault-tolerant and predictable distributed systems. In particular, fault tolerance for soft real-time systems will be investigated. The approach to predictable implementation of real-time systems on multiprocessor SoC will be further developed.

DTU and LiU will continue their collaboration on the FlexRay communication protocol. So far, the topic of transmission reliability has not been addressed during FlexRay optimization. FlexRay has two independent channels that can be used for message replication to increase redundancy. Another option is to retransmit the message in order to protect against faults. DTU and LiU will determine reliability equations for FlexRay messages, and propose an optimization method to increase reliability of transmission. The optimization will decide if a message is to be replicated on the two channels, or retransmitted, such that the timing constraints are still satisfied.

DTU will continue its work on efficient NoC architectures. In particular the will work on techniques to automatically generate efficient NoC topologies. They will investigate reconfigurable NoC structures based on combining circuit switching and packet switching. Finally, work will be started on linking the NoC architecture with the application program through the development of programming models for NoC-based systems.

TU Braunschweig will further investigate the application of hierarchical event models for performance verification of embedded systems. One promising application will be the detailed analysis of effect that COM-Layers have on communication timing. Additionally, TU Braunschweig will pursue its research in the domain of online performance verification. Main focus will be the development of heuristic optimization algorithms performing what-if analyses to continously improve system robustness. Similar strategies will be investigated to deal with faulty hardware, such as degrading processors or applications breaking their service contract, in order to remain in a feasable system state. Additionally, TU Braunschweig will consider timed automata as a further modelling construct to be coupled to MPA and SymTA/S.

3.2 Current and Future Milestones

TU Braunschweig and ETH Zürich

1. The plan for the next months is to implement the changes needed for a combination and analyse an example application to show the strength of the new approach. These steps should also result into a joint publication of the results.

ETHZ and TU Braunschweig have organized an integration week and the tools SymTA/S and MPA are now fully coupled and can be used for mixed performance analysis of distributed embedded systems. The analyses of example applications have shown that the combined approach is superior in terms of accuracy compared to the results of the individual approaches. The technical details and experimental results have been published in a joint paper [KHE+07].

ESLAB Linköping

1. Further development of optimization approaches for systems built on heterogeneous communication protocols, in particular, Flexray.
2. Further development of the analysis and optimization techniques for fault-tolerant distributed systems. These techniques will be incorporated into the tools developed by the various partners, in particular, Symta/S in Braunschweig.

*Both milestones were achieved. An optimization approach for Flexray was developed and published in [*PPE+07b*]. Fault tolerance techniques under energy constraints were proposed in [*PPI+07*].*

TU Braunschweig

1. Further research in the extension of the SymTA/S model with hierarchical event models.

TU Braunschweig has integrated a first model for hierarchical event models into the tool SymTA/S. The model has already been successfully applied to the detailed analysis of the effects that COM-layers have on the communication timing. The results are submitted to a conference, and a currently under review.

2. Development of advanced techniques for system robustness optimization. This would leverage the applicability of the SymTA/S methodology for reliable and predictable embedded system design.

TU Braunschweig has developed sophisticated robustness optimization techniques for embedded systems. The proposed techniques can be used to efficiently evaluate and explore system robustness with respect to variations of several dependent system properties. The results are published in several papers [HRE06, HRE07a, HRE07b].

3. Development of mapping optimization approaches with automatic communication synthesis.

This topic has been postponed to the next period.

4. Refinement and further development of semantical extensions for formal analysis of MPSoCs with focus on shared memory accesses. This includes the coupling of the tools SymTA/S und SymTA/P (both developed at TU Braunschweig). This activity could profit from synergy effects with 1.

The results of this milestone have been transferred and are discussed in the activity progress report on system modeling infrastructure (D14-EP-Y3).

University of Bologna

1. Network-on-chip architecture exploration: a more modular and scalable system-inteconnect architecture development approach will be studied in details, along with crossbenchmarking against traditional system interconnects

Technical University of Denmark

1. Further development of network-on-chip architectures and exploration at both circuit and system level. Development of NoC benchmarks and conducting comparative NoC studies.
2. Further development of communication models for distributed embedded systems, in particular wireless sensor networks and fault-tolerant distributed systems.
3. Development of mapping approaches which explores optimized communication architectures in terms of metrics like performance, power consumption, cost and faulttolerance.

DTU has continued its research in the domain of NoC architectures. Thereby, mainly circuit complexity and power consumption issue has been investigated. For this reason DTU has studied „leight-weight" NoC architectures as well as more efficient clock-distribution methods [SBS06], [BSS07].

3.3 Indicators for Integration

As a result, we will have developed an important prerequisite for the design of embedded systems, namely analytic methods to estimate system properties. In particular, the approaches followed so far in the context of Hard Real Time and Embedded System Design Communities will be integrated and related to each other.

3.4 Main Funding

- Hogthrob (project on Sensor Networks funded by the Danish Research Council);
- STMicroelectronics (direct industrial grant),
- SRC (coordinated project with Penn State University);
- Swedish Foundation for Strategic Research (SSF);
- Centre for Industrial Information Technology (Linköping University);
- IBM Research Rueschlikon (Network Processor Design).
- DFG (Deutsche Forschungsgemeinschaft)
- BMBF (Bundesministerium für Bildung und Forschung)