IST-004527 ARTIST2

Network of Excellence

on Embedded Systems Design

Cluster Progress Report for Year 3

Cluster:

Testing and Verification

Cluster Leader:

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Policy Objective (abstract)

The objective is to combine the efforts and skills of the individual leading researchers and research groups in Europe into a world-class virtual team, for advancing the state-of-the-art in verification and testing methodologies.

Testing and verification is a transversal topic interacting with all the other topics in embedded systems design aiming to ensure that the different design steps meet given properties as well as the overall correctness of the implementation. Focus within the cluster is on two aspects being of extreme importance for embedded systems. First is the verification and testing of quantitative properties ensuring that real-time constraints and quality of service constraints are met. Second is the verification of security properties. A particular objective is the successful transfer of knowledge, methods and tools to industry.

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1. Overview

In this section we give an overview of the current situation for the cluster's research area in terms of overall objectives and trends.

1.1 High-Level Objectives

The high level objectives for the 18 months period, September 2006 until February 2008, are as follows:

- *Quantitative Testing and Verification:* work has continued with respect to development of metrics for testing coverage, abstraction methods and compositional methods allowing properties of a composite system to be inferred from those of its components.

  Also, based on existing powerful (real-time) verification techniques work towards maturing and further development of important topics such as optimal scheduling, monitoring and fault diagnosis, controller synthesis, robustness and implementability of quantitative models and analysis of hybrid models, stochastic and timed models has been planned.

- *Verification of Security Properties*: our goal is to *broaden the horizon of the verification on security protocols* in such a way that it meets the requirements and the (future) expectations of industrial partners. To this end we have tackled three related groups of problems, which can be considered as the natural extensions of the problems tackled last year: 1) Bridging the gap between the formal and computational views of security protocols; 2) The verification of voting and e-payment protocols and 3) Laying the basis for new trust model.

- *Testing and Verification Platform for Embedded Systems*: the individual tools have been further refined – both with respect to functionality and performance. Also, the work of dissemination of the tools through case study demonstrators has been continued and documented through the joint web page for industrial case studies. Finally, in order to clarify the possibilities with respect to the establishment of an experimental high-performance tool server, the academic tool providers have been questioned wrt. their ability to handle large state spaces.

For *Quantitative Testing and Verification* all objectives have been accomplished with substantial amount of work focusing on controller synthesis and games (finite and timed): here several results contributing to the theoretical foundation of controller synthesis has been given – e.g. decidability versus undecidability for priced models, but also effiecient on-the-fly algorithms with tool implementation has been given. Also work pointing towards quantitative verdicts rather than boolean answers (yes/no) in comparing quantitative models with each other and temporal logic specifications have been pursued in several papers.

For *Verification of Security Properties* prototypes capable of performing automatic analysis of security protocols have been produced. This has been achieved also by defining a constraint-based tool for the automatic verification of security protocols in which the user can specify arbitrary properties to be checked. Work partially completed includes the development of acompositional proof techniques for verifying services security properties, and for verifying group protocols.

Within *Testing and Verification Platform for Embedded Systems* the objectives related to the individual tools, their advancement and dissemination via web-portals containing (links to) tools and industrial case studies has been accomplished. The Whereas several individual partners have distributed implementations of their own tools on PC-clusers, the original idea of establishing a European high-performance Verification Grid has not been pursued in a concerted manner. It is long-term ambition and is still relevant and should be pursued even beyond ARTIST". However, it requires direct involvement with (and from) Grid consortia (e.g. NorduGrid) and requires substantial additional, dedicated funding which has not been granted at this point in time.

1.2 Industrial Sectors

The testing and verification techniques and tools developed and disseminated within the cluster have relevance and potential impact on literally *all* industrial sectors developing or using embedded systems solutions. Within the Strategic Research Agenda of the ARTEMIS research platform[1] *Design Methods and Tools* is one of the three research priorities put forward. Here model- and component-based approaches are proposed as necessary for coping with the growing complexity of systems while meeting "time-to-market" requirements. Methods and tools for testing and verification are to play a central role in the ARTEMIS research strategy, as can be seen from the following citations:

- ".. methods and tools for simulation, automatic validation and proving, and virtual Verification and Validation (V&V). Methods and tools for developing product lines of embedded systems."
- ".. reduce the cost of the system design by 50%. Matured product family technologies will enable a much higher degree of strategic reuse of all artifacts, while component technology will permit predictable assembly of Embedded Systems."
- ".. achieve 50% reduction in development cycles. Design excellence will aim to reach a goal of "right first time, every time" by 2016, including Validation, Verification and certification (to the same and higher standards as today)."
- "..manage a complexity increase of 100% with 20% effort reduction. The capability to manage uncertainty in the design process and to maintain independent hardware and software upgradeability all along the life cycle will be crucial."
- ".. reduce by 50% the effort and time required for re-validation and recertification after change, so that they are linearly related to the changes in functionality."

The industrial needs for improved tools and methods for system validation have also been witnessed by a number of industrial and industry inspired case-studies and projects using model-based testing and verification carried out by the individual partners. Detailed information of these (and others) is to be found in the ARTIST2 Open Repository for Test and Verification Case Studies (https://bugsy.grid.aau.dk/artist2) and include:

- Danfoss (Aalborg): The continuation (From February 2006, to approx. January 2007) emphasizes automated testing. The project has two main goals. One is to develop an automated test execution environment for system level testing of the EKC series refrigeration controllers. The other is to improve model-based online testing given the experiences from the first trials
- Ericsson Telebit (Aalborg): The goal of this project has been to use Live Sequence Charts in a model-driven approach to the testing of TCP/IP internet protocols. Live Sequence Charts are used to capture (informal) RFC in a formal, yet intuitive, way.

[1] http://www.artemis-office.org/

- TK Systemtest (Aalborg): From timed automata design models the verification engine of UPPAAL is used for off-line generation of test-sequences which covers the model. In the project a tool for translating these logical test-sequences to test-scripts executable in QTP of Mercury's Test Director. The resulting tool-chain has been applied to automatic testing of web-services of TDC (Danish Telecom). A commercial spin-off tool (V+) is under development.
- Skov A/S (Aalborg): In this work, we provide a complete tool chain for automatic controller synthesis using UPPAAL Tiga and Simulink. The tool chain is explored using an industrial case study for climate control in a pig stable. The problem is modelled as a game, and UPPAAL Tiga is used to automatically synthesize a safe strategy that is transformed for input to Simulink, ´which is used to run simulations on the controller and generate code that can be executed in the actual pig stable. The models allow for guiding the synthesis process and generate different strategies that are compared through simulations.
- ESI (Embedded Systems Institute, Eindhoven) has carried out (is carrying out) large industrial case studies with Océ, ASML, Philips Semiconductors (now NXP), Philips Medical Systems, Vanderlande Industries.
- Uppsala University: As a case study, we have developed a formal model for a Biomedical Sensor Network (BSN). The sensor nodes of the network are constructed based on the IEEE 802.15.4 Zig-Bee standard for wireless communication. The UPPAAL tool is used to tune and validate the temporal configuration parameters of the network in order to guarantee the desired QoS properties for a medical application scenario. The case study shows that even though the main feature of UPPAAL is model checking, it is also a promising and competitive tool for efficient simulation.
- OFFIS, University of Freiburg, Aalborg University: The "Single-tracked Line Segment" (SLS) case study stems from an industrial partner of the UniForM-project . It is the specification of a control system for a single-tracked line segment for tramways. It is implemented by distributed PLC automata. We took three different models of the SLS case study as examples. As the safety property to verify, we chose the mutual exclusion of drive permissions, i.e., the control system never gives permission to both directions simultaneously.
- OFFIS; Univ. of Oldenburg; Albert-Ludwigs-Universität Freiburg; Max-Planck-Institut für Informatik: The flap controller (high-lift) case study is derived from a case study for Airbus, a controller for the flaps of an aircraft. The flaps are extended during take-off and landing to generate more lift at low velocity. They are not robust enough for high velocity, so they must be retracted for other periods. The controller can perform a load-relief function to correct the pilot's commands if he endangers the flaps. Additionally, there is also an extensive monitoring of the health of its sub-systems, checking for instance for hardware failures. Typically this will give rise to large discrete state spaces when model checking models derived from the flap controller.
- OFFIS, Univ. of Oldenburg : Automating verification of cooperation, control, and design in traffic applications. Here we present a verification methodology for cooperating traffic agents covering analysis of cooperation strategies, realization of strategies through control, and implementation of control. For each layer, we provide dedicated approaches to formal verification of safety and stability properties of the design. The range of employed verification techniques invoked to span this verification space includes application of pre-verified design patterns, automatic synthesis of Lyapunov functions, constraint generation for parameterized designs, model-checking in rich theories, and abstraction refinement. We illustrate this approach with a variant of the

European Train Control System (ETCS), employing layer specific verification techniques to layer specific views of an ETCS design.

1.3 Main Research Trends

Within the area of Testing and Verification the overall trend is that systems of increasing complexity with an increasing number of features taking into account may be dealt with.

A definite trend is also, that model-checking and testing techniques are being applied directly to software validation (in particular C and JAVA) with noticeable successes given by the SLAM, Blast, VeriSoft, Bandera and JAVA-Path-Finder projects. Here, the method of *abstraction-refinement* provides a combination of abstract interpretation with model-checking with success within given application domains (e.g. SLAM and Blast addresses debugging of device drivers).

Another trend within the research area of verification is the (re-)discovery of SAT-solving as a technique for performing so-called *bounded* model-checking. Advances made on SAT-solving during the last 5 years has made this approach competitive compared to other techniques including symbolic model-checking. Members of the T&V cluster are active in pursuing extensions of SAT-solving to extended logics with quantitative aspects (difference constraints, linear constraints) in order to make bounded model-checking applicable to models of embedded systems.

Yet another trend is that the features and properties supported by current technology goes beyond that of pure functional correctness to also include timed, stochastic and hybrid phenomena. Within the Testing and Verification Cluster research on all of these quantitative extensions are pursued actively pursuing different techniques (bounded model checking, regular model checking, decision diagrams, automata for symbolic representation) are finding their way into powerful tools (e.g. UPPAAL, IF, CMC, MoDeST, EMTCC, FAST).

Advances in verification technology (in particular the development of symbolic data structures) are finding their way into mature testing tools (e.g. TGV, STG, ToRX). Substantial effort has been made by several partners on model-based testing and monitoring of real-time systems with UPPAAL Tron and IF being some resulting tools. Also, related work on monitoring, controller synthesis, planning and scheduling, and schedulability analysis for real-time systems has been made resulting in tools such as TIMES and UPPAAL Cora and UPPAAL Tiga and several applications.

Model-driven development is highly appreciated in software engineering particularly because of the possibility of automatic code-generation. However, for quantitative models the realization on real hardware raises several problems. Indeed, the quantitative models are theoretical frameworks, assuming infinitely fast hardware, infinitely precise clocks, etc. However, these characteristics are not fulfilled on real CPUs, that are digital and have a finite frequency. Current research within the cluster is addressing this problem in the setting of real-time and involves identification on when (and how) given timed automata models are implementable and to what extent properties proved by the model also may be guaranteed to hold of the final implementation.

Within verification of security properties work has been made on the semantic foundations and the verification of security protocols and web-services. A general verification method for security protocols with possible unbounded sessions has been provided as well as a sound and complete inference systems for bounded-sessions cryptographic protocols. The work also include a classification and relation of different existing specification methods (multi-set rewriting and process algebra) for security protocols as well as the use of standard model-checkers for analysing various security protocols (e.g. use of muCRL, SPIN and CADP) and for addressing security treats based on real-time issues (using UPPAAL).

In the area of parallel and distributed model checking of embedded systems we are in close collaboration with other research teams in Europe (INRIA Rhone-Alpes, CWI, Technical University Munich and Aachen Technical University) attempting to gather the European research communities working in the area on cluster and/or grids. Scientifically the work within the cluster has primarily focused on new algorithms for the enumerative distributed checking of reachability properties, and on extended the scope of *efficient* distributed algorithms to cover model checking of general CTL and LTL properties and of real-time models. The general environment DiVinE has been deployed and has also been extended by a Promela front-end for SPIN.

2. State of the Integration in Europe

The objective of the Testing and Verification cluster is to combine the efforts and skills of the individual leading researchers and research groups in Europe into a world-class virtual team, for advancing the state-of-the-art in verification and testing methodologies. As will be described below the partners span the leading research teams in European level and are well connected with leading research teams outside Europe.

2.1 Brief State of the Art

We refer to section 1.3 in this deliverable for an account of the main trends within testing and verification. With respect to testing and verification of quantitative and security aspects and the construction of a testing and verification platform the following gives a brief state of the art:

Quantitative Test and Verification

An important step towards supporting quantitative analysis of real-time aspects is provided by the modeling formalism of timed automata. The potential of timed automata for the modeling and analysis of real-time systems has been documented extensively in the literature. Since their introduction by Alur and Dill in 1990, several verification tools for timed automata have been developed (in particular UPPAAL, Kronos and IF) which are now applied routinely to industrial-size case studies.

More recently priced extensions of the timed automata formalism has been introduced - permitting consumption of resources to be taken into account. During this second year partners within the cluster has provided a number of results concerning decision problems wrt to this model of priced timed automata providing the foundation on which the future implementation within tools will be based. This involves design of data-structures and efficient algorithms. These are now to be found within the special purpose tool UPPAAL Cora.

Also controller synthesis and stochastic extension has been considered as well as the transfer of successful techniques for timed automata to classes of hybrid automata.

In addition, the foundational principles for generation of predictable code from timed automata models, and conformance testing based on timed automata models are being provided during this second year.

Significant effort on stochastic model checking has been made during the last decade. However, technology still lack for making stochastic analysis as tractable as that of analysis of timed or untimed models.

The partners are participating very actively in the research aiming to improve the above state of the art on specific areas within quantitative testing and verification as mentioned below, i.e. within the areas of timing, resources, schedulability, stochastic and hybrid aspects as well as testing theory,

Verification of Security Properties

Security engineering is about building systems to remain reliable despite the presence of malice errors. As a discipline, it studies and develops the tools and methods to design, implement and validate systems that guarantee security properties. Many security systems and in particular embedded systems have critical requirements. Their failure may cause serious economic damages (cash machines, electronic purse and other bank systems), endanger personal privacy (medical record systems), endanger the viability of whole business sectors (pay-tv), etc….

Within Artist2, the focus is on tools and methods needed to design embedded systems that guarantee security protocols. More specifically, the focus is on security protocols.

There are by now a number of efficient validation tools for authentication protocols, e.g., Hermes (Verimag), H1 (LSV), CASRUL (LORIA) mention tools developed by Artist2 partners.

Such validation tools have, however, not yet reached the level of maturity to be autonomously used by protocol designers. What is missing? A major obstacle is that these tools are based on a semantic model that is commonly called symbolic or Dolev-Yao model. This essentially means that cryptographic primitives are idealized and their behaviour is, hence, simplified.

Platform for Testing and Verification

Testing and verification of embedded systems are computationally hard and memory intensive activities as the underlying models contain (multiple) quantitative aspects in order to enable the expression of important properties concerning real-time constraints, impact on physical environment, expected resource consumption and performance of a given design, etc.

During the second year the partners of the cluster have been active in implementing, improving and disseminating a large number of testing and verification tools allowing for the analysis of quantitative models including real-time aspects, resource models, hybrid and stochastic models. We refer to the deliverable for the *Testing and Verification Platform* for a more detailed account. What is important to note here is that there is a very short distance (time-wise) from foundational decidability results to their impact on performance of tools in terms of improved data-structures and algorithms.

2.2 Main Aims for Integration and Building Excellence through Artist2

As demonstrated in the section above the integration of the research groups within the cluster is excellent and with significant impact on the larger research community on testing and verification through strong impact on a number of important international conferences within the area. Also, partners of the cluster – often in collaboration with other clusters – have made significant effort in spreading of excellence beyond the ARTIST2 NoE through PhD schools and industrial seminars. More systematic knowledge transfer to industry through long-term collaboration on industrial development projects has been performed by individual partners. Here the national centers ESI (Embedded Systems Institute, Eindhoven, The Netherlands) and CISS (Center for Embedded Software Systems, Aalborg, Denmark) have specific resources reserved for such activities.

However, given the limited resources available within ARTIST2 it is paramount that substantial, additional European funding is obtained to support the man-power required to fully transform the research ideas and prototype tools into industrial testing and verification practice with a supporting collection of tools integrated with existing industrial tool chains. Here we are looking forward to undertake this exercise in the follow-up European projects such as Quasimodo (STEP under FP7). Also at the national level of the various partners in the Testing and Verification cluster involvement in ARTEMIS are planned with the ambition of having an impact on the long-term take-up of testing and verification technology in industrial practice.

2.3 Other Research Teams

Other prominent research groups not being partner of the cluster include a number of teams from United Kingdom, in particular School of Computer Science, Birminghan (probabilistic

model checking), Oxford University Computing Laboratory (real-time verification), Microsoft Research Laboratory at Cambridge and Royal Holloway, University of London (security).

From Italy important contributions come from the Automated Verification and Synthesis Group, Trento University (symbolic model-checking, SAT-solving, applications to planning) with support of the nuSMV tool.

The partners of the cluster are collaborating extensively with leading research teams outside Europe both on the level of concrete research problems and topics and in terms of organising the testing and verification research community. The cluster has strong links to the work on software verification and testing taking place at Microsoft Research, Redmond, (Ball), NASA Ames and Kestrel Technologies (Holzman, Visser and Havelund) and Kansas (Hatcliff). Extraordinary strong links exist to Cadence (Sangiovanni Vincentelli, director of Cadence and core-partner of ARTIST2), Rice University, Texas (Vardi, longstanding collaboration with Wolper on the highly appreciated and influential automata theoretic approach). Also ARTIST2 has collaborated with leading research groups and researchers from Israel including Weizmann Institute (Pnueli, Harel), Haifa (Grumberg) and Hebrew University (Kupfermann).

2.4 Interaction of the Cluster with Other Communities

Model-checking technology forms the basis for automatic verification and is utilized for test-case generation. However, model-checking is also increasingly applied successfully within and by other communities including hardware/software co-design, control theory, planning and scheduling and performance evaluation. Members of the cluster has published and given invited talks at main conferences and in journals of these other communities. Similarly leading research groups within AI are finding applications of existing search heuristics from planning to the improved model-checking (e.g. Friburg University, Germany within the AVACS project and Trento University, Italy).

3. Overall Assessment and Vision for the Cluster

3.1 Assessment

Each research activity within the cluster has successfully pursued the research goals of the given 18 months period.

As last year the cluster integration activities within *Quantitative Testing and Verification* and *Verification of Security Properties* have been particularly active during this third year as is most clearly demonstrated by the (very) extensive lists of publications made by members of the cluster during the first year at leading scientific conferences and journals witnessing true excellence within the area

The activities within *Testing and Verification Platform* are tightly connected to the activities within *Quantitative Testing and Verification* in that the latter provides the theoretical foundation, as well as design of data-structures and algorithm necessary for the development of efficient and mature tools. Within this activity the objectives related to the individual tools, their advancement and dissemination has been fully accomplished. The objective of designing a joint infrastructure for a European Verification Grid has not been pursued during this third year: the main people involved in setting up the Verification Grid are currently occupied by building up the infrastructure for general high performance computing on grids with natural science applications in mind.

Dissemination to research and industry has been done extensively during the third year period by partners individually and in concerted efforts as witnessed by the long list of key note presentations, tutorials and workshops organised.

3.2 Vision and Long Term Goals

As clearly observed by the many industrial contacts of the two national embedded systems centers, ESI (The Netherlands) and CISS (Denmark), testing is *by far* the most used and important validation technique applied by industry today. It is estimated that some *30-70% of the total development cost* for embedded systems is spent on testing at various stages. It is also a general observation that current testing practice is very ad-hoc often with manual construction and even execution of test-scripts. There is clearly a gap between current industrial practice and existing academic state-of-the art technology. It is important that the cluster continues its contribution to the bridging of this gap though collaborative projects attempting to make industry take-up existing state-of-the-art testing and verification techniques.

To focus on aspects such as performance, timeliness, and efficient resource-usage, the testing and verification techniques should be based on models with *quantitative information.* To provide a coherent model-based testing and verification methodology with a well-integrated chain of tools applied in industrial practice is a long-term vision of the cluster. In addition to modelling this will require a strong focus on analytical techniques that address the combination of nondeterminism, real-time and stochastic information. Also support for high abstraction levels must be provided to overcome the inherent complexity of modern embedded systems. Finally, (semi-)automatic generation of code that preserves the relevant design properties will be essential to ensure industrial impact. The start of the European project Quasimodo will allow us to pursue this challenge with substantially increased effort over the next three eyars.

The partners of the cluster intends to play an active role in the forth-coming Joint Technology Initiative ARTEMIS' research priority on Design Methods and Tools.

3.3 Plans for Year 4

The plans for the final year of ARTIST2 within the Testing and Verification cluster within the three activities are as follows:

Quantitative Testing and Verification: the planned work includes continuation of work on combining testing and verification approaches, further development and tool implementation of important topics such as optimal scheduling, fault diagnosis and controller synthesis. For finite state systems very efficient methods have been developed and for timed models UPPAAL Cora and UPPAAL Tiga provides efficient platforms on which new aspects (e.g. partial observability and robustness) may be integrated and made available. Also, continued work on quantitative models involving hybrid and stochastic phenomena and interface specifications sensitive to resources will be dealt with. We expect that the work within this activity will take place in close interaction with the Quasimodo STREP project. This will intensify in particular the efforts on property-preserving code-generation from models, and the work on a range of new powerful debugging and analysis techniques based on different combinations of testing and verification approaches.

Verification of Security Properties: our goal is to *broaden the horizon of the verification on security protocols* in such a way that it meets the requirements and the (future) expectations of industrial partners. Two concrete problems we are going to tackle in the next year are

- start bringing into practice the results from bridging the gap between the formal and computational views of security protocols by designing new practical tools.
- lay the basis for a new trust management framework which generalizes present approaches, and is *not* application specific.

Testing and Verification Platform for Embedded Systems: The case tool repository will be updated along with the ongoing work on tool evaluation through case studies. The three candidates for high-performance verification (SPIN, DUPPAAL, DeVine) will be tested on the new cluster in Aalborg and will be made available for experiments after special agreements with NoduGrid and the tool developers. Also a number of concrete developments of the tools STG (Irisa), UPPAAL Tiga (Aalborg) and CATS (Uppsala) has been planned.

4. Cluster Participants

4.1 Core Partners

Cluster Leader Activity Leader for "Testing and Verification Platform for Embedded Systems" Team Leader for Aalborg on the activities "Testing and Verification Platform for Embedded Systems" and "Quantitative Testing and Verification"	
	Professor, Director Kim G. Larsen (Aalborg) http://www.cs.aau.dk/~kgl/
Technical role(s) within Artist2	Leads and coordinates the overall activities in the cluster; coordinates the activities of the "Test and Verification Platform for Embedded Systems"; member of the Artist2 strategic management board; highly activie on the development of algorithms and tools within the activity on "Quantitative Testing and Verification".

Team Leader for Aalborg on the activity "Verification of Security Properties"	
	Dr. Hans Hüttel (Aalborg) http://www.cs.aau.dk/~hans/
Technical role(s) within Artist2	Contributes to the security activity with foundational work the development on process calculi to describe security aspect sof embedded systems.

Assistant for the Cluster Leader	
	Dr.Arne Skou (Aalborg) http://www.cs.aau.dk/~ask/
Technical role(s) within Artist2	Takes part in the cluster coordination; contributes with expertise on model based testing and tools, industrial contacts, and industrial

	dissemination.

Team Leader for CFV on the activity "Testing and Verification of Security Properties"	
	Professor Jean-François Raskin (CFV) http://www.ulb.ac.be/di/ssd/jfr/
Technical role(s) within Artist2	Contributes with his expertise on controller synthesis and design and development of the LaSH tool.

Team Leader for CFV on the activities "Testing and Verification Platform for Embedded Systems" and "Quantitative Testing and Verification"	
	Professor Pierre Wolper (CFV) http://www.montefiore.ulg.ac.be/~pw/
Technical role(s) within Artist2	Contributes with his expertise to all activities on model checking within the cluster.

Team Leader for EPFL on the activities "Testing and Verification Platform for Embedded Systems" and "Quantitative Testing and Verification"	
	Professoe Tom Henzinger (EPFL) http://mtc.epfl.ch/~tah/
Technical role(s) within Artist2	Contributes with his seminal expertise on models and tools for quantitative aspects of embedded systems.

Team Leader for FT-R&D on "Verification of Security Properties"	
	Researcher F. Klay (France Telecom R&D)
Technical role(s) within Artist2	Francis Klay is collaborating with protocol designers within FT R&D on two important case studies: an electronic purse protocol and e-vote protocol. He is acting as an intermediate between the protocol designers and some of the other partners in Artist in the sense that he is spending a great anount of effort explaining the validation tools and methods developed by these partners.

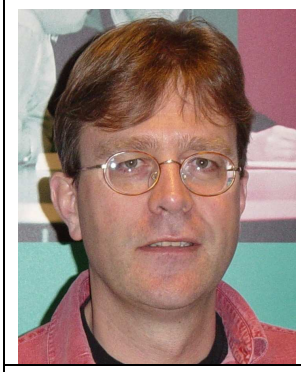
Team Leader for INRIA on the activities "Testing and Verification Platform for Embedded Systems" and "Quantitative Testing and Verification"	
	Scientific Leader Thierry Jeron (INRIA) http://www.irisa.fr/prive/jeron/
Technical role(s) within Artist2	Contributes with his expertise on model based testing and verification and in particular on design and development of the TGV too as well as industrial dissemination.

Team Leader for LSV on "Verification of Security Properties"	
	Hubert Comon (LSV) http://www.lsv.ens-cachan.fr/~comon/
Technical role(s) within Artist2	Contributes to the activity on security with his expertise on cryptographic protocols.

Team Leader for LSV on the activities "Testing and Verification Platform for Embedded Systems" and "Quantitative Testing and Verification"	
	Director Philippe Schnoebelen (LSV) http://www.lsv.ens-cachan.fr/~phs/
Technical role(s) within Artist2	Contributes with his expertise on logics and model checking in general.

Team Leader for Offis on the activities "Testing and Verification Platform for Embedded Systems" and "Quantitative Testing and Verification"	
	Professor, Director Werner Damm (Offis) http://wwwphp.informatik.uni-oldenburg.de/mitarbeiter.php?MNr=19

Technical role(s) within Artist2	Contributes with his expertise on specification formalisms, tool development as well as industrial dissemination

Activity Leader for "Quantitative Testing and Verification" Team Leader for Twente on the activities "Testing and Verification Platform for Embedded Systems" and "Quantitative Testing and Verification"	
	Professor, Director Ed Brinksma (University of Twente/Embedded Systems Institute) http://wwwhome.cs.utwente.nl/~brinksma/
Technical role(s) within Artist2	Coordinates the cluster activities of "Quantitative Testing and Verification"; contributes with industrial dissemination and case studies as well as development of algorithms and tools.

Activity Leader for "Verification of Security Properties" Team Leader for Twente on "Verification of Security Properties"	
	Dr. Sandro Etalle (Twente) http://wwwhome.cs.utwente.nl/~etalle/
Technical role(s) within Artist2	Coordinates the cluster activities on "Verification of Security Properties"; contributes with methods on constraint based logics and trust management.

Team Leader for Uppsala on the activities "Testing and Verification Platform for Embedded Systems" and "Quantitative Testing and Verification""	
	Professor Wang Yi (Uppsala) http://user.it.uu.se/~yi/
Technical role(s) within Artist2	Contributes with his expertise on algorithms and tools for model checking of real time systems – in particular the development of the Uppaal tool and industrial dessimination.

Team Leader for Verimag on the activity "Verification of Security Properties"	
	Professor Yassine Lakhnech (Verimag) http://www-verimag.imag.fr/~lakhnech/
Technical role(s) within Artist2	Contributes with his expertise on model checking in general and on verification of security properties and industrial dissemination in particular.

4.2 Affiliated Industrial Partners

	Boutheina Chetali (Axalto/SchlumbergerSema)
Technical role(s) within Artist2	Contributes with industrial needs wrt. security in embedded systems

	Thomas Hune (Terma A/S)
Technical role(s) within Artist2	Contributes with knowledge on industrial needs for mission critical systems; also with expertise on model driven development In general.

	System architect Jan Lindblad (Enea Embedded Technology)
Technical role(s) within Artist2	Contributes with industrial requirements to testing and verification as they are relevant for operating systems.

	Researcher Alain Ourghanlian (EDF)
Technical role(s) within Artist2	Contributes with knowledge about the industrial needs for efficient, verified code in embedded systems.

	Line Manager Sven H. Sørensen (Motorola A/S)
Technical role(s) within Artist2	Contributes with knowledge about industry needs on model driven development and testing.

4.3 Affiliated Academic Partners

	Professor Andrea Bondavalli (University of Firenze) http://rcl.dsi.unifi.it/aboutus/andrea.php
Technical role(s) within Artist2	Contributes with expert knowledge on the verification of dependability and fault tolerance for embedded systems.

	Professor Ahmed Bouajjani (LIAFA) http://www.liafa.jussieu.fr/~abou/
	Contributes with general knowledge on model checking – in particular within infinite state systems

	Professor Lubos Brim (Brno) http://www.fi.muni.cz/usr/brim/
Technical role(s) within Artist2	Contributes significantly to the cluster activity on Platforms for Embedded Systems; in particular within the development of cluster based distributed model checking through the Distributed Verification Environment DeVinE.

	Senior Researcher Fabio Martinelli (CNR-IIT) http://www.iit.cnr.it/staff/fabio.martinelli/
Technical role(s) within Artist2	Is an expert on security protocols and trust management and contributes with important knowledge to the security acticity.

	Researcher Michael Rusinowitch (INRIA) http://www.loria.fr/~rusi/
Technical role(s) within Artist2	Is an expert on formal methods on embedded systems – in particular on verification of security properties.

	Professor Jan Tretmans (Nijmegen) http://www.cs.ru.nl/~tretmans/
Technical role(s) within Artist2	Contributes with expert knowledge on model based testing. Also tools and industrial dissemination.

5. Internal Reviewers for this Deliverable

Contributions and internal review has been made by Bruno Bouyssounouse (UJF/Verimag), Ed Brinksma (ESI and Twente University) and Arne Skou (Aalborg).