Validation and Verification of Real Time Systems

Kim G. Larsen
Jan Madsen

Outline

- Validation and Performance Analysis in UPPAAL / Kim G Larsen
- Formalising the ARTS MPSoC Model in UPPAAL / Jan Madsen
- Industrial Applications of UPPAAL / Kim G Larsen
  - Optimizing a Memory Interface (Terma)
  - Dynamic Voltage Scaling (Analog Devices)

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Validation and Performance Analysis of Real Time Systems

Using UPPAAL

Kim G. Larsen

AALBORG UNIVERSITY DENMARK

DaNES
Danish Network for Intelligent Embedded Systems

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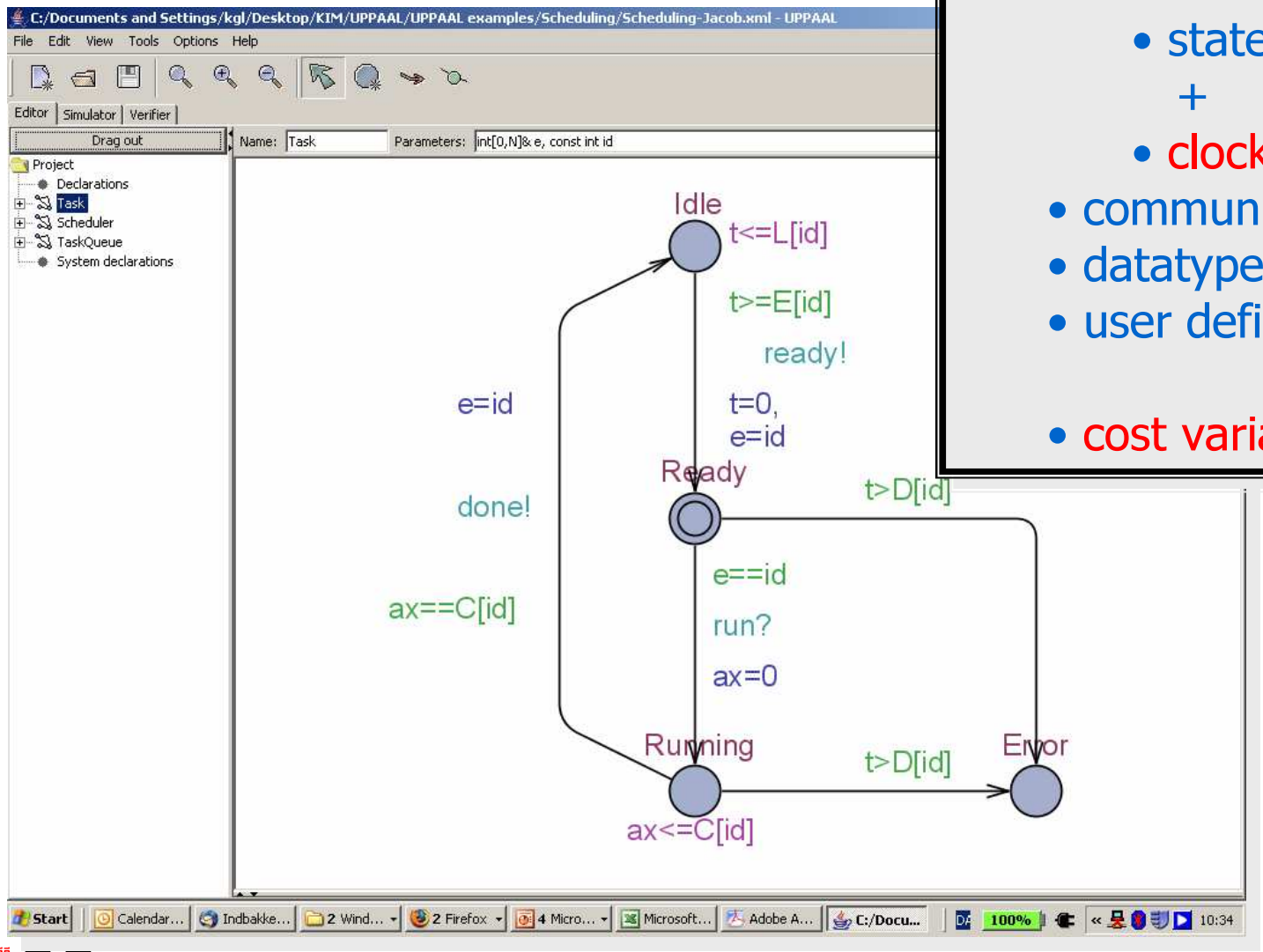
UPPAAL



Graphical Design Tool

- timed automata =
  - state machines
    +
  - clocks
- communication
- datatypes
- user defined functions
- cost variable

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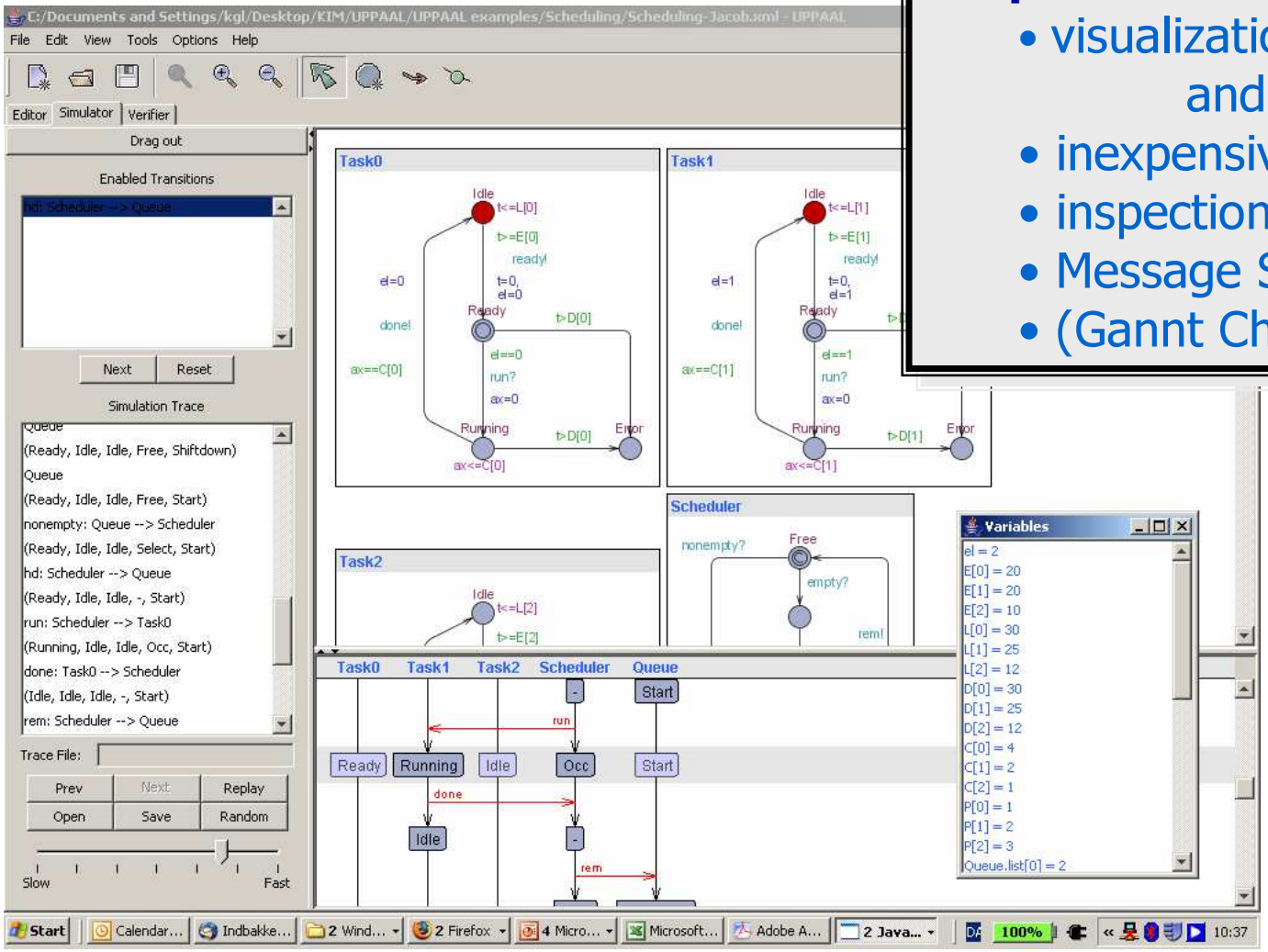
UPPAAL



Graphical Simulator

- visualization and recording
- inexpensive fault detection
- inspection of error traces
- Message Sequence Charts
- (Gannt Charts)

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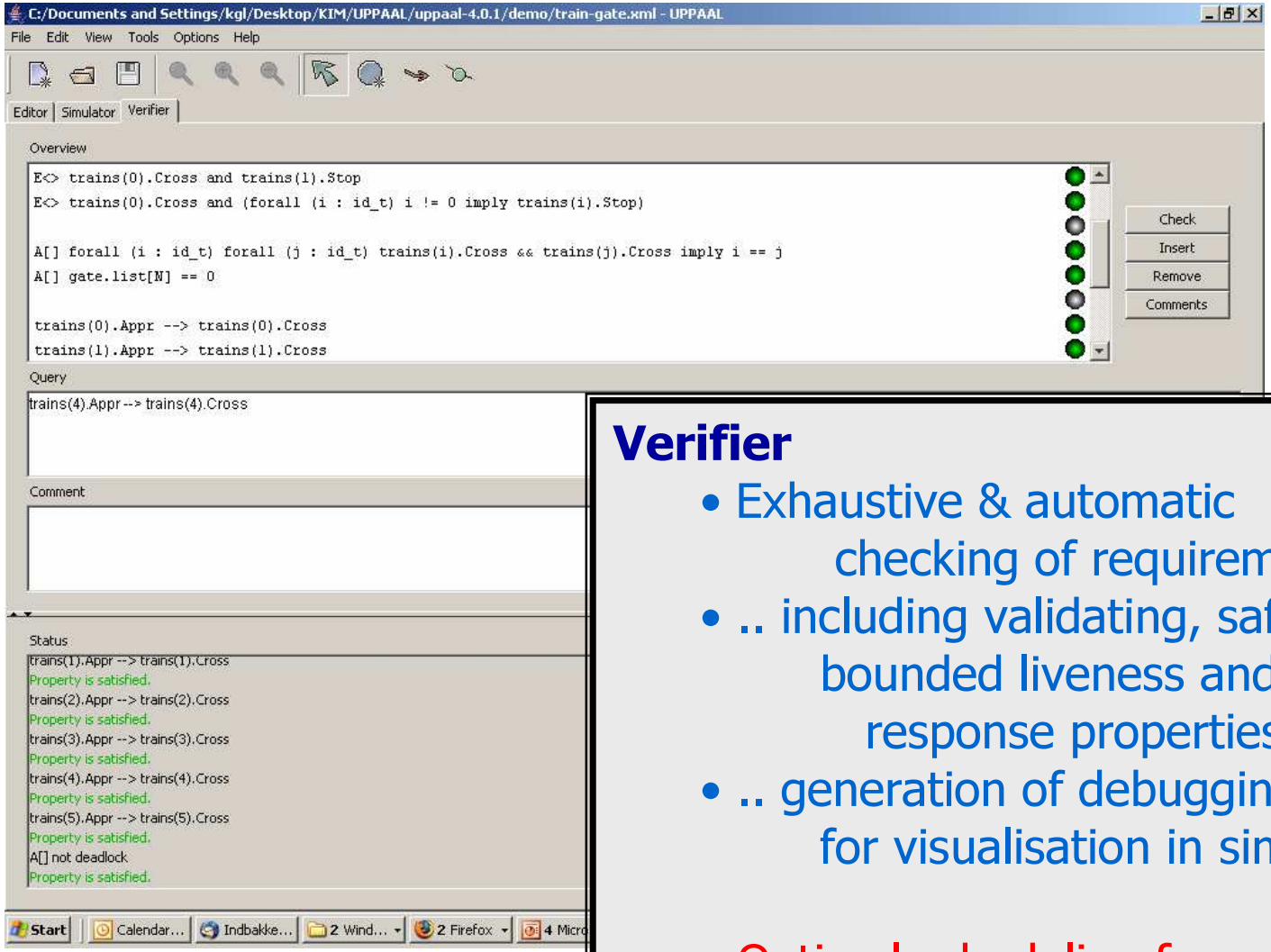
UPPAAL



Verifier

- Exhaustive & automatic checking of requirements
- .. including validating, safety, liveness, bounded liveness and response properties
- .. generation of debugging information for visualisation in simulator.

- Optimal scheduling for cost models

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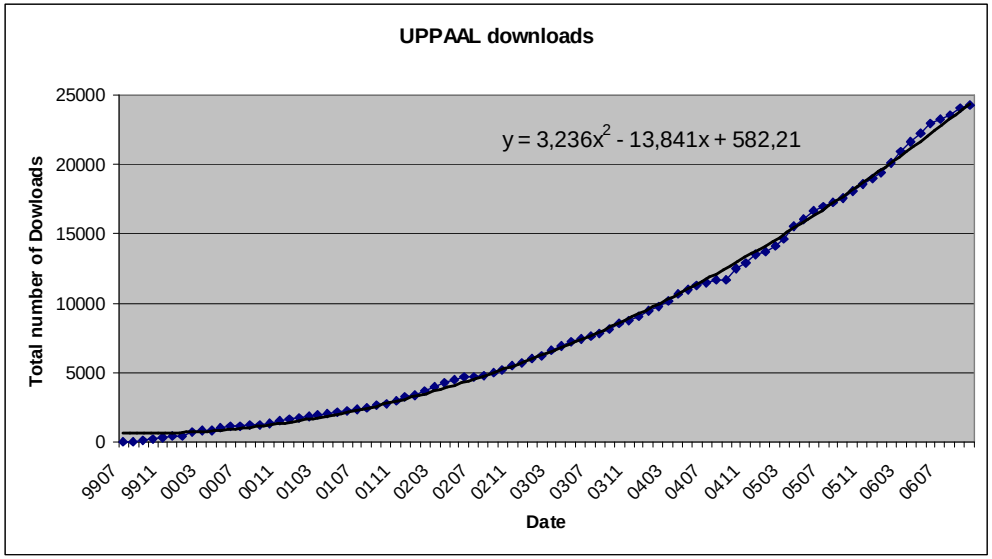

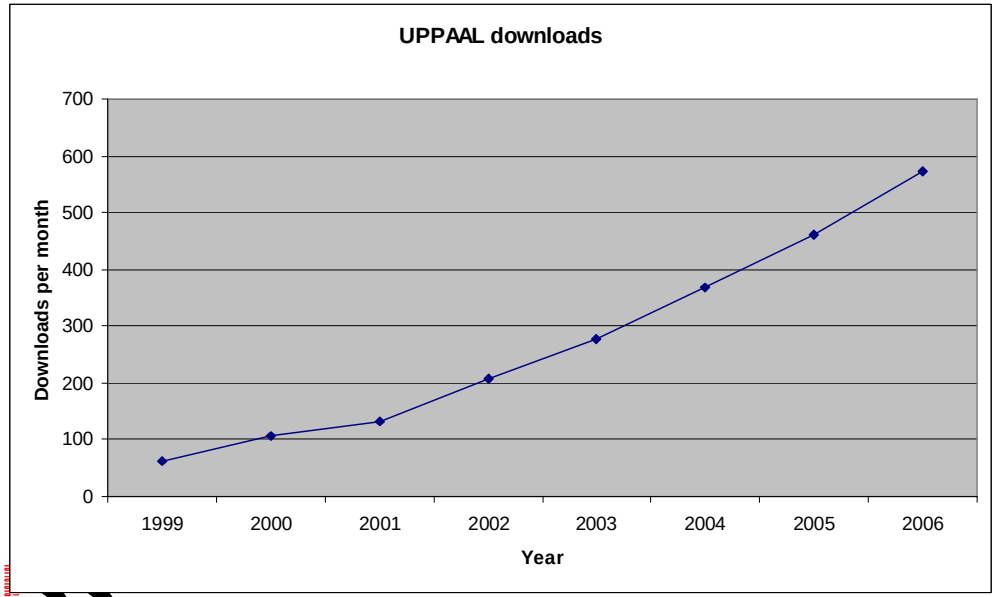

Google:

UPPAAL:	134.000
SPIN Verifier:	242.000
nuSMV:	57.700

> 1.500
Google Scholar Citations
(Rhapsody/Esterel < 3.500)

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Academic Courses @

DTU, MCI, IT-U (DK)

Chalmers, Linköping,Lund, Chalmers,

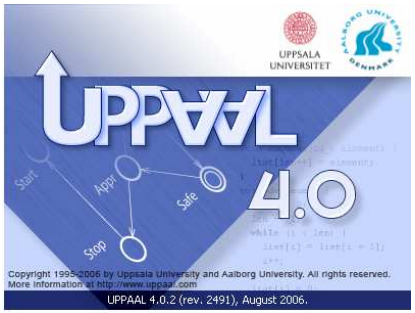
Mälardalarn (S)

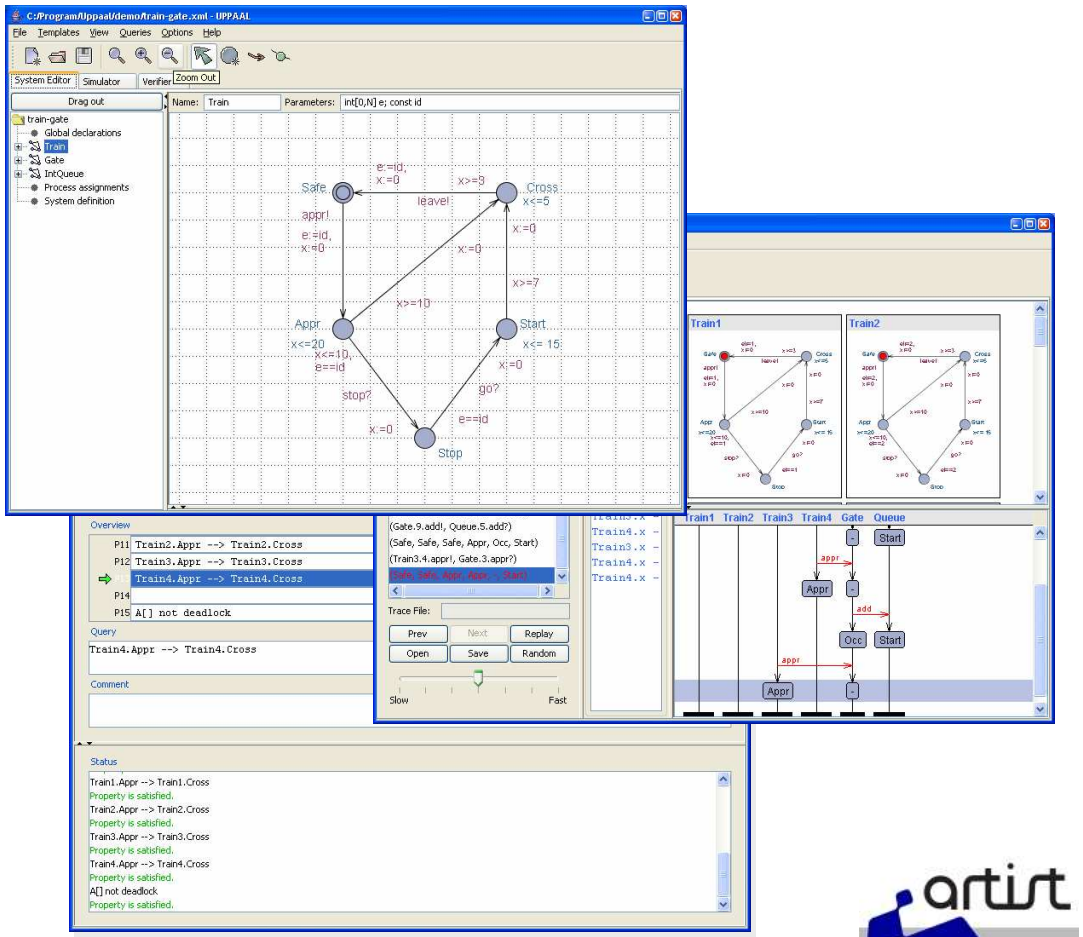
Nijmegen, Twente, CWI (NL)

Upenn, Northumbria(US)

Braunschweig, Oldenborg, Marktoberdorf (D)

Tsinghua, Shanghai, ISS, NUS (Asia)





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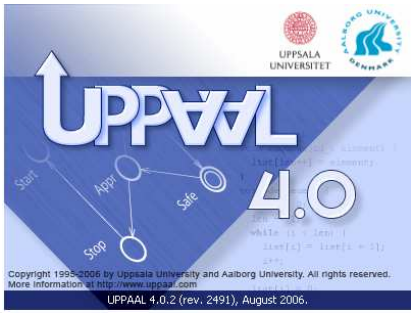
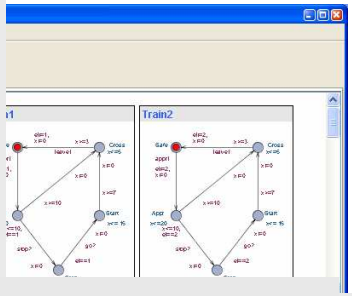
Tutorials Given @

Estonian School (01)
IPA Fall D
FTRTFT
CPN (02)
SFM (02)
MOVEP (
DISC Sch
MOVEP (
PRISE (0
PDMC (0
ARTIST2
EMSOFT
RTSS (05)
TECS week (06)
TAROT (06)
ARTS (06)
GLOBAN (06)
ARTIST ASIAN SCH (07)




UPPAAL2k: Small Tutorial
日本語版
Ver.1.0



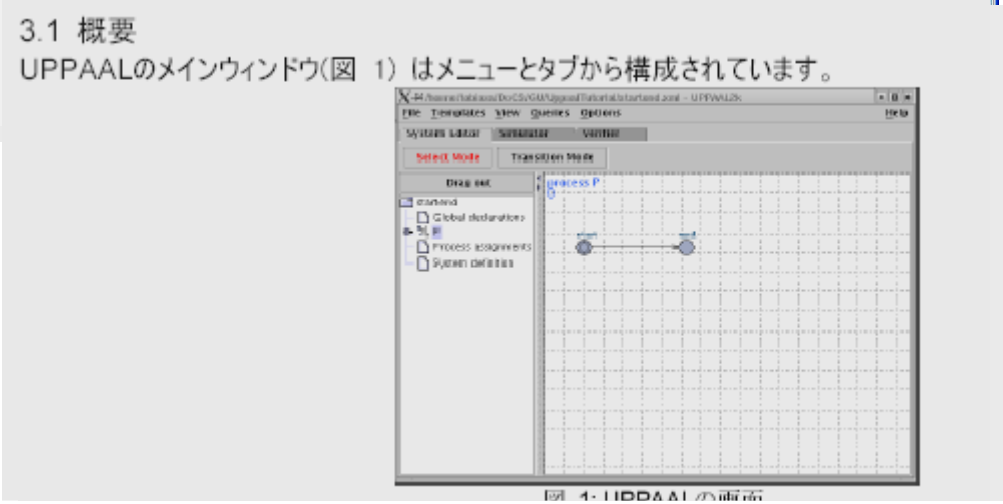

3.1 概要
UPPAALのメインウィンドウ(図 1) はメニューとタブから構成されています。

図 1: UPPAAL の画面

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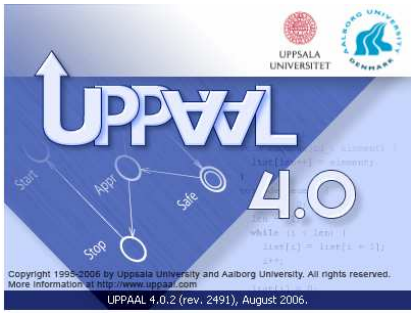
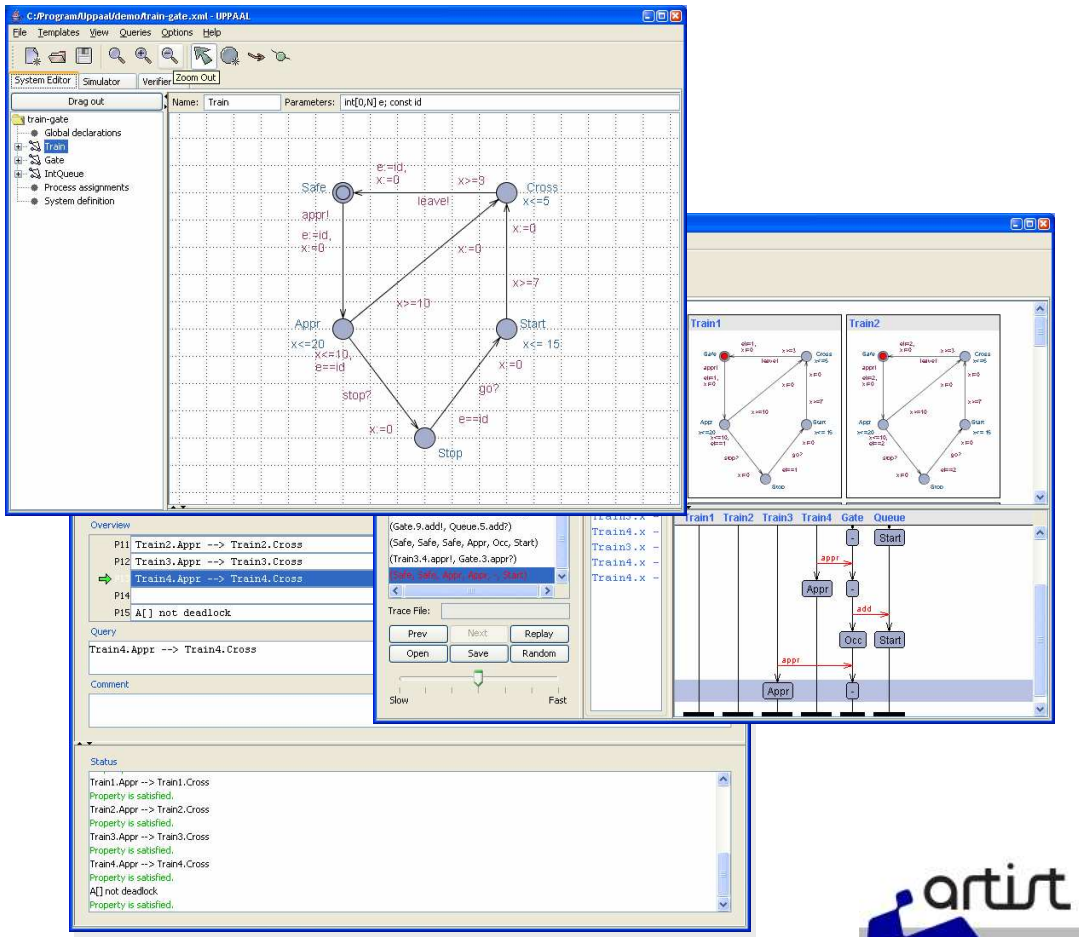
Company Downloads

Mecel
Jet
Symantec
SRI
Relogic
Realwork
NASA
Verified Systems
Microsoft
ABB
Airbus
PSA
Saab
Siemens
Volvo
Lucent Technologies





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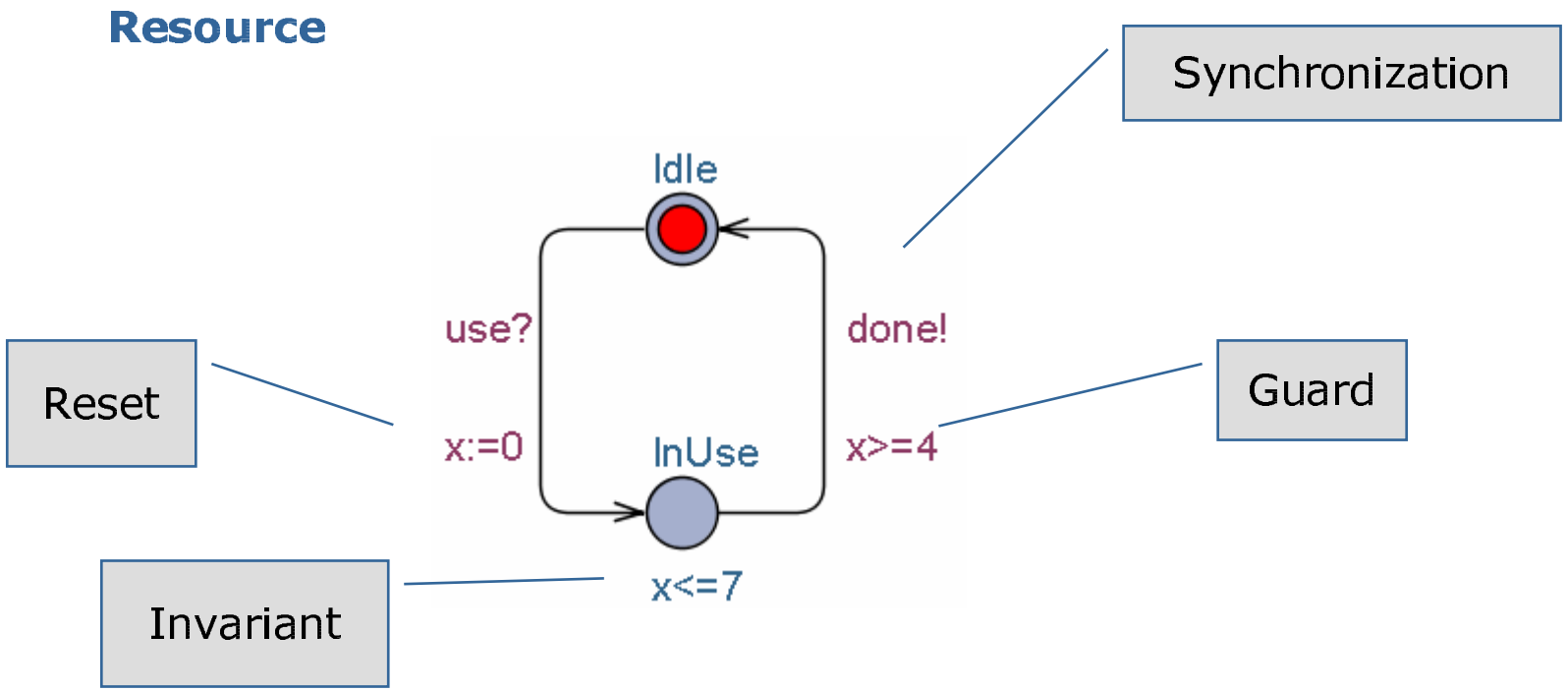
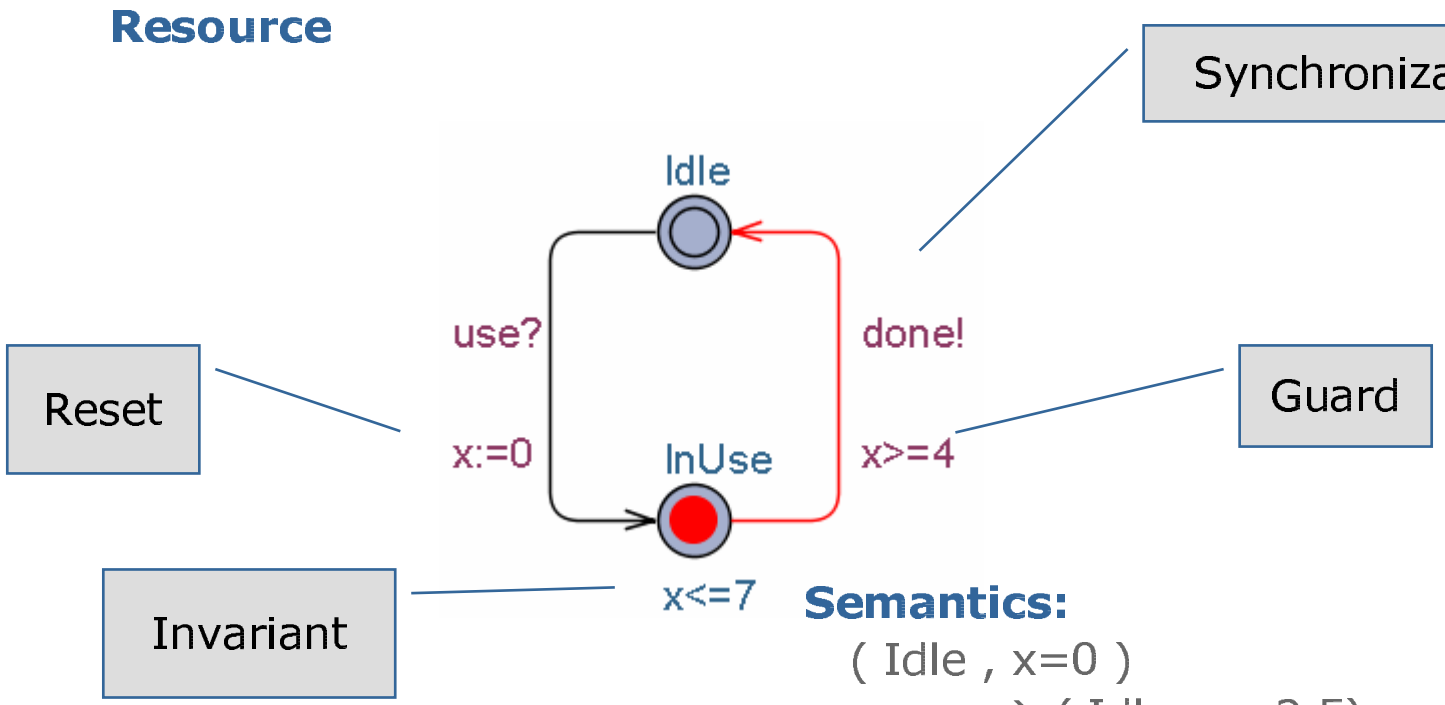
Timed Automata

[Alur & Dill'89]



Timed Automata

[Alur & Dill'89]

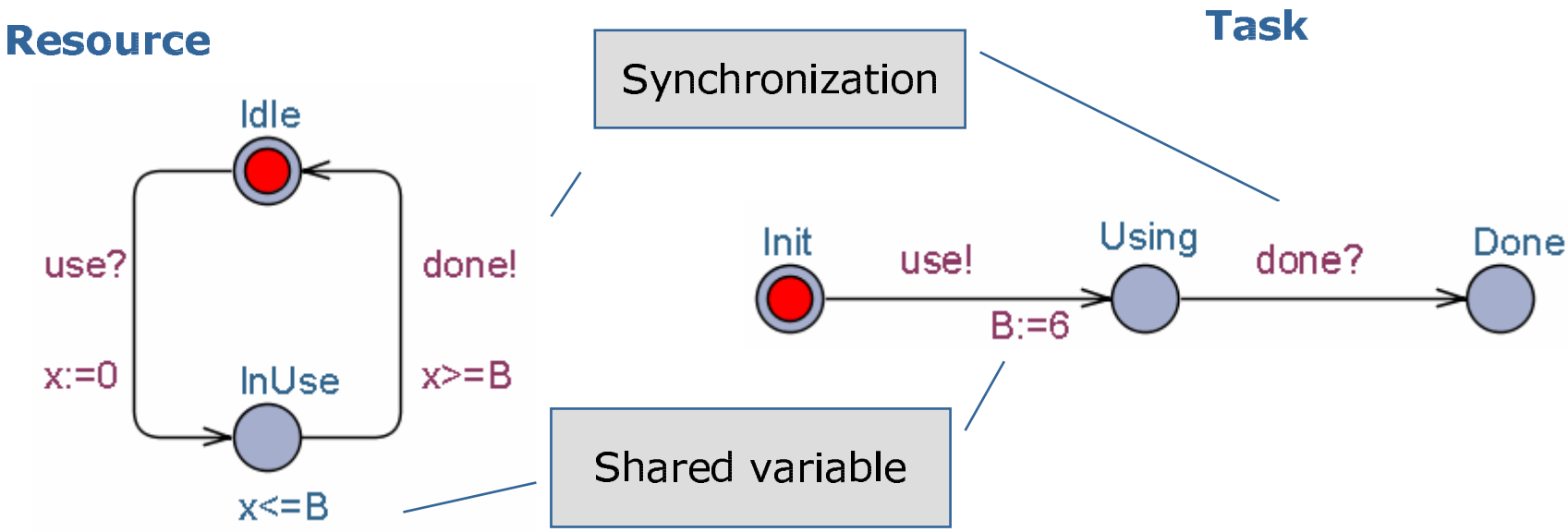


Semantics:

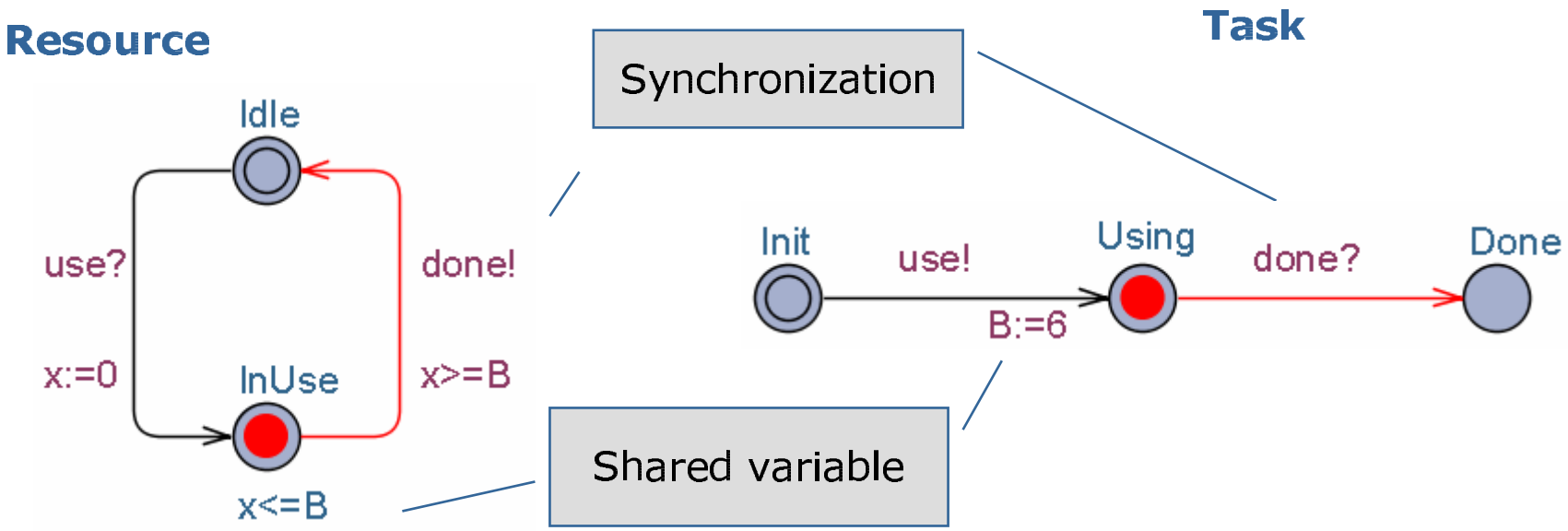
(Idle , x=0)

→ (Idle , x=2.5)	d(2.5)
→ (InUse , x=0)	use?
→ (InUse , x=5)	d(5)
→ (Idle , x=5)	done!
→ (Idle , x=8)	d(3)
→ (InUse , x=0)	use?

Composition



Composition



Semantics:

(Idle , Init , B=0, x=0)

→ (Idle , Init , B=0 , x=3.1415) d(3.1415)

→ (InUse , Using , B=6, x=0) use

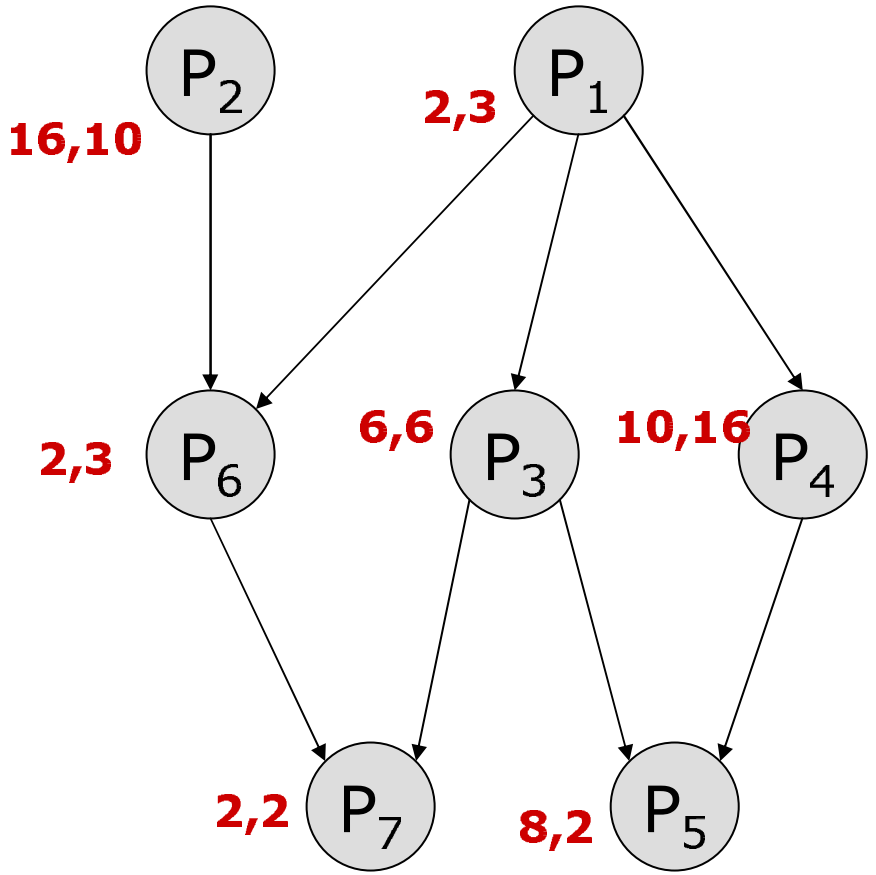
→ (InUse , Using , B=6, x=6) d(6)

→ (Idle , Done , B=6 , x=6) done

Task Graph Scheduling

Optimal Static Task Scheduling

- Task **P**={P_1,.., P_m}
- Machines **M**={M_1,..,M_n}
- Duration Δ : **(P£M) ! N_1**
- < : p.o. on **P** (pred.)



- A task can be executed only if all predecessors have completed
- Each machine can process at most one task at a time
- Task cannot be preempted.

M = {M_1,M_2}

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Task Graph Scheduling

Optimal Static Task Scheduling

- Task **P**={P_1,.., P_m}
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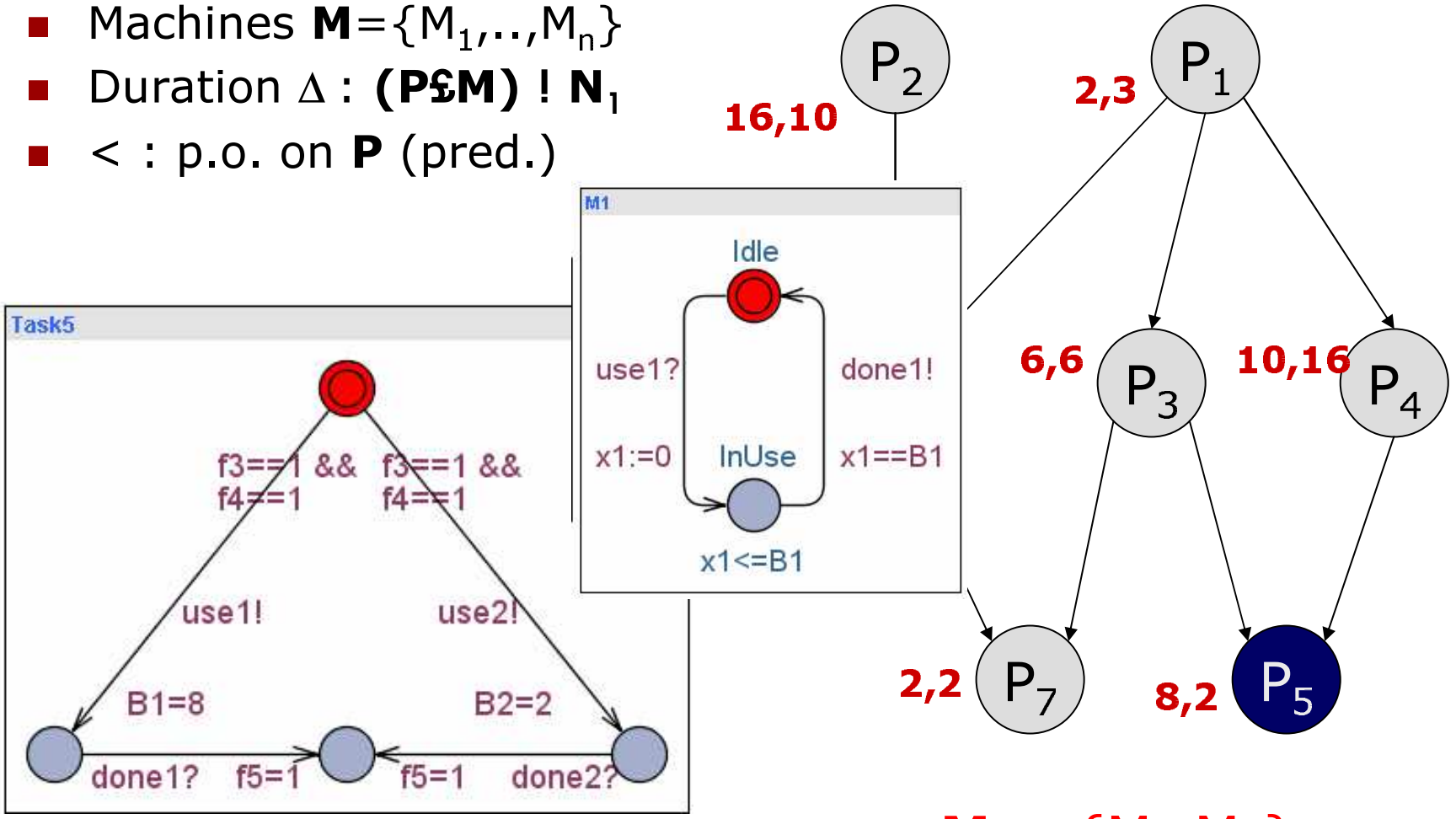


M = {M_1,M_2}

Experimental Results

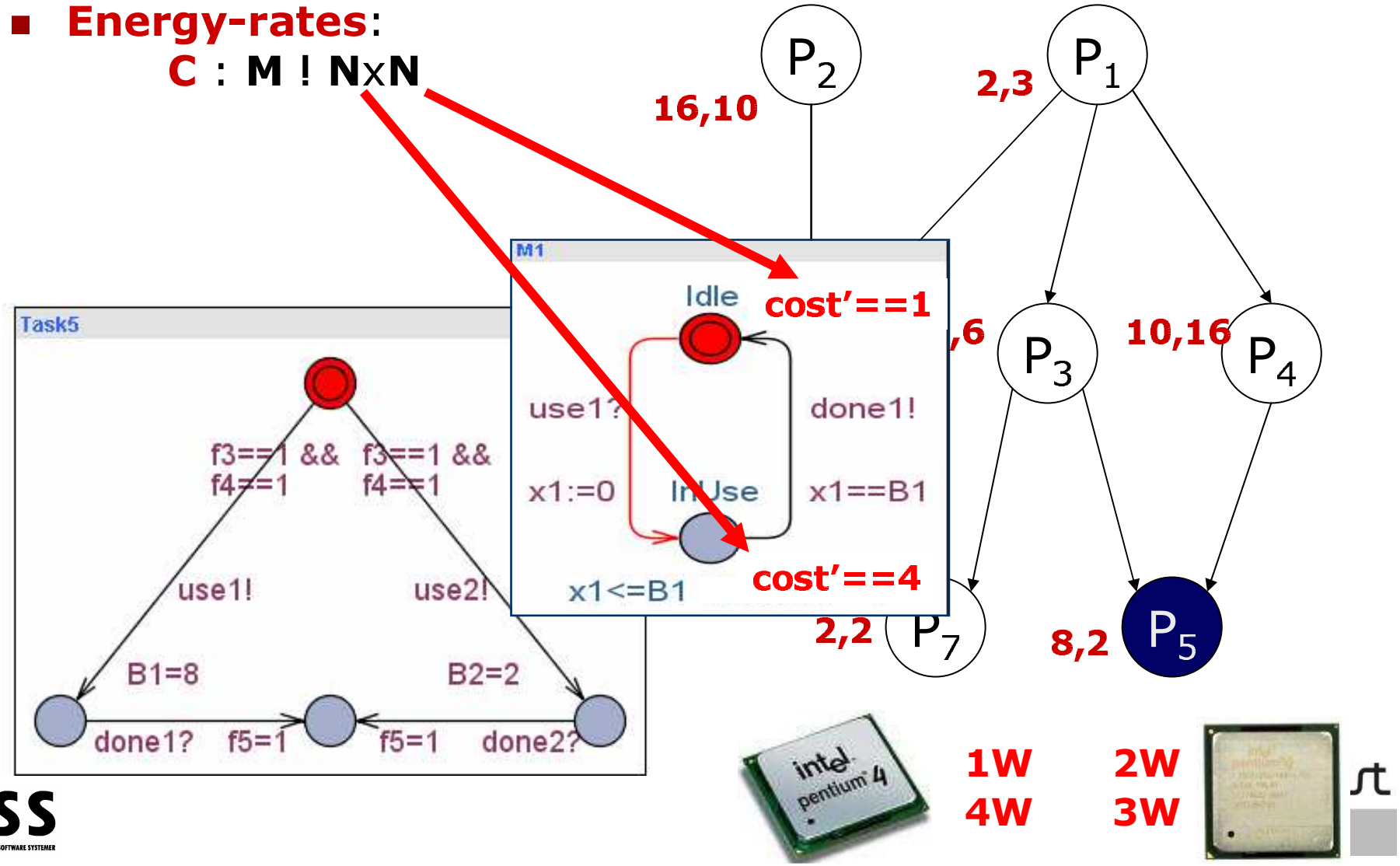
name	#tasks	#chains	# machines	optimal	TA
001	437	125	4	1178	1182
000	452	43	20	537	537
018	730	175	10	700	704
074	1007	66	12	891	894
021	1145	88	20	605	612
228	1187	293	8	1570	1574
071	1193	124	20	629	634
271	1348	127	12	1163	1164
237	1566	152	12	1340	1342
231	1664	101	16	t.o.	1137
235	1782	218	16	t.o.	1150
233	1980	207	19	1118	1121
294	2014	141	17	1257	1261
295	2168	965	18	1318	1322
292	2333	318	3	8009	8009
298	2399	303	10	2471	2473

Abdeddaïm, Kerbaa, Maler

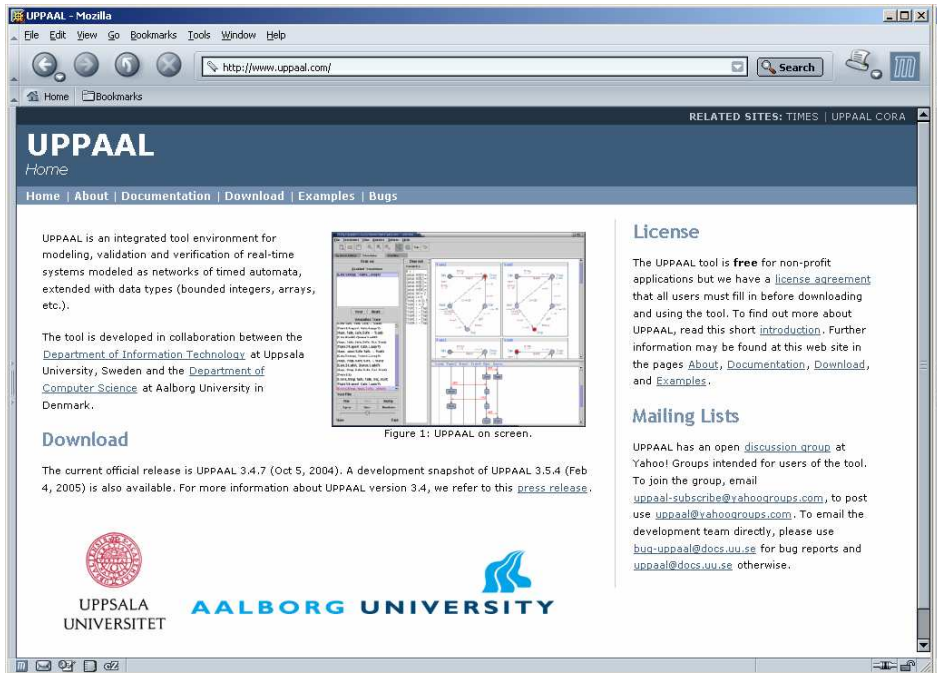
Optimal Task Graph Scheduling

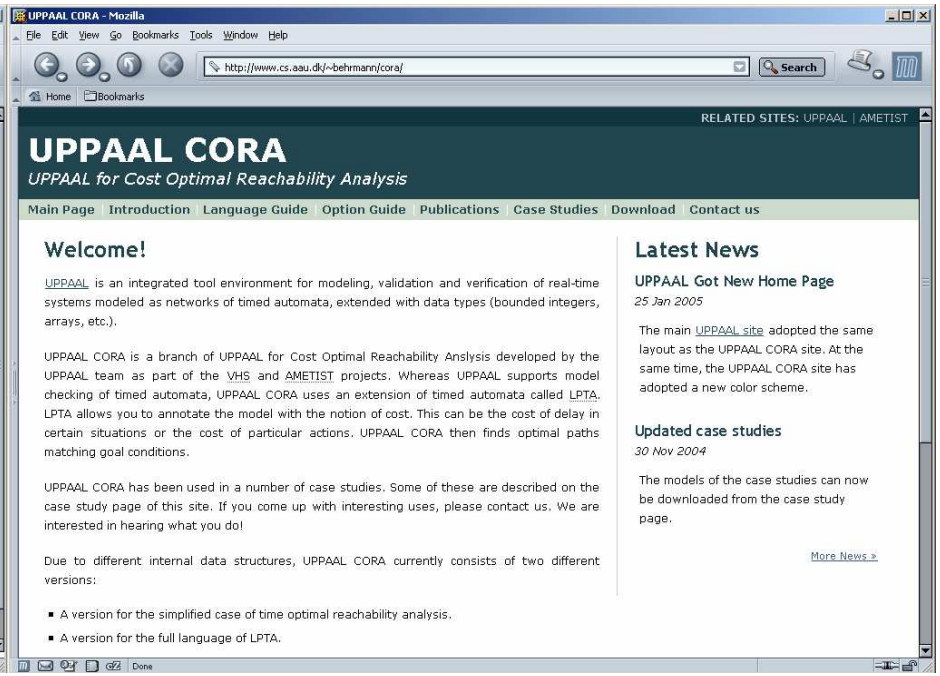
Power-Optimality

- **Energy-rates**:
  C : M ! NxN



Further Information





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