ARTIST2

Network of Excellence on Embedded Systems Design
September 2004 – August 2008

Joseph Sifakis, Bruno Bouyssounouse
Verimag Laboratory
History

ARTIST - FP5 Accompanying Measure (2002-2005):

- Coordinate the R&D effort in the area of Advanced Real-time Systems
- Improve awareness of academics and industry in the area
- Define innovative and relevant work directions

Achieved through activities along 3 axes:

- Roadmaps for selected actions:
  (Hard Real Time, Component-based Design, Adaptive Real Time, Execution Platforms)
- International Collaboration
- Education

Information about these results is publicly available:
http://www.artist-embedded.org/Roadmaps/
Objectives

Reinforce and strengthen scientific and technological excellence in Embedded Systems Design:

• The NoE will act as a Virtual Center of Excellence

• Two levels of integration to create critical mass from selected European teams
  
  ➢ Strong integration within selected topics by assembling the best European teams, to advance the state of the art in the topic.

  ➢ Integration between topics to achieve the multi-disciplinary excellence and skills required for the development of future embedded technologies.

• Integration will be around a Joint Programme of Activities
Selected Topics: ARTIST2 Clusters

- Real-Time Components
- Adaptive Real-Time
- Compilers & Timing Analysis
- Execution Platforms
- Testing and Verification

Control for Embedded Systems
<table>
<thead>
<tr>
<th>Short Name</th>
<th>Full Name and Country</th>
<th>Key researchers</th>
</tr>
</thead>
<tbody>
<tr>
<td>CDC</td>
<td>Caisse des Dépots et Consignations (France)</td>
<td>None</td>
</tr>
<tr>
<td>UJF / Verimag</td>
<td>University Joseph Fourrier / Verimag (France)</td>
<td>Paul Caspi, Susanne Graf, Nicolas Halbwachs, Yassine Lakhnech, Oded Maler, Joseph Sifakis</td>
</tr>
<tr>
<td>Aachen</td>
<td>RWTH Aachen (Germany)</td>
<td>Rainer Leupers</td>
</tr>
<tr>
<td>Aalborg</td>
<td>BRICS – Aalborg University (Denmark)</td>
<td>Kim Larsen, Anders Ravn</td>
</tr>
<tr>
<td>AbsInt</td>
<td>AbsInt Angewandte Informatik GmbH (Germany)</td>
<td>Christian Ferdinand</td>
</tr>
<tr>
<td>Aveiro</td>
<td>University of Aveiro (Portugal)</td>
<td>Luis Almeida</td>
</tr>
<tr>
<td>Cantabria</td>
<td>Universidad de Cantabria (Spain)</td>
<td>Michael Gonzalez Harbour</td>
</tr>
<tr>
<td>CEA</td>
<td>Commissariat à l’Énergie Atomique – Laboratoire LIST (France)</td>
<td>François Terrier</td>
</tr>
<tr>
<td>CFV</td>
<td>Centre Fédéré en Vérification, Université de Liège (Belgium)</td>
<td>Pierre Wolper</td>
</tr>
<tr>
<td>Czech TU</td>
<td>Czech Technical University (Czech Republic)</td>
<td>Vladimir Kucera</td>
</tr>
<tr>
<td>Dortmund</td>
<td>Dortmund University (Germany)</td>
<td>Peter Marwedel</td>
</tr>
<tr>
<td>DTU</td>
<td>Technical University of Denmark (Denmark)</td>
<td>Jan Madsen</td>
</tr>
<tr>
<td>ETHZ</td>
<td>Swiss Federal Institute of Technology – Zurich (Switzerland)</td>
<td>Lothar Thiele, Manfred Morari</td>
</tr>
<tr>
<td>FTR&amp;D</td>
<td>France Telecom R&amp;D</td>
<td>Pierre Combes, Kathleen Milsted</td>
</tr>
<tr>
<td>INRIA</td>
<td>Institut National de Recherche en Informatique et Automatique (France)</td>
<td>Albert Benveniste, Benoît Caillaud, Alain Girault, Thierry Jéron, Jean-Marc Jézéquel, Paul Le Guernic, Eric Rutten, Yves Sorel, Robert de Simone</td>
</tr>
<tr>
<td>KTH</td>
<td>Royal Institute of Technology (Sweden)</td>
<td>Martin Törngren</td>
</tr>
<tr>
<td>Linköping</td>
<td>Linköping University (Sweden)</td>
<td>Petru Eles</td>
</tr>
<tr>
<td>LSV / CNRS</td>
<td>Centre National de la Recherche Scientifique / Laboratoire LSV (France)</td>
<td>Michel Bidoit, Hubert Comon, Philippe Schnoebelen</td>
</tr>
<tr>
<td>Core Partner</td>
<td>Short Name</td>
<td>Full Name and Country</td>
</tr>
<tr>
<td>--------------</td>
<td>------------</td>
<td>---------------------------------------------</td>
</tr>
<tr>
<td>19</td>
<td>Lund</td>
<td>Lund University (Sweden)</td>
</tr>
<tr>
<td>20</td>
<td>Mälardalen</td>
<td>University of Mälardalen (Sweden)</td>
</tr>
<tr>
<td>21</td>
<td>OFFIS</td>
<td>Kuratorium OFFIS e. V. (Germany)</td>
</tr>
<tr>
<td>22</td>
<td>PARADES</td>
<td>PARADES EEIG (Italy)</td>
</tr>
<tr>
<td>24</td>
<td>UP Madrid</td>
<td>Universidad Politecnica de Madrid (Spain)</td>
</tr>
<tr>
<td>25</td>
<td>Saarland</td>
<td>Saarland University</td>
</tr>
<tr>
<td>26</td>
<td>STM</td>
<td>ST Microelectronics – Central R&amp;D (France)</td>
</tr>
<tr>
<td>27</td>
<td>Eindhoven</td>
<td>Technical University of Eindhoven (Netherlands)</td>
</tr>
<tr>
<td>28</td>
<td>TU Vienna</td>
<td>Technical University of Vienna (Austria)</td>
</tr>
<tr>
<td>29</td>
<td>TUBS</td>
<td>Technical University Braunschweig (Germany)</td>
</tr>
<tr>
<td>30</td>
<td>Twente</td>
<td>University of Twente (Netherlands)</td>
</tr>
<tr>
<td>31</td>
<td>UoB</td>
<td>University of Bologna (Italy)</td>
</tr>
<tr>
<td>32</td>
<td>Uppsala</td>
<td>Uppsala University (Sweden)</td>
</tr>
<tr>
<td>33</td>
<td>UPVLC</td>
<td>Universidad Polytecnica de Valencia (Spain)</td>
</tr>
<tr>
<td>34</td>
<td>York</td>
<td>University of York (UK)</td>
</tr>
<tr>
<td>35</td>
<td>Porto</td>
<td>Polytechnic of Porto</td>
</tr>
<tr>
<td>36</td>
<td>EPFL</td>
<td>Ecole Polytechnique Fédérale de Lausanne</td>
</tr>
<tr>
<td>37</td>
<td>Pisa</td>
<td>Scuola Superiore Sant'Anna (Pisa)</td>
</tr>
<tr>
<td>38</td>
<td>Ace</td>
<td>Ace</td>
</tr>
<tr>
<td>39</td>
<td>Tidorum</td>
<td>Tidorum</td>
</tr>
<tr>
<td>40</td>
<td>Kaiserslautern</td>
<td>University of Kaiserslautern</td>
</tr>
</tbody>
</table>
ARTIST2 NoE : Team Leaders

Real Time Components

Hard Real Time
Albert Benveniste – INRIA
Alberto Sangiovanni – PARADES
Paul Caspi – Verimag
Hermann Kopetz – TU Vienna
Werner Damm – OFFIS

Modeling and Components
Bengt Jonsson – Uppsala
François Terrier – CEA/LIST
Jean-Marc Jezequel – INRIA
Susanne Graf – Verimag
Tom Henzinger - EPFL

Adaptive Real-time
Giorgio Buttazzo – Pisa
Alan Burns – University of York
Michael Gonzalez - Cantabria
Luis Almeida – Aveiro
Gerhard Fohler – Kaiserslautern
Juan de la Puente – Polytechnic de Madrid

Testing & Verification
Kim Larsen - Aalborg/ CISS
Ed Brinksma – Twente/Eindhoven
Pierre Wolper – Centre Fédéré de Verification
Michel Bidoit - LSV
Thierry Jeron - INRIA

Control for Embedded
Karl-Erik Arzen – Lund
Martin Torngren – KTH
Alfons Crespo – UP Valencia
Vladimir Kucera - Czech TU

Compilers and Timing Analysis
Reinhard Wilhelm - Saarland
Rainer Leupers - Aachen
Christian Bertin – ST Microelectronics
Christian Ferdinand – AbsInt
Peter Marwedel - Dortmund
Puschner, Krall – TU Vienna
Bjorn Lisper –Maalardalen
Guillem Bernat – University of York
Joseph van Vlijmen – Ace
Niklas Holsti - Tidorum

Execution Platforms
Lothar Thiele – ETH Zurich
Jan Madsen –DTU (TU Denmark)
Luca Benini – UoB
Petru Eles – ESLAB/Liu
Rolf Ernst – UBR
Josef Hooman - Eindhoven
Joint Programme of Activities

JPA
Joint Programme of Activities

JPIA
Joint Programme of Integration Activities
  a. Sharing research platforms, tools, and facilities
  b. Staff mobility and exchanges

JPRA
Joint Programme of Research Activities
  NoE Integration
  Cluster Integration:
  a. Real Time Components
  b. Adaptive Real-Time
  c. Compilers, and Timing Analysis
  d. Execution Platforms
  e. Testing, Verification
  f. Control for ES

JPASE
Joint Programme of Activities to Spread Excellence
  a. Education & Training
     - Courseware
     - Graduate Studies
     - Summer Schools
  b. Dissemination and communication
  c. Industrial Liaison
  d. International Collaboration

JPMA
Joint Programme of Management Activities
  a. Strategic Management
  b. Operational Management
Affiliated Industrial Partners

Christer Norström
Göran Arinder

Sven Holme Sørensen

Dr. Michael Winokur

Magnus Hellring

ABB

SIEMENS

Volvo

Thomas Thurner
Matthias Grochtmann

Roberto Zafalon

Petter Mårtensson

Jakob Axelsson

DAEWOO Chemical

ST

MAQUET

Volvo for life

Alain Ourghanlian

Dr. Kai Richter

Symta Vision

Johan Eker

ERICSSON

Dominique Potier

Thales

Philippe Baufreton

Hispano-Suiza

Fabian Wolf

Volkswagen

Vladimir Havlena

Honeywell

Magnus Hellring

Volvo