SEVENTH FRAMEWORK PROGRAMME
THEME ICT-1-3.4

Multi-Core Execution of Hard Real-Time Applications Supporting Analysability (MERASA)

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Overview

- Principal MERASA Research Focus
- MERASA Overall Strategy: phases, work packages and timeline
- Management Structure of MERASA
  - MERASA Partners/Beneficiaries
  - Industrial Advisory Board
- MERASA Administrative Information
- MERASA Next Steps

Principal MERASA Research Focus

- Processor architecture
  - In particular embedded high-perfomance processors
  - Hard-real-time capable design
  - Multi-core and multithreading
- WCET analysis tools for for multi-cores
  - Static WCET analysis – Otawa tool
  - Measurement-based WCET analysis – RapiTime tool
- System software for multi-cores
- Embedded hard-real-time applications: aerospace, automotive, construction machinery

Main Objectives of MERASA

OBJ1) to investigate the impact of using multi-core processors on static and measurement-based WCET analysability
- Outcome: a multi-core processor with high-performance features designed such that hard real-time threads can run in provable temporal isolation on different cores to enable accurate WCET analysability.

OBJ2) developing static and measurement-based WCET analysis techniques and tools
- Outcome: a thorough exploration of the high-performance features of the MERASA multi-core processor with respect to an effective WCET analysability with static and with measurement-based WCET analysis techniques and enhancements to the OTAWA and the RapiTime tools.

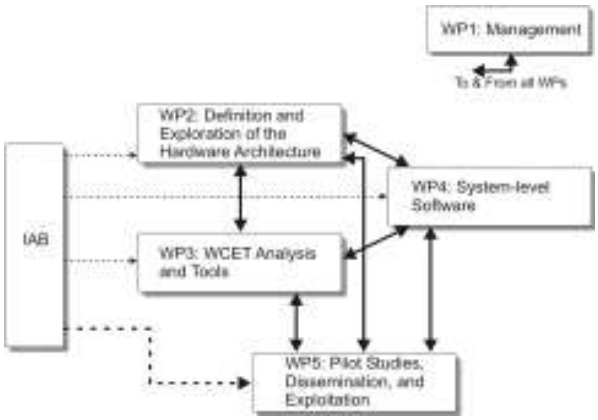
OBJ3) developing appropriate system-level software for MERASA multi-core processor

OBJ4) to verify the reached progress by pilot studies of industrial partners of aerospace (Honeywell, ESA, Airbus), automotive (Honeywell, Infineon Automotive Development AIM Department), and construction machinery (Bauer) areas.

MERASA Overall Strategy

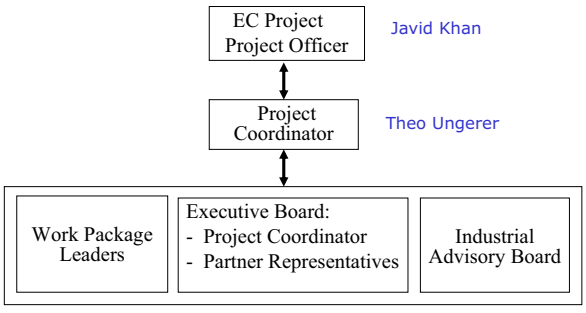
- **36 months in duration**, **5 work packages**
- structured in **three overlapping phases**:
  - **Phase 1: Design Space Exploration Phase:**
    Development and use of a high-level simulator starting with the CMP-SMT simulator already developed and used at BSC
  - **Phase 2: Architectural Refinement Phase:**
    Development and use of a much more accurate timing SystemC simulator starting with the single-core CarCore simulator already developed at University of Augsburg
  - **Phase 3: FPGA Prototyping and Pilot Study Phase**
    A very limited number of cores and high-performance features that fit on the FPGA.
    Pilot studies of IAB members.
- WCET tools and system software target the different prototypes.

Overview of relationships between work packages



MERASA Project Timeline

Management Structure of MERASA



MERASA Partners/Beneficiaries

- University of Augsburg (UAU, coordinator)
  - Architecture, system-level software, System-c simulator, and FPGA
- Barcelona Supercomputing Centre (BSC)
  - Architecture, software scheduling, high-level simulator
- Université Paul Sabatier, Toulouse (UPS)
  - WCET analysis
- Rapita Systems Ltd., York (RPT)
  - WCET analysis
- Honeywell spol. s.r.o., Bruno (HON)
  - Pilot studies

Tasks of the Industrial Advisory Board

- Provide advice and support to the project concerning technical and management decisions.
- Analyse the progress of project, help planning of future activities.
- Pilot studies by Industrial Advisory Board members fostered particularly in the last project phase.

- Industrial Advisory Board (IAB) integrated into the MERASA project planning.
- Meetings of IAB members with the Executive Board of MERASA project every 6 months

Industrial Advisory Board Members

- European Space Agency ESA
- Airbus, France
- Bauer Maschinen GmbH, Germany
- Infineon Technologies AG
  - Dept. AIM Automotive Industrial & Automotive, Germany
  - Infineon Technologies UK Ltd, UK
- NXP semiconductors, The Netherlands