Year Final Review
Brussels, December 12th, 2008

Achievements and Perspectives :

Compilers and Timing Analysis

Cluster leader : Peter Marwedel

TU Dortmund, Germany

High-Level Objectives

- Objectives
  - Code synthesis providing efficient embedded code
  - Coordination of work on timing analysis
- Evolution during the project:
  - Integration of compilers and timing analysis added
  - Shift toward source-to-source tools
  - Increasing importance of multi-core systems
- Industrial relevance:
  - Timing analysis tools have entered industrial practice
  - Code efficiency (in particular energy efficiency) very crucial
  - Compiler technology challenged due to appearing multi-processor systems

Members

- **TU Dortmund (Peter Marwedel et al.)**
- **TU Berlin (Sabine Glesner et al.)**
- **Mälardalen University (Björn Lisper et al.)**
- **RWTH Aachen (Rainer Leupers et al.)**
- **AbsInt (Christian Ferdinand et al.)**
- **ACE (van Someren et al.)**
- **Saarland University (Reinhard Wilhelm)**
- **Tidorum (Niklas Holsti et al.)**
- **TU Vienna (P. Puschner, A. Krall, M. Schordan et al.)**
- **University of York (Guillem Bernat)**
- IMEC* (Francky Catthoor, Stylianos Mamagkakis)
- IRISA* (Isabelle Puaut)

* Affiliated

State of the Integration in Europe

- Starting point: fragmented research scenery
  - National boundaries, multiple approaches for TA
  - Each group too small for the problems at hand
- ☞ Interaction of the Cluster with other communities required and implemented
  - With other clusters of the NoE (in particular exec. platforms)
  - With other networks (Hipeac, KDUbiq, …)
  - With industry (ACE, Philips, ST, Infineon, Coware, NXP…)
  - …

Building Excellence

- Cluster meetings, activity meetings
- Workshops (SCOPES, WCET, …)
- Summer Schools (China, South America, cooperation with KDUbiq, AIIT (Seoul), ACACES (☞ hipeac), …)
- ☞Artist2 improved cooperation
  - Education (ALARI, …)
  - Text book, comes along with educational material
  - Joint and individual publications
  - Joint projects defined (Predator, Mnemee, ALL-TIMES, ..)
  - Several extensions made to existing CoSy platform
  - Other extensions platform independent (source2source)
  - WCET challenge identified necessary cooperation
  - …

Year 4 Review
Brussels, December 12th, 2008

Achievements and Perspectives :

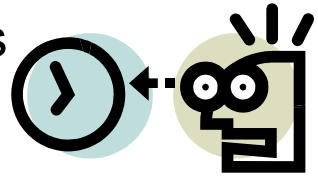
Compilers activity

Activity leader: Sabine Glesner

Affiliation: TU Berlin

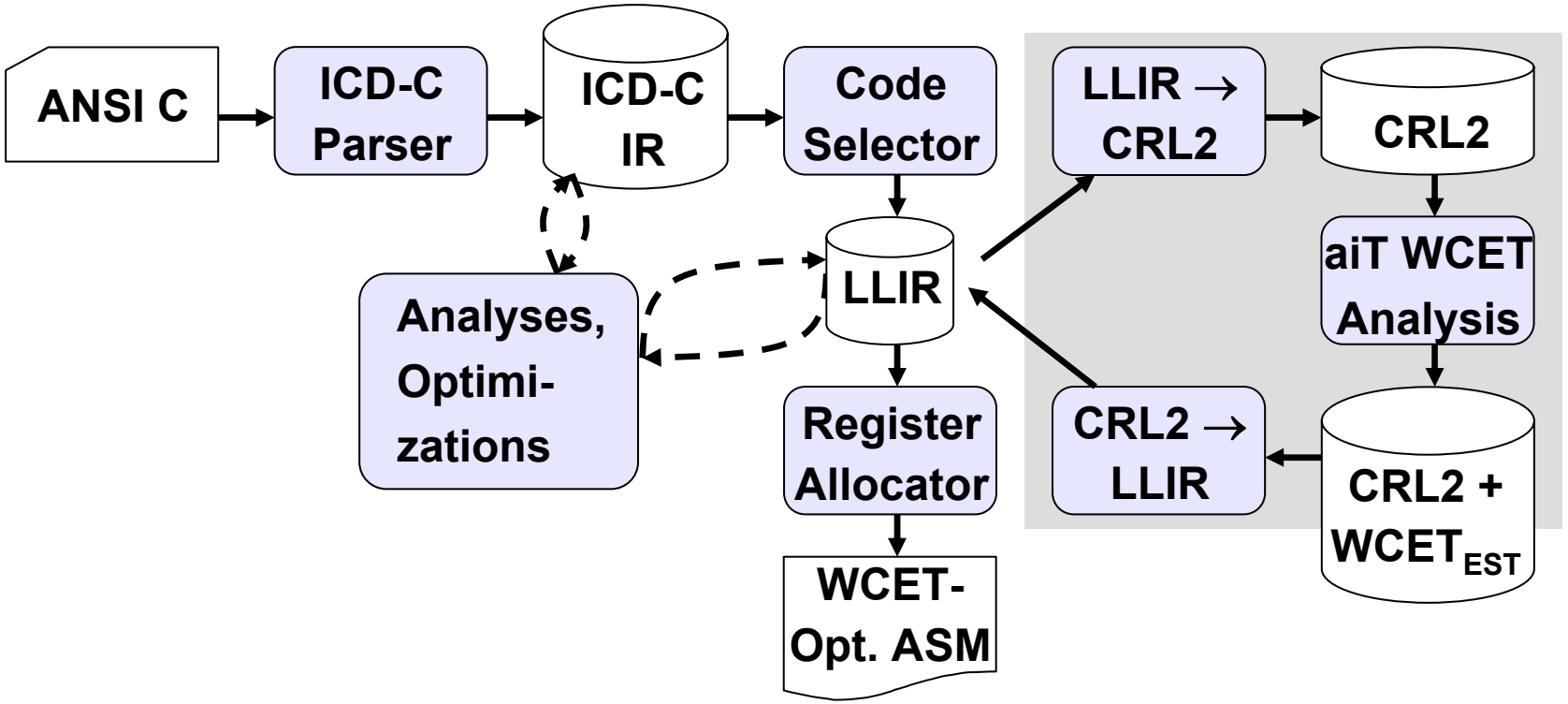
Integration of compilers and timing analysis (1)

- Aims and goals
  - Modelling of time a distinguishing feature of embedded software
  - Re-introducing time into models of computing platforms
  - Using single timing model in the tool flow
  - Explicitly using WCET as a cost function in optimizations
  - Enable explicit trade-off between WCET and other criteria
  - Avoiding long trial-and-error sequences of compiler runs with modified parameters
  - Obtain code optimized for minimum WCET for critical (automotive, avionics) applications
  - Demonstrating resulting potential benefits



Integration of compilers and timing analysis (2)

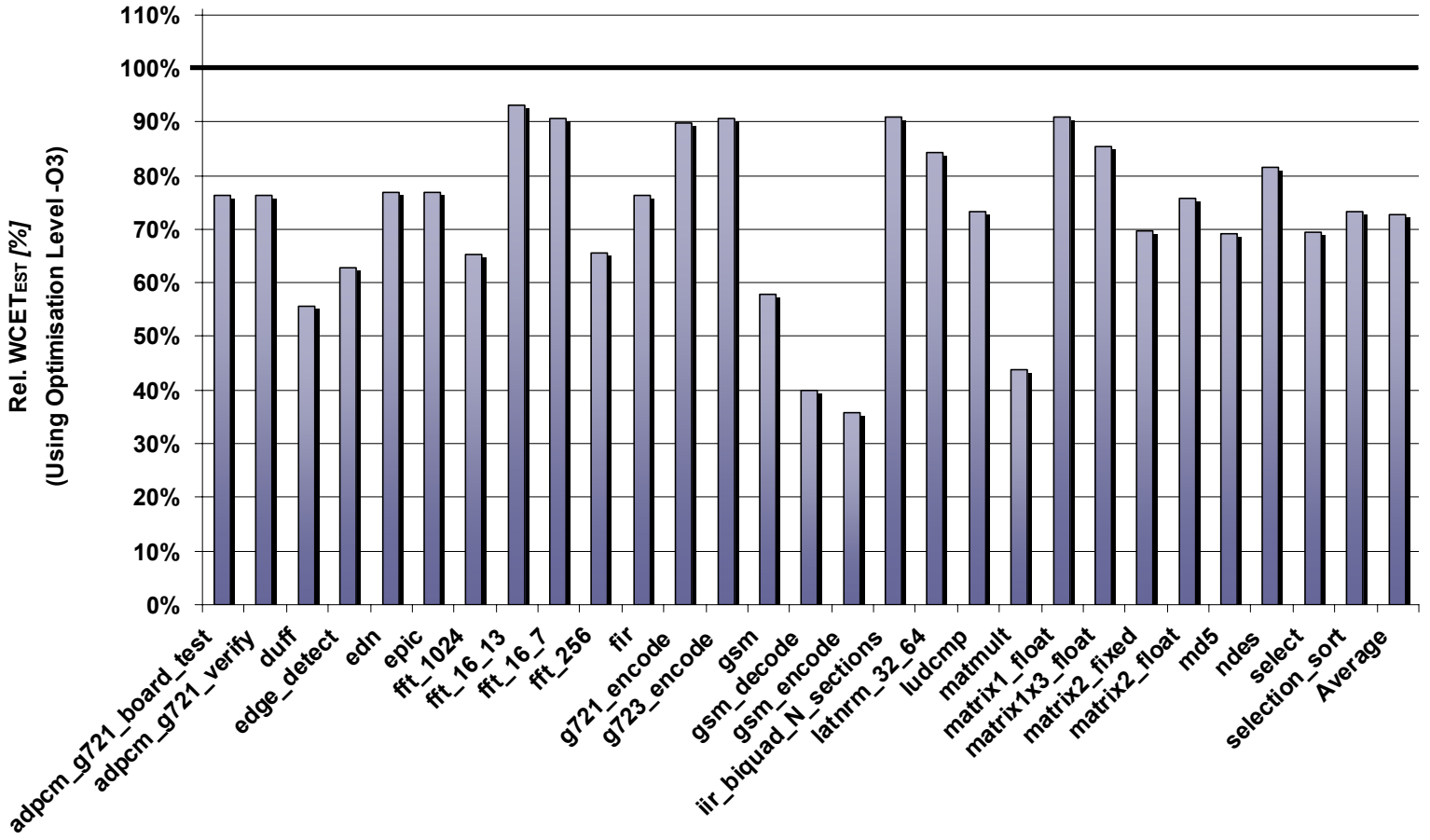
Approach



WCET information generated by aiT available during optimizations on intermediate representations IR and LLIR

Integration of compilers and timing analysis (3)

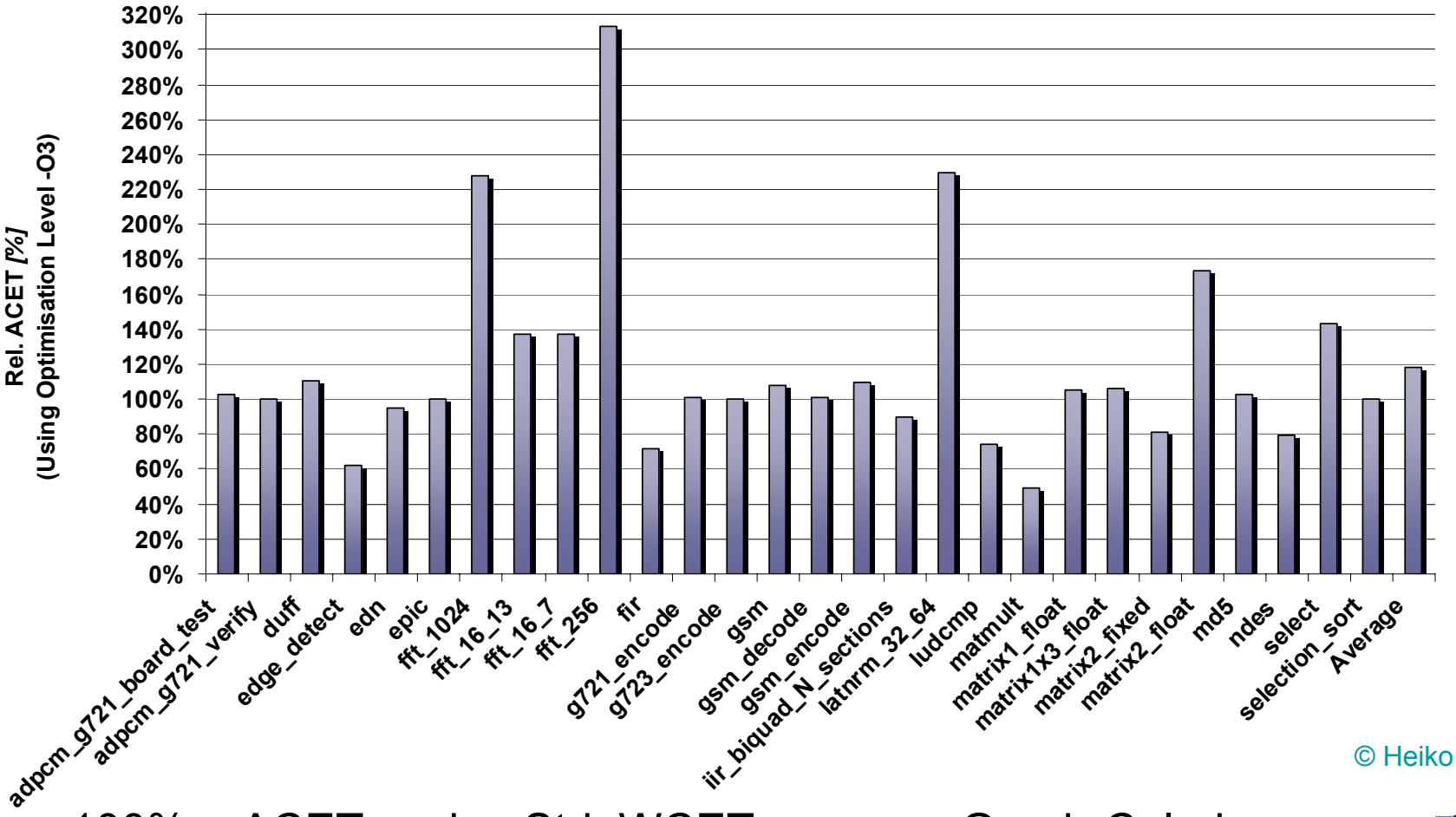
Results – $WCET_{EST}$ Reductions



100% = $WCET_{EST}$ using Std. WCET-unaware Graph-Coloring

Integration of compilers and timing analysis (4)

Results – Simulated Execution Times



100% = ACETs using Std. WCET-unaware Graph-Coloring

Generation of efficient embedded code (1)

- Exploitation of memory hierarchies
  - Extraction of memory hierarchy specific information
  - Scratch pads (SPM) now considered a viable alternative to caches
    - Paper from TU Dortmund #2 in citations at ISSS/CODES 1996-2006 (according to F. Vahid, ISSS/CODES 2008)
    - Unique dynamic memory allocator from IMEC, which is compiled with the software application, MH tools being made available
    - Samsung hired SPM specialist

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Generation of efficient embedded code (2)

- Extensions of the CoSy Platform
  - SIMD-enabling loop transformations
  - Conditional execution
- Formalized the scheduling phase in a theorem prover
  - Discovered a bug in the scheduler of the GNU assembler

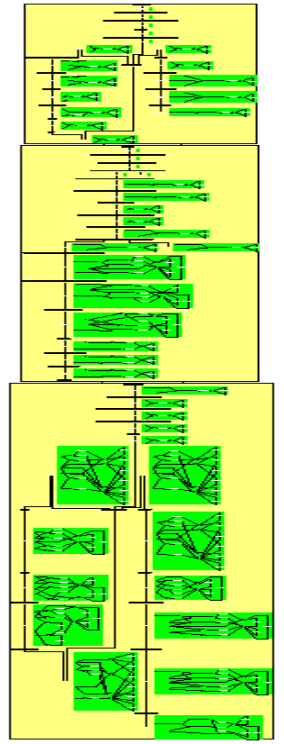
RWTH AACHEN
RHEINISCH-WESTFÄLISCHE TECHNISCHE HOCHSCHULE AACHEN

TU berlin

ACE

Generation of efficient embedded code (3)

- Automatically generated may/must alias pairs as C++ program annotations
- Generated external program representation for tool interoperability



TU WIEN
Technische Universität Wien
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Angewandte Informatik

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Achievements and Perspectives :

Timing Analysis activity

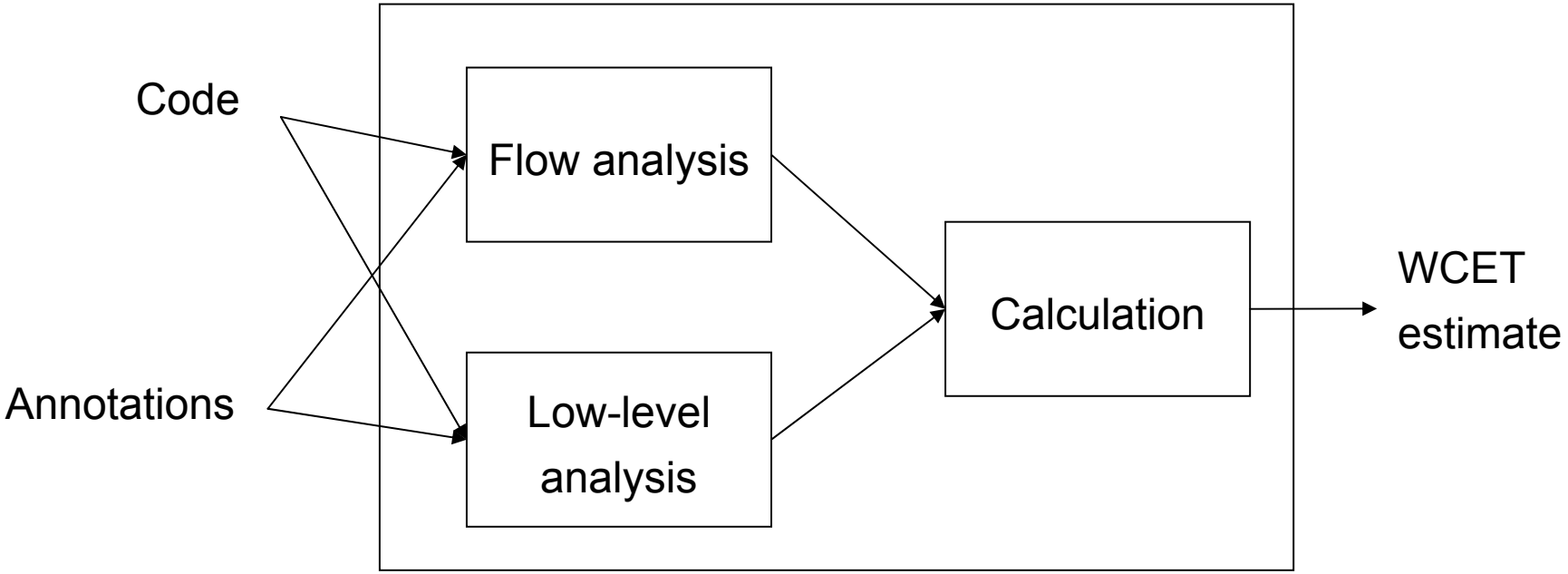
Activity leader: Björn Lisper

Affiliation: MDH

Timing Analysis in Artist2

- Tool integration and -interfacing
- “Services to the scientific community”
- Selected scientific highlights

WCET Analysis Tool Structure



WCET Tool Integration

- **Aim:** use the best of all the worlds in TA
- CRL2 (later AIR) chosen as common interchange format
- CFG representation carrying code, analysis results, and other information
- C++ library
- Used in:
  - Integration of compilers and timing analysis
  - Experiments with tree-based representations on top of CFG (timing schema calculations)
- CRL2/AIR forces use of C++, rewrite of existing code
- Textual format defined, allows less tight integration

Interfaces

- Trend towards tool interfacing rather than tool integration
- Allows looser integration, wrapping analysis components rather than rewriting them
- “ALF” code format for flow analysis has been defined:
  - a common interface for many different code formats
  - a single tool can analyze different kinds of code (source and binary level)
- Investigation into common flow description attributes
- Work is continued in the ALL-TIMES project

Mälardalen WCET Benchmark Suite

- A collection of WCET analysis benchmark programs
- For each benchmark program;
  - Source code
  - Precompiled binary (gcc, Renesas H8/300 CPU)
  - Classification w.r.t. different attributes
  - Actual WCET
- Has become much used, also outside WCET analysis community
- http://www.mrtc.mdh.se/projects/wcet/benchmarks.html

WCET Challenge

- Bi-annual event (2006, 2008 so far)
- Evaluation of WCET analysis tools using standardized benchmarks, compilers, hardware
- Different aspects evaluated: precision of WCET estimate, level of automation, ...
- Will turn into a continuous event (within ARTIST-DESIGN), self-managed through wiki, homepage serves as “tool display”
- http://www.mrtc.mdh.se/projects/WCC08/

Timing Analysis and Timing Predictability

- Influence of cache architecture on timing predictability
- Turns out that the replacement policy can make a big difference
- LRU well-behaved, other common policies yield *very poor predictability* of worst case
- Memory performance may differ by a constant *factor* depending on initial cache state
- Breaks common assumption of bounded penalty for context-switches in preemptive scheduling

WCET Analysis for Systems with Preemptive Scheduling

- Necessitated by the findings about timing predictability
- Computes set of possibly evicted cache entries at preemption
- This information is used in the subsequent WCET analysis

Parametric WCET analysis

- Computes WCET as a formula in input parameters rather than a single number
- Initial ideas from Mälardalen
- Integrated in a parametric version of aiT for PowerPC
- Provides proof of concept
- Comparison with non-parametric analysis shows reasonable precision

Timing Analysis: Future and Perspectives

- Multicore/MPSoC provide formidable challenges
- Timing predictability of HW architectures decreases unless something is done
- Tool interfacing still important, as interaction with compilers
- ARTIST-DESIGN, PREDATOR will address predictability issues for Multicore/MPSoC
- Tool interfacing continues in ALL-TIMES

Overall Assessment at the end of the NoE

- Artist2 has significantly improved the cooperation between researchers, in particular at the European level
  - ☞ several joint European projects
- Visibility of European research has been improved
  - ☞ invitation by Korean advanced institute of information technology
- The embedded system world has undergone substantial changes since the start of ARTIST2
  - The importance of compilers has been recognized due to the transition toward multi-core systems
  - The importance of timing models for embedded software is being more widely recognized.
- Performed work provides lasting platform
  - ☞ CoSy integration, WCC, …

Lasting Impact, for example:

- Better understanding of the embedded research community in Europe.
- ARTIST2 led to the formation projects such as PREDATOR, Mnemee, All-times, …
- Lasting results on resource-efficient compilation
  Scratch pads, predication, SIMD, ….
- Connection between compiler and TA activities through the cooperation TU Dortmund/AbsInt and SATIRE.
- The WCET Tool Challenge provided for the first time insight into the relative strengths of the approaches
- Joint research in parametric timing analysis
- Understanding of IRs or tool (component) couplings

Conclusion

- Integration of Compilers and Timing analysis
  - 1st comprehensive integration ever, leads to a reconsideration of many of the compiler optimizations
- Compilers
  - Cooperation led to integration into the CoSy platform
  - Several approaches for generating efficient code
- Timing analysis
  - Björn: propose something

Building Excellence

Complete table!

	Compilers		Timing analysis	
	Y4	Total	Y4	Total
Individual publications	10			
Joint publications	3			
Workshops	2		1	
Keynotes, lectures	1			
Tutorials, courses	3			
Joint projects	Predator, Mnemee, All-times, Mosart, …			
Visits				
Invitations	AIIT (Seoul), MIT (Auckland), KDUbiq, …			
Cooperation with industry	ACE, ST, NXP, Infineon, AbsInt, Airbus, Bosch,			