IST-004527 ARTIST2
Network of Excellence
on Embedded Systems Design

Cluster Progress Report for Year 4

Cluster:
Compilers and Timing Analysis

Cluster Leader:

Prof. Dr. Peter Marwedel (TU Dortmund)
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Policy Objective (abstract)

Compilation tools and their associated technologies play a fundamental role for the implementation of a system on a given target platform. For embedded systems, we need tools capable of combining platform independent software and a description of the target platform, to generate executable code having the desired properties related to resources such as memory, power, energy, network bandwidth, and computation time. The main objective is to strengthen the European research community in the area of compilers and timing analysis for embedded processors by two major activities in the excellence areas of the partners: (1) compilers for embedded processors, exploiting a common compiler platform and resource aware compilation (2) timing analysis for embedded processors. Coupling timing analysis tools with compilation tools enables resource-aware compilation incorporating worst case execution time information.

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1. Overview

1.1 High-Level Objectives

This cluster is composed of the two areas Compilation and Timing Analysis. There are overlaps in the research areas. The emphasis in the activities is on the platforms for the two areas and on one approach to combine both areas. The contributions in this cluster document are split into a **Timing-Analysis** and a **Compilation** part. Additional contributions are described in activity reports. In addition, information regarding the **link** between the two is included.

The objectives on the **Timing-Analysis** side are:

- to achieve a common representation for an intermediate exchange format for the various timing analysis components from the different partners,
- to achieve an integration of different modules from different partners for timing analysis,
- to foster research addressing existing and new timing analysis challenges.

Run-time guarantees play a key role in embedded systems and especially in hard real-time systems. Such systems are typically subject to stringent timing constraints. It is essential that the computations are completed within their time bounds. Therefore, a schedulability analysis has to be performed which guarantees that all timing constraints will be met. All existing techniques for schedulability analysis require the worst case execution time (WCET) of each task in the system to be known before the task is executed. Since in general, the problem of computing WCETs is not decidable, estimations of the WCET have to be calculated. These estimations have to be safe, i.e., they may never underestimate the real execution time. Furthermore, they should be tight, i.e., the overestimation should be as small as possible.

The objectives on the **Compilation** side are

- to provide world-class code-synthesis and compiler tools for the generation of efficient machine code, including the integration of existing compiler-generation approaches,
- to provide resource-aware compilation techniques which reduce the overhead introduced by compilation to a level which is acceptable even for very resource-constrained designs.

The integration of compiler-generation approaches has been enabled through the use of the CoSy compiler platform. Resource-aware compilation aims at the exploitation of known hardware characteristics such as the underlying memory hierarchy.

Link between Compilation and Timing Analysis: Tools for estimating WCET and compilers have traditionally evolved as independent classes of tools. This results in information lacking in both kinds of tools which, however, is available in the other set of tools. Traditional approaches for adding the missing information result in a duplication of efforts: regeneration of flow facts in timing analysis tools and adding timing as a cost function in compilers. The partners aimed at avoiding this duplication of efforts.

1.2 Industrial Sectors

Timing Analysis: During the previous years, timing-analysis tools entered industrial practice and are in routine use in the aeronautics and automotive industry. AbsInt's timing-analysis tool, aiT, has been used in the certification of time-critical subsystems of the Airbus A380 and has thus acquired the status of a *validated* tool. WCET estimations are relevant for all industrial sectors using hard real-time systems. Therefore, industrial sectors in this case include avionics, automotive, defence and some areas where control systems are applied. Especially in the automotive and the aeronautical domains, there is a need to have precise knowledge on the worst-case timing behaviour of safety critical software. This need is underlined by the fact

that the worst-case timing of large parts of the software used within the new Airbus A380 has been analyzed using AbsInt's aiT.

Compilers: The work performed in the cluster is relevant for all industrial sectors using embedded software. This includes semiconductor houses, system houses, companies working on audio processing, video processing, data streaming applications in the TV, Set Top boxes, DVD players and recorders, mobile phones, base stations, printers and disk drives. Efficiency of embedded software, in particular the efficiency of memories, is relevant for high-speed embedded systems. It is expected that most mobile devices will provide some kind of multimedia processing.

Link between timing analysis and compilers: The availability of precise timing analyses does not fulfil all industrial needs. Since the code of safety critical applications is typically generated by a compiler, the compiler should also be aware of worst-case timings. Currently, this is not the case leading to the unacceptable situation that, whenever it is detected that an application does not meet its real-time constraints, manual code transformation, recompilation and timing analysis need to be done repeatedly.

1.3 Main Research Trends

Timing analysis: The construction of timing-analysis tools is difficult, tedious, and error-prone. Research has been performed to develop computer support for this task. A standard tool architecture for WCET analysis has evolved. Typically, several phases can be distinguished:

1. In a first phase, which may itself consist of several subphases, the software is analyzed to determine invariants about the sets of execution states at each instruction. Abstract interpretation is mostly used for this phase. The invariants constrain the possible program flows, as well as allowing the prediction of conservative execution times for individual instructions and for basic blocks.
2. A second phase determines a worst-case path through the program. This is often done by implicit path enumeration; the control flow is translated into an integer linear programming problem and then solved.

For non-hard real time tasks, measurement-based methods are being evaluated and tested.

Compilers: Embedded system software (if compared to hardware) usually involves a significant overhead in terms of energy consumption and execution time. However, for flexibility reasons, hardware cannot be used in applications with changing requirements. In order to make a software implementation feasible, efficiency of embedded software is a must. Due to the efficiency requirements, using power-hungry, high-performance off-the-shelf processors from desktop computers is infeasible for many applications. Various approaches for achieving this efficiency have been explored.

1. Using customized processors is becoming more common. These processors are optimized for a certain application domain or a specific application. As a consequence, corresponding processors have appeared in the semiconductor market.
2. Source-to-source level transformations are another approach for improving the efficiency of embedded software. These transformations are applied before any compiler is started. The advantage is that it can be used with almost any compiler.
3. A third approach is the use of sophisticated optimizations within a compiler. Optimizations tuned towards embedded systems have been designed by a number of members of the ARTIST2 compiler cluster. Due to the increasing importance of the memory interface, various memory-aware optimizations have been designed.

Objectives and trends are described in the activities reports in more detail.

2. State of the Integration in Europe

2.1 Brief State of the Art

Timing Analysis: Several commercial WCET tools are available. They have experienced positive feedback from extensive industrial use in the automotive and aeronautics industry. The existing tools serve some particular and highly relevant points in this space. AbsInt's tool for example has been used in the development and the certification of safety-critical systems in the Airbus A380. On the other hand, they currently do not serve distributed architectures well.

Compilers: A large number of compiler platforms are available in industry and academia, e.g. GCC (GNU), LANCE (Dortmund/Aachen), OCE (Atair/Mentor), SUIF (Stanford), ICD-C (ICD/Dortmund) and CoSy (ACE). Compiler platforms are usually conceived as software systems that allow for quick development of compilers for new target machines and that permit efficient research by means of an open, easily extensible infrastructure. Each of the available platforms has its specific strengths and weaknesses w.r.t. openness, IP rights issues, code quality etc. Furthermore, different platforms serve different research requirements. Therefore, it is expected that the heterogeneous platform landscape will continue to exist in the future.

Timing problems are expected to become more severe in the future, due to the increasing speed gap between processors and memories. Due to this gap, efforts for improving the performance of systems have been predicted to hit the "memory wall". Work was done in the context of caches (loop caches, filter caches etc.). However, these approaches have mostly focussed on hardware approaches for reaching the goals. For these approaches, compilers were considered to be black boxes and untouchable. Only few authors (e.g. Barua, Catthoor, Dutt, Kandemir) have taken a holistic approach, looking at hardware and software issues.

2.2 Main Aims for Integration and Building Excellence through Artist2

The Compiler and Timing Analysis Cluster and the Execution Platforms Cluster aim at developing a common methodology to enable resource aware design and compilation. The aim of this integration activity is to increase predictability while retaining a performant system. The main aim of using the ARTIST2 network is to get access to competences, knowledge and tools which are not available locally at each of the institutions. The cooperation provides the required size of research teams, necessary to handle the complexity of today's technology. Furthermore, a major goal is the combination of areas of excellence of the different partners by defining and implementing interfaces between their design flows and tools in order to achieve compilation platforms applicable to a wider problem scope.

To compute the WCET of programs in general, additional flow information is needed to guide the WCET computation. Due to different research approaches and framework architectures, there exist many different flow description languages for WCET analysis, making it hard to connect different components of WCET analysis frameworks together. It was the ambitious goal within ARTIST2 to define flow description attributes that serve as an exchange format among different tool components. Partners worked together to define flow description attributes to enable an integration of WCET analysis components.

2.3 Other Research Teams

Essentially three more research teams have competed with Europe in the area of Timing Analysis, one at Seoul National University (SNU), one at Florida State University, now with some branches in North Carolina etc., and Singapore National University. Seoul has turned to

power-aware computing, and flash memory based components research. Singapore and Florida have cooperated with the ARTIST2 partners in writing a survey paper. Singapore has participated in the WCET Tool Challenge, arranged within ARTIST2, with their academic prototype. There is a continuous exchange of PhD students and PostDocs with the team of Prof. Sang Lyul Min at SNU.

Only few groups have been working on the integration of worst case execution times and compilers. Smaller, apparently volatile efforts have been reported from Sweden and South Korea. Some work was performed in the group of David Whalley at the Computer Science Department of the Florida State University. However, only very simplified timing models and highly predictable processor architectures are considered at Florida.

2.4 Interaction of the Cluster with Other Communities

Cluster members performed teaching activities (e.g. Peter Marwedel from Dortmund and Rainer Leupers from Aachen at ALARI, Lugano and EPFL, Lausanne) in cooperation with other ARTIST2 members (e.g. Luca Benini/Bologna and Lothar Thiele/Zürich). Further links of ARTIST2 members existed to the SHAPES project and to the HiPEAC Network of Excellence.

TU Dortmund:

The interaction with the local technology transfer centre ICD (see http://www.icd.de/index_eng.html) is key for interacting with industry. ICD is headed by Peter Marwedel. ICD is used for transferring research results to industry. The group promoted education in embedded systems through a published text book and through courses at EPFL, at ALARI and at spring or summer schools in New Zealand, China, Brazil, Portugal, Korea, and Germany. TU Dortmund organizes the SCOPES series of workshops on compilation for embedded systems.

RWTH Aachen:

A close cooperation existed with the ARTIST2 Execution Platforms cluster, in particular between Dortmund, Aachen, and Bologna University. RWTH Aachen participated in the HiPEAC network of excellence and started new cooperations related to code optimization, e.g. with Edinburgh University. Furthermore, Aachen maintained tight industry cooperations, e.g. with CoWare, ACE, and Infineon. Since Oct 2006, RWTH Aachen is running the UMIC research cluster (http://www.umic.rwth-aachen.de) of the German excellence initiative.

ACE:

ACE worked closely with ST and with Philips having both a commercial relationship with them as well as being co-members of EU project consortia – in one case along with Verimag. ACE has been working closely with Aachen in this domain for some time. One of the results of this cooperation has been the integration of compiler technology in a start-up company that span out of the university. Cooperation with Imperial College and Edinburgh has also started.

AbsInt:

Within the EmBounded Project (IST-510255), AbsInt was also involved in the development of the Hume compiler. Hume is a domain-specific high-level programming language for real-time embedded systems.

TU Berlin:

TU Berlin is generally involved in methods and tools for software engineering for embedded systems. TU Berlin has cooperated with Edinburgh University (Björn Franke) concerning the optimization of compilers based on machine learning techniques. Furthermore, TU Berlin has done research on the verification of embedded operating systems, also by cooperating with the Fraunhofer institute FIRST. Finally, TU Berlin visited and was visitied by other cluster members, e.g. ACE, RWTH Aachen and TU Vienna.

IMEC:

IMEC is integrated in European research networks, including HiPEAC. Moreover, IMEC is the central partner of a Marie Curie Host Fellowship project that involves more than 10 universities across Europe. IMEC also has many industry co-operations including most large European multi-media and communication systems oriented companies.

Mälardalen:

The WCET analysis group maintains close contacts with several industrial partners, and has conducted a number of case studies using their production codes. The group also interacts heavily with the Component-based Software Engineering community through the national centre PROGRESS for research on component-based software design for embedded systems.

Saarland University:

Timing-Analysis activities in the cluster interacted closely with the Execution-Platform cluster in the area of increasing the timing-predictability of real-time systems. Airbus and Bosch participated in the Predator FP7 proposal aimed at reconciling performance with predictability. The PREDATOR project started in 2008. Saarland University worked on modularizations of the Sagiv/Reps/Wilhelm shape analysis together with Mooly Sagiv, Tel Aviv University, and Arnd Poetzsch-Heffter, University of Kaiserslautern.

Tidorum, York:

Tidorum (and partially York through Rapita Systems) were engaged in a project for the European Space Agency to study the timing and verification aspects of cache memories in space systems. The PEAL project ended in February 2007. An extension was started in late 2007. The main partner from the aerospace domain was Thales Alenia Space, France.

TU Vienna:

TU Vienna worked on measurement-based timing analysis together with TU Munich. It also maintained a close interaction with the Lawrence Livermore National Laboratory, CA, USA, in optimizing high-level abstractions.

See ARTIST2 Y1, Y2, Y3, and Y4 deliverables on activities for a more exhaustive description of the state of the integration.

3. Overall Assessment and Vision for the Cluster

3.1 Assessment for Year 4

The integration of tools from the partners has been extended. The cooperation of various partners has been strengthened. For example, tools from TU Berlin and RWTH Aachen have been integrated with the CoSy environment. Tools from AbsInt and TU Dortmund have also been integrated. The same is true for tools from the Saarland University and TU Vienna. For timing analysis, integration of tool components has also progressed. There are now specifications of interface formats. The WCET Tool Challenge 2008 has taken place as planned. Work on Timing Predictability, Measurement-based Timing Analysis, and WCET-aware Compilation has progressed according to plan. As regards flow description formats, a list of essential features for such formats has been identified. Details about the results are available in the timing analysis activity report. Results and pointers The work performed provides a sound basis for the research and implementation work of the partners in the coming years.

3.2 Overall Assesment since the start of the Artist2 NoE

The embedded system world has undergone substantial changes since the start of ARTIST2. Embedded systems are now receiving significantly more attention. The creation of ARTEMIS proves that the European industry recognized the importance of embedded systems for many of their products. This general statement also applies to the compilers and timing analysis cluster. Initially, timing analysis was more a niche topic. Its importance is now recognized by a growing segment of the European industry. A growing number of companies (Rapita Systems, Symtavision) and the presence of Bosch in the PREDATOR project are proofs of this fact.

Also, the essential role of code generation tools has been recognized by the industry. When ARTIST2 was started, it was still expected that processor clock speed would scale for a number of years. It is now clear that further performace increases require parallel processing. Parallel processing needs substancial support by code generation tools. Standard tools for desktop systems comprising homogeneous multiprocessors are inadequate for heterogeneous embedded systems. Code generation from SCADE and dSPACE demonstrates the industrial interest in code generation. The same holds for ARTEMIS work plans, mostly defined by the industrial partners.

ARTIST2 was an essential context for many of these changes. ARTIST2 led to an increased cooperation of the various partners, within the cluster and beyond. Common workshops, summer schools, and meetings have helped spreading the knowledge about leading new technologies. These events are listed in the activity reports on “Platform-based Code Optimization and Verification”, “Timing Analysis”, and “Resource Aware Design”. Partners have improved their ability to cooperate. The large number of common projects is a proof of this effect.

Visibility of European excellence in the area of the network and the cluster has also improved due to ARTIST2. For example, invitations to spring schools on ubiquitous computing (see www.kdubiq.org) were based on the visibility as an Artist2 member. The cluster leader was the first European who was invited to a full week summer course organized by the Advanced Institute of Information Technology in Seoul (see ttt.aiit.or.kr). This course was sponsored by the Korean Ministry of Knowledge Economy (MKE). Earlier, only professors of top US universities had been invited.

Timing Analysis: the original goal of this activity was to achieve a framework for integration of timing analysis tools, and to provide an integrated platform. The necessary formats and interfaces have been defined. Many unforeseen activities and collaborations arose: the WCET Tool Challenge, and work on timing predictability, measurement-based timing analysis, WCET-aware compilation, and parametric WCET analysis to mention a few. The ARTIST2 network has been instrumental in making these collaborations happen. It is now accepted that the need to consider timing is one of the key distinctions between general software and embedded software.

Compilers: compiler technology advanced during the project. Additional optimizations are now available on the CoSy platform. Code verification approaches are also based on the CoSy platform. Several partners (RWTH Aachen, TU Berlin, IMEC etc.) are using the CoSy platform. Additional optimizations are available in the form of pre-pass optimizations which can be used with various compiler backends. Significant work was performed on scratch pad memories. The hiring of Bernhard Egger (one of the key researchers in this area) by Samsung indicates the likely introduction of this technology into industrial products.

Link between Compilation and Timing Analysis: the link between compilers and timing analysis was essentially missing when the project was started. Only few isolated papers existed**.** The creation of a methodology for linking the two areas can be attributed to ARTIST2.

The mini-cluster structure worked well. In general, all partners agree that ARTIST2 has improved the cooperation within Europe. However, the limited funding did not support comprehensive implementation work. The right balance between the amounts of work supported by ARTIST2 and required management and reporting efforts had to be found during the project. Fortunately, many of the partners are involved in projects providing additional resources. Many of those projects were stimulated by ARTIST2. Due to those projects, cooperation can reach the next level (see below).

3.3 Vision Beyond the Artist2 NoE

Fortunately, the successful cooperation within the ARTIST2 NoE will be continued in the ArtistDesign NoE. For ArtistDesign, the scope has been extended. There is now the focus on multiprocessor systems, due to the needs of the industry in this area. This includes the integration of the single-task-on-uniprocessor methods. Also, this includes the integration of tools into design flows considering distributed and communication-centric systems. This new direction is considered by both subclusters, as multiprocessor systems generate new problems for compilation and for timing analysis. The subclusters are also cooperating on this issue. A first workshop has been held. Also, code generation beyond compilers receives more attention. Work on compiler platforms, timing analysis, and resource aware design continues.

New projects extending the cooperation between the partners include the following:

- AbsInt, Mälardalen, York spinoff Rapita Systems, and TU Vienna are partners in the FP7 STREP ALL-TIMES (ICT-215068, duration Dec. 2007 – Feb. 2009). Their work on tool integration and analysis of C code will be continued within ALL-TIMES.
- AbsInt, Saarland University, and TU Dortmund are partners in the FP7 project PREDATOR (Ref. 216008, duration Feb. 2008 – Jan. 2011) aiming at reconciling predictability and efficiency. Joint work on the WCET-aware compiler will continue in that framework.
- IMEC, TU Eindhoven and ICD (a spin-off of TU Dortmund) are partners in the FP7 Mnemee (IST-216224, duration Jan. 2008-Dec. 2010) project.

Timing Analysis: code-level timing analysis is now in a state where it is being applied in industry for the analysis of time- and safety-critical systems. Still, many challenges remain.

Code-level analysis tools and techniques must be integrated into tool chains and development processes, interacting with system-level tools. The usability can be improved, increasing the level of automation. Early, approximate estimates of timing properties are needed for the dimensioning of systems. As computer architecture develops, the timing models become more complex and the subsequent analysis becomes harder. In particular, the introduction of explicitly parallel multicore and MPSoC architectures is very problematic from a timing analysis point of view since shared resources, like buses and memories, easily can cause very unpredictable timing behaviour.

What is needed is a new design discipline, Design for Predictability, that deals with resource handling in general and cuts across several disciplines such as timing analysis (as well as other resource analyses), computer architecture, software design, system software, compilers, and HW/SW codesign/synthesis..

The ultimate vision is a fully integrated development process with resource needs and safely and precisely determined resource consumption communicated between components and layers through resource interfaces. The PREDATOR project addresses these issues.

Compilers: multiprocessor systems challenge compiler technology. Significant progress is required to support the forthcoming parallel architectures. Significant investments into compiler technology are needed to meet the continuing trend towards more performance hungry applications. The lack of adequate compiler technology could potentially inhibit new applications in a large variety of domains. In many cases, required technologies can use available compilers as backends. Hence, fortunately, there is a decreasing need to integrate all new optimizations into a single monolithic compiler.

The generation of embedded systems from specifications in standard von-Neumann languages comes with a number of problems, like potential deadlocks, priority inversion etc. Therefore, new models of computation are being tried out. New code generation techniques are needed for such new models.

Research along the lines of the ARTIST2 project continues to be needed. New optimization engines are required. Resource aware design will be an important topic in the future. This includes memory-architecture aware compilation in particular. Due to the obvious impact of the memory-wall problem, embedded systems will become memory-speed limited and all techniques easing the problem can be expected to find a major attention. Also, optimization engines for SIMD architectures must be improved. Energy efficiency of embedded systems will become even more important than it was in the past. The required high levels of optimization will need to be supported by advanced code analysis techniques. Code correctness is urgently needed. Hence, techniques for code verification are also needed.

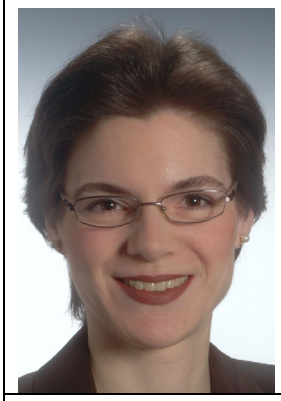
Synergies between compilers and timing analysis: Linking compilers and timing analysis can be expected to be an area of further research. Improved availability of timing information in compilers is certainly overdue. It can be expected that this will be recognized outside this consortium as well and that timing issues will be given more attention. It is unknown, how quickly this will be taken up by the industry.

4. Cluster Participants

4.1 Core Partners

Cluster Leader	
	Prof. Dr. Peter Marwedel (TU Dortmund) http://ls12-www.cs.tu-dortmund.de/~marwedel/
Technical role(s) within Artist2	Cluster leader in year 4. Improved code quality for embedded applications is the main goal of the work at Dortmund University. Due to the widening gap between processor and memory speeds, emphasis has been on improving the efficiency of memory accesses, in terms of average and worst case execution time and in terms of the energy consumption.
Research interests	Peter Marwedels Embedded Systems Group focuses on embedded software. Particular emphasis is on compilers for embedded processors. One of the very first publications in this area, the book “Compilers for Embedded Processors”, edited by Peter Marwedel and Gert Goossens, was the result of the CHIPS project, funded by the European Commission. The group’s current focus is on advanced optimizations for embedded processors (e.g. by using bit-level data flow analysis) and energy-aware compilation techniques. Current research also includes high-level transformations of algorithms as well as WCET-aware code generation.
Role in leading conferences/journals/etc in the area	Member of the EDAA (European Design and Automation Association) Main Board. Editorial Board Member of the Journal of Embedded Computing. Editorial Board Member of the Microelectronics Journal. Co-Founder and Steering Board Chair of the SCOPES Workshop (Software and Compilers for Embedded Systems) Series. >14 years of service for the DATE conference and its predecessors (program chair: 3 times, chairman of the steering committee, European representative to ASPDAC) DAC: Topic chair and reviewer Various other conferences
Notable past projects	MAMS: Multi-Access modular-services framework, national project funded by the German Federal Ministry of Education and

	Research (BMBF) MORE: Network-centric Middleware for group communications and resource sharing across heterogeneous embedded systems, supported by the European Commission http://www.ist-more.org HiPEAC: European NoE on High-Performance Embedded Architecture and Compilation; http://www.hipeac.net Others: Various earlier projects supported by the EC, DFG etc.
Awards / Decorations	Teaching award, TU Dortmund, 2003 DATE fellow, 2008
Further Information	CEO of the Informatik Centrum Dortmund (ICD), a technology transfer centre founded in 1989.

Activity Leader for "JPIA-Platform: Platform-based Code Optimization and Verification"	
	Prof. Dr. Sabine Glesner (Technical University of Berlin) www.pes.cs.tu-berlin.de
Technical role(s) within Artist2	Activity Leader for Compiler Platform Compiler Verification
Research interests	Compilers, Verification, Embedded Systems and Software, Formal Semantics
Role in leading conferences/journals/etc in the area	PC Member of Compiler Construction 2007 Date'06, Design, Automation and Test in Europe, TPC Member of Topic B9 on Formal Verification Workshop Compiler Optimization meets Compiler Verification COCV, ETAPS Conferences, PC Member in 2005 and 2006, Program Co-Chair in 2007 Workshop Formal Foundations of Embedded Software and Component-Based Software Architectures (FESCA), ETAPS Conferences, PC Member 2005 and 2006 Editorial Board Member of "Informatik – Forschung und Entwicklung" by Springer, starting with Vol. 21, No. 1

Notable past projects	VATES (Verification and Transformation of Embedded Systems), funded by DFG Aktionsplan Informatik (Emmy Noether-Program), funded by DFG, support for young researchers to build a research group, with a focus on optimization and verification in the compilation of higher programming languages, from 2004 to 2009 Correct and Optimizing Compilers for Modern Processor Architectures, funded by a postdoc excellence program of Baden-Württemberg, Germany, 2003-2005 Grant in the Wrangell-Habilitation Program of Baden-Württemberg, Germany, 2001-2005
Awards / Decorations	Award of the "Forschungszentrum Informatik" for one of the two best PhD theses of the Faculty for Computer Science, University of Karlsruhe, 1998/99 Member of the "Studienstiftung des deutschen Volkes", the German national scholarship organization, 1991-1996 Fulbright grant to study at the University of California, Berkeley, 1993-1994 Member of the Siemens Internationaler Studenten / Doktorandenkreis, 1993-1999

Activity Leader for "Timing Analysis Platform"	
	Prof. Björn Lisper (Mälardalen University) http://www.idt.mdh.se/personal/blr/
Technical role(s) within Artist2	Activity leader for "Timing Analysis Platform" in year 4. Timing analysis, program analysis.
Research interests	Timing analysis, static program analysis, language design for embedded and real-time systems, program transformations, parallelism
Notable past projects	FP7 STREP ALL-TIMES, Integrating European Timing Analysis Technology (coordinator). http://www.all-times.org Several national projects, funded by Swedish Research Council, VINNOVA, KKS, SSF, Ericsson

	Prof. Dr. Rainer Leupers http://www.iss.rwth-aachen.de
Technical role(s) within Artist2	Cluster co-leader in years 1-3. Compiler platform, code optimization
Research interests	Compilers, ASIP design tools, MPSoC design tools
Role in leading conferences/journals/etc in the area	TPC member of DAC, DATE, ICCAD etc. Co-founder of SCOPES workshop
Notable past projects	HiPEAC NoE, SHAPES IP, several DFG-funded projects Industry-funded projects with Infineon, Philips, Microsoft, CoWare, ACE, Tokyo Electron etc.
Awards / Decorations	Several IEEE/ACM best paper awards
Further Information	Co-founder of LISATek Inc. (acquired by CoWare Inc.) European Commission expert in FP7 Editor of “Customizable Embedded Processors”, Morgan Kaufmann, 2006

	Dr. Christian Ferdinand (AbsInt Angewandte Informatik GmbH) http://www.absint.com/
Technical role(s) within Artist2	Christian Ferdinand coordinates the activities of AbsInt within Artist 2.
Research interests	Timing analysis, program optimization, compiler construction.
Notable past projects	Transferbereich 14 "Run-time Guarantees for modern Processor Architectures" of the German DFG. DAEDALUS RTD project IST-1999-20527 of the European FP5 program on the validation of software components embedded in future generation

	critical concurrent systems by exhaustive semantic-based static analysis and abstract testing methods based on abstract interpretation. http://www.di.ens.fr/~cousot/projects/DAEDALUS/index.shtml INTEREST EU Framework VI Specific Targeted Research Project IST-033661 aiming at overcoming the lack of integration and interoperability of tools for developing Embedded Systems software. http://www.interest-strep.eu/
Awards / Decorations	Dr. Ferdinand received the Dr. Eduard Martin Preis in 1999 (award for best Ph.D Thesis in computer science at Saarland University). AbsInt has been awarded a 2004 European Information Society Technology (IST) Prize for its timing analyzer aiT.

	Hans van Someren (ACE, Netherlands) www.ace.nl
Technical role(s) within Artist2	Supporting ARTIST2 partner use of compiler platform (CoSy compiler development system) – ranging from initial training through to project/design reviews. The design and construction of extensions to CoSy required for ARTIST2 projects.
Research interests	The development and exploitation of compilation techniques and development systems in the wider contexts of SoC and EDA supported by descriptions of the system including application and target architectures. Particular interests include MPSoC and highly parallel system.
Role in leading conferences/journals/etc in the area	Programme Committees of SCOPES and DATE.
Notable past projects	COMPARE/PREPARE ESPRIT projects: These projects, particularly COMPARE, were precursors for CoSy. PREPARE focused on retargetable compilation for Fortran 90 and High Performance Fortran using massively parallel MIMD machines. MESA/NEVA (ongoing): Framework IPs addressing the challenges of designing and constructing multi-processor systems.
Further Information	Principal architect of the CoSy. Previously, architect of ACE's shared

	memory heterogeneous multiprocessor UNIX OS.

	Prof. Dr. Reinhard Wilhelm (Saarland University) http://rw4.cs.uni-sb.de/users/wilhelm/wilhelm.html
Technical role(s) within Artist2	Cluster co-leader in years 1-3. Activity leader for “Timing Analysis Platform” in years 1-3.
Research interests	Compilers, Static Analysis, Timing Analysis
Role in leading conferences/journals/etc in the area	EMSOFT 2007 program cochair.
Notable past projects	DAEDALUS
Awards / Decorations	Prix Gay-Lussac-Humboldt

	Dr. Niklas Holsti (Tidorum Ltd) http://www.tidorum.fi
Technical role(s) within Artist2	Participate in the definition of the common WCET tool-set architecture, the analysis modules and the interchange representations (languages, file formats). Adapt Tidorum’s WCET tool, Bound-T, to integrate with the architecture and interchange formats defined in ARTIST2.
Research interests	Static analysis of the worst-case execution time of embedded programs.

	Prof. Dr. Peter Puschner (TU Vienna) Real-Time Systems Group Institute of Computer Engineering Vienna University of Technology http://www.vmars.tuwien.ac.at/people/puschner.html
Technical role(s) within Artist2	Peter Puschner and his group are participating in the Timing-Analysis activities of the Compilation and Timing Analysis cluster. Within ARTIST2 the contributions are in the area of path-description languages for static WCET analysis, compilation support for WCET analysis, methods and problems of measurement-based execution-time analysis, and on software and hardware architectures that support time predictability.
Research interests	Peter Puschner's main research interest is on real-time systems. Within this area he focuses on Worst-Case Execution-Time Analysis and Time-Predictable Architectures.
Role in leading conferences/journals/etc in the area	Member of the Euromicro Technical Committee on Real-Time Systems, the steering committee of the Euromicro Conference on Real-Time Systems (ECRTS) Member of the advisory board and organizers committee of the IEEE International Symposium on Object- and Component-Oriented Distributed Computing (ISORC) conference series Chair of the Steering Committee of the Euromicro Workshop on Worst-Case Execution-Time Analysis (WCET) series
Notable past projects	DECOS - Dependable Embedded Components and Systems Develop the basic enabling technology to move from a federated distributed architecture to an integrated distributed architecture. http://www.decos.at MoDECS - Model-Based Development of Distributed Embedded Control Systems Model-based construction of distributed embedded control systems: shift from a platform-oriented towards a domain-oriented, *platform-independent* development of composable, distributed embedded control systems. http://www.modecs.cc NEXT TTA Enhance the structure, functionality and dependability of the

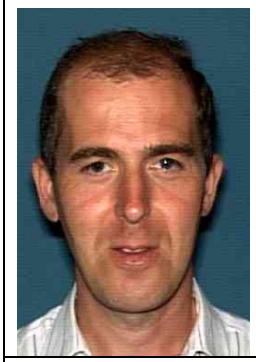
	time-triggered architecture (TTA) to meet the cost structure of the automotive industry, while satisfying the rigorous safety requirements of the aerospace industry. http://www.vmars.tuwien.ac.at/projects/nexttta/

	Dr. Guillem Bernat (University of York) http://www-users.cs.york.ac.uk/~bernat/
Technical role(s) within Artist2	Responsible for the WCET cluster at University of York. Also involved in the flexible scheduling cluster.
Research interests	Worst-case execution time analysis. Especially measurement based methods. Flexible scheduling and real-time systems in general.
Further Information	Also CEO of Rapita Systems Ltd. a spin-off company commercialising RapiTime. A tool for measurement based WCET analysis.

4.2 Affiliated Industrial Partners

None (see core partners).

4.3 Affiliated Academic Partners

	Professor Francky Catthoor (IMEC vzw.)
Technical role(s) within Artist2	Collaboration with TU Dortmund on high-level transformations for source code optimization.
Research interests	Francky Catthoor received a Ph.D. in El. Eng. from the K.U.Leuven, Belgium in 1987. Since then, he has headed several research domains in the area of architectural methodologies and system synthesis for embedded multimedia and telecom applications,

	all within the DESICS division at IMEC, Leuven, Belgium. His current research activities mainly belong to the field of system-level exploration, with emphasis on data storage/transfer and concurrency exploitation, both in customized and programmable (parallel) instruction-set processors.
Role in leading conferences/journals/etc in the area	Francky Catthoor has (co-)authored over 500 papers in international conferences and journals, and has worked on 8 text books in this domain. He was the program chair and organizer of several conferences including ISSS'97 and SIPS'01.
Notable past projects	CATHEDRAL II project Production of a synthesis system for multiprocessor DSPs. DAB-LP project Specification transformations to minimise access to large memories and distant data in DSP systems; applied to a DAB IC. DACMA project Design Methodologies and Advanced Designs for Communication and Multimedia Applications
Awards / Decorations	Francky Catthoor is currently a research fellow within the DESICS division at IMEC and an IEEE fellow.
Further Information	Francky Catthoor is also professor at the K.U.Leuven.

	Dr. Stylianos Mamagkakis (IMEC vzw.) http://www.imec.be
Technical role(s) within Artist2	Collaboration with TU Dortmund on high-level transformations for source code optimizations.
Research interests	Stylianos Mamagkakis received his Master and Ph.D. degree in Electrical and Computer Engineering from the Democritus Uni.

	Thrace (Greece) in 2004 and 2007, respectively. Since 2006, he coordinates a team of PhD students within the NES division at IMEC, Leuven, Belgium. His research activities mainly belong to the field of system-level exploration, with emphasis on dynamic resource management and system integration.
Role in leading conferences/journals/etc in the area	Stylianos Mamagkakis has published more than 25 papers in International Journals and Conferences. He was investigator in 6 research projects in the embedded systems domain funded from the EC as well as national governments and industry.
Notable past projects	EASY IST project Energy-Aware SYstem-on-chip design of the HIPERLAN/2 standard, http://easy.intranet.gr/ AMDREL IST project Architectures and Methodologies for Dynamic REconfigurable Logic, http://vlsi.ee.duth.gr/amdrel/

	Prof. Andreas Krall (TU Vienna) www.complang.tuwien.ac.at/andi/
Technical role(s) within Artist2	Leader of the TU Vienna group working on program analysis and back end optimizations.
Research interests	Implementation of object oriented languages, compiler back ends and computer architecture, implementation of logic programming languages.
Role in leading conferences/journals/etc in the area	PC Member of the International Workshop on Software and Compilers for Embedded Systems
Notable past projects	Christian Doppler Laboratory: Compilation Techniques for Embedded Processors The aim of the CD laboratory Compilation Techniques for Embedded

	Processors is to develop the necessary compilation and decompilation techniques to make the production of highly optimizing compilers and decompilers for embedded processors feasible. http://www.complang.tuwien.ac.at/cd/

	Dr. Markus Schordan (TU Vienna) www.complang.tuwien.ac.at/markus
Technical role(s) within Artist2	Leader of the TU Vienna project group working on program analysis and optimization tools for high-level languages.
Research interests	Analysis of object-oriented languages, alias analysis, source-to-source infrastructures, high-level optimizations, and parallelization.
Role in leading conferences/journals/etc in the area	PC Member of Joint Modular Languages Conference (JMLC) since 2003. PC Member of International Symposium on Symbolic and Numeric Algorithms for Scientific Computing (SYNASC) since 2005.
Notable past projects	ROSE (2001-2003) The goal in the project ROSE was to build an infrastructure for C/C++ source-to-source transformation of multi million line applications at Lawrence Livermore National Laboratory, CA, USA. This work has been continued as a cooperation with TU Vienna since 2004. http://www.llnl.gov/casc/rose/ PAOLA (1999-2001) The goal of PAOLA was the research of techniques for context-sensitive analysis of object-oriented languages (with focus on Java programs). The project was a cooperation between University Klagenfurt (Austria) and Friedrich Schiller-Universität Jena (Germany).

	Prof. Isabelle Puaut (IRISA) http://www.irisa.fr/caps/people/puaut/puaut.html
Technical role(s) within Artist2	Affiliated member

5. Internal Reviewers for this Deliverable

Dr. Heiko Falk, TU Dortmund

Prof. Dr. Olaf Spinczyk, TU Dortmund