IST-004527 ARTIST2
Network of Excellence
on Embedded Systems Design

Periodic Activity Report for Year 4

Executive Summary

Joseph Sifakis – Artist2 Scientific Coordinator
Bruno Bouyssounouse – Artist2 Technical Coordinator

Artist2 Consortium

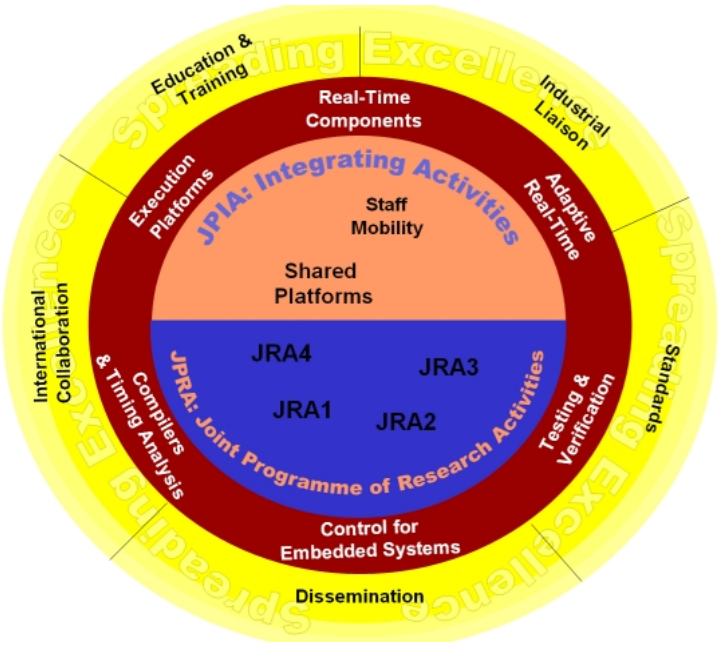
1. Project Objectives

These objectives have remained in place since the start of the Artist2 NoE.

The strategic objective of the ARTIST2 Network of Excellence is to strengthen European research in Embedded Systems Design, and promote the emergence of this new multi-disciplinary area. We gather together the best European teams from the composing disciplines, and will work to forge a scientific community. Integration will be achieved around a Joint Programme of Activities, aiming to create critical mass from the selected European teams.

The ARTIST2 Network of Excellence on Embedded Systems Design implements an international and interdisciplinary fusion of effort to create a unique European virtual centre of excellence on Embedded Systems Design. This interdisciplinary effort in research is mandatory to establish Embedded Systems Design as a discipline, combining competencies from electrical engineering, computer science, applied mathematics, and control theory. The ambition is to compete on the same level as equivalent centres in the USA (Berkeley, Stanford, MIT, Carnegie Mellon), for both the production and transfer of knowledge and competencies, and for the impact on industrial innovation.

ARTIST2 has a double core, consisting of leading-edge research in embedded systems design issues (described later in this document) in the Joint Programme of Research Activities (JPRA), and complementary activities around shared platforms and staff mobility in the Joint Programme of Integration Activities (JPIA).



Building the embedded systems design scientific community is an ambitious programme. To succeed, ARTIST2 builds on the achievements and experience from the ARTIST1 FP5 Accompanying Measure on Advanced Real-Time Systems. ARTIST1 provided the opportunity to test the concept of a two-level integration (within and between clusters) – four clusters in ARTIST2 originated as “actions” in ARTIST1. Building the ARTIST2 consortium and associated structure is the culmination of discussions and ambitions elaborated within ARTIST1.

ARTIST2 addresses the full range of challenges related to Embedded Systems Design, covering all aspects, ranging from theory through to applications.

2. Contact Details and Contractors Involved

2.1 Core Partners

For a complete description including web links, see:
http://www.artist-embedded.org/artist/-Core-Partners-.html

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Partic N°	Participant name	Country
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2	UJF / Verimag	France
3	RWTH Aachen	Germany
4	BRICS – Aalborg University	Denmark
5	AbsInt GmbH	Germany
6	University of Aveiro	Portugal
7	Universidad de Cantabria	Spain
8	Commissariat à l'Énergie Atomique – Laboratoire LIST	France
9	CFV, Université de Liège	Belgium
10	Czech Technical University	Czech Rep.
11	Dortmund University	Germany
12	Technical University of Denmark	Denmark
13	Swiss Federal Institute of Technology – Zurich	Switzerland
14	France Telecom R&D	France
15	Institut National de Recherche en Informatique et Automatique	France
16	Royal Institute of Technology (KTH)	Sweden
17	Linköping University	Sweden
18	CNRS / Laboratoire LSV	France
19	Lund University (Sweden)	Sweden
20	University of Mälardalen	Sweden

Partic N°	Participant name	Country
21	Kuratorium OFFIS e. V.	Germany
22	PARADES	Italy
24	Universidad Politecnica de Madrid	Spain
25	Saarland University	Germany
27	TU of Eindhoven	Netherlands
28	TU of Vienna	Austria
29	TU Braunschweig	Germany
30	University of Twente	Netherlands
31	University of Bologna	Italy
32	Uppsala University	Sweden
33	Universidad Polytechnical de Valencia	Spain
34	University of York	UK
35	Polytechnic Institute of Porto	Portugal
36	EPFL	Switzerland
37	Scuola Sant'Anna – Pisa	Italy
38	Ace	Netherlands
39	Tidorum	Finland
40	TU Kaiserslautern	Germany
41	TU Berlin	Germany

The following partners have withdrawn from the NoE:

- Partner 23 – University of Pavia (Italy)
- Partner 26 – ST Microelectronics, Central R&D (France)

2.2 Affiliated Partners

Affiliated partners play a very strong role in the Spreading Excellence from the core partners to the research and industrial communities at large.

Affiliated partners generally play an active role in the research activities, either participating directly in research, or transferring the results directly to industry.

Each of the JPRA and JPIA activities' deliverables provides the list of the corresponding affiliated partners and roles.

Affiliated Industrial Partners

The complete set of Affiliated Industrial partners, including web links, is available online, here: http://www.artist-embedded.org/artist/-Affiliated-Industrial-Partners-.html

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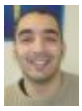

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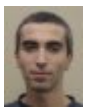

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3. Vision and Assessment of the Work Performed

Artist2 has financed durable integration between teams and not the concrete elements of the JPA which most often belong to other projects. These specific technical objectives may or may not be attained (this is the essence of research as opposed to development), but we feel that the main product of Artist2 is the emergence of a lasting European research community, that has a significantly enhanced capacity for preparing Europe's future.

The research is completed by work on the JPIA Platforms, which aim to transform research results in tangible tools and components.

We believe that the topics chosen provide a good coverage of the area, for embedded software and systems.

The ARTIST2 NoE is a complex construction assembled from world-leading communities, teams, and individuals. This is certainly an asset, but also a source of complexity in management. Each team has two essential characteristics: world-class excellence and strong interaction with top industrial players. Artist2 partners play a leading role in the different communities in embedded systems design, and they advance the state of the art in each of these.

Over the course of Years 1-4, Artist2 has been extremely active in submitting new proposals

It is difficult to abstract out a global synthesis of the overall technical achievements. This is due to the diversity and the low granularity of the actions to be covered (meetings, publications, attendance at workshops, visits, and platforms).

The following is a certainly non-exhaustive assessment of the work in the Joint Programme of Activities' 4 main branches.

3.1 Joint Programme of Research Activities (JPRA)

3.1.1 Structure of the Research Effort

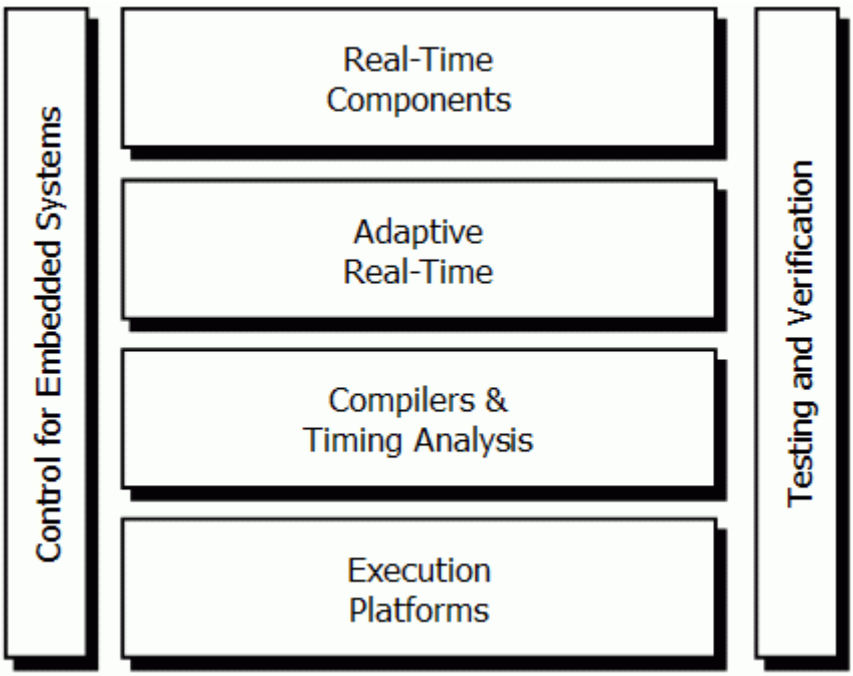
This is unchanged with respect to the end of Year 3 – included here as a useful introduction.

The JPRA is composed of intra and inter-cluster research activities on cutting-edge topics in embedded systems design. While the main bulk of financing for these activities is taken up by outside programmes (Integrated Projects, National Programmes, Industrial Contracts, etc), the Artist2 NoE finances the extra burden due derived from integrating these into a single coherent research programme.

Thus, the essential ingredient within Artist2 is the JPRA, which motivates the participating research teams far more than the actual financing, which is tiny in comparison with the overall research aims. It is completed by the Joint Programme of Integrating Activities (JPIA), and the Joint Programme of Activities for Spreading Excellence (JPASE), and overseen by the Joint Programme of Management Activities (JPMA).

The structure of the research activities reflects the following decomposition of the embedded systems design flow.

This design flow is composed of the following cooperating activities, starting with component-based modelling and leading to implementation. These activities must be well coordinated, and supported by tools and methods to ensure satisfactory levels of productivity and quality. Accordingly, we have structured the area of embedded systems design into the following topics.



Real-Time Components: The development of a general framework for component-based engineering of complex heterogeneous embedded systems is a grand challenge which spans many research problems. A key characteristic of component-based embedded systems is heterogeneity of component models. This heterogeneity concerns different execution models (synchronous, asynchronous, vs. timed), communication models (synchronous vs. asynchronous), as well as different scheduling paradigms. Technology must be provided to allow designing heterogeneous embedded systems from diverse types of components, and allow predicting and optimizing functional and non-functional properties of the designed systems.

Adaptive Real-time: This is a more recent approach to embedded systems design, where temporal constraints can be relaxed, which allows optimized use of resources. This includes applications – where managing the Quality of Service (QoS) is essential, such as telecommunication systems, multi-media, and wide-area networked applications. In this relatively new area, there is a recognized lack of design theory and tools.

Compilers and Timing Analysis: Once the application software has been developed, using the above, the system must be implemented on a given target platform. Compilation tools and their associated technologies play a fundamental role for automating this process. For the implementation of embedded systems, we need tools capable of combining platform independent software and a description of the target platform, to generate an executable code having the desired properties related to use of such resources as memory, power, energy, network bandwidth, and computation time). Resource-aware compilation requires the use of Timing Analysis tools to estimate the execution times of embedded software on a given platform.

Execution Platforms: This topic is strongly linked to the compilation and implementation of embedded systems. For a given application, it is important to have the technology, methods and tools to make rational choices about the platform and the design used, before proceeding to final implementation. Research in Execution Platforms targets the development of the theoretical and practical tools for modelling the dynamic behaviour of application software for a given platform. This is a new area of research, which will allow greater flexibility in designing optimal embedded systems.

Testing and Verification: This is transversal topic, which interacts with all the other topics in embedded systems design. It aims to ensure that the different design steps meet given properties, as well as the overall correctness of the implementation. This is a very active research topic, with results at different levels of the design process. The current challenge is in achieving on overall approach for testing and verification, focussing on two important aspects.

First is the Verification and Testing of real-time properties, to ensure that hard real-time constraints or quality of service constraints are met. Second is for Verification of Security Properties, where identification of gaps in security is desired.

Control for Embedded Systems: Embedded systems are deployed in the real world, and are often reactive to it. This interaction with the environment is intrinsic to the service provided. A large proportion of embedded systems can be considered to be controllers. On the other hand, most automated control applications will be implemented as embedded components. Thus, it is essential that work on joining control theory and embedded systems be included in the ARTIST2 NoE.

3.1.2 *Overview of the Year4 Research Results*

An overview of each intra-cluster ("Cluster Integration") and inter-cluster ("NoE Integration") research activities is provided.

3.1.2.1 Real Time Components

We have obtained some very significant results, on modelling heterogeneous systems:

- Work by INRIA, PARADES, and VERIMAG, on the theory of tagged systems provides conditions for correct implementation of synchronous systems on "less synchronous" architectures. Work by INRIA on new models of computation, the Kahn-extended Event Graph (KEG), which adds "static control" in the Model of Computation of Marked Graphs.
- Work on the BIP component framework, introduces a notion of expressiveness for component-based formalisms, which provides a basis for their comparison. This notion drastically differs from the usual one, as it takes into account the expressive power of composition operators (glue operators).
- Significant progress has been achieved in methods for distributed implementation of non-distributed specifications. VERIMAG studied a method for the automatic generation of distributed implementations of BIP models. INRIA, PARADES and VERIMAG studied the concept of loosely time-triggered architectures, implementing time-triggered architectures. Finally, fully asynchronous implementations of synchronous systems have been studied.
- Other results on distributed implementations include reliability, new heuristics in scheduling for reliability, design of communication architectures and time-triggered system-on-chip architectures.

We have also obtained significant results on Interfaces and Composability, including:

- The development of interface theories supporting component reuse (EPFL). We have shown that existing interface theories provide no formal support for component reuse. We enriched interface theories with a new operation allowing the same component to implement several different interfaces in a design.
- The development of contract-based verification techniques for the heterogeneous rich component (HRC) model (INRIA, PARADES, VERIMAG), in the framework of the SPEEDS project. The techniques allow handling multiparty interaction, as well as many different languages for describing notions of refinement under contexts. These results found application in the verification and analysis of HRC models.
- In joint work, ETHZ and Uppsala propose modular performance analysis techniques, based on the real-time calculus and timed automata. A prototype tool name CATS for compositional timing and performance analysis has been developed.
- VERIMAG has continued the work on compositional deadlock verification of BIP programs, and its implementation in the DeadlockFinder tool. Other results include the enhancement of existing component models, such as the synthesis of controllers from specifications and the generation of component models from their observed behaviour.

3.1.2.2 Adaptive Real Time

The main results on "Flexible Resource Management for Real Time Systems" deal with flexible scheduling frameworks and their implementation:

- The architectural model developed in previous years has been updated and its API has been redesigned to support: Updated energy management, disk bandwidth management services, feedback control, and memory management. New communication networks have been added: CAN bus, WiFi, wired Ethernet, and switched Ethernet.
- The architectural model has been designed to be implementable on different platforms. Work has been performed in cooperation with Thalès Communications France, to integrate the contract-based scheduling framework, with a component-based framework.
- A work on the implementation of flexible traffic scheduling for switched Ethernet has been carried out in collaboration with the University of Pennsylvania and CMU. The aim of the work is to equip COTS switches with new scheduling capabilities allowing dynamic QoS management.
- A number of theoretical developments have been made this year including hierarchical scheduling, a multiframe extension to fixed priority scheduling, and adaptive algorithms for flexible resource management.

The main results on "Real Time Languages" deal with:

- The production of a survey on Real-Time Programming Languages.
  http://www.artist-embedded.org/artist/ARTIST-Survey-of-Programming.html
  The survey includes contributions from a large number of Artist2 partners and non-Artist2 individuals linked to the ARTIST community. It considers over 20 programming languages by presenting an overview of the main features and a classification allowing the comparison of their main features.
- Work on Ada 2005, including development of real-time utilities and the implementation of specific real-time mechanisms.
- Work on RT-Java, including a distributed version of RTSJ.

The main results on "Dynamic and Pervasive Networking" deal with:

- *Work on the analysis and implementation of Wireless Sensor Networks.*
  - We have studied a methodology for modelling cluster-tree Wireless Sensor Networks. The methodology enables the computation of the worst-case end-to-end delays, buffering and bandwidth requirements across source-destination paths.
  - We also implemented QoS add-ons to the IEEE 802.15.4 and ZigBee protocols.

  For these protocols, we have worked towards the implementation of the protocol stack over Erika, the real-time operating system for adaptive resource management developed by Pisa.

- *Work on the analysis and implementation of Wired Networks.*
  - We studied topologies for robust communication in CAN and Ethernet networks. Robustness is characterized as protection against faults in the time domain and overloads.
  - We studied schedulability analysis techniques for specific traffic types involving the transmission of long messages.
- Other work includes real-time support for middleware layers, as well as an Educational Testbed, supporting teaching of industrial wired/wireless networks.

The main results on "QoS Aware Components" are described in the section on "Inter-cluster Integration" below.

3.1.2.3 Compilers and Timing Analysis

Timing Analysis

In addition to experimental work, we developed important results on Timing Analysis.

We have studied a notion of time predictability of cache architectures, which is the first precise notion found in the literature. Four different cache replacement strategies were compared and the LRU strategy was found to be optimal. This research is related to work within the PREDATOR FP7 project, which attempts to reconcile performance and predictability.

The study of Timing anomalies, where local worst-case choices may not lead to the global worst-case scenario, is essential for time predictability. We have studied techniques for handling timing anomalies for efficient WCET analysis, as well as for measuring the impact of timing anomalies on WCET analysis.

Other work on Timing Analysis includes parametric Timing Analysis, where some parameters of the program can remain unknown until execution. We also developed Timing Analysis techniques, in collaboration with BOSCH, taking into account operating modes of programs, computed semi-automatically. Finally, we developed WCET analysis for systems with preemptive scheduling.

Compilers

We developed research in the following directions:

- We studied the influence of scratchpad memory allocation techniques on worst case execution times (WCET). We developed integer linear programming models to decide which parts of a program's code or data can be moved onto the highly predictable scratchpad. First experiments show WCET reductions of more than 50% for several benchmarks.
  We also investigated WCET-aware register allocation techniques, by extending existing techniques based on graph colouring.

- TU Berlin studied optimization and verification methods for compilers. These techniques have been applied in a platform based on the Cosy compiler provided by ACE. We investigated new compiler optimizations to mitigate the impact of the memory wall on program performance, in particular for VLIW processors, such as Itanium. Furthermore, we investigated how code generation can be verified formally. The code generation process is specified by a set of rules describing how an abstract-level construct can be mapped to the machine level.
- We continued work on scalable source-level analysis and annotation-based timing analysis methods. The SATIrE infrastructure allows building analysers that take source code annotations as additional input, and generate output as annotations. This allows a significant increase in productivity, by requiring the user to annotate the relevant timing information that cannot be automatically computed. The integration of PAG was instrumental in investigating the scalability of analyses.

3.1.2.4 Execution Platforms

For “Communication-centric Systems”, we developed the following results:

- We have developed new compositional performance evaluation techniques, based on modelling of systems as a hierarchically-structured network of functional nodes. The technique allows merging several single event streams to a hierarchical event-stream. It greatly improves the accuracy of the performance analysis.

  Furthermore, we have studied online performance analysis techniques, allowing performing optimisations based on pending resource demands.

- We studied fault tolerance techniques for soft real-time systems. The issue is to be able to guarantee the deadlines for hard real-time processes, even in the presence of faults, while maximising the overall utility of the system. We have proposed a new scheduling strategy, where a set of fault-tolerant schedules is synthesized offline.

  Furthermore, we have investigated fault-tolerance aspects related to the FlexRay protocol. Several techniques have been proposed for tolerating transient faults.

- We have studied analysis techniques for distributed wireless sensor networks.

  Furthermore, we have extended existing communication-centric performance analysis techniques to systems with cyclic dependencies. We have shown that the analysis requires the iterative solution of fixpoint equations.

- We have studied programming models for NOC-based systems, with a focus on parallelisation of the application, and reduction of load imbalance.

For “Design for Low Power”, we have developed the following results:

- We have worked on modelling and optimisation of a miniaturized solar energy harvester. We focused on the optimisation of two important metrics: a) maximisation of the energy harvesting efficiency and b) the minimisation of the energy used for ineffective operations. A hierarchical control solution has been designed which overcomes several drawbacks of previously proposed approaches. A novel algorithm for approximate multi-parametric linear programming has also been proposed.
- We studied scheduling-based energy optimisation techniques for energy-scavenging wireless sensor networks.

- We have worked on temperature-aware system level power optimisation techniques. The main challenge is to integrate temperature modelling into the framework of energy-efficient system-level scheduling and voltage selection. The results obtained include power optimisation and analysis for nanometer technologies, system-level performance and power analysis for multi-processor systems on chip (SoC), system-level energy optimisation of real-time systems.

3.1.2.5 Control for Embedded Systems

For “Control in Real-Time Computing”, we have worked in the following directions:

- The work on control of server systems in Lund has continued.

  We have expanded the feedback-based prediction scheme for controlling a single server queue, with a new control strategy. Our method maintains or improves performance, regarding average response time and loss of computational resources.

- We studied, in collaboration with Ericsson, techniques for feedback-based resource management in cellular devices.

- We studied, in collaboration with ABB, techniques for control and optimisation of networked systems.

For “Real-time techniques in control system implementations”, we have worked in the following directions:

- We studied properties of event-based control systems. We have continued our previous investigation of sporadic control of first-order stochastic systems. We have analysed how delay, jitter and measurement noise affect the performance of the control loops.

  We have also studied event-based control for higher-order systems.

  The implementation of event-based PI controllers has been studied, for measurements available at irregular intervals.

  Finally, we studied state estimation techniques for event-based systems. The event-based characteristics of the measurements are modelled as uncertainty sets. In each timestamp, the uncertainty sets and the regular noise descriptions are combined and simplified, keeping the complexity bounded.

- We developed a control kernel, which plays a role similar to an OS kernel. An efficient implementation has been completed and experimented for small control systems.

- We developed control-based techniques for networked systems.

  We studied a modular control design methodology, ensuring maximal performance, stability, and adaptability.

  We developed new results on optimal flow routing in multi-hop sensor networks.

- In a continuation of work from Year 3, we have studied scheduling techniques for control and signal processing. We have implemented our own heuristics and evaluated their performances.

3.1.2.6 Inter-cluster Integration

The planned NoE Integration activities have led to the following results:

QoS Aware Components:

We developed results along the following directions:

- Specification of QoS properties using UML profiles and aspect-based approaches. We studied methods for the composition of applications in real-time, taking into account their corresponding QoS properties.
- Generation of analysable models from the UML models. We studied techniques for extracting, from UML models, models for safety analysis. These models synthesize safety annotations included in the UML models.
  We have participated in collaboration with companies and universities for defining the OMG standard « MDA Tool Component RFP ».
- Composition of QoS-aware components and adaptability. Our contributions include important results on achieving fault tolerance and adaptability in component frameworks (CEA-LIST, Thalès, UPM). We studied a concept of quality of service adaptability characterising a component's ability to adapt its quality during runtime. We have extended the UML standard profile to define adaptable elements with the associated QoS functions and their composition. The results obtained should allow the evaluation of architectural models to predict a system's QoS behaviour before its implementation.
- QoS support in run-time components frameworks. Our work in this direction includes a contribution to an API standard for QoS support in runtime components for multimedia middleware (UPM), as well as the design of a QoS management platform using a model-driven engineering process (INRIA).

Resource-aware Design

We developed work in the following directions:

- We studied resource analysis and management techniques. We used timed automata and the UPPAAL tool has been used for solving resource optimization problems. Furthermore, we studied experimental techniques for dynamic configuration on a coprocessor-coupled architecture.
- A key issue is predictability for multi-processor systems with a shared communication infrastructure. To cope with uncertainty in such systems and thus enforce their predictability, we studied the application of control-based techniques.

  Other work on predictability included deals with the uncertainty of execution times. To reduce this uncertainty, we have studied parametric timing analysis techniques, allowing a more precise estimation of execution time bounds. Another avenue for improving predictability is the study of cache replacement strategies.
- As reported in a section on Timing Analysis, various Timing Analysis techniques have been studied in collaboration with teams from the CTA cluster.
- We worked on resource-aware techniques, both for design space exploration and mapping. These techniques use performance analysis by simulation and/or analytic models to determine optimal mappings for given efficiency requirements.

- We integrated MPARM multiprocessor simulation platform from Bologna, and the MEMSIM versatile memory hierarchy simulator from Dortmund.

Adaptive Real-time, HRT and Control

Work has progressed in the following directions:

- We studied various scheduling techniques, which require competencies, both from Adaptive Real Time and Control. These include: a) optimal period selection for multiple controllers under fixed-priority scheduling; b) optimal period selection and scheduling for multiple distributed controllers; c) event-driven control, embedded control and feedback scheduling.
- We also studied control-based mechanisms for multimedia systems and protocols. Three key technologies have been combined: a) reservation-based resource management; b) feedback scheduling; and c) dataflow modelling of multimedia applications.
- As mentioned for RTC, the LTTA (Loosely Time-Triggered Architecture) architecture has been proposed in the form of a middleware.

Quantitative Testing and Verification

Work has been carried out in the following directions:

- Significant contributions to game-theoretic approaches to real-time system testing. By modelling the systems as timed game automata and specifying the test purposes as formulas, we developed a timed game solver Tiga to synthesize testing strategies.

  We studied games for different extensions of timed automata such as weighted timed automata, priced timed automata, multi-priced timed automata. The results relate to the complexity of decision problems for these automata, as well as model checking and synthesis algorithms. The notion of timed parity games has been studied, with a focus on robustness and complexity. We have also studied reachability in timed games.
- Continuing on work from previous years, we have extended and improved the functionality of the UPPAAL tool, including the use of slicing techniques for model optimization as well as features supporting interface theory for real-time systems.
- We have studied quantitative testing techniques. In particular, we have developed a theory allowing testing of systems in the presence of measurement imprecisions. We also studied testing methods for probabilistic processes.
- We have studied quantitative model checking techniques for timed models, including timed automata, linear hybrid automata and general non-linear hybrid systems. The work on verification has been applied to non-trivial case studies and systems, in particular in collaboration with industry.
- Finally, we have studied compositional synthesis and verification techniques. These include modular supervisory control, as well as the verification of component-based systems.

3.2 Joint Programme of Integration Activities (JPIA)

3.2.1 Structure of the Integration Effort

This introduction has remained constant since the beginning of the project.

The Joint Programme of Integrating Activities contains the technical but non-research activities that participate in the overall effort. As with the JPRA, the main financing for these technical activities is derived from other sources, and is small in comparison with the overall objectives.

The JPIA is composed of Platform Activities (roughly one for each cluster), and Mobility actions between partners – both core and affiliated partners.

Integration between research teams work to achieve critical mass in 2 important dimensions:

- Strong integration within selected topics by assembling the best European teams, to advance the state of the art in the topic.
- Integration between topics to achieve the multi-disciplinary excellence and skills required for the development of future embedded technologies.

The ARTIST2 platforms integrate the results of long-term efforts, and are meant to be durable, evolving with the state of the art. The partners are committed to durability, and have invested significant resources into their development. The construction of ARTIST2 has provided the opportunity to assemble existing pieces into a rationally-structured set of platforms, covering the area of embedded systems design.

Some of the ARTIST2 platforms have international visibility, and the ambition is for these to serve as world-wide references in their respective topics.

Both types of integration are achieved through Joint Programme of Integration Activities (JPIA) activities involving state of the art research platforms, composed of competencies, resources, and tools targeting specific technical and scientific objectives around a chosen topic. These are made available to the R&D community for experimentation, demonstration, evaluation, and teaching.

Our assessment of Artist2 progress on integration over Year 4 is very positive.

3.2.2 Progress on the Platforms

The following are the main highlights from the different clusters over the course of Year 4. These represent only a part of the total effort deployed.

3.2.2.1 Real Time Components

Important results come from the SPEEDS IP, which developed modelling and validation techniques for the HRC (Heterogeneous Rich Component) framework. We defined and implemented a semantic-based common meta-model; developed a framework for a multiple-viewpoint component engineering; developed a framework for the composition of heterogeneous components. The HRC environment is connected to the BIP and Metropolis toolsets via translation tools. In particular, this allows the application of analysis and design space exploration techniques.

Work within the French national platform “OpenEmbeDD” includes the following contributions from CEA, INRIA and VERIMAG, in collaboration with industrial partners: 1) The development of the Papyrus editor for the UML / MARTE profile; 2) the performance evaluation tool PERSIFORM; 3) the BIP toolset.

Applications of our tools include work on “componentisation” of complex software by using BIP in collaboration with ASTRIUM, the simulation of wireless sensor networks by using PERSIFORM, and the certification of Smart-Card applications.

3.2.2.2 Adaptive Real Time

We have concentrated our efforts on the development of an embedded platform for running real-time applications under severe resource constraints. The platform is composed of the Erika Enterprise real-time kernel, and the Flex hardware platform. We have developed a set of challenging real-time applications which are made available via the web. The same platform is used for educational experiments including a real-time controller.

3.2.2.3 Compilers and Timing Analysis

Timing Analysis

Work on the AIR format has continued. The format was extended and adapted to the needs of the partners. The attribute database was extended with new attributes.

We also worked on the development and improvement of formats for ensuring the interoperability of the tools. The work on formats includes ALF for computation semantics representation, conversion of the ABSINT AIR format to SWEET format, and the definition of common flow description attributes.

As was the case last year, the WCET Challenge 2008 consisted of a set of benchmark programs and analysis tasks to be performed by the contestants.
http://www.artist-embedded.org/artist/-WCET-08-.html

Compilers

We developed work in the following directions:

- We designed a Static Loop Analyzer, allowing to estimate loop iteration bounds. This information is essential for a large number program analyses. Our analyser improves analysis techniques based on conventional abstract interpretation by integrating a new static polytope-based loop evaluation method.
  We have demonstrated the applicability of the analyser on benchmarks taken from the benchmark suites MRTC, DSPStone, MiBench, UTDSP and MediaBench. Our loop analyser was the only tool able to answer all questions related to flow fact during the WCET tool challenge 2008.
- In continuation of work performed in Year 3, we developed a new WCET-aware procedure positioning and cloning technique. The compiler optimisations obtained were exploited for WCET reduction. Results on real-world benchmarks show WCET reductions of 10% on average, while ACET is reduced by 2 on average.
- The cooperation between ACE and Aachen on the retargetable code optimizations has been continued. The conditional execution engines have been extended by a strong retargeting formalism.

3.2.2.4 Execution Platforms

For “System Modeling Infrastructure”, the work for Year4 was concentrated on extending formal models for platform modelling and performance, although some simulation-based work was continued. We developed work in the following directions:

- We worked on the formal verification of embedded systems and hardware architectures. The modelling is performed by using timed automata, and verification by using the UPPAAL tool. The models are generated automatically from high-level description languages. The properties verified are real-time with a focus on schedulability analysis, as well as design properties for a few circuits including the Simplified Data Encryption Standard (SDES).
- An important work direction is modelling and performance analysis for multi-processor and/or networked systems.

  We studied relations between simulation-based and analytical methods for performance evaluation of distributed real-time systems. Based on experimental simulation results, we were able to draw interesting conclusions regarding the pessimism of formal approaches. The experiments were performed on FlexRay and CAN-based distributed systems.

  We also studied interesting relations between MPA (Modular Performance Analysis) and Timed Automata.
- We have extended the fault-tolerant process model, to consider a combination of hardware and software fault-tolerant techniques. We have proposed a method for computing the reliability of a system, taking into account: a) hardening levels in hardware; b) the re-execution levels in software; c) scheduling for sharing recovery slacks.
- DTU has extended its simulation framework COSMOS to study the dynamic behaviour of runtime reconfigurable systems through design-space exploration experiments. Critical design issues in the reconfigurable architecture have been identified.

3.2.2.5 *Control for Embedded Systems*

Work has been carried out in the following directions:

- Continuing on work in previous years, we have added new features to TrueTime, a Matlab/Simulink -based tool for co-simulation of real-time control systems. New features in TrueTime include a new Ultrasound Network block, better support for Constraint Bandwidth Server scheduling and an improved user interface. The tool is available under the GNU General Public License (GPL). It has been used in laboratories and for educational purposes.

  TrueTime is also used in the EUROSYSLIB ITEA2 project, led by Dassault Systems, as well as in the DySCAS project for modelling and simulating dynamically configurable systems.
- Continuing on work in previous years, we have extended and added new features to the TORSCHE scheduling toolbox for Matlab.
- We have worked within the framework of the DySCAS project, to provide simulation and analysis techniques. DySCAS is an autonomic platform-independent middleware for automotive embedded systems. It supports automatic configuration for context-aware behaviour, resource use efficiency, and self-healing to handle runtime-detected faults. Simulations within the Matlab/Simulink environment have been carried out, to

validate interfaces and functional behaviour as well as to validate quality of service and load balancing.

- In the framework of the ATESST project, a UML profile for automotive embedded systems modelling has been studied. We developed a tool translating Simulink behavioural models into UML models for the CEA's Papyrus tool. Furthermore, a new approach for representing safety cases in Papyrus has been implemented.

3.2.2.6 Testing and Verification

In continuation of the work initiated in previous years, we have pursued the following directions:

- We have further developed the UPPAAL Tiga tool for controller synthesis. The UPPAAL model checker has been further improved and optimized.
- IRISA have improved the symbolic test generation tool, STG, and a new version can be downloaded from INRIA Gforge: https://gforge.inria.fr/plugins/scmsvn/viewcvs.php/?root=bjeannet
- VERIMAG have applied their test generation tool TTG http://www-verimag.imag.fr/~krichen/ttg/index.html for the automatic generation of robotics observers.
- OFFIS have developed a modelling and verification framework for protocol validation and illustrated the concepts through a major industrial traffic communication protocol.
- BRNO have further optimized the DiVinE tool and evaluated its performance and scalability on large-scale parallel systems.

3.3 Joint Programme of Activities for Spreading Excellence *(JPASE)*

The achievements and results from the Joint Programme of Activities for Spreading Excellence (JPASE) are contained in a separate deliverable, entitled: "Spreading Excellence".

Our actions for Spreading Excellence are at 2 levels:

- *Targeted towards affiliated partners*
  Affiliated partners are not core members in the consortium, but receive support for travelling to Artist2 meetings, and actively contribute to the implementation of the Joint Programme of Activities (JPA). These affiliated partners include industrial, SME, academic, and international collaboration affiliates.
- *Targeted towards the scientific and technical community in the large*
  This is achieved mainly bottom-up through the organisation of scientific events, publications, distribution of tools and components, industrial partnerships (not funded by Artist2), education; and through the Artist2 web pages.
- *Targeted towards students*
  A particular focus has been placed on the Artist2 Summer Schools this year – with a truly outstanding programme of lecturers, and the innovation of providing the lectures in video form on the Artist website.

Regarding Scientific events, we distinguish between conferences and workshops, schools, and high-level events mainly for International Collaboration.

3.3.1 International Collaboration

Here, we focus on the workshops and schools organized outside the EU, globally by the NoE.

Further International Collaboration is carried out within the clusters, as reported in the cluster–level activity reports.

ARTIST2 South-American School for Embedded Systems 2008
http://www.artist-embedded.org/artist/-ARTIST-2-South-American-School-.html
August 25-29, 2008 Universidade Federal de Santa Catarina, Florianopolis, Brazil
Organised and funded by Artist.

After the successful First ARTIST2 South-American School for Embedded Systems in Buenos Aires, Argentina, this second edition in Florianopolis, Brazil, strengthens the cooperation between Europe and South America in the area of embedded systems, both at educational and research levels. For this purpose, the goal of the school is to provide state-of-the-art courses on embedded systems oriented towards advanced students and young researchers.

We believe the school provides the ground for cross-fertilization between Europe and South-America with an expected mutual high added-value. Therefore, the lectures given by European researchers were accompanied by talks and a poster session for participants to present and discuss their ongoing work.

Artist2 Summer School in China 2008
http://www.artist-embedded.org/artist/-Artist2-Summer-School-in-China-.html
July 12-18, 2008 Shanghai, China
Organised and funded by Artist.

This was the 3rd edition of a school on Embedded Systems Design.
This year, the school was organized in collaboration with the SEI/ECNU and the LIAMA.

This year, we were able to do a far stricter degree of selection amongst the candidates. We selected 81– the fill list is available here.

Foundations of Component-based Design
September 30th, 2007 Salzburg, Austria - within EmSoft / ES Week
http://www.artist-embedded.org/artist/-Foundations-of-Component-based-.html
Artist2 organised and funded this event, within Embedded Systems Week.

Discuss recent results on component-based design with emphasis on design frameworks for real-time systems encompassing heterogeneous composition and models of computation. Especially frameworks for handling non-functional and resource constraints, design under conflicting dependability criteria, trade-offs between average performance and predictability.

The workshop aims to gather together researchers from computer science and electrical engineering and will seek a synthesis between the underlying paradigms and techniques. The focus is not only on fundamental results but also on their implementation in methods and tools and their concrete application in areas such as automotive, avionics, consumer electronics and automation.

Workshop on Embedded Systems Education (WESE 2007)
October 4-5, 2007 Salzburg, Austria (within ES Week)
http://www.artist-embedded.org/artist/-WESE-07-.html
Organised and funded by Artist

It is widely recognized that the embedded system domain is a multidisciplinary one, requiring a large variety of skills from control and signal processing theory, electronics, computer engineering and science, telecommunication, etc., as well as application domain knowledge.

This has motivated a recent but ever growing interest in the question of educating specialists in this domain and this has also been recognized as a particularly difficult problem.

This third workshop on the subject aims to bring researchers, educators, and industrial representatives together to assess needs and share design, research, and experiences in embedded systems education. Industrial needs regarding embedded systems education

Year 4 Event: ARTIST2 meeting on Integrated Modular Avionics
November 12-13, 2007 Roma, Italy
http://www.artist-embedded.org/artist/-ARTIST2-meeting-on-Integrated-.html
Organised and funded by Artist

Today, the exponentially increasing diversity of airborne systems results in an increasing number of computers and controllers for system management, monitoring, and control. The development of specific ad-hoc solutions causes increases in costs, which in turn impacts purchase prices and operational costs. To overcome this, standardization principles and reuse of function units are now considered, via Integrated Modular Avionics.

Integrated Modular Avionics (IMA) has set the principles of standardized components and interfaces of hardware and software in aircraft. These principles have been applied for the first time in the development of the Airbus A380. Further developing IMA raises a number of issues that require fundamental research efforts, in tight coordination with engineering needs.

ARTIST2, the European Network of Excellence on embedded systems has organized, as part of its activity on "scientific challenges in specific industrial sectors", a two-day workshop dedicated to Systems, Software, and Architecture, aspects of IMA.

3.3.2 Organisation of Schools

In Year 4, Artist2 has directly organized and funded the following schools and courses:

Special Year 4 Event: ARTIST2 Summer School 2008 in Europe
September 8-12, 2008 Autrans (near Grenoble), France
http://www.artist-embedded.org/artist/-ARTIST2-Summer-School-2008-.html
Organised and funded by Artist –this school was an outstanding success.

NB: Videos from the lectures are in post-production and will be made available free of charge to the general public.

The Summer School offered a number of foundational tutorials, accompanied by a selection of lectures on exciting emerging technologies and industrial applications - given by leading scientific and/or industrial experts.

An innovative step has been to provide the lectures in the form of videos, available for free via the website (currently under preparation – this will be shown at the review).

The ARTIST Summer School 2008 was held in the beautiful Vercors mountains in Autrans, near Grenoble, Sept 8-12. The school was organised by the Artist2 European Network of Excellence on Embedded Systems Design, which gathers 42 top European institutions. Artist's mission is to coordinate European research in the area around an ambitious joint research agenda, and to spread excellence through targeted events such as international workshops, schools and seminars.

Artist has a strong tradition in organising top-quality schools. This is the fourth edition of yearly schools on embedded systems design, and is meant to be exceptional in terms of both breadth of coverage and invited speakers.

The topics covered include Modeling and Validation, Compilers and Timing Analysis, Adaptive Real Time Systems, Control for Embedded Systems, Execution Platforms and MPSoC. We seek a balance between foundational aspects and applications. Speakers included recognized leading researchers and engineers.

The school was open to PhD students, researchers, and engineers. Attendance will be limited to 80 selected participants.

ARTIST2 South-American School for Embedded Systems 2008
August 25-29, 2008 Universidade Federal de Santa Catarina, Florianopolis, Brazil
http://www.artist-embedded.org/artist/-ARTIST-2-South-American-School-.html

After the successful First ARTIST2 South-American School for Embedded Systems in Buenos Aires, Argentina, this second edition in Florianopolis, Brazil, strengthens the cooperation between Europe and South America in the area of embedded systems, both at educational

and research levels. For this purpose, the goal of the school is to provide state-of-the-art courses on embedded systems oriented towards advanced students and young researchers.

This school is described in detail above, in the section on International Collaboration.

Artist2 Summer School in China 2008
July 12-18, 2008 Shanghai, China
http://www.artist-embedded.org/artist/-Artist2-Summer-School-in-China-.html

This was the 3rd edition of a school on Embedded Systems Design.
This year, the school was organized in collaboration with the SEI/ECNU and the LIAMA.

This year, we were able to do a far stricter degree of selection amongst the candidates. We selected 81participants – the fill list is available here.

This school is described in detail above, in the section on International Collaboration.

Real-Time Kernels for Microcontrollers: Theory and Practice
June 23-25, 2008 Pisa, Italy
http://www.artist-embedded.org/artist/-Real-Time-Kernels-for-.html

The course on Real-Time Kernels for Microcontrollers aims to introduce the basic concepts of Real-time Systems targeted to Embedded Systems, which are often implemented using microcontrollers. The course will briefly illustrate the theoretical background of real-time scheduling, resource-aware techniques, and wireless communication based upon the IEEE 802.15.4 protocol.

ARTIST2 Graduate Course on: Automated Formal Methods for Embedded Systems 2008
June 16-24, 2008 DTU - Lyngby, Denmark
http://www.artist-embedded.org/artist/-Automated-Formal-Methods-for-.html

In the lectures, we introduce a comprehensive set of state-based models as well as automatic procedures for their analysis. The exercise classes will complement this by providing hands-on experience with appropriate verification tools.

ARTIST2 Graduate Course on Embedded Control Systems
May 26-30, 2008 Stockholm, Sweden
http://www.artist-embedded.org/artist/-Graduate-Course-on-Embedded-.html

The course provides an account of state of the art theory and techniques that address the connection and integration of the areas of Control systems and Embedded systems.

3.3.3 Organisation of Workshops

In Year 4, Artist2 has directly organized and funded the following workshops.

MoCC 2008
July 3-4, 2008 Eindhoven, Netherlands
http://www.artist-embedded.org/artist/-MoCC-2008-.html

Embedded systems are omnipresent in modern society, and society crucially depends on their proper functioning. The complexity of embedded system design however is increasing rapidly, through the use of multiprocessor cores, through the integration of embedded systems in

ubiquitous networks, and through the increasing interaction between embedded systems and their users and environments. To obtain a reliable operation of embedded systems while maintaining resource efficiency, the embedded system design process needs to be based on a solid basis of computational models.

WCET'08
July 1st, 2008 Prague, Czech Republic (with ERCTS 2008)
http://www.artist-embedded.org/artist/-WCET-08-.html

The goal of the workshop is to bring together people from academia, tool vendors and users in industry that are interested in all aspects of timing analysis for real-time systems. The workshop fosters a highly interactive format with ample time for in-depth discussions.

OSPERT 2008
July 1st, 2008 Prague, Czech Republic (in conjunction with ECRTS)
http://www.artist-embedded.org/artist/-OSPERT-2008-.html

This workshop is intended as a forum for researchers and practitioners of RTOS to discuss the recent advances in RTOS technology and the challenges that lie ahead.

Movep'08
June 23-27, 2008 Orleans, France
http://www.artist-embedded.org/artist/-Movep-08-.html

MOVEP brings together researchers, students and people from industry working in the fields of control and verification of concurrent and reactive systems.

COMES 2008
June 17-18, 2008 Sigtuna, Sweden
http://www.artist-embedded.org/artist/-COMES-2008-.html

Component-based development aims of separation of development of components from systems, and reuse of existing components. This approach brings many (known) advantages, but also many challenges of which some are specific or in particular important for embedded systems. Since for embedded systems non-functional properties and resource constraints are of particular importance, this workshop focus on component-based approaches that ensure predictability of the system properties.

Mapping of Applications to MPSoCs
June 16-17, 2008 Schloss Rheinfels, St. Goar, Germany
http://www.artist-embedded.org/artist/-Mapping-of-Applications-to-MPSoCs-.html

1st Workshop on Mapping of Applications to MPSoCs

DataFlow Modeling for Embedded Systems
May 5th, 2008 Pisa, Italy
http://www.artist-embedded.org/artist/-DataFlow-Modeling-for-Embedded-.html

The topic of this workshop is the dataflow model/language CAL (CAL Actor Language), that recently has been developed within the Ptolemy II project at University of Berkeley. CAL is currently being used within the FP7 STREP project ACTORS and by Xilinx for modelling FPGA applications. CAL is also in the process of being adopted as the specification language for codecs within the MPEG-4 standard.

The aim of this workshop is to bring together the groups that are working with CAL and to discuss how CAL can be used within the context of embedded systems. The workshop is a

one day event with a number of invited speakers, both from industry and academia. It is aimed at the novice CAL programmer, as well as the more seasoned dataflow researcher.

APRES'08
April 21st, 2008 St. Louis, MO, USA
http://www.artist-embedded.org/artist/-APRES-08-.html

Adaptive systems can respond to environmental changes including hardware/software defects, resource changes, and non-continual feature usage. As such, adaptive systems can extend the area of operations and improve efficiency in the use of system resources. However, adaptability also incurs overhead in terms of system complexity and resource requirements. The purpose of the workshop is to discuss new and on-going research that is centred on the idea of adaptability as first class citizen and consider the involved tradeoffs.

SLA++P'2008
April 5th, 2008 Budapest, Hungary - an ETAPS'08 event.
http://www.artist-embedded.org/artist/-SLA-P-2008-.html

Model-driven High-level Programming of Embedded Systems, SLA++P'2008

ARTIST2 Timing Analysis activity meeting
March 13th, 2008 Munich, Germany
http://www.artist-embedded.org/artist/-ARTIST2-Timing-Analysis-activity-.html

Timing Analysis activity meeting within the Compilers and Timing Analysis cluster of ARTIST2 (in conjunction with the DATE'08 conference)

ATESST Open Workshop
March 3rd, 2008 Brussels, Belgium
http://www.artist-embedded.org/artist/-ATESST-Open-Workshop-.html

Model based development of embedded systems: the EAST-ADL approach for automotive applications - An ATESST project Event.

Synchron 2007
November 26-30, 2007 Bamberg, Germany
http://www.artist-embedded.org/artist/-Synchron-2007-.html

This workshop is devoted to all aspects of synchronous programming: languages, compiling techniques, formal methods, programming environments, execution platforms, semantics issues, code generation.

ARTIST2 meeting on Integrated Modular Avionics
November 12-13, 2007 Roma, Italy
http://www.artist-embedded.org/artist/Integrated-Modular-Avionics.html

Integrated Modular Avionics (IMA) has set the principles of standardized components and interfaces of hardware and software in aircraft, applied for the first time in the development of the Airbus A380.

WESE'07: WS on Embedded Systems Education
October 4-5, 2007 Salzburg, Austria (within ES Week)
http://www.artist-embedded.org/artist/WESE-07.html

This third workshop on the subject aims to bring researchers, educators, and industrial representatives together to assess needs and share design, research, and experiences in embedded systems education.

Foundations of Component-based Design
September 30th, 2007 Salzburg, Austria - within EmSoft / ES Week
http://www.artist-embedded.org/artist/Foundations-of-Component-based.html
Discuss recent results on component-based design with emphasis on design frameworks for real-time systems encompassing heterogeneous composition and models of computation.

Between Control and Software (in honour of Paul Caspi)
September 28th, 2007 VERIMAG - Grenoble, France
This workshop, synchronized with the retirement of Paul Caspi in autumn 2007, brought together experts in the field and collaborators of Paul at different periods for a series of lectures.
http://www.artist-embedded.org/artist/Between-Control-and-Software.html

3.3.4 Keynotes, Tutorials provided to the Embedded Systems Community

Over the course of Year 4, the Artist2 consortium has provided at least 178 keynotes, workshops, and tutorials to the embedded systems community.

Details including web links are available in the deliverable on Spreading Excellence.

3.3.5 Industrial Liaison

Artist2 has a wide array of affiliated industrial and SME partners, as described above. Most of these partners have participated in some way in the Artist2 technical meetings and the overall effort. There is strong, high-level industry participation through the various Spreading Excellence events organised by Artist2. Our active involvement in the European Technology Platform ARTEMIS also has a significant and long-term impact.

A more detailed description of industrial liaison activities is provided below.

3.3.5.1 ARTEMIS ETP

Several RTC Cluster partners, including CEA, INRIA, OFFIS, PARADES, VERIMAG; and TU Vienna, are actively involved in ARTEMIS, an initiative to form a European technology platform on embedded systems supporting the needs for various industrial and academic embedded application domains, such as the automotive, avionics, but also the real-time requirements of consumer electronics. The interaction with ARTEMIS is expected to influence the work within ARTIST2 positively towards establishing a well-defined conceptual fundament that is useful for academia and industry. Several partners (CEA, INRIA, OFFIS) are involved in EICOSE, the recently established European Institute for COmplex and Safety Critical Embedded Systems Engineering pushed by two French clusters System@tic Paris Région and Aerospace in association with the German cluster SafeTrans. EICOSE has been selected as the ARTEMIS Innovation Cluster on Transportation. VERIMAG and FT R&D contribute within French MINALOGIC cluster to promote the creation of a center of excellence in ARTEMIS encompassing "Nomadic environments" and "Private space" application contexts of

the ARTEMIS SRA chart. Contacts have been taken with Nokia and ElectroBit from the Finlandais Symetra Consortium.

The Joint Undertaking Artemis has been created in February 2008, and is about to close the evaluation of proposals submitted to the first call of the Artemis Joint Undertaking. As described above, EICOSE has played an instrumental role in coordinating the research priorities of both industrial and academic stakeholders in the transportation domain, contributing significantly to the Artemis Multi Annual Strategic Plan in the formation of three out of eight subprograms also forming the basis for the 1st call. Both OFFIS and CEA are members of the EICOSE steering board.

3.3.5.2 Industrial Liaison within the clusters

In the section on “Industrial Sectors”, within the cluster-level activity reports, detailed descriptions of collaborations between Artist2 teams and industrial partners are provided.

3.3.6 Publications

The Artist2 community has continued to be very active in publishing in scientific journals and conferences, as attested by the list of publications provided in this document. Clearly, this represents a huge amount of work. Publication of research is a bottom-up process, which may seem chaotic – but this is intrinsic to research.

Over the course of Year 4, the Artist2 consortium has published at least 184 joint papers, involving at least two distinct Artist2 core or affiliated partners. References for these are provided in the deliverable on Spreading Excellence.

The ARTIST community clearly leads the area, through the organisation of scientific events, the publication of seminal papers, education, and international collaboration.

3.4 Managing the Network of Excellence (JPMA)

Joint Programme of Management Activities

We believe that the current two-tiered Management structure - dividing the management amongst cluster leaders and the Strategic Management Board composed of both cluster leaders and a limited number of other selected prominent core partners – has been the right one for managing such a large research entity. It has provided the right combination of flexibility and accountability, while leaving room for innovation and evolution.

This management structure is reproduced with adaptations in the ArtistDesign NoE. The adaptations reflect the greater cohesion between partners, and move to capitalize on and strengthen the integration achieved in Artist2.

4. End Results

We have achieved a significantly more integrated scientific community. Initially, there was a strong fragmentation by topics and communities, with little interaction between them. Over the course of the NoE, the clusters have evolved and merged. A gradually cohesion has taken place, through transversal “NoE Integration” activities, and more importantly through strategic alliances.

We are seeing a convergence of interests, and the gradual emergence of recognized leaders.

IST-004527 ARTIST2
Network of Excellence
on Embedded Systems Design

Periodic Activity Report for Year 4

Joseph Sifakis – Artist2 Scientific Coordinator
Bruno Bouyssounouse – Artist2 Technical Coordinator

Artist2 Consortium

Table of Contents

1. Overview

1.1 Project Objectives and Major Achievements

A detailed description of objectives, and particularly the main aims for integration, is provided for each cluster in the sections labelled « State of Integration in Europe ».

1.1.1 Historical Perspective

Before setting up the Artist2 NoE, a subset of the current consortium implemented an FP5 Accompanying Measure, whose objectives were to:

- Coordinate the R&D effort in the area of Advanced Real-time Systems
- Improve awareness of academics and industry in the area
- Define innovative and relevant work directions

This was achieved through work along 3 axes:

- Roadmaps for selected actions: (Hard Real Time, Component-based Design, Adaptive Real Time, Execution Platforms)
- International Collaboration
- Education

Information about these results is publicly available:

http://www.artist-embedded.org/Roadmaps/

1.1.2 Current Relation to the State of the Art

The NoE's current relation to the State of the Art is provided in the deliverables for this review:

- This document:
  sections "Description of the Area", for each Artist2 cluster.
- Each of the sections called "Brief Description of the State of the Art", provided within each of the 24 activity deliverables.

1.2 Workpackage progress of the period

Given the size of this NoE, and the structuring by clusters, this information is provided in detail in sections 3-10 of this document.

1.3 Deliverables for the Reporting Period

The due date for all the Year4 deliverables was November 15th, 2008.

WP0 JPMA: Joint Programme of Management Activities

CDC	D1-Mgt-Y4	Year 4 Project Management Report	
UJF/VERIMAG	D2-Mgt-Y4	Year 4 Project Activity Report	
		Executive Overview	
	chapter 1	Overview	
	chapter 2	Real Time Components	RTC
	chapter 3	Adaptive Real Time	ART
	chapter 4	Compilers & Timing Analysis	Compilers&TA
	chapter 5	ExecPlatforms	Execution Platforms
	chapter 6	Control for ES	Control
	chapter 7	Testing and Verification	Test&Verif

WP1 JPIA: Joint Programme of Integration Activities

UJF/ VERIMAG	D4-RTC-Y4	Component Modelling and Verification (Platform)	RTC
Scuola Sant'Ana	D7-ART-Y4	A common infrastructure for adaptive Real-time Systems (Platform)	ART
Saarland	D12-CTA-Y4	Timing - Analysis (Platform)	Compilers&TA
Aachen	D13-CTA-Y4	Compilers (Platform)	Compilers&TA
DTU	D14-EP-Y4	System modelling infrastructure (Platform)	ExecPlatf
KTH	D18-Control-Y4	Design Tools for Embedded Control (Platform)	Control
Aalborg	D22-TV-Y4	Testing and Verification Platform for Embedded Systems (Platform)	Test&Verif

WP2 JPASE: Spreading Excellence

UJF/ VERIMAG	D3-Mgt-Y4	Report on Spreading Excellence	Global

WP3 JPRA : NoE Integration - Research Activities

UP Madrid	D8-ART-Y4	QoS aware Components (NoE Integration)	ART
Dortmund	D15-EP-Y4	Resource-aware Design (NoE Integration)	ExecPlatf
Lund	D19-Control-Y4	Adaptive Real-time, HRT and Control (NoE Integration)	Control
Twente	D23-TV-Y4	Quantitative Testing and Verification (NoE Integration)	Test&Verif

Please note that workpackages WP5-WP10 concern only Cluster integration (not NoE Integration), and do not include the Platforms (which are in WP1).
Workpackage 4 (Modelling and Components) was halted at the end of Year 1

WP5 JPRA: Real-Time Components

CEA	D5-RTC-Y4	Development of UML for Real-time Embedded Systems (Cluster Integration)	RTC
Uppsala	D6-RTC-Y4	Component-based Design of Heterogeneous Systems (Cluster Integration)	RTC

WP6 JPRA: Adaptive Real-time

Kaiserslautern	D9-ART-Y4	Flexible Resource Management (Cluster Integration)	ART
York	D10-ART-Y4	Real-Time Languages (Cluster Integration)	ART
Porto	D11-ART-Y4	Dynamic and Pervasive Networking (Cluster Integration)	ART

Please note that the only activity in WP7 was merged into the Timing Analysis Platform at the end of Year2.

WP8 JPRA: Execution Platforms

TUBS	D16-EP-Y4	Communication-centric systems (Cluster Integration)	ExecPlatf
Linkoping	D17-EP-Y4	Design for low power (Cluster Integration)	ExecPlatf

WP9 JPRA: Control for Embedded Systems

Lund	D20-Control-Y4	Control in real-time computing (Cluster Integration)	Control
UPVLC	D21-Control-Y4	Real-time techniques in control system implementations (Cluster Integration)	Control

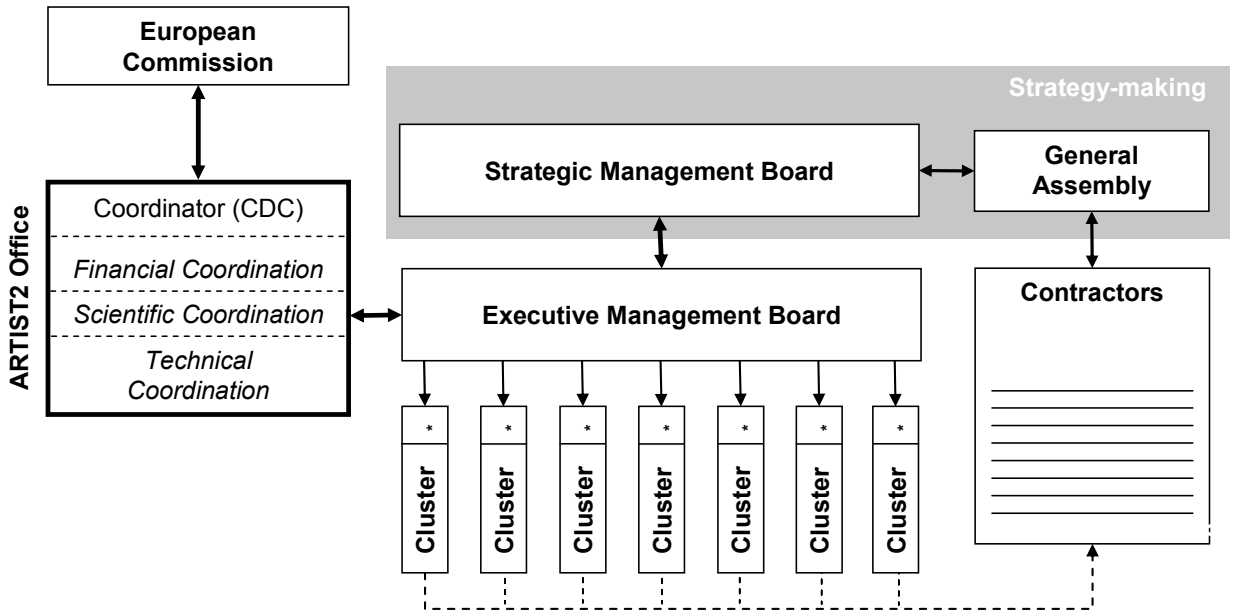
1.4 Consortium Management

This is unchanged from last year.

1.4.1 Governance Structure

Scientific Coordinator:	Technical Coordinator:
Joseph Sifakis	Bruno Bouyssounouse
Tel: +33 4 56 52 03 51	Tel: +33 4 56 52 03 68
Joseph.Sifakis@imag.fr	Bruno.Bouyssounouse@imag.fr
Mailing address: Verimag Laboratory - Centre Equation - 2, ave de Vignate - 38610 Gières - France	

The methodology adopted for achieving the JPA objectives follows the same lines as for managing a laboratory. The activities, their objectives, their technical description, the partners involved, their roles, and the resources available have been clearly defined in the initial Description of Work, and updated in the deliverables. This will be monitored and guided by a tight and rigorous management, as defined in the diagram below:



The main governance bodies are:

The **General Assembly** is composed of one representative per core partner. It is convened at the beginning of the project and meets once per year. It is chaired by the Scientific Manager.

The **Strategic Management Board** is initially composed of the NoE cluster leaders, and a representative of the Coordinator – who attends, with no voting rights. It is chaired by the Scientific Manager, assisted by the Technical Manager. It meets at least once per year – close to the General Assembly meeting. Its members are elected by the General Assembly every two years, according to modalities to be determined in the Consortium Agreement.

The **Cluster Leaders** (who compose the Executive Management Board) are responsible for the overall coordination of the activities led by their cluster. A cluster functions as a virtual team – with a degree of autonomy for defining its internal meetings and day to day management.

1.4.2 Partners Involved

This is provided in the publishable Executive Summary, in the first part of this document.

1.4.3 Contractors

There are no changes to the consortium at the end of Year 4.

1.4.4 Project Timetable

The JPA is organized into activities. The activities should not be considered as tasks of a workprogramme, with begin/end and synchronisation dependencies. Of course, the detailed description of an activity could be decomposed into sub-tasks and intermediate milestones, but this would imply a granularity that is too fine for research activities.

The inter-dependencies between activities are complex and rich, and will evolve dynamically. The work plan and major milestones for the activities are provided in cluster description, and repeated in the 18 month workplan.

1.4.5 Other Issues

None

1.4.6 Plan for using and disseminating the knowledge

The main instruments for using and disseminating knowledge are:

- Workshops and Schools organised.
  The list is quite impressive, and is provided in the deliverable on “Spreading Excellence”.
- Artist2 Web Portal.
  Here also, the quantity of information made available to the greater embedded systems community is quite impressive, and continuously growing. This is possible through the efforts of the entire consortium, who now have direct access for updating the contents.
- Course Materials.
  There is a growing body of course materials made available via the Artist2 web portal.
- Publications.
  The Artist2 consortium is very prolific in publishing research articles, surveys, textbooks, roadmaps, and position papers.

1.5 Metrics

It should be noted that these metrics are imperfectly measured, relying on voluntary feedback from partners.

1.5.1 Excellence Indicators

Indicator	number	*Method used*
Number of publications (journals, proceedings, etc) by ARTIST Partners in Embedded System Design over Year4	645	*from partners, (web form)*
Number of course books published by ARTIST Partners in the area over Year4	24	*from partners, (web form)*
Number of public keynotes, conferences, seminars and workshop in the area by ARTIST Partners over Year4. *NB: Due to differing definitions and data collection methods from one partner to the next, it should be noted that this figure is probably not very reliable.*	178	*From JPASE deliverable, section 5*
Number of white papers published in the area by ARTIST Partners over Year4	35	*from partners, (web form)*

1.5.2 Integration indicators

Indicator	number	*Method used*
Number of EC-funded projects in embedded systems, involving two or more ARTIST2 partners over Year 4 *NB: Due to differing definitions and data collection methods from one partner to the next, it should be noted that this figure is probably not very reliable.*	32	*from partners, (web form)*
[ICT-2007.1.2] IRMOS; [IST FP6] ACTORS (2008-2011), [ST] WASP (2008-2011), [FP6] HYCON NoE, [FP6] PREDATOR, [FP6] RIMACS, [FP7] COMBEST (2007-2010), [FP7] Speeds (2006/2009), [FP6] WASP (2006-2010), [FP6]FRESCOR (May 2006 May 2009), [FP7] MNENEE (2007-2010), [IST] ASSERT (2004-2007), [IST] MORE (2006-2009), [ITEA]ES_PASS (2007-2009), [ITEA2] TECOM (2007/2010), [NABIIT] MoDES (2006-2009), [VTU] D-ARTEMIS (2007-2009), ALL-TIMES 2008-2009, EU FP7 CONET (2008/2011), EU MORE 6/2006-5/2009, FP6 HiPEAC (2004-2008), FP7 HiPEAC (2008 – 2011), FP6 SHAPES (2006-2009), FRESCOR (2007-2010), [IST-FP7] Genesys FP7 18 months, [IST] ATESST, 04/01/2006 => 03/31/2008, KKS WCET 2006-2008, Quasimodo (Jan 2008-Dec2010), SPEEDS, Verisoft (03-10), VINNOVA FISS2 May 2007 - Dec 2009;; [FP7] FEEEDNETBACK; FP7 INTERESTED		

Number of other source funded projects in embedded system design, implying two or more ARTIST2 partners over year 4 *NB: Due to differing definitions and data collection methods from one partner to the next, it should be noted that this figure is probably not very reliable.*	18	*from partners, (web form)*
[CH] FIRE, [CH] MICS, [CH] PerformanceEvaluation, [ESA] Prototype Execution Time Analyzer for SPARC (Sept 2006/Feb 2007), [HTF] DaNES (2007-2010), [NABIIT] MoDES (2006-2009), [Spain PN] THREAD (2005-2008), [Spanish Government]THREAD (05/08), [Spanish project]THREAD (Jan 2005, Dec 2008) [Swedish Foundation for Strategic Research] SAVE(2003-2008), [US DARPA and Industry]: GSRC, [US NSF] CHESS, [VTU] D-ARTEMIS (2007-2009), ALL-TIMES 2008-2009, KKS WCET 2006-2008, SuReal (German BMBF, 2006-2008), Verisoft (03-10), VINNOVA FISS2 May 2007 - Dec 2009; EUROSYSLIB (Summer2007 - Dec2009)		
Number of PhD visiting other partners in the network over year 4	71	*from partners, (web form)*
Number of joint PhDs over year 4	35	*from partners, (web form)*
Number of visits between teams over year 4	115	*from partners, (web form)*
Number of public conferences, special sessions and workshop organised by ARTIST2 over year 4	31	*from website*
Number of jointly published papers from two or more partners from ARTIST2 over year 4 *NB: Due to differing definitions and data collection methods from one partner to the next, it should be noted that this figure is probably not very reliable.*	184	*From JPASE deliverable section 11*
Number of seminars and meetings attended by ARTIST partners from different clusters	*This is impossible to measure.*	
Number of research platforms or facilities shared for research	6	*JPIA*

1.5.3 Indicators about Spreading Excellence

Indicator	**number**	***Method used***
Summer Schools organised and funded by ARTIST2	6	*from website, section 3.3.2 of this document*

Other Summer Schools with Artist2 funding or participation	4	*from website*
Adoption of the recommended curricula in major European Schools	*This is impossible to measure.*	
Education: International seminars / training sessions organised specifically on Education WESE'08: WS on Embedded Systems Education *October 23rd, 2008 Atlanta, Georgia - USA (within ESWEEK)*	1	
Other international seminars / training sessions organised:	79	*from JPASE deliverable, section 5*
JPIA / Platforms : Number of uses for the platforms	*This is impossible to measure.*	
Number of papers published in top international journals and conferences	*Very large. This is very difficult to measure with any meaningful degree of accuracy.*	
Number of hits on the ARTIST2 web portal	2759886	*from JPASE deliverable, section 6*
International collaboration : nb of projects defined at the events	*This is impossible to measure.*	
Number of external links referring to ARTIST2 web portal	171	
Obtained from google, by searching for: `link:www.artist-embedded.org`		

1.5.4 Indicators on the financial independence from EC funding and from other sources

Indicator	**number**	***Method used***
Number of affiliated industrial partners	22	*from website*
Number of spinoff companies created	12	*from partners, (web form)*
Percentage of the ARTIST2 funding, respective to the partners' overall operating budget	*This is absolutely impossible to measure any meaningful way.*	
Number of affiliated partners willing to pay for membership in ARTIST2 *This would depend on the cost of membership, and the benefits they would get. Part of the benefits is the "seal of approval" involved in obtaining EC funding.*		
Overall revenue from membership dues from affiliated partners. *See previous question.*		

1.5.5 Indicators for Integrating the Gender Dimension

Indicator	**number**
Number of women currently active in the NoE	4
Number of women initially active in the NoE	1
Promotion of women in the area	No statistics