IST-004527 ARTIST2
Network of Excellence
on Embedded Systems Design

Activity Progress Report for Year 4

JPIA-Platform

Testing and Verification Platform for Embedded Systems

Clusters:

Testing and Verification

Activity Leader:

Professor Kim Guldstrand Larsen (Aalborg University)
http://www.cs.aau.dk/~kgl

Policy Objective (abstract)

Construction of powerful analysis tools by establishing a joint server platform providing extraordinary computational resources for conducting large-scale verification and testing efforts for embedded systems with respect to real-time requirements, quality-of-service guarantees as well as security properties.

The platform will provide a uniform, open and secure access and to all testing and verification tools of the academic as well as industrial partners of the consortium. The platform builds on existing works from the various partners and will also make available new powerful analysis tools developed within the network, in particular those from the related Joint Research Activities ("Quantitative Testing and Verification" and "Verification of Security Properties").

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1. Overview of the Activity

1.1 ARTIST Participants and Roles

Team Leader: Ed Brinksma (University of Twente)
verification and testing of reactive and stochastic systems.

Team Leader: Pierre Wolper (Centre Fédéré de Verification)
model checking.

Team Leader: Philippe Schnoebelen (LSV)
model checking.

Team Leader: Thierry Jeron (INRIA)
testing theory and tools.

Team Leader: Yassine Lakhnech (Verimag)
infinite state model checking.

Team Leader: Wang Yi (Uppsala)
model checking for real-time systems.

Team Leader: Tom Henzinger (EPFL)
model checking of embedded software and hybrid systems.

1.2 Affiliated Participants and Roles

Team Leader: Lubos Brim (University Brno)
distributed model checking.

Team Leader: Henrik Leerberg (IAR Systems A/S)
tool provider.

Team Leader: Tommy Ericsson (Telelogic)
tool provider.

Team Leader: Jan Tretmans (Nijmegen)
models and tools for model based testing

Team Leader: Sven H. Sørensen: (Motorola A/S)
end user.

Team Leader: Thomas Hune: (Terma A/S)
end user.

1.3 Starting Date, and Expected Ending Date

Start date September 1, 2004 to September 30, 2008

1.4 Baseline

The teams collaborating on this activity are leading tool providers for testing and verification, with particular emphasis on real-time, hybrid and stochastic aspects.

Automatic analysis of such quantitative aspects are crucial in validating embedded systems, but are computationally significantly more difficult than validation of simple functional aspects.

Thus, to address industrial size models continued development of new algorithmic techniques and data structures should be combined with powerful computational resources. We seek to establish this by maximal use, coordination and extension of existing local resources (e.g. PC-clusters) and by exploiting on-going work on exchange between and combinations of tools.

Despite advances in algorithmic techniques verification and test case generation are computationally notoriously hard problems.

Consideration of quantitative phenomena (real-time, stochastic) adds to the complexity. Thus, to address industrial size models powerful computational resources are necessary for example by maximal coordination of existing local resources.

The computational resources of the platform will initially be provided by existing powerful stand-alone computers with the various verification and testing tools being made available via a common web-based interface. A procedure for controlling access in a flexible and secure (e.g. in accordance with the individual tools licence agreements) manner will be investigated.

Among the tools that are candidates for beeing made available we mention: SPIN, SMV, UPPAAL, Kronos, Blast, TorX, TGV, FAST, CADP, IF; HyTech, visualSTATE, TAU, LASH, EMTCC and Rapture where the individual consortium member will have responsibility for integrating their tools into the platform.

The emerging advances in parallel and distributed model checking also motivate the development of a generally accessible server platform consisting of local clusters of (inexpensive) PCs.

Long term vision includes an experimental GRID infrastructure targeted specifically towards verification and testing.

1.5 Problem Tackled in Year 4

The following problems have been addressed during year 4:

- *Development of the individual tools*. First of all, the individual tools have been further refined – both with respect to functionality and performance:
  - Several improvements have been made to the real-time model checker UPPAAL: The engine is now able to merge DBMs dynamically when exploring the state-space. Another new feature is the addition of stop-watches. Any clock can be stopped. However, the algorithm used becomes an over-approximation whenever a state that is stopping a clock is reached.
  - The tool UPPAAL Tiga for timed games analysis has been extended with the possibility of simulating the synthesised winning strategies.
  - The probabilistic version of the distributed model checker DiVinE has been extended with quantitative LTL checking. Also, the regular DiVinE tool has been extended with algorithms that can exploit parallel disks in the model checking.

- *Dessimination and evaluation through industrial case studies.* The work of dessimination of the tools through case study demonstrators has been continued and documented through the joint web page for industrial case studies. Also, a number of additional dessimination and evaluation activities have been carried out by the partners via a number of national and international projects.
- *High performance tools serve interface.*The tools that are suitable for 64 bit architectures (SPIN) or distributed PC clusters (DiVine and UPPAAL) have been made accessible via a common web interface.

1.6 Comments From Year 3 Review

1.6.1 Reviewers' Comments

There were no specific comments from the reviewers – apart from a spelling error and a pending internal editorial note.

1.6.2 How These Have Been Addressed

There were no specific comments from the reviewers – apart from a spelling error and a pending internal editorial note. These have been corrected in the final deliverable.

2. Summary of Activity Progress

2.1 Previous Work in Year 1

During the first 12 months a number of improvements have been made on the individual tools as developed by the partners:

- The Vertecs team (IRISA) supports two test generation tools: TGV and STG. During the period, a new version of TGV (based on on-the-fly enumerative algorithms) linked to the IF toolbox (Verimag) has been developed using STL libraries (in place of CADP libraries).
- Results have been implemented in the TIMES tool for automated schedulability checking.
- CFV supports the verification tool LASH and hosts powerful servers dedicated to verification tools.
- A number of improvements have been made on the Uppaal real-time model checker (www.uppaal.com). This includes the possibility to enrich the timed automaton models with C code. An extension of Uppaal (Uppaal Cora), dedicated to solving optimal scheduling and planning problems, has been introduced. Recently, a version of Uppaal (Uppaal Tron), dedicated to online testing of real time systems, has been announced.

Also, a general distributed verification environment (DiVinE, Brno) has been deployed. The environment supports the development of distributed enumerative model checking algorithms, enables unified and credible comparison of these algorithms, and makes the distributed verification available for public use in a form of a distributed verification tool.

Finally, an overview of existing tools has been made accessible via a common web portal (the Yahooda web-page maintained by Brno).

2.2 Previous Work in Year 2

Development of existing and new tools

Brno has completed deployment of the distributed verification tool *"DiVinE"* (version 0.7) for enumerative model checking of LTL properties on a network of workstations. This includes the development of new algorithms for cluster-based decomposition of state spac into strongly connected components to be used in reduction of state spaces

Neijmegen has recently implemented an initial extension of the *TorX* tool (*TorXakis*) for symbolic testing – based on the formalism of Symbolic Transition Systems.

IRISA has worked on symbolic test selection for extended automata using abstract interpretation and included the results by improving test selection in their toolset *STG*.

Verimag has continued work on conformance testing for real-time systems and in particular worked on general improvements on the tool *TTG* (Timed Test Generator).

A new version of *UPPAAL* (Aalborg, Uppsala), UPPAAL 4.0, has been released with a number of new facilities and algorithms *user defined functions* (syntax follows the style of C/C++/Java, and most control-flow constructs of C are supported), *priorities and channels* may be specified and dealt with during analysis, full support for *symmetry reduction* is implemented enabled by

the introduction of a *scalar* datatype and the so-called *swep-line* method may be used to reduce memory consumption.

The online testing tool *Uppaal Tron* (Aalborg) has been ported to MS windows, and a new version 1.4 has been released. This represents a significant development effort since the OS and development environments on windows are quite different from those of Linux. We have identified specific technical problems with timing under windows. We believe that the windows version will greatly extend the applicability of the tool

A new variant of Uppaal, *Uppaal Tiga*, for the analysis and synthesis of winning strategies for times games has been released. Extensive evaluation of an experimental implementation of the algorithm yields very encouraging performance results.

Evaluation of tools

The planned work on tool dissemination and evaluation through case studies has been initiated through the establishment of an open repository for Artist2 Test and Verification Case Studies (https://bugsy.grid.aau.dk/artist2). The repository can be maintained by the individual tool providers and users through the use of Wiki.

Exploiting European Grid activities

ARTIST2 partners have participated in two European meetings on parallel and distributed model checking where the issue of exploiting grid activities to build a joint infrastructure has been discussed. The meetings showed that

- There are a number of ongoing European projects with respect to the usage of high performance and Grid-based servers for model checking. Each of the projects have made contributions through new distributed algorithms, new parallel architectures and new interesting applications, and it is likely that these activities will be their main focus for the immediate future. This means that the question of mutual exploitation of resources and the provision of a common web interface will be postponed for the time being.
- The long term vision of a joint high-performance verification platform is still relevant and should be maintained.
- There are already a number of facilities (e.g.) NorduGrid available that may be exploited be the individual tool providers and users. So far, a distributed version of Uppaal (DUppaal) has been made available on the NorduGrid in a certified manner via manual certificate distribution.

2.3 Previous Work in Year 3

The technical results below are based on joint collaboration between the partners in terms of tool sharing and evaluation (all partners) and the development of new algorithms for test generation and controller synthesis (Twente, CFV, LSV, Aalborg). Also, IRISA, Brno, Aalborg and Uppsala are contributing with further tool development – partly based on the new algorithms., and Aalborg and Brno are investigating the high performance platform issue. Finally, the partners contribute to cross-cluster activities on tools and platform integration, and also interact with communities out ARTIST2.

2.3.1 Technical Achievements

Development of existing and new tools

IRISA has improved the STG tool (test generation for models with control and data) and it is now freely distributed (http://www.irisa.fr/vertecs/software.html#STG). Its integration with the NBAC analyzer and the APRON library has been improved. Also, a number of cases studies have been developped and experimented.

UPPSALA has developed a prototype tool (named CATS) for compositional timing and performance analysis using timed automata and the real time calculus developed at EPFL. It is based on an over-approximation technique in which a component of a system, modeled as a timed automaton is abstracted as a transducer of event streams described by arrival curves from the real-time calculus. This allows us to characterize the semantics of a system as a set of equations over streams. Many interesting properties such as schedulability and buffer boundedness can be checked in solving the equations.The CATS tool is implemented in the Eclipse tool platform. As the main feature of the current version, it can be used to check the schedulability of a system and to estimate the best and worst case response times of its computation tasks. The tool is available for evaluation at www.timestool.com/cats.

AALBORG has continued its work on improving *UPPAAL* (www.uppaal.com) and its variants *UPPAAL Tron* (online testing) and *UPPAAL Tiga* (analysis and synthesis of winning strategies for timed games). In particular, the basic common DBM library has been improved and several industrial cases have been carried out. Also, the performance and the presentation of winning strategies have been improved significantly.

VERIMAG has implemented new techniques for deadlock detection in DeadlockFinder - a prototype tool that generates from BIP models sufficient conditions for deadlockfreedom.

BRNO has put a major effort into the development of tools to support parallel verification of complex embedded systems. The DiVinE tool has been made publically available and extended by a Promela front-end for SPIN compatible distributed model checking. With DiVinE Multi-Core (published at SPIN'07 and released in October 2007) the world-wide first parallel model-checker for multi-core architectures has been lunched. Furthermore, in the area of parallel techniques for the verification and analysis of embedded systems we focused on the development of new and enhanced algorithms for the enumerative parallel checking of reachibility, safety and liveness properties, in particular taking into account stochastic aspects of embedded systems.

Evaluation and dessimination of tools

A number of industrial case studies have been carried out by OFFIS, Twente, Aalborg and Uppsala. Apart from being documented via scientific papers, they are also collected and desseminated through the open repository for Artist2 Test and Verification Case Studies (https://bugsy.grid.aau.dk/artist2). Links to mature versions of the applied tools may also be found at the web page.

Investigations wrt. High-performance tool server

In most verification cases, the performance bottle neck is the state space explosion, i.e. the size of the internal memory for representing the state space. As a result of questioning the development teams and experimenting with the tools, it turns out that most academic verification tools are limited by the fact that they have been developed for a 32-bit architecture. In fact, only a few of them are considering to become upgraded to 64-bit architectures, and our investigation only identified a single 64-bit tool, namely the SPIN model checker. The SPIN team is currently working on extending the tool to exploit a multi-cpu shared memory architecture.

Hence, the available tools for a possible high performance tool server are currently SPIN (on a shared memory architecture) and UPPAAL/DiVinE (on distributed PC clusters).

Aalborg is currently installing a large (600 node) PC cluster which will be made available via NoduGrid (www.nordugrid.org). It will mainly be dedicated to scientific computing, but experiments with high-performance model checking (also parallel and distributed model checking) will be possible to a certain extent.

2.4 Final Results

2.4.1 Technical Achievements

Development of existing and new tools

IRISA have improved the symbolic test generation tool, STG, and a new version can be downloaded from Inria Gforge: https://gforge.inria.fr/plugins/scmsvn/viewcvs.php/?root=bjeannet.

VERIMAG have applied their test generation tool TTG http://www-verimag.imag.fr/~krichen/ttg/index.html for the automatic generation of robotics observers. Also, they have demonstrated how transformations between different tool formats may be applied for verification of quantitative properties (BIP tool suite vs. FXML/Jahuel).

AALBORG have further developed the UPPAAL Tiga tool for controller synthesis. Especially, the tool now supports simulation of the identified winning strategi. Also, the UPPAAL real time model checker has been further improved and optimized, and a new version is being distributed in near future.

OFFIS have developed a modelling and verification framework for protocol validation and illustrated the concepts through a major industrial traffic communication protocol.

BRNO have further optimized the DiVinE tool and evaluated its performance and scalability on large-scale parallel systems. For preliminary experiments they have used the Distributed ASCI Supercomputer, a wide-area distributed system for Computer Science research in the Netherlands. As a next step they plan to make large scalability tests on the new cluster in Aaalborg. BRNO have extended the DiVinE tool with I/O efficient verification algorithms, which allow to exploit parallel hard disks. Quantitative LTL mode-checking has been added to the probabilistic version of DiVinE.

Evaluation and dessimination of tools

Industrial case studies have been carried out by OFFIS, TWENTE and Aalborg. Apart from being documented via scientific papers, they are also collected and dessiminated through the open repository for Artist2 Test and Verification Case Studies

(https://bugsy.grid.aau.dk/artist2). Links to mature versions of the applied tools may also be found at the web page. In addition, Aalborg and OFFIS are involved in a number of industrial projects, where their own and also commercial tools are being applied in product development. E.g.:

- Uppaal Tron is being applied in the testing of new climate controllers for pig stables, and also in the testing of on-board satellite navigation software.
- Uppaal CORA (for cost optimal analysis) is being applied in the generation of cost optimal test cases for medical devices. As part of this development, a plugin for importing UML Stachart diagrams has been implemented.
- A commercial variant of UPPAAL (Vplus) is now being distributed for generating test cases to web services. The test cases provide plugins to commercial test execution tools like e.g. Mercury.

High Performance tool server

A common web interface for the tools supporting 64 bit architectures or distributed PC clusters has been developed and made accessible at https://benedict.grid.aau.dk/duppaal/ . In order to avoid misuse of the servers, one has to obtain certificate from the host organisation before it can be applied.

2.4.2 Individual Publications Resulting from these Achievements

BRNO

J. Barnat and L. Brim and S. Edelkamp and D. Sulewski and P. Simecek: Can Flash Memory Help in Model Checking, 13th International Workshop on Formal Methods for Industrial Critical Systems (FMICS 2008), 2008, 159--174.

J. Barnat and L. Brim and P. Rockai: DiVinE Multi-Core -- A Parallel LTL Model-Checker, ATVA 2008, to appear., 2008.

J. Barnat and L. Brim and I. Cerna and M. Ceska and J. Tumova: Local Quantitative LTL Model Checking, 13th International Workshop on Formal Methods for Industrial Critical Systems (FMICS 2008), 2008, 63--78.

J. Barnat and L. Brim and I. Cerna and S. Drazan and D. Safranek: Parallel Model Checking Large-Scale Genetic Regulatory Networks with DiVinE.

ENTCS, volume 194(3), 2008, 35--50.

J. Barnat and L. Brim and P. Simecek and M. Weber: Revisiting Resistance Speeds Up I/O-Efficient LTL Model Checking, Tools and Algorithms for the Construction and Analysis of Systems (TACAS)., Springer, 2008, volume 4963 of LNCS, 48-62.

J. Barnat and P. Rockai: Shared Hash Tables in Parallel Model Checking. ENTCS, volume 198(1), 2008, 79--91.

L. Brim and J.Barnat: Squeeze All the Power Out of Your Hardware to Verify Your Software! ISOLA 2008, Springer Verlag, 2008, volume 17 of CCIS, 604-618.

VERIMAG

Saddek Bensalem, Marius Bozga, Joseph Sifakis, Thanh-Hung Nguyen. Compositional Verification for Component-based Systems and Application. 6th International Symposium on Automated Technology for Verification and Analysis, October 20-23, 2008, Seoul, South Korea

Saddek Bensalem, Doron Peled, Hongyang Qu and Stavros Tripakis. Automatic Generation of Path Conditions for Concurrent Timed Systems. In Theoritical Computer Science, Volume 404, number 3, 28 Septembre 2008.

Saddek. Bensalem, Marius. Bozga, Matthieu. Gallien, Felix. Ingrand, Moez. Krichen and Stavros Tripakis. Automatic Generation of Observers for the Dala Robot with TTG. In the International Conference CISA 2008, Annaba, Algeria.

Ananda Basu, Matthieu Gallien, Charles Lesire, Thanh-Hung Nguyen, Saddek Bensalem, Felix Ingrand and Joseph Sifakis. Incremental Component-Based Construction and Verfication of a Robotic System. ECAI 2008 The 18th European Conference on Artificial Intelligence, Patras, Greece, July 21 - 25, 2008.

OFFIS

Werner Damm, Alfred Mikschl, Jens Oehlerking, Ernst-Rüdiger Olderog, Jun Pang, André Platzer, Marc Segelken, and Boris Wirtz. Automating verification of cooperation, control, and design in traffic applications.. In Cliff Jones, Zhiming Liu, and Jim Woodcock, editors, Formal Methods and Hybrid Real-Time Systems, volume 4700 of LNCS, pages 115-169. Springer, 2007.

TWENTE

H. Boudali and P. Crouzen and B.R.H.M. Haverkort and M. Kuntz and M.I.A. Stoelinga: Architectural dependability evaluation with Arcade. Proceedings of the 38th IEEE/IFIP International Conference on Dependable Systems and Networks (DSN2008). IEEE Society, 2008.

H. Boudali and P. Crouzen and M.I.A. Stoelinga: A compositional semantics for Dynamic Fault Trees in terms of Interactive Markov Chains, Proc. of the 5th International Symposium on Automated Technology for Verification and Analysis, 2007, 441-456.

H. Boudali and H. Sozer and M.I.A. Stoelinga: Model-based Availability Analysis of Software Decomposition for Local Recovery, submitted to Fundamental Approaches to Software Engineering (FASE09).

H. Sozer and B. Tekinerdogan: Introducing Recovery Style for Modeling and Analyzing System Recovery, Proceedings of the 7th Working IEEE/IFIP Conference on Software Architecture (WICSA), 2008, 167-176.

AALBORG

P. Bouyer, U. Fahrenberg, K. G. Larsen, N. Markey and J. Srba. Infinite Runs in Weighted Timed Automata with Energy Constraints. In Proceedings of the 6th International Conference on Formal Modelling and Analysis of Timed Systems (FORMATS'08), Saint-Malo, France, September 2008, LNCS 5215, pages 33-47. Springer.

P. Bouyer, K. G. Larsen and N. Markey. Model Checking One-clock Priced Timed Automata. Logical Methods in Computer Science 4(2:9), 2008.

P. Bouyer, E. Brinksma and K. G. Larsen. Optimal Infinite Scheduling for Multi-Priced Timed Automata. Formal Methods in System Design 32(1), pages 2-23, 2008.

Anders Hessel, Kim Guldstrand Larsen, Marius Mikucionis, Brian Nielsen, Paul Pettersson, Arne Skou: Testing Real-Time Systems Using UPPAAL. Formal Methods and Testing 2008: 77-117.

Sebastian Kupferschmid, Jörg Hoffmann, Kim Guldstrand Larsen: Fast Directed Model Checking Via Russian Doll Abstraction. TACAS 2008: 203-217

2.4.3 Interaction and Building Excellence between Partners

The partners developing tools meet on a regular basis with the partners that contribute to the further development of algorithms in order to evaluate and improve the tools as may be seen from list of joint publications below.

Several partners (CFV,LSV,Twente,Aalborg) participate in a FP7 project on quantitative aspects of embedded systems (Quasimodo). A key element of this project is the development of tool plugins aimed to be applied in a variety of tools (commercial or academic).

Uppsala and Aalborg meet on a regular basis to coordinate ethe further development of the UPPPAAL tool which forms the basis of a large part of the platform activities.

At a national level, a cross cluster collaboration between the Danish ARTIST2 partners Aalborg and DTU (execution platforms) is taking place via a large national grant in an industrial project (DaNES) on tools and platforms for intelligent embedded systems. Also, a national grant is used to promote industrial awareness towards the forthcoming FP7 calls within the ARTEMIS JTI programme.

2.4.4 Joint Publications Resulting from these Achievements

P. Bouyer, U. Fahrenberg, K. G. Larsen, N. Markey and J. Srba. Infinite Runs in Weighted Timed Automata with Energy Constraints. In Proceedings of the 6th International Conference on Formal Modelling and Analysis of Timed Systems (FORMATS'08), Saint-Malo, France, September 2008, LNCS 5215, pages 33-47. Springer.

P. Bouyer, K. G. Larsen and N. Markey. Model Checking One-clock Priced Timed Automata. Logical Methods in Computer Science 4(2:9), 2008.

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Anders Hessel, Kim Guldstrand Larsen, Marius Mikucionis, Brian Nielsen, Paul Pettersson, Arne Skou: Testing Real-Time Systems Using UPPAAL. Formal Methods and Testing 2008: 77-117.

Sebastian Kupferschmid, Jörg Hoffmann, Kim Guldstrand Larsen: Fast Directed Model Checking Via Russian Doll Abstraction. TACAS 2008: 203-217

2.4.5 Keynotes, Workshops, Tutorials

Keynotes

T. Jeron, invited talk at SBMF 2008, Symbolic model-based test selection, In Brazilian Symposium on Formal Methods (SBMF 2008), Salvador, Bahia, Brazil, August 2008, to appear in ENTCS. http://www.lasid.ufba.br/sbmf2008/

Kim G. Larsen. 'Timing and Performance Analysis: Static Analysis versus Model Checking'. Invited Talk on the Honoris Causa to Professor Dr. Reinhard Wilhelm from RWTH Aachen. Germany. October 24, 2008.

Kim G. Larsen. Model-driven Test and Verification of Real-Time and Embedded Systems. Test Conference, Aalborg University. Denmark. October 20, 2008.

Kim G. Larsen: Verification, Performance Analysis, and Controller Synthesis for Real-Time Systems. Invited talk. Marktoberdorf Summerschool. Marktoberdorf, Germany. August 5-16, 2008. http://asimod.in.tum.de/

Workshops

7th International Workshop on Parallel and Distributed Methods in verifiCation - PDMC 2008. Affiliated to ETAPS 2008, March 29-April 6, 2008. http://pdmc.informatik.tu-muenchen.de/PDMC08/

Dagstuhl seminar on Distributed Verification and Grid Computing. 10.08.08 - 14.08.08, Seminar 08332, Organized by: Henri E. Bal (Vrije Universiteit Amsterdam, NL),Lubos Brim (Masaryk University, CZ), Martin Leucker (TU München, DE). http://www.dagstuhl.de/de/programm/kalender/semhp/?semnr=08332

3. Milestones, and Future Evolution Beyond the NoE

3.1 Milestones

Below, the milestones for September 1, 2007 until September 30, 2008 are recalled and commented (se also current technical annex page 26 and D22-TV-Y3 page 14):

- The case tool repository will be updated along with the ongoing work on tool evaluation through case studies. This includes links to stable and mature tool versions will. *This is achieved through a few additional cases (https://bugsy.grid.aau.dk/artist2) and also through a number of industrial collaborations (see section xxx of the cluster report for Testing and Verification).*
- The three candidates for high-performance verification (SPIN, DUPPAAL, DiVine) will be tested on the new cluster in Aalborg and will be made available for experiments after special agreements with NoduGrid and the tool developers. *This is achieved through the joint web interface at https://benedict.grid.aau.dk/duppaal/ . The interface accesses mature versions of the three model checkers (30GB single CPU memory for SPIN and 96GB distributed memory on 48 CPU´s for DUPPAAL and DiVine). Certificates has to be obtained on an individual basis in order to avoid misuse of the facility.*
- Links to existing activities on high performance verification resources will be maintained. *This is achieved through Brno's participation in the European project . . . on high performance model checking.*

3.2 Indicators for Integration

Establishment of a common access to *all mature* tools that are available on scalable architectures (64 bit and/or cluster based). The successful integration of several of the computational resources available to the consortium in a verification grid, as this will provide an extremely powerful, yet inexpensive platform.

The leading quality of the tools available should make the web access attractive for all clusters of ARTIST2 as well as industry.

As for the tool evaluation through industrial case studies, partners are regularly reporting their results into the shared repository. Furthermore, the particular techniques of the individual tools are subjects for ongoing discussions at the project meetings.

The close links to the European Grid projects via Aalborgs participation in NorduGrid assures the access to the most recent Grid technology when it becomes available. Also, BRNO participates in the European project ec-moan and keeps thereby close links to the scientific computing community.

3.3 Main Funding

Funding from various national funding agencies and centres, such as:

- Centre for Embedded Systems, CISS (http://ciss.auc.dk/),

- MoDES (http://www.cs.aau.dk/modes),
- DaNES (http://danes.aau.dk),
- Dutch national projects STRESS, HaaST, IMPASSE, MC=MC, CASH (see http://fmt.cs.utwente.nl/),
- EU (EC-MOAN project): Modeling and analysis techniques to study emergent cell behaviour,
- Swedish strategic research (SAVE project): Component Based Design of Safety Critical Vehicular Systems
- Swedish research council (UPPAAL/TIMES): Modeling and verification of timed systems
- DCGC: Danish Center for Grid Computing (http://www.dcgc.dk, in Danish).
- French RNTL project Testec (Testing of real-time embedded control-command systems) with Lurpa (Ens Cachan), Inria (Rennes), I3S (Nice) , Labri (Bordeaux), EDF R&D, TNI Software has been accepted.

3.4 Future Evolution Beyond the Artist2 NoE

The international collaboration on further tool development will be continued in in the ArtistDesign NoE through the activities on modelling and validation. Also, a more focused effort will be made on tool development for quantitative aspects of embedded systems within the EU FP7 STREP Quasimodo (www.quasimodo.aau.dk) where most of the partners are also ARTIST2/ArtistDesign partners. Finally, additional EU applications on tool development are foreseen within the EU Artemis Joint Initiative.

As for the high performance tool servers, additional tools will be added when they become available on modern architectures. Also, the servers are likely to be replaced and/or upgraded as new facilities become available.

4. Internal Reviewers for this Deliverable

Contributions and internal review has been made by Bruno Bouyssounouse (UJF/Verimag), Arne Skou (Aalborg).