ArtistDesign Kickoff Meeting

Paris, January 29-30, 2008

Cluster presentation

Design for Predictability and Performance

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Main Research Trends in the Area

Overall Goal: Achieve predictability for timing and resource (energy, memory, …) consumption, without sacrificing performance

Some current research directions:

- Modeling and analysis techniques
  - Component-based design,
  - For timing, energy consumption, …
- Networks
  - Predictable communication networks
- Scheduling of Tasks
  - Techniques to minimize interference between tasks,
  - Predictable scheduling in spite of variable load
    - Contract-based scheduling, …
    - Energy-aware scheduling, ….

Main Research Trends in the Area (ctd.)

- Increased predictability of software mechanisms
  - Coding for predictability (of memory access,
  - Predictable/real-time garbage collection, method dispatch, etc.
  - Contracts/component-based systems,
  - Predictable middleware (with QoS guarantees)
  - resource-aware abstraction
- Hardware architectural features
  - Predictable memory systems (scratchpads, predictable caches)
  - predictable virtual memory systems
  - Multicore platforms (how to make them predictable?)
  - (* add *)

High-Level Objectives

Overall Objective: Develop technology, design, and analysis techniques for system predictability, on modern platforms, without sacrificing performance

Approach:

- Modeling and analysis techniques for non-traditional system structures, component-based design techniques, mappings from design models to platform architectures, scheduling techniques
- Timing analysis, esp. for modern multi-core and MPSoC platforms
- OS/MW/Networks: Trade-off between predictability and performance in scheduling
- Hardware Platforms: resource modeling, predictable features,

Cluster Participants

Core Partners:

- Luca Benini (Bologna – Italy)
- Michael Gonzalez–Harbour (Cantabria – Spain)
- Peter Marwedel (Dortmund – Germany)
- Tom Henzinger (EPFL – Switzerland)
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- Alan Burns (Univ. of York – UK)
- Alberto Sangiovanni – Vincentelli (PARADES – Italy)

Affiliated Partners:

- Rolf Ernst (Graunschweig – Germany)

Planned Activities Y1

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Modeling and Validation:

- Techniques for analyzing timing properties for distributed architectures
- Component resource contracts for scheduling

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Compilation and Timing analysis

- WCET analysis for intra-task scheduling, and multiprocessor systems, shared memory
- Compiler techniques for memory-wall problem
- Synergetic implementation of code synthesis, compilation, and timing analysis

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OS/MW/Networks

- Predictable OS Architecture

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System Architectures and Hardware Platforms

- Predictable low power design
- Memory structures and bus architectures
- Flexible multi-level architectural models for “horizontal” and “vertical” composition with predictable performance

Plans for Year 1 (Summary)

Planned tools and platforms work in the Description of Work

- WCET tool (Braunschweig) + system analysis tool (Linköping)
- Comparison MPA-RTC (ETHZ), SymTA/S (Braunschweig), UPPAAL (Uppsala)
  - Investigate connection to FRESCOR contracts technology (Cantabria)
- Cooperation between PREDATOR project (Saarland) and TU Dortmund:
  - Overall goal: achieving predictability over all levels of the HW/SW stack:
  - Dortmund does: Reconciliation of compilers and timing analysis
    Explicit timing cost model within the compiler
    Multi-objective optimization within the compilation tool flow
- Cooperation between Dortmund and ICD (MNEMEE project) on predictability for memory accesses using scratchpads and optimizations for caches
- Architecture activities for predictability
- Time-predictable operating system (Vienna).
  - Definition of such an OS available at time t+18
- Architectural models for non-functional properties (PARADES)

Compiler activities for predictability (more detailed view)

- Cooperation inside PREDATOR project (Saarland) and TU Dortmund:
  - Overall goal: achieving predictability over all levels of the HW/SW stack:
  - Dortmund does: Reconciliation of compilers and timing analysis
    Explicit timing cost model within the compiler
    Multi-objective optimization within the compilation tool flow'
  - Specific planning will be done at PREDATOR Kick-Off, March 2008, Bologna
- Cooperation between Dortmund and IMEC, ICD (MNEMEE project) on predictability for memory accesses using scratchpads and optimizations for caches

Architecture activities for predictability (more detailed view)

- Predictable Memory hierarchies
  - caches
  - virtual memory systems,
  - can be shared between processing elements
- Predictable communication fabric (Bologna, Linköping)
- Concrete plans (part of PREDATOR)
  - Extend the MP-ARM simulator (Bologna)
  - Low-level software support (hardware abstraction layers) (Bologna)
  - Plans will be made at PREDATOR Kick-Off

Indicators, Milestones,

Indicators (my suggestion)

- Joint publications, organization of workshops, ….
- Tool connections

OTHER

- Planned workshop on Predictability (Summer 2008) (Saarland, …)

Concrete Contributions

Workshops

Interaction with Industry

Schools

Education and training

Publications with collaborating authors

Industrial liaison

International collaboration