ARTIST2 Summer School 2008 in Europe

Autrans (near Grenoble), France

September 8-12, 2008

Heterogeneous Platforms for Embedded Systems

Invited Speaker: Giovanni De Micheli

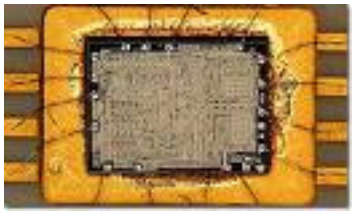
EPFL

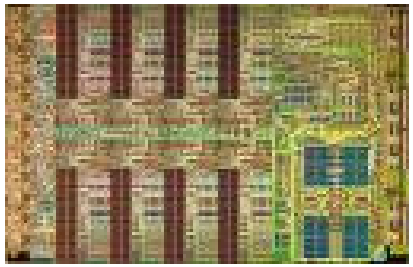
Centre SI
Integrated Systems Centre

Quo vadis ?

- We came a long way …
  - 50 years of electronics


[Bell labs]


[Intel]


[IBM]

- … and where are we going?
  - The next 50 years


[Kubrick:2001]

How did we affect society ?

- From transistor radio …

[Motorola]


[IBM]

[Sony]

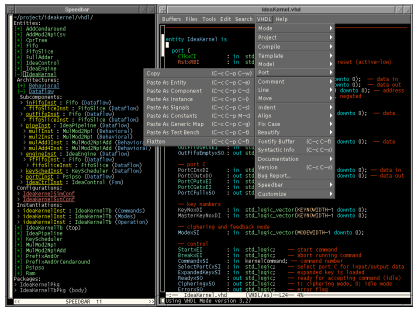

[Apple]

- Entertainment, personal computing, communication

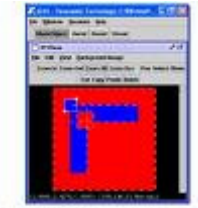
- Can we have a deeper impact into market and society?
  - Who will benefit?
    - Socially?
    - Economically? Which market sector?

How did we engineer products ?

- Electronic Design Automation (EDA)
  - Provides us with the enabling technology
  - Formal modeling, analysis, synthesis



- But EDA
  - … is entangled in solving *deep submicron* issues
  - … missed opportunities at system-level design
  - … is still a small niche market



- Can we reposition DA as a central engineering task?
  - Broader in scope
  - Scientifically challenging
  - Attracting the best young researchers
  - Creating more value

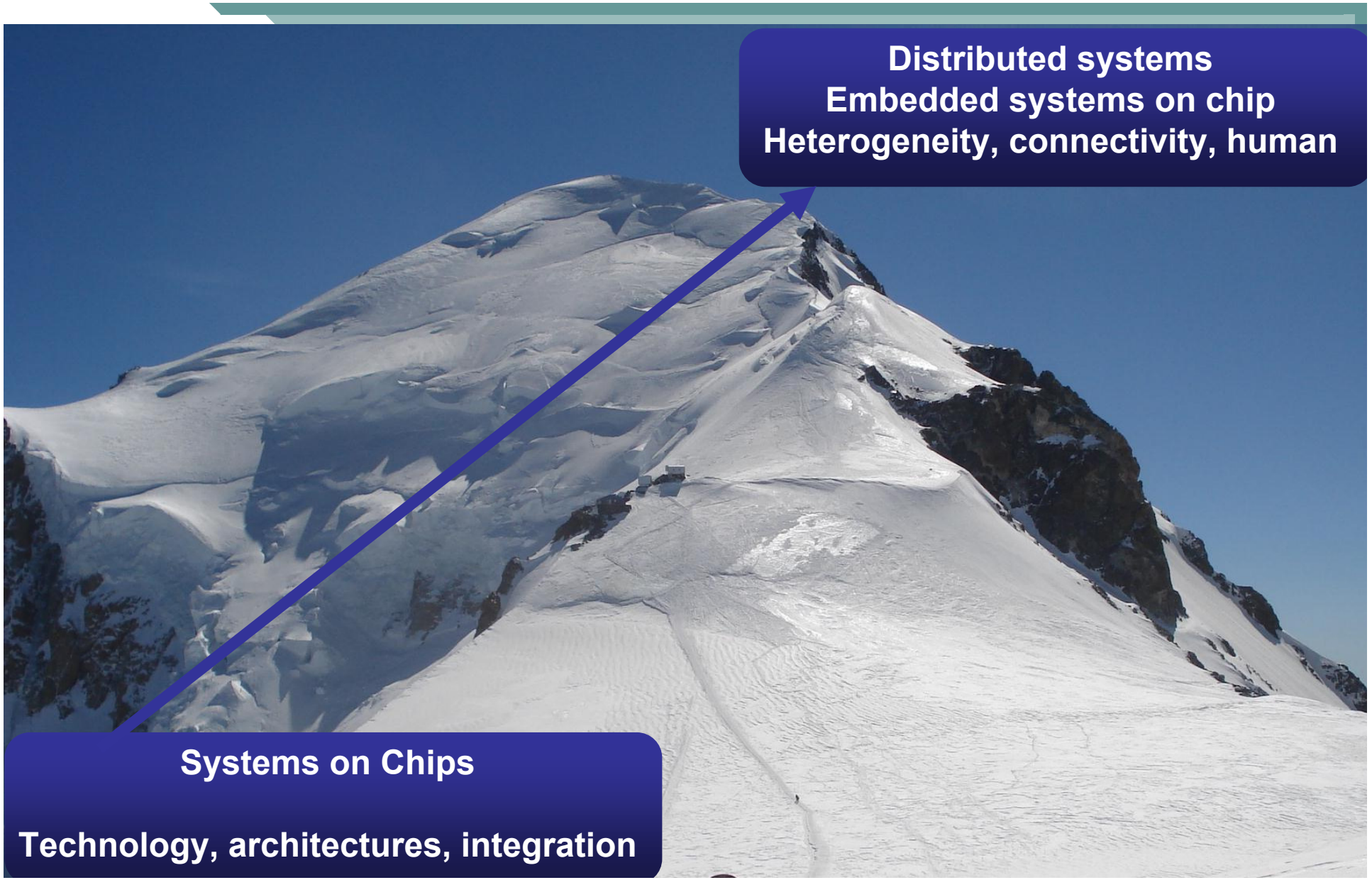
The next fifty years…

- Ubiquitously-distributed electronics
  - Electronic circuits and systems distributed in clothing, car, home, office, environment…
- A global market affecting everybody's everyday's life
- Some audacious goals:
  - Break language barriers
  - Eliminate energy dependence
  - Link up every human
  - Better health, safety and longevity
  - Protect and monitor our environment

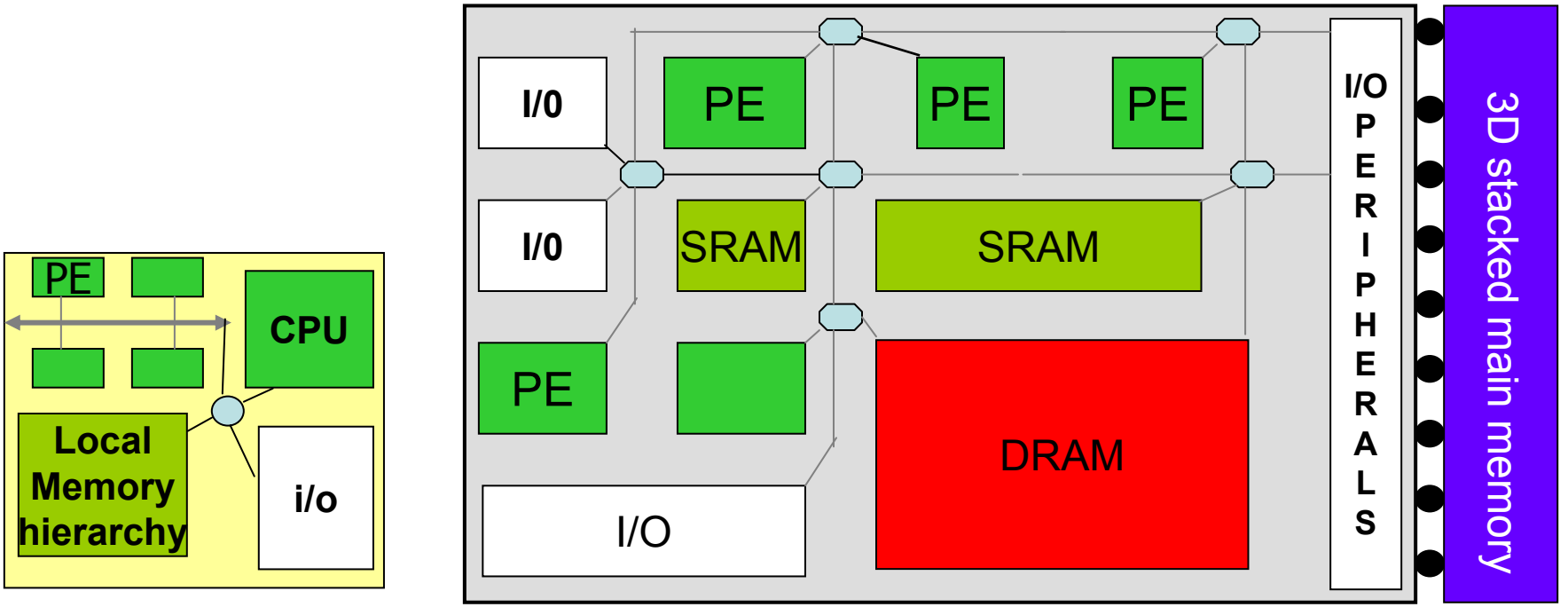
[Infineon]

[QBUS Domotica]

The way ahead

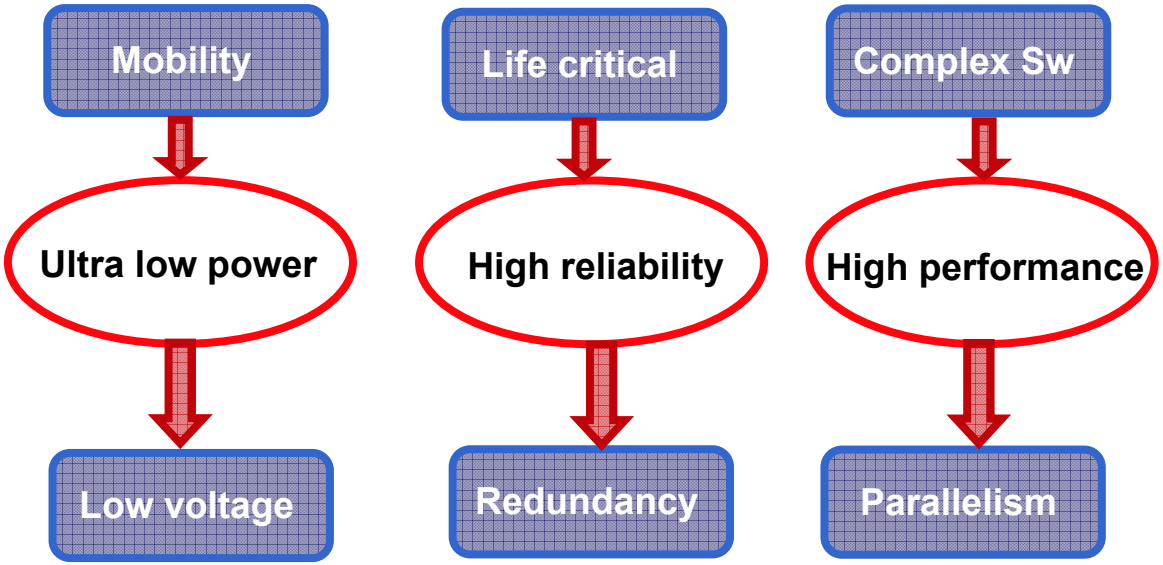


System on Chip evolution

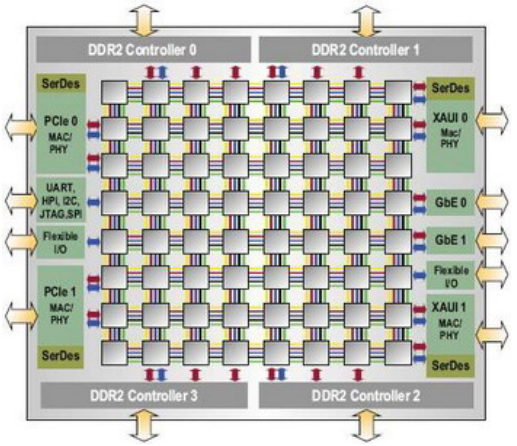


- Roadmap continues: 90→65→45 nm
- “Traditional” Bus-based SoCs fit in one tile !!
- Communication demand is staggering, but unevenly distributed, because of architectural heterogeneity

Requirements for electronic chip design



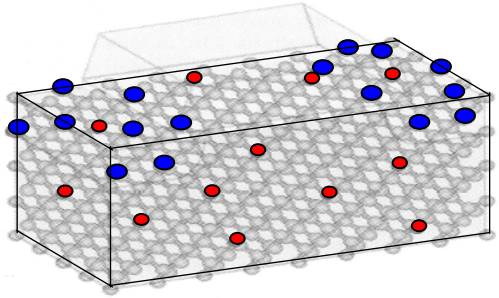
- From processors to multi-processors
  - Technology support
  - Systems and software redesign



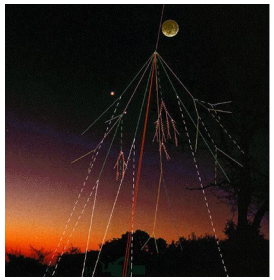
[Tilera]

Major SoC design issues

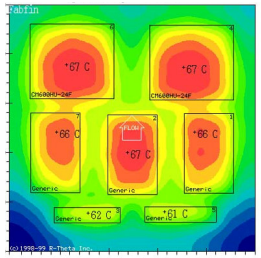
- Variability
  - Physical parameter variation
  - Microscopic structural effects



- Reliability
  - Higher failure rate
  - Higher exposure to environmental effects

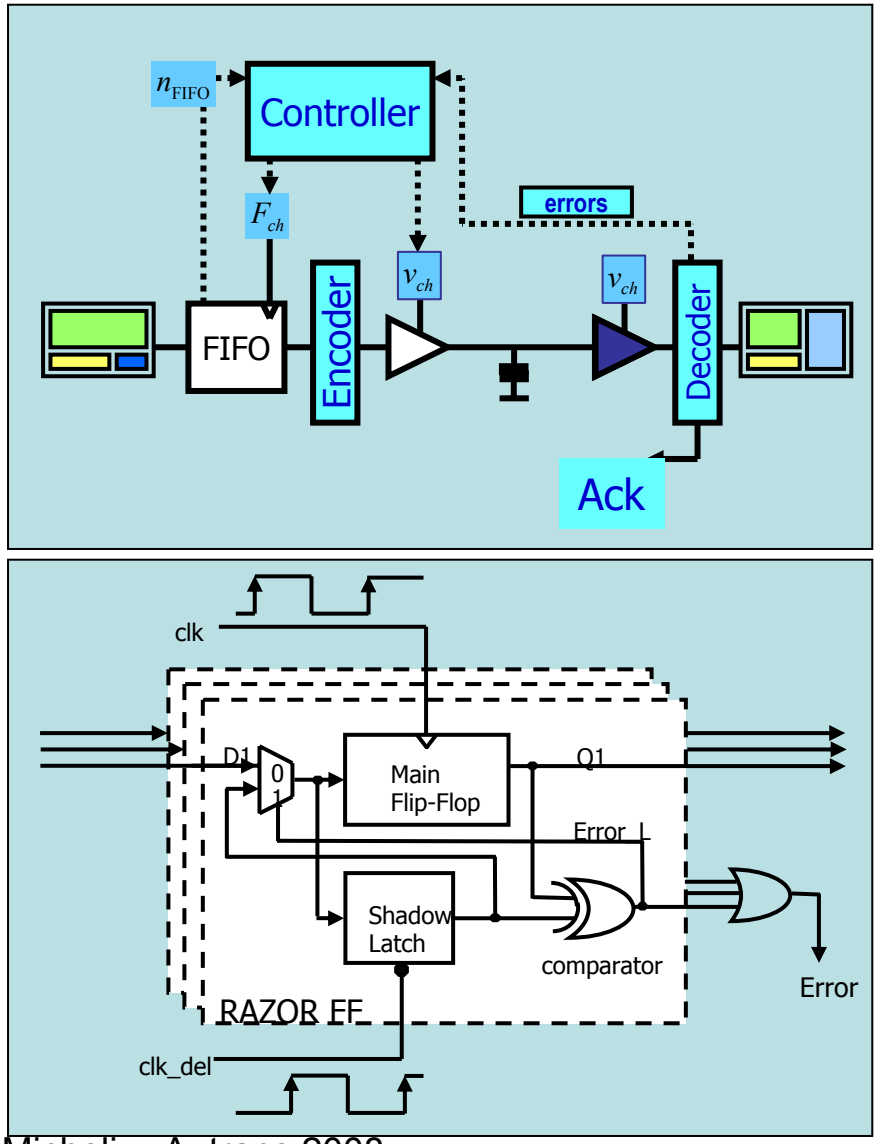


- Thermal management
  - Heat extraction and temperature gradient avoidance
  - Temperature correlates with higher failure rates



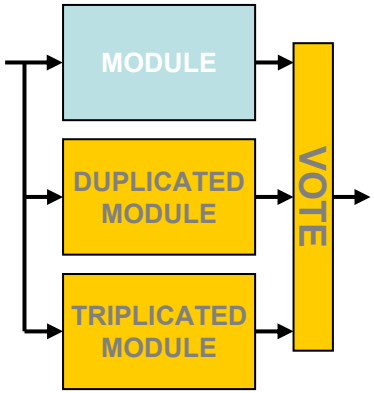
Self-calibrating circuits

- Design self-calibrating circuits operating at the edge of failure
- Examples:
  - Dynamic voltage scaling of bus swings [Worm,Ienne –EPFL]
  - Dynamic voltage scaling in processors
    - Razor [Austin – U Michigan]
  - Dynamic latency adjustment for NoCs
    - Terror [Tamhankar -Stanford]
- Autonomic computing
  - Systems that understand and react to environment [IBM]



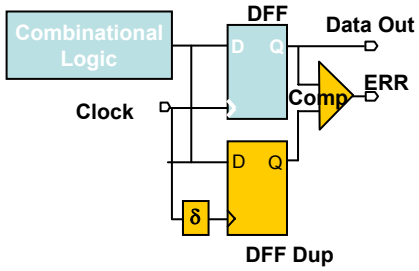
Soft-error protection

Redundancy (TMR)



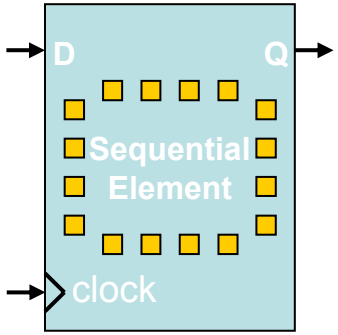
100% to 200% overhead

Detection + System Correction



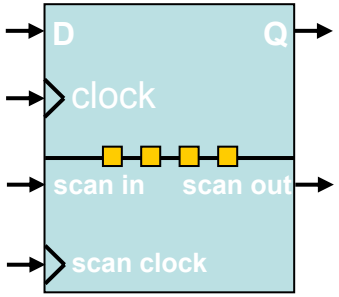
ERR signal used by system (Hardware or Software) to correct the error

Hardened Libraries



Protection Transistor embedded in the cell

Other Techniques



Scan Sequential Element

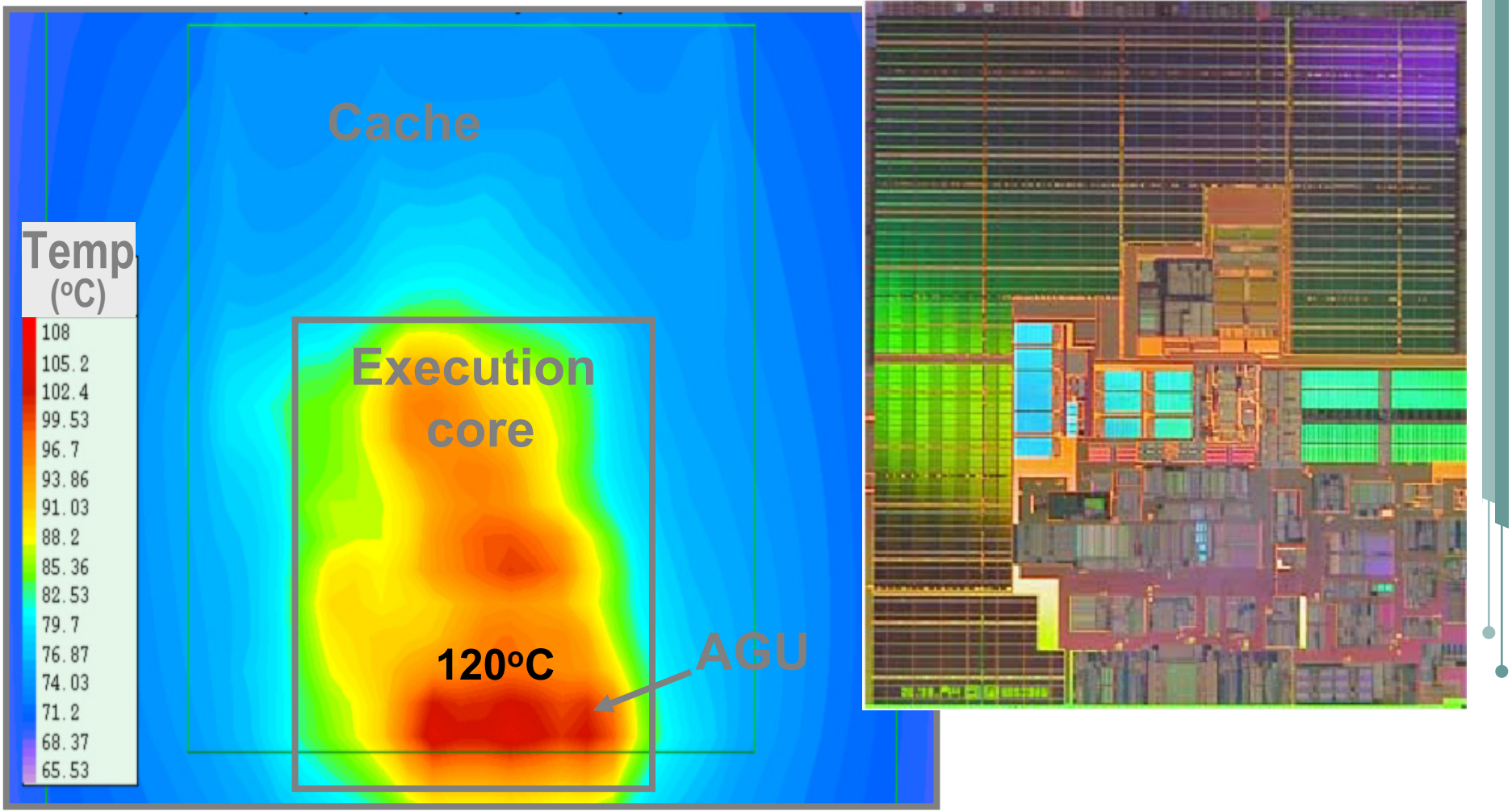
SCAN hardware used as DETECTION hardware in functional mode

Redundancy ***Shielding*** ***Others***

[Source IROC]

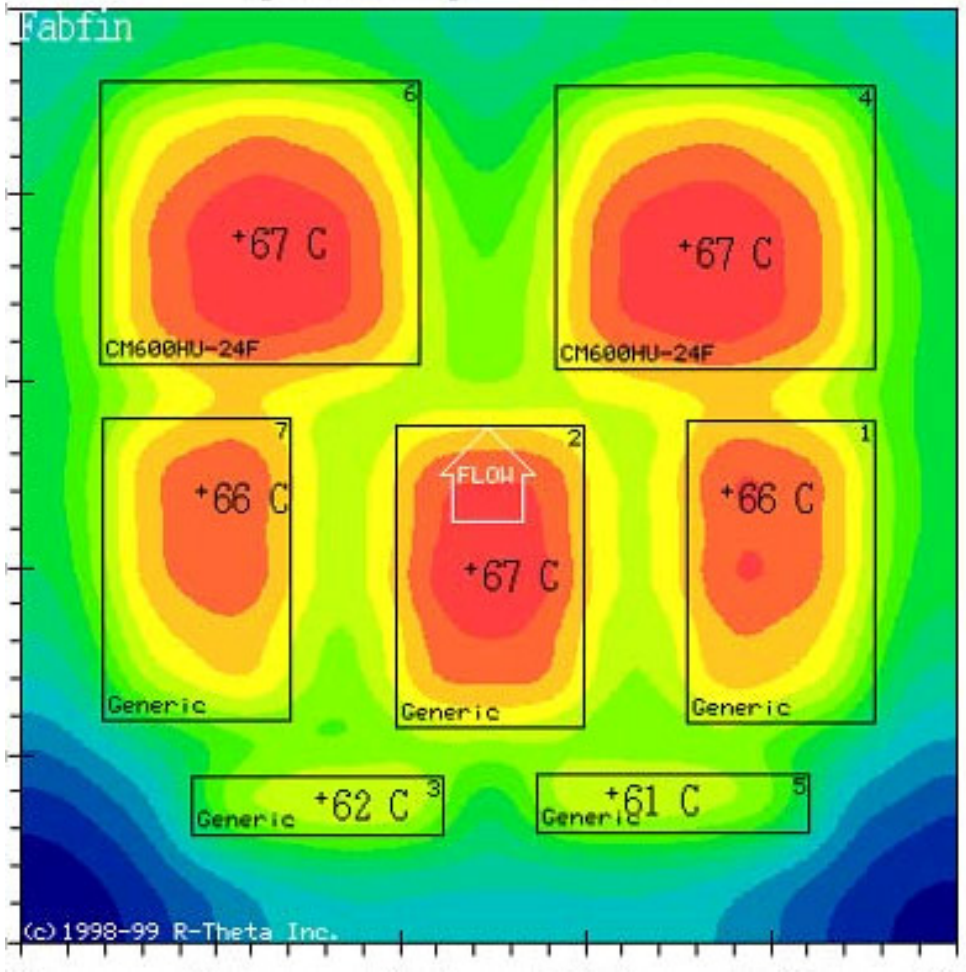
Thermal issues

1.5 GHz Itanium-2



[Source: Intel Corporation and Prof. V. Oklobdzija]

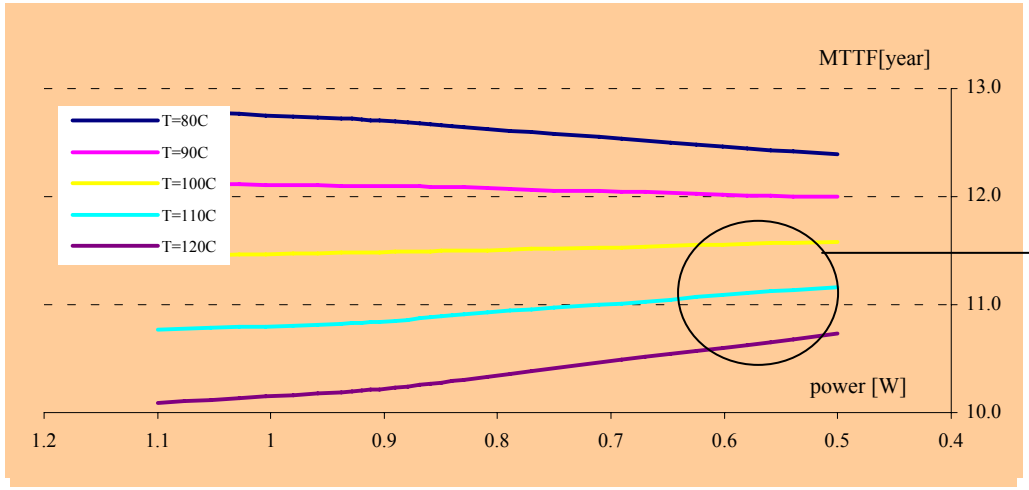
Thermal map: multiprocessosr



- Temperature gradients:
  - Time-varying because of DPM/DFS/DVS

Thermal management

- Keep chip as cool as possible
  - Reduce failure rates and power consumption
- In multi processor (core) system, power management shuts down idle cores
  - The temperature distribution will change in time
  - Thermal stress may increase
- Balance temperature reduction and thermal stress

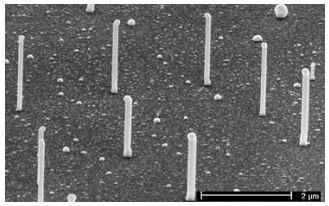
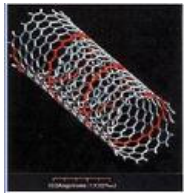
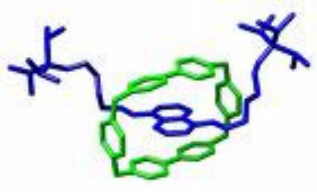


Positive effect of DPM
EM and TTB dominate
High T – small gap

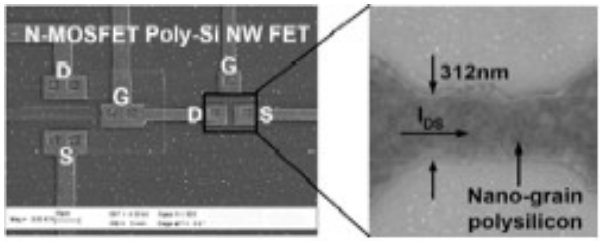
[Simunic, UCSD]

The fabrication technology support

- Beyond CMOS: a myriad of new ideas

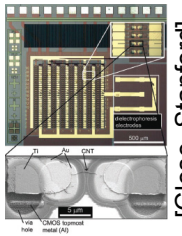




- Are these technologies apt/ready for system design?
- Can they mix and match with CMOS?



[Leblebici, EPFL]

[Infineon]

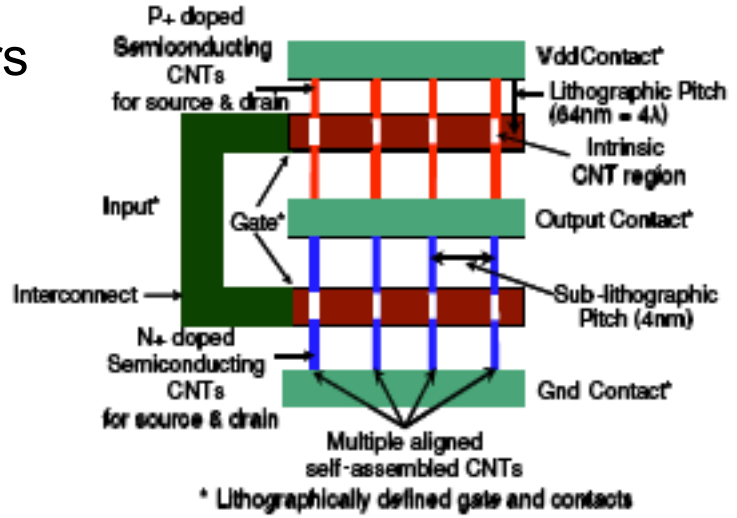


[Close, Stanford]

- How do we design with these technologies?
  - Higher defect densities and failure rates

Enhancing silicon technology

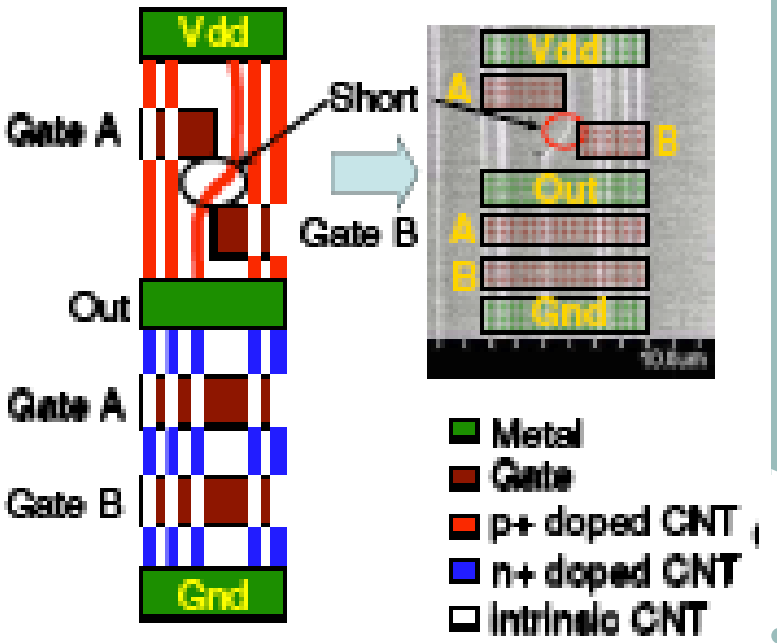
- CMOS-like process
  - CNT wires deposited on Si wafers
- CNT transistors within CMOS-style layout
  - Higher speed
  - Smaller size
- Physical design must allow for CNT misalignment

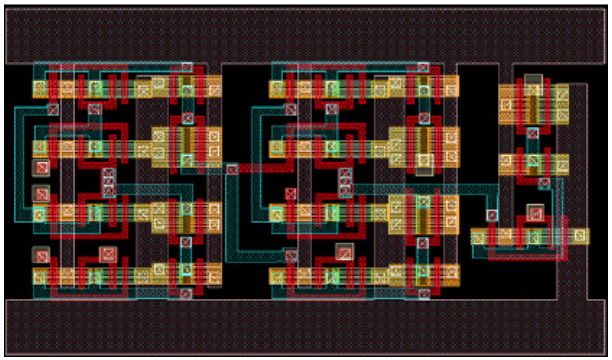


[Mitra - Stanford 07]

Design issues

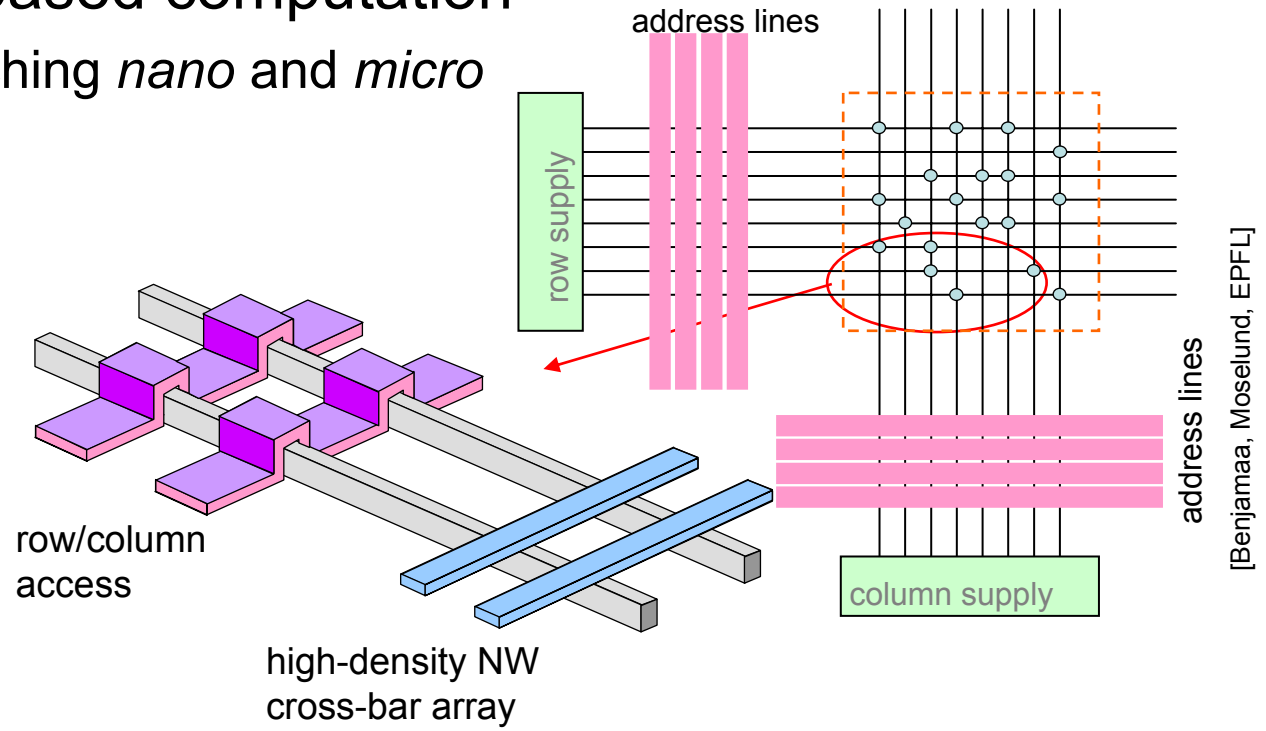
- CNT wires directions are statistically distributed
- A misaligned CNT can create a logic malfunction
- Specific design and etching steps can insure correct operation



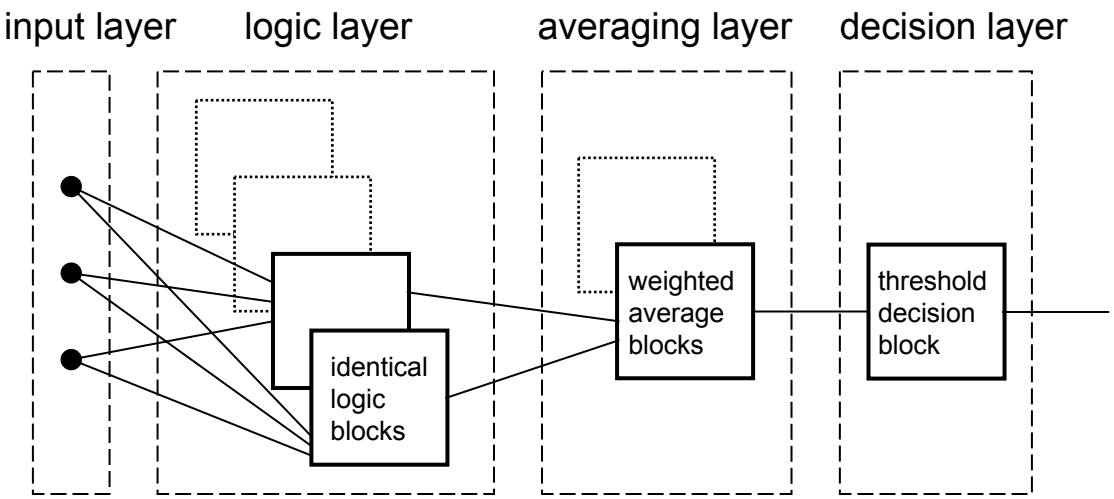


New computational structures

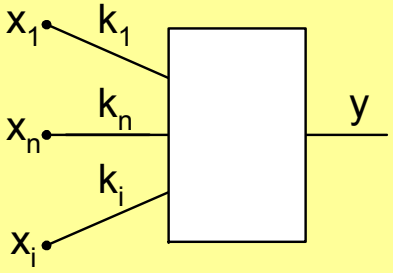
- Computation requirements
  - Predictable design
  - Fast design closure
- Array based computation
  - Matching *nano* and *micro*



Reliable nano-design
Weighted averaging



Fault tolerant architecture based on multiple layers



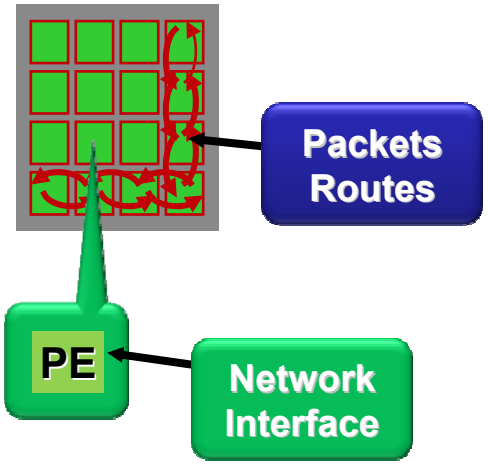
$$y = \frac{V_{fs}}{\sum_i k_i} \sum_i k_i \, x_i$$

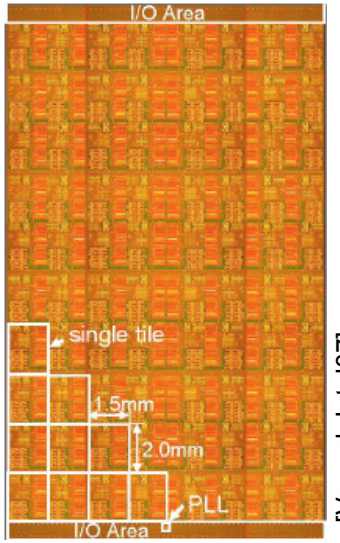
General weighted averaging and re-scaling function used in the third layer

[Source: Leblebici and Schmid]

New communication structures

- Design requirements:
  - Predictable design
  - Fast design closure
- Network on Chip communication
  - Modular and flexible interconnect
  - Reliable on-chip communication
  - Structured design with synthesis and optimization support

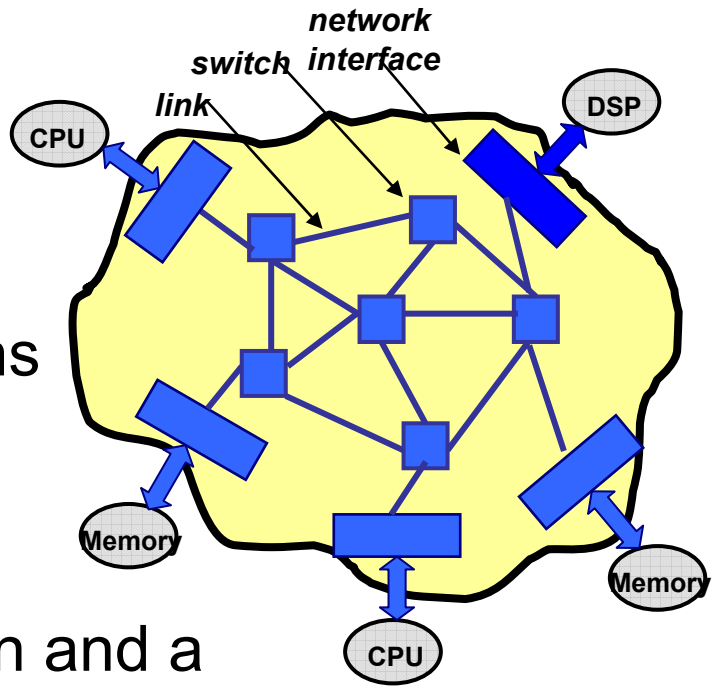




[Vangal, Intel07]

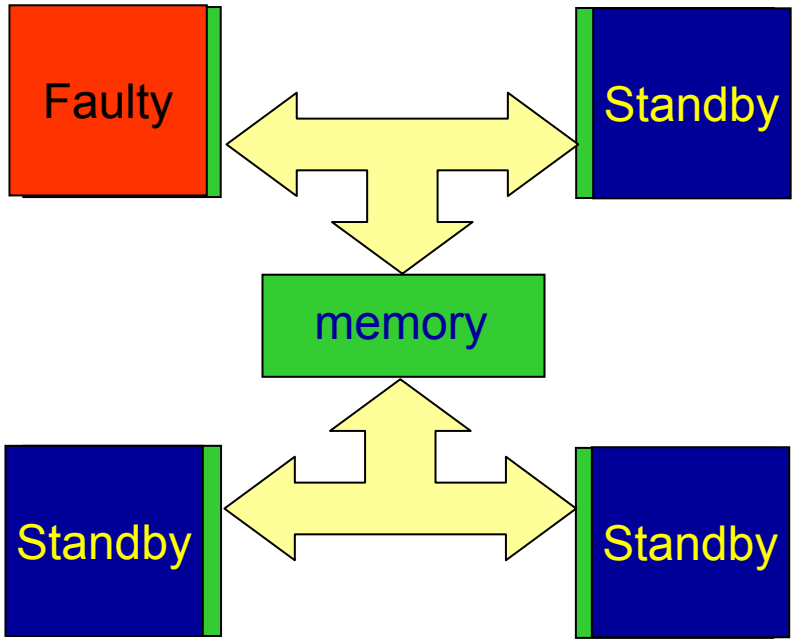
Flexibility in NoC design

- NoCs have modular structure
  - Core interfaces
  - Switches/routers
  - High-speed links
- NoCs can be tailored to applications
  - Topology selection
  - Switch/link sizing
  - Protocols
- Several parameters for optimization and a large design space
  - NoC synthesis and optimization



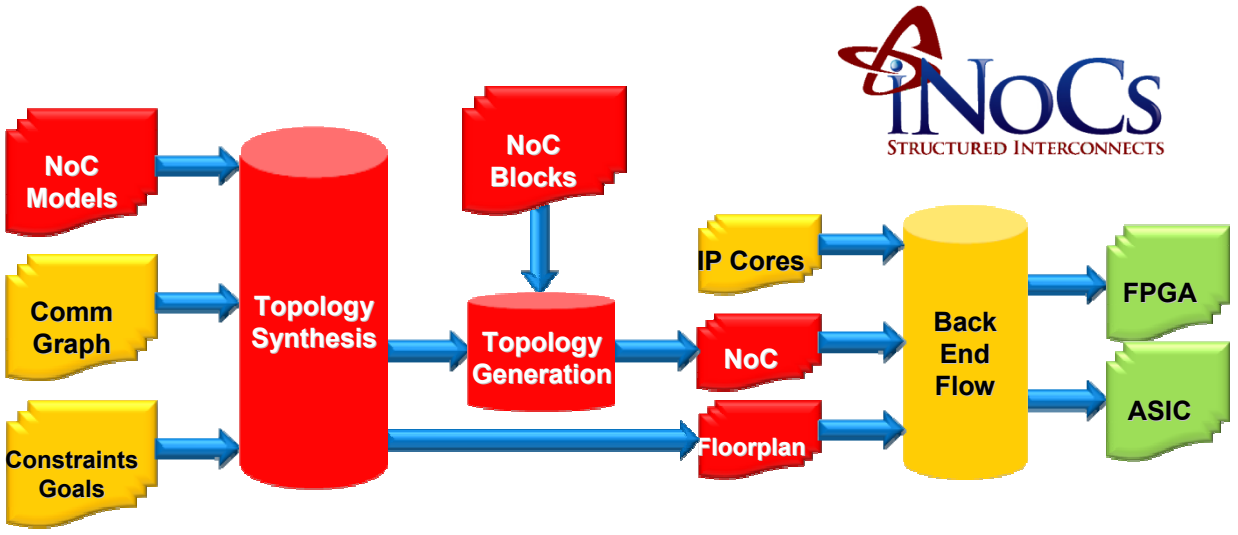
Reliability with NoC design

- Error detection/correction at various levels
  - Small electric swings allowed: electrical / physical imperfections corrected at the logic levels
  - SoCs can scale-up in size and performance
- Multi-path links provide redundancy of the interconnect structure
  - Alterative paths
  - Graceful degradation
- NoCs support seamlessly component redundancy
  - Insertion of stand-by components
  - Removal of failed components
  - Load sharing

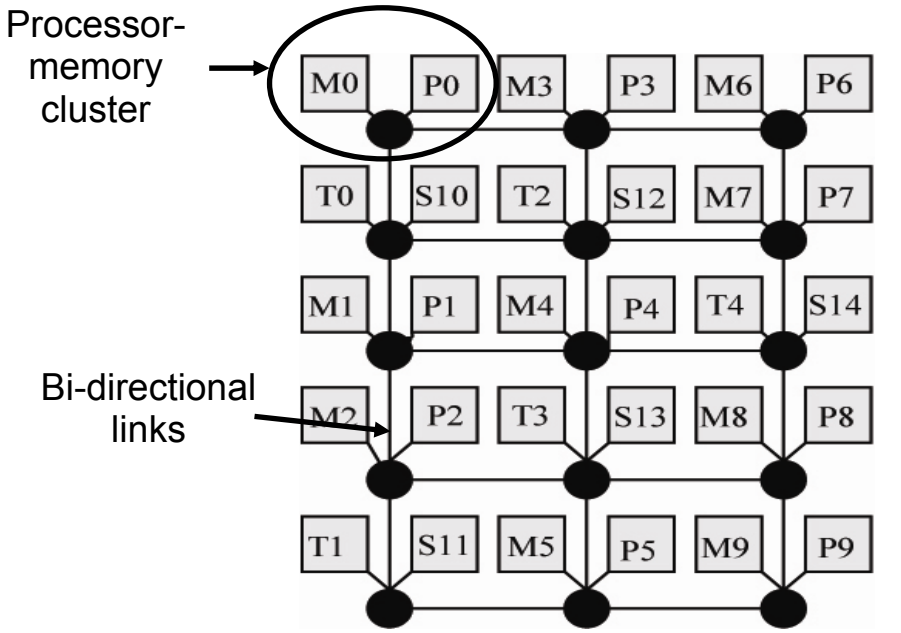


Synthesis and optimization for NoCs

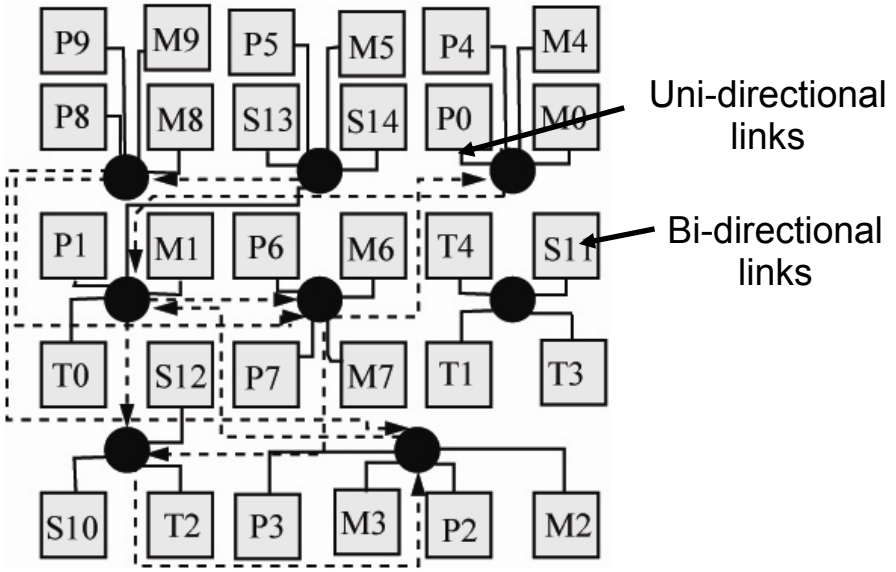
- Full tool flows for NoC Design
  - Raising the paradigm of physical design
  - From topology selection to component-level synthesis
- Synthesis and optimization at various levels



SUNFLOOR vs. manual design multimedia chip with 30 cores



Hand-mapped topology



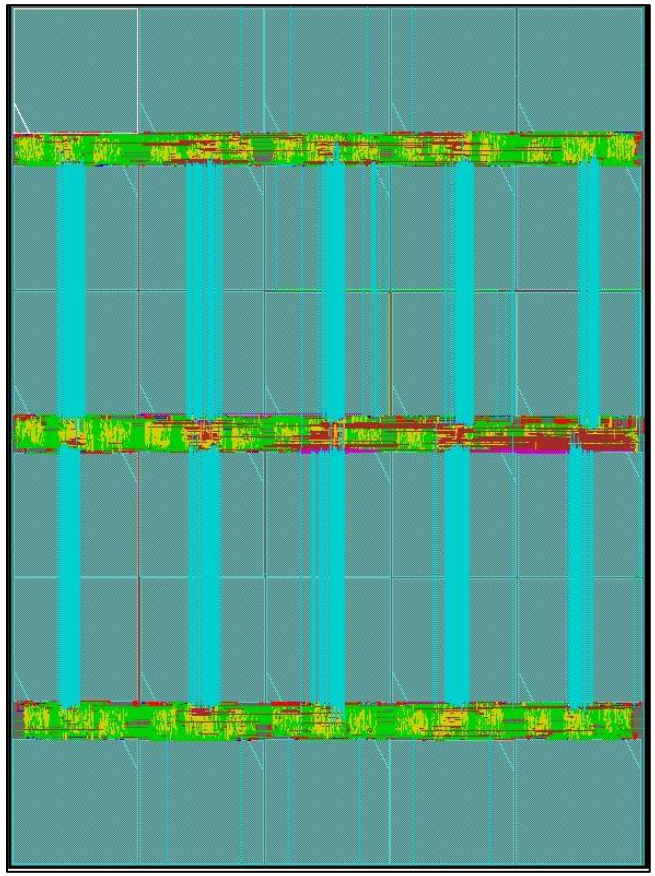
SUNFLOOR custom topology

P-processors, M-private memories,

T-traffic generators, S-shared slaves

Design layouts

From Cadence
SoC Encounter



Hand-design (custom mesh)

SUNFLOOR Design

SUNFLOOR vs manual design

Manual design:

- Topology: 5x3 mesh (15 switches)
- Operating frequency: 885 MHz (post-layout)
- Power consumption: 368 mW
- Floorplan area: 35.4 mm^2
- Design time: weeks
- 0.13 µm technology

SunFloor:

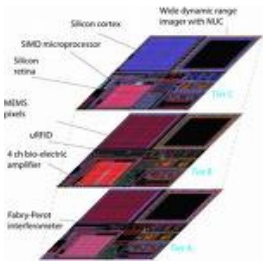
- Topology: custom (8 switches)
- Operating frequency: 885 MHz (post-layout)
- Power consumption: 277 mW **(-25%)**
- Cell area: 37 mm^2 **(+4%)**
- Design time: **4 hours design to layout**
- 0.13 µm technology

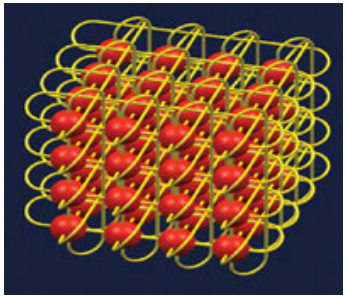
Benchmark execution time comply with application requirements and are even 10% better on SunFloor topology

New packaging technology

- From planar to 3D integration
  - Chips have limited wiring resources
  - Electrical and manufacturing constraints limit heterogeneous planar integration
- *Through silicon vias* allow designer to stack:
  - Computing arrays
  - Memory arrays
  - Analog and RF circuitry
- 3D NoCs provide effective and reconfigurable means of realizing communication

[Fraunhofer]

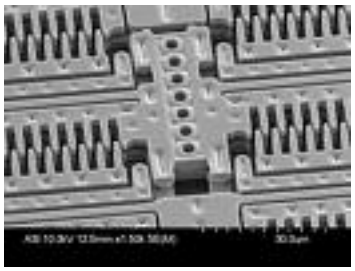


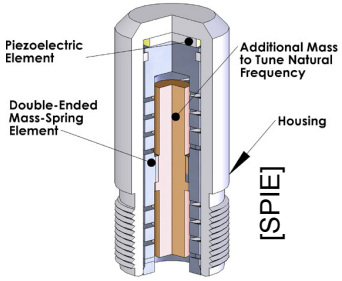


[IBM]

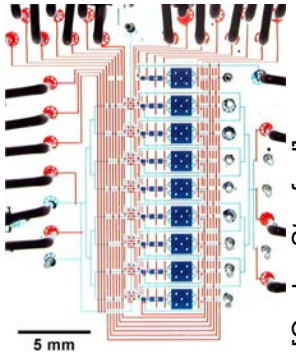
Heterogeneous integration

- Electrical and mechanical parts
  - Microactuators, scavengers, microfluidics


[Sandia]

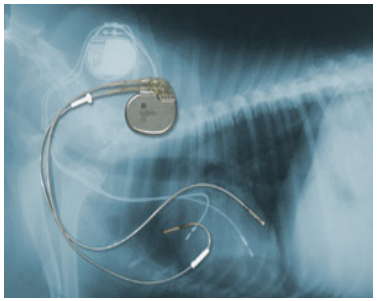


[SPIE]



[Quake, Stanford]

- Electronics meets the living world


[Un. Missouri]


[RSC]

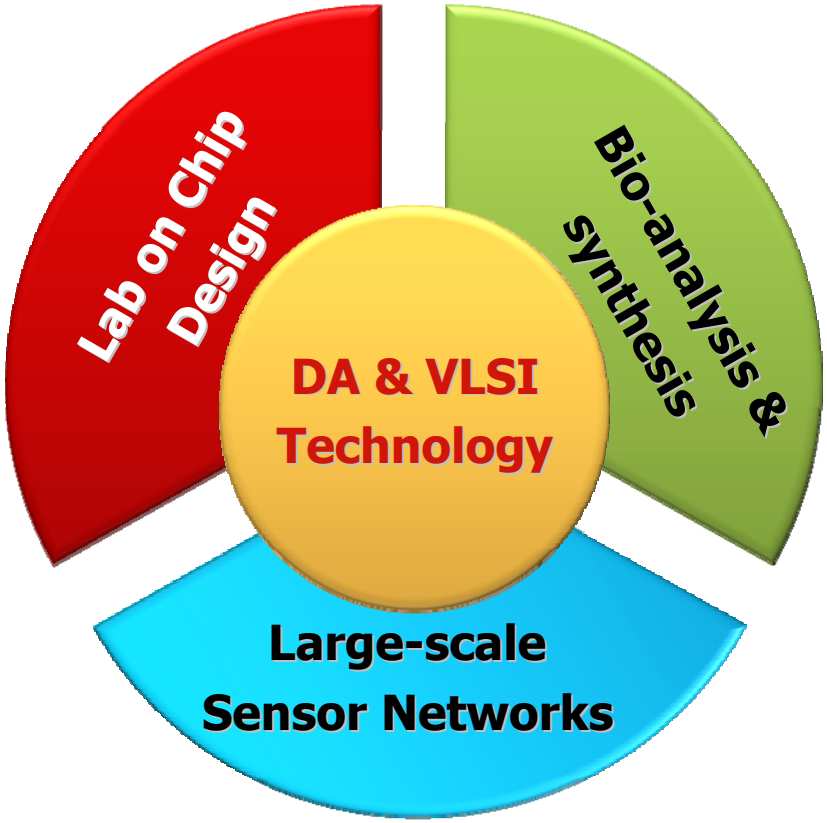
- Universal co-design


SYSTEM FAILURE

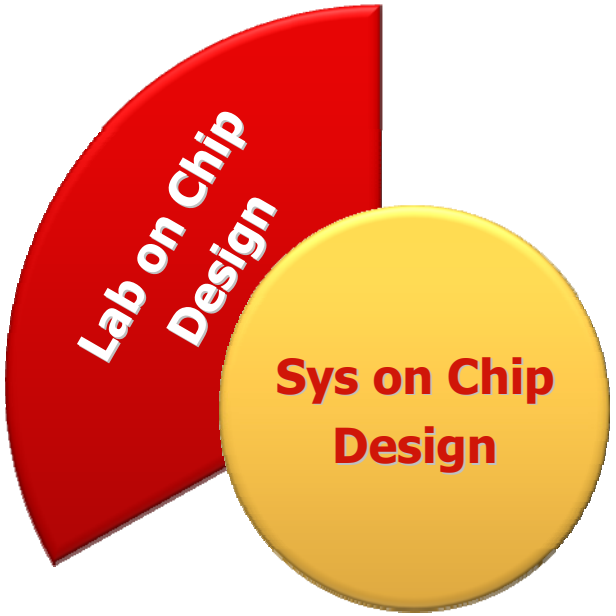
The enabling design technology

- System-level design technology
  - Evolution of EDA
- Modeling, analysis, synthesis
  - The discipline brought by EDA enabled very complex chips to be successfully designed and operated
- A bigger perspective
  - How to engineer complex multivariate systems
  - Address all aspects of embedded system design
- Scientific and commercial value stems from the systems aspect

DA evolution
through three illustrative examples



Lab on Chip design



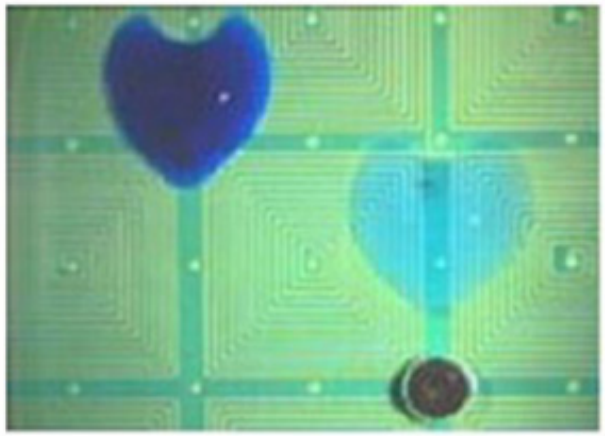
Computer-aided diagnosis (CAD?)

- *Lab on chip* at point of care
  - Perform biochemical test on the field
  - Faster, cheaper, more effective…

[STMicroelectronics]

- How
  - The ultimate hybridization of technologies:
    - Microfluidic: sample transport
    - Sensors: binding proteins, DNA to probes
    - Low-noise electronics
    - Powerful data processing algorithms and software
- A promise of lab on chip is to revolutionize medical care and offer personalized medicine

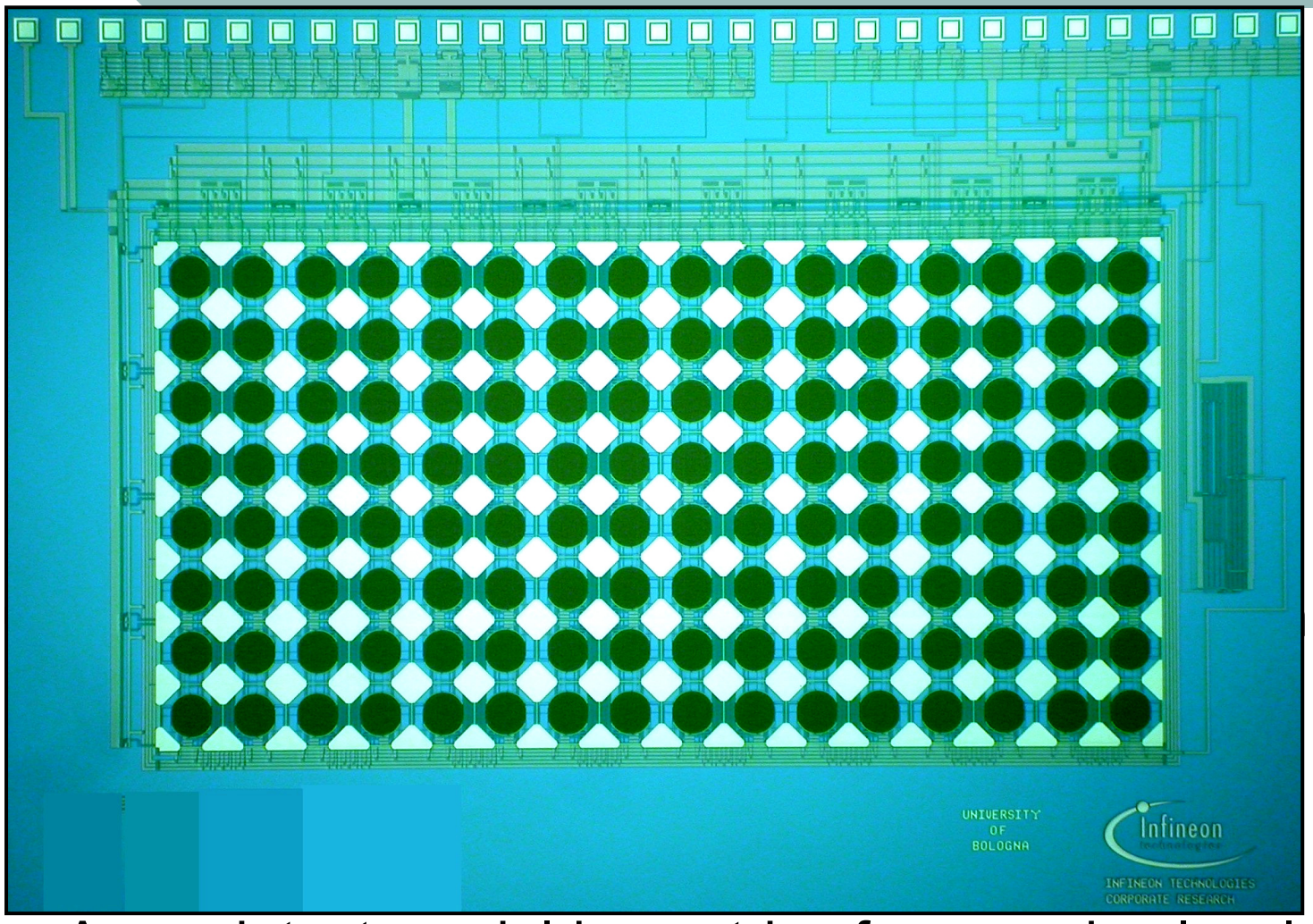
Sample transport



[Gijs, EPFL]

- Cell or sample transport, split and merge
  - On a 2-dimensional array
- Parallel scheduling and routing of multiple samples

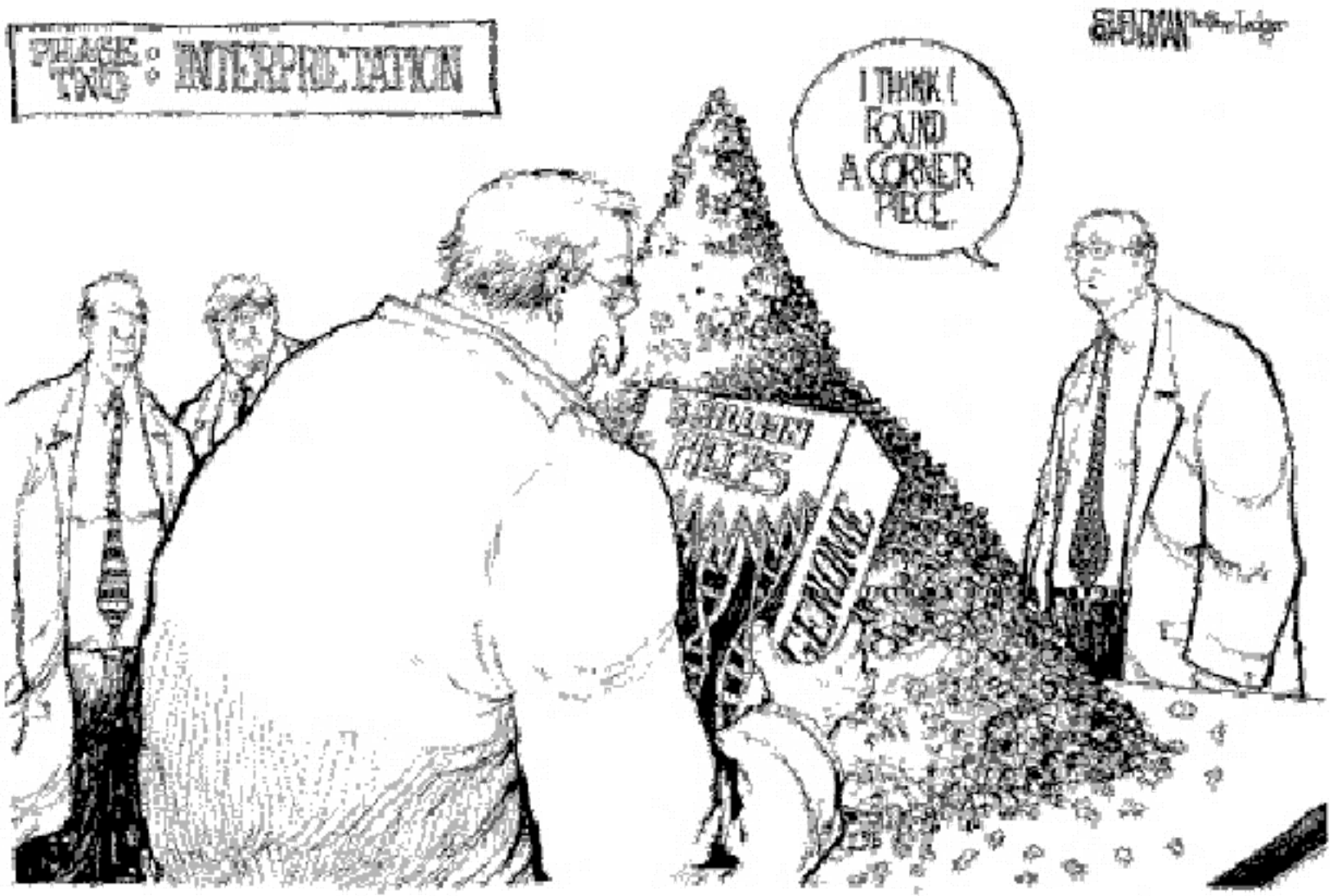
Sensing



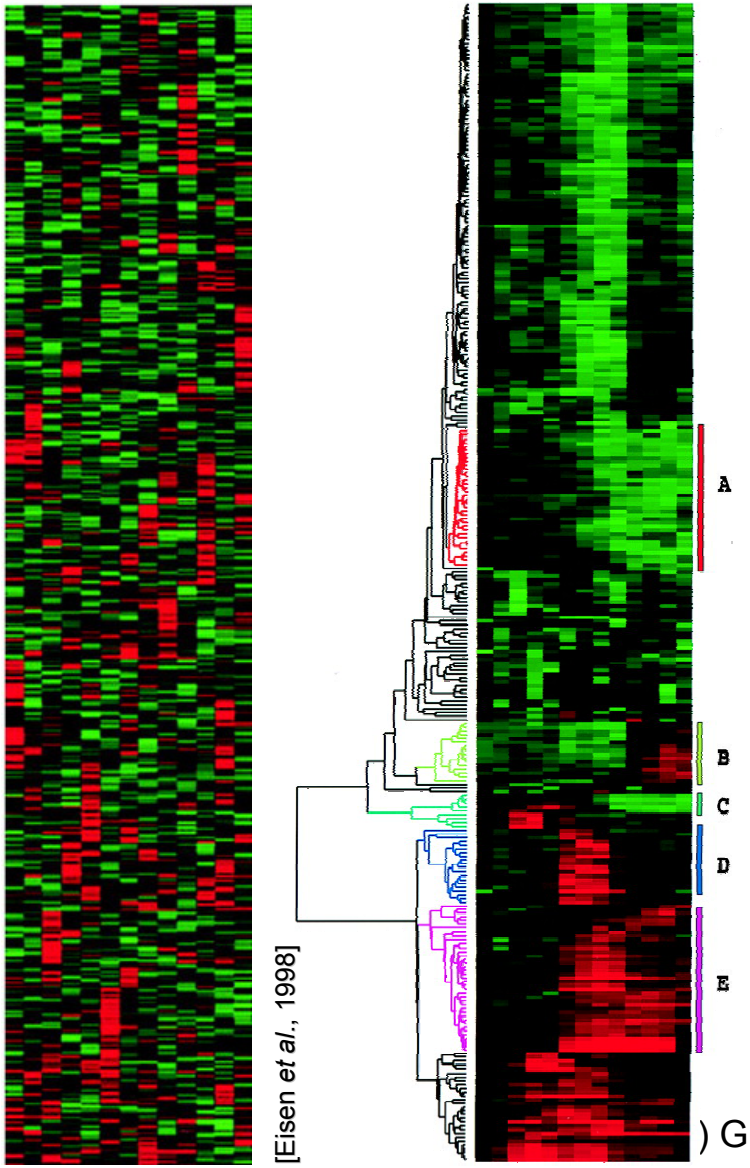
[Stagni et al., ISSCC]

- Array detectors yield a matrix of expression levels

Data mining and interpretation

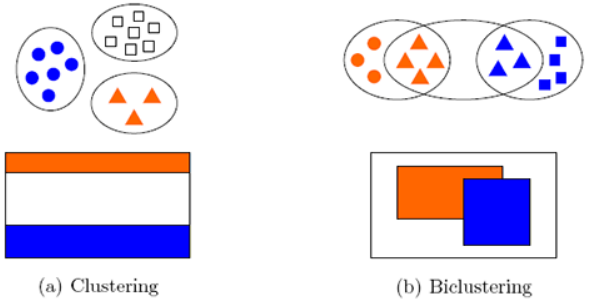


Data interpretation and clustering



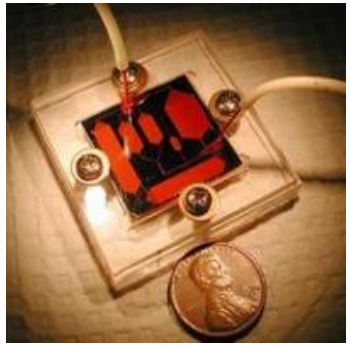
[Eisen *et al.*, 1998]

- Grouping similar objects together
  - Detecting gene variations consistent with the sample choice
  - Inference of specific conditions
- Bi-clustering on large data sets
  - Simultaneous cluster of subsets of rows and columns
    - Gene and samples



- Problem solved with ZDD technology
  - Fast and complete data interpretation

Global *Lab on Chip* objectives



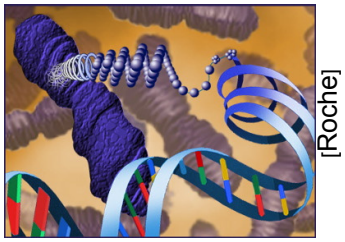
[Schuler,Comell]

- Bio-discovery
  - New biological mechanisms
- Medical practice
  - Better diagnosis via genetic information
  - Linking genetic data to clinical traits and databases
- Micro-chemistry
  - Creating organic compounds by micro-reactions
- Support for experiments/tests on the field
  - Generic versus application-specific *lab on chips*
  - Programmable, field-programmable?

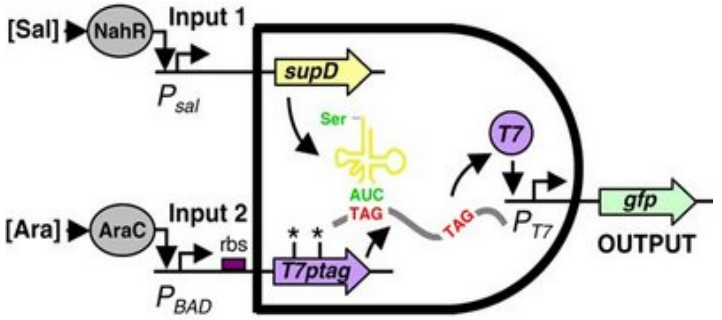
Bio analysis and synthesis

Analysis and synthesis

- Analysis - understand biological mechanisms
  - Comprehend in full the value of the *omics*
    - Genomics, proteinomics, trascriptomics
- Synthesis - modify/create new realities
  - Synthesize drugs that alter genetic/metabolic pathways
    - Pharmacogenomics
  - Synthesize biological compounds that support computation
    - Synthetic biology



[Roche]

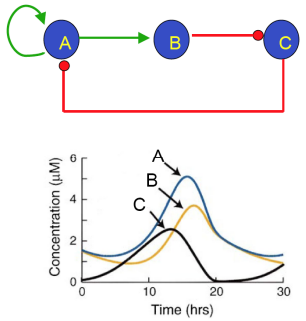


[UCSF, UCB]

- Multiple abstractions are needed for analysis and synthesis

Abstractions

- Bio-chemical abstraction
  - Event timing
  - Differential equation models

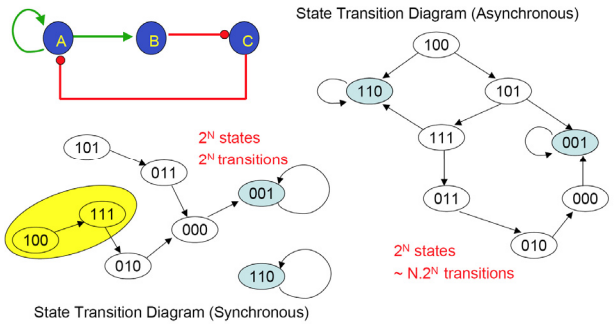


$$\frac{dx_a}{dt} = r_{aa}x_a + r_{ac}x_c - \gamma_a x_a$$

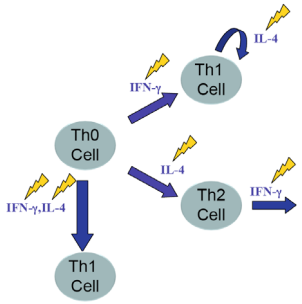
$$\frac{dx_b}{dt} = r_{ba}x_a - \gamma_b x_b$$

$$\frac{dx_c}{dt} = r_{cb}x_b - \gamma_c x_c$$

- Logic level abstraction
  - Zero-delay model
  - Finite-state system
    - Synchronous, asynchronous

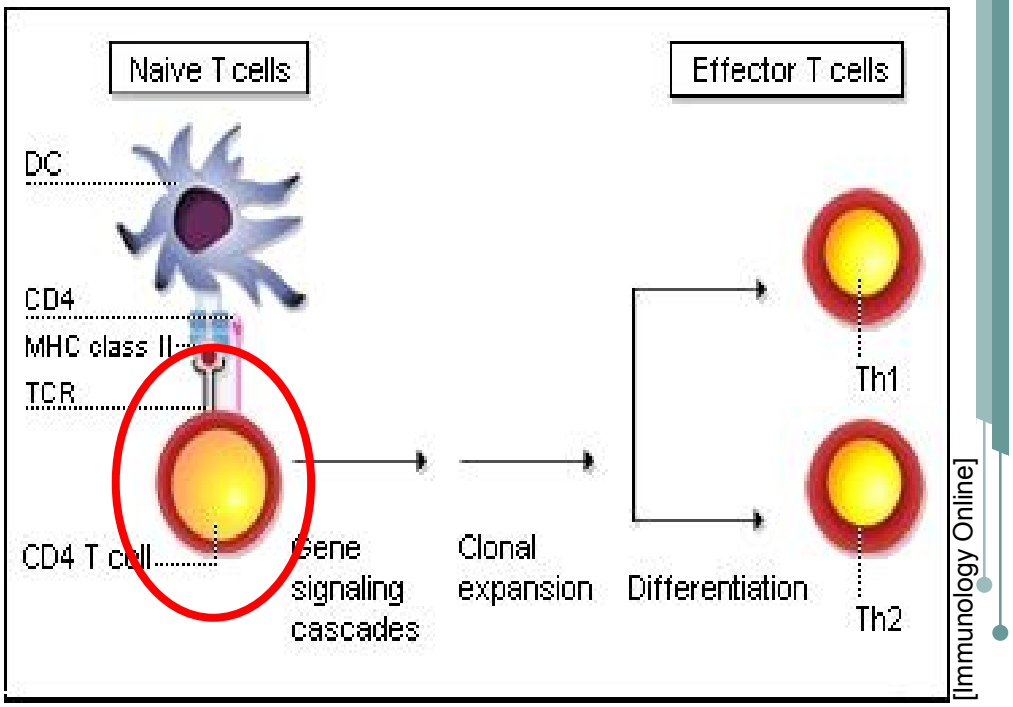


- Functional abstraction
  - Biological function
  - Input-output analysis

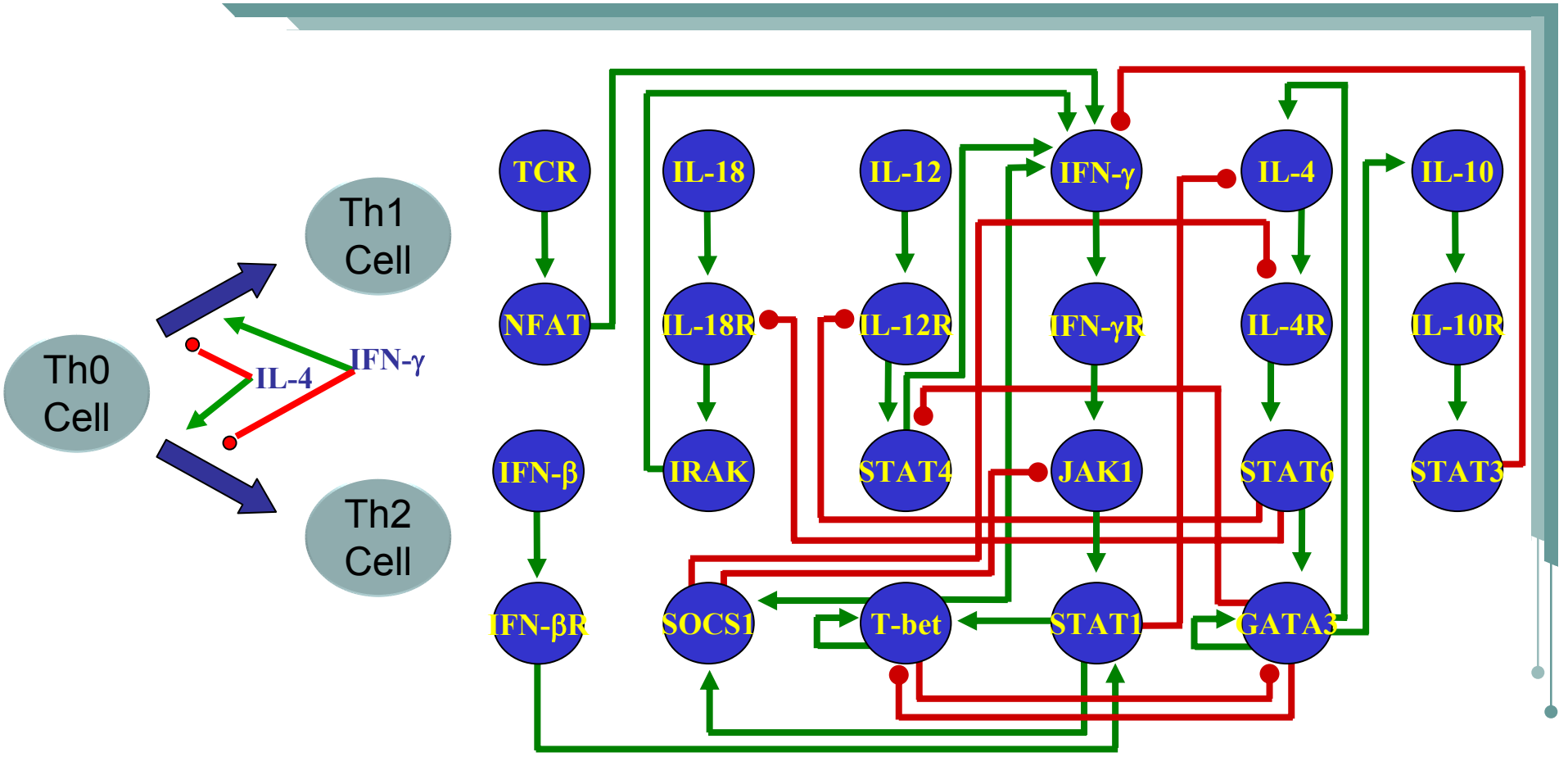


T-helper cells

- Observed behavior:
  - Precursor Th0 cells yield:
    - Effector Th1 cells
    - Effector Th2 cells
- Evolutions depends on specific gene expressions
- Evolution can be captured by a *gene regulatory network*



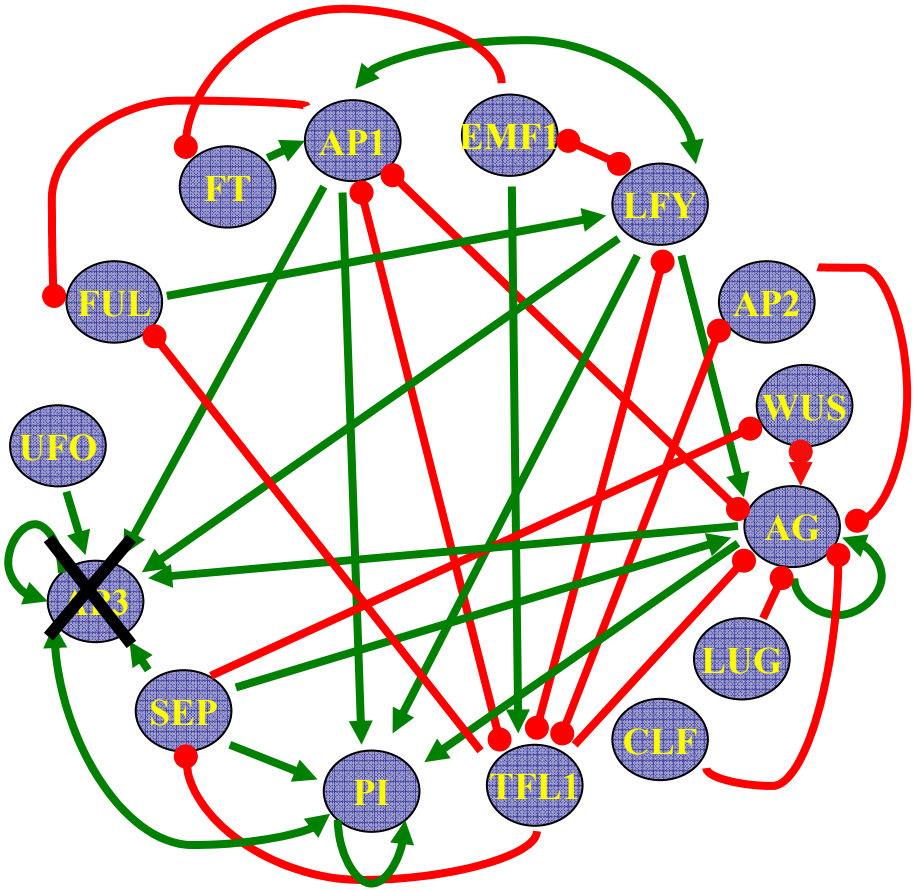
Functional and logic-level model of T-helper cell



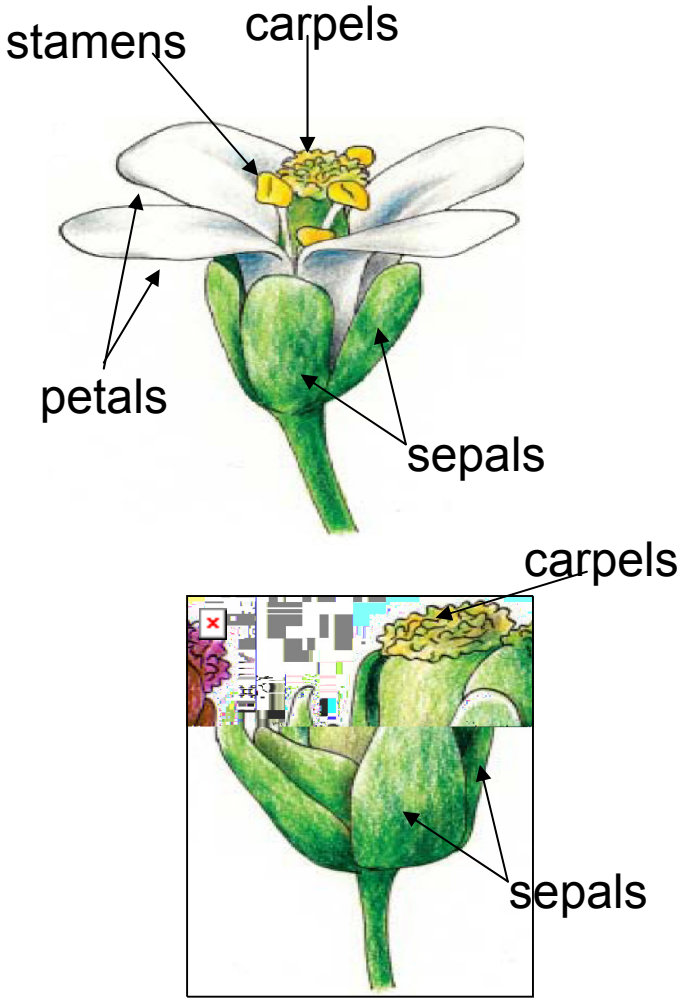
Issues

- Orthogonalization of concerns
  - Focus on terminal behavior independent from timing
- Simulation versus traversal
  - Steady state is often the objective
  - Implicit methods can handle large amount of data
- Modify system by perturbation
  - Knock-out experiment *in silico*
    - Silence a gene
  - Stuck-at 0 (déjà vu?)

Knock-out example: *Arabidopsis Thaliana*



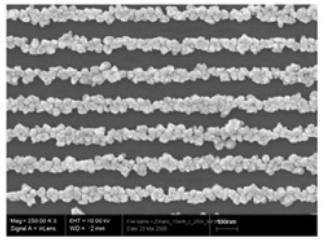
[Soto et.al. *Plant Cell*, (16):2004]

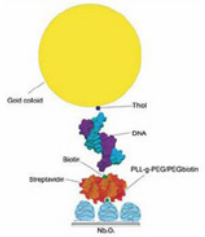


AP3 knockout

Bio analysis and synthesis objectives

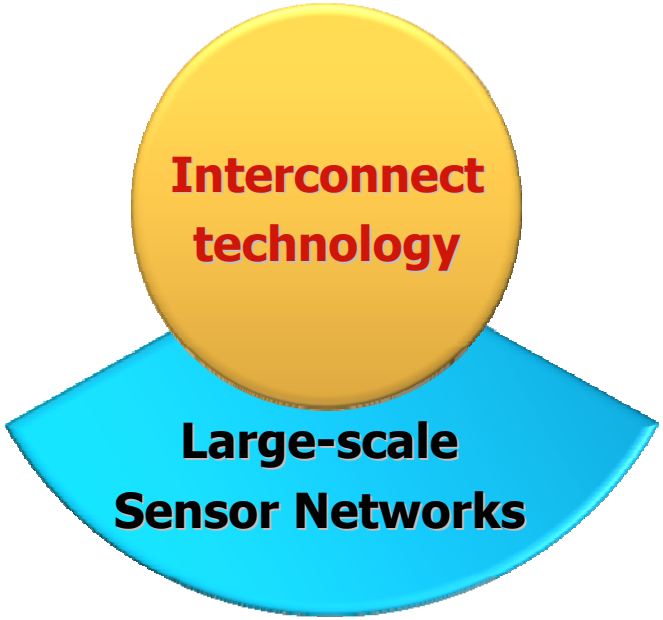
- Pharmacogenomics
  - Develop drug therapy, cognizant of patient genotype
  - Study effects of altering genetic/metabolic pathways
- Synthetic biology
  - Engineer systems based on biological components
  - Abstraction: libraries, synthesis process
- Biology-driven computation
  - Devise computational processes performed by DNA
- Biologic scaffolding
  - Construct nano structures/circuits using DNA composition





[Vörös, ETHZ]

Environmental monitoring and control



The environment

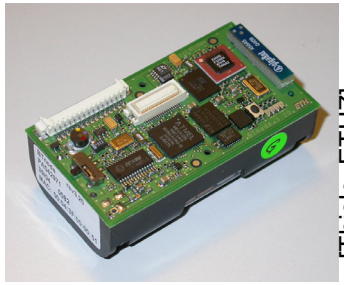
- We are embedded in the environment
  - Many inconvenient truths




- What are the challenges of wireless sensor networks to monitor/control the environment ?
  - Massive amount of data to process
  - Distributing and powering the nodes
  - Providing redundancy to tolerate local failures

Engineering environmental systems

- Integrated sensing, computation, communication and embedded software
  - Local vs. global data processing and communication
- The power of data abstraction
  - Data reduction and integration
- The distributed intelligence approach
  - Reason and act locally with (some) global information
  - New computational paradigms, as compared to classical supercomputer approaches



[Thiele, ETHZ]

The quest for energy efficiency

- Distributed wireless systems must (eventually) be autonomous
  - Energy harvesting from the environment
    - Mobile and fixed applications
  - Convert unused (degraded) energy into information


[Perpentum]

- Energy distribution systems must be efficient
  - Use information on the system to optimize energy distribution
    - Smart home, building, factory, …
    - Electric grid management
  - Convert information into energy savings


[Sandia]

- Mutual interaction: energy ↔ information
  - Policies for run-time energy/information management will play a key role in system design

How do we interact with the environment?

[Summer School 2058@ 172.165….]

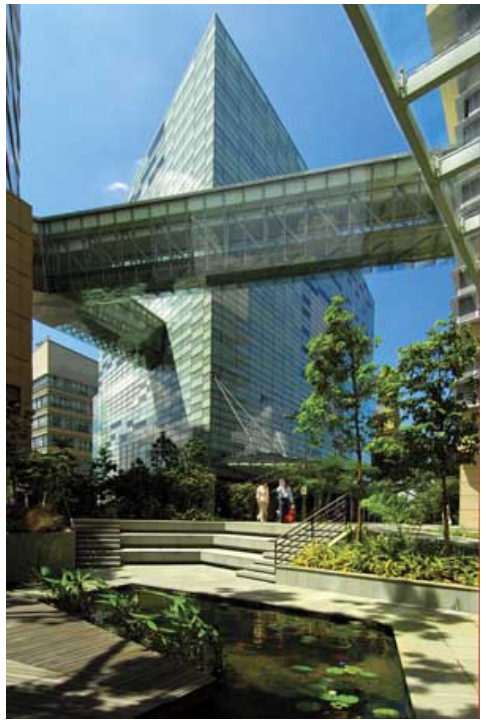
[Masternewmedia]

- How to design evolvable embedded environments with user interaction and immersion?

Cooperative engineering

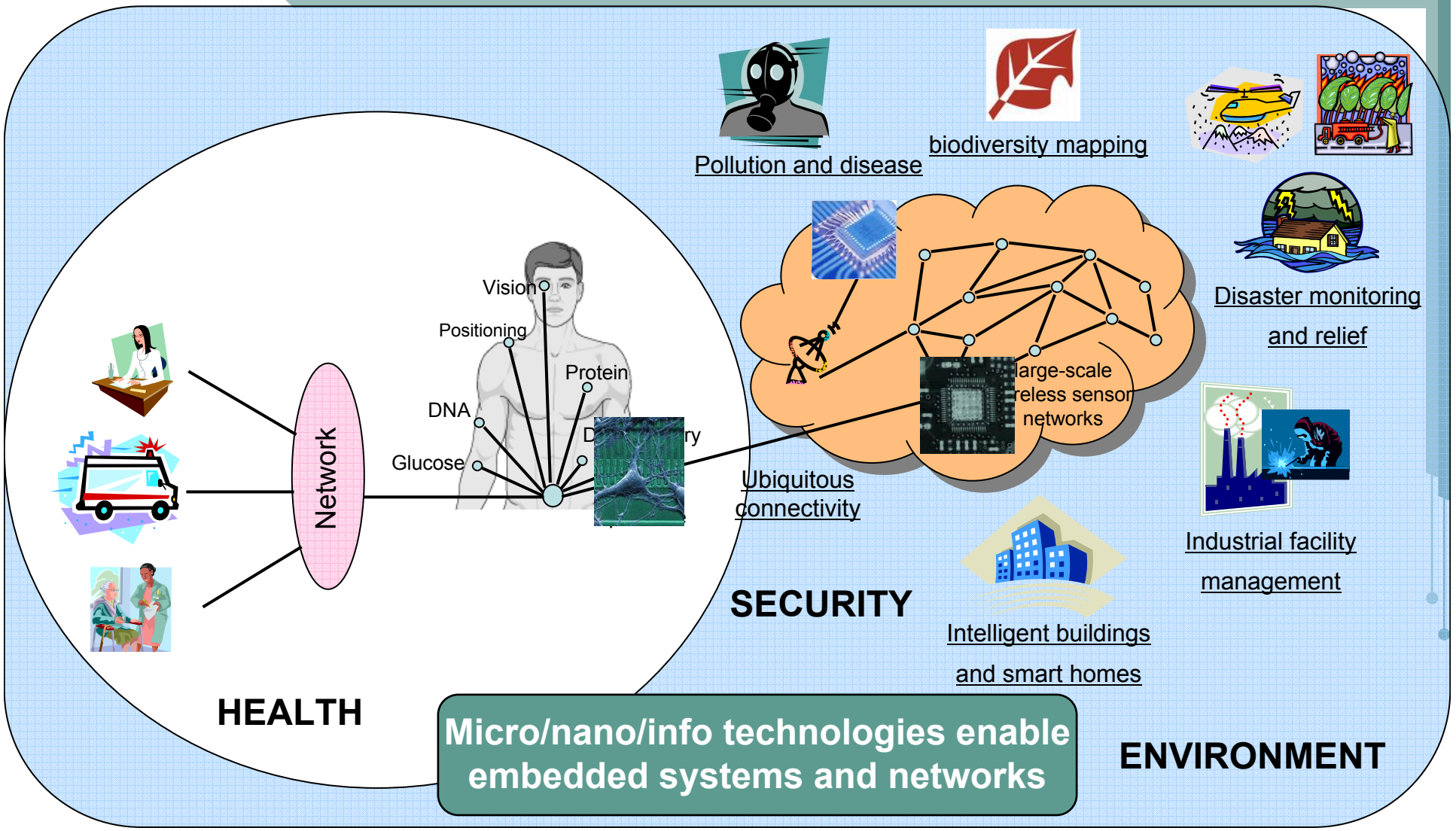
- Bringing together engineer/scientists/doctors with different skills
  - Communication and vocabulary
  - Abstraction and modularity
- Collaborative workspaces

[Stanford Clark Center]

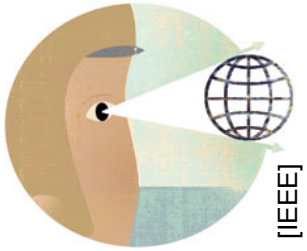


[Singapore Biopolis]

The nano-tera.ch program



The humanitarian technology challenge



- A new partnership between the IEEE and the UN
- Identify technologies in the health/environment domain that can benefit developing countries
  - Food, water, health monitoring
- Using cellular technology to link data
  - Ubiquitous connectivity and local data processing
  - Autonomous or very low-power consumption because of limited availability of energy
- An ethical objective that can raise enthusiasm among engineers

Summary

- The road ahead has challenges and rewards:
  - Expanding our horizon is key to scientific viability and commercial profitability
- We need heterogeneous hardware design and the corresponding software infrastructure
  - Product/system design is an extremely complex task, because of the variety of facets and technologies involved
- System-level design technologies are crucial for system conception, design and management
  - Progress leads us beyond advanced silicon chip design
  - Scientific and financial benefits will stem from the system/service perspective

Thank you