Mapping Flow for Car-Entertainment Applications on Embedded Multiprocessor Systems

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- Name? and address?

Outline

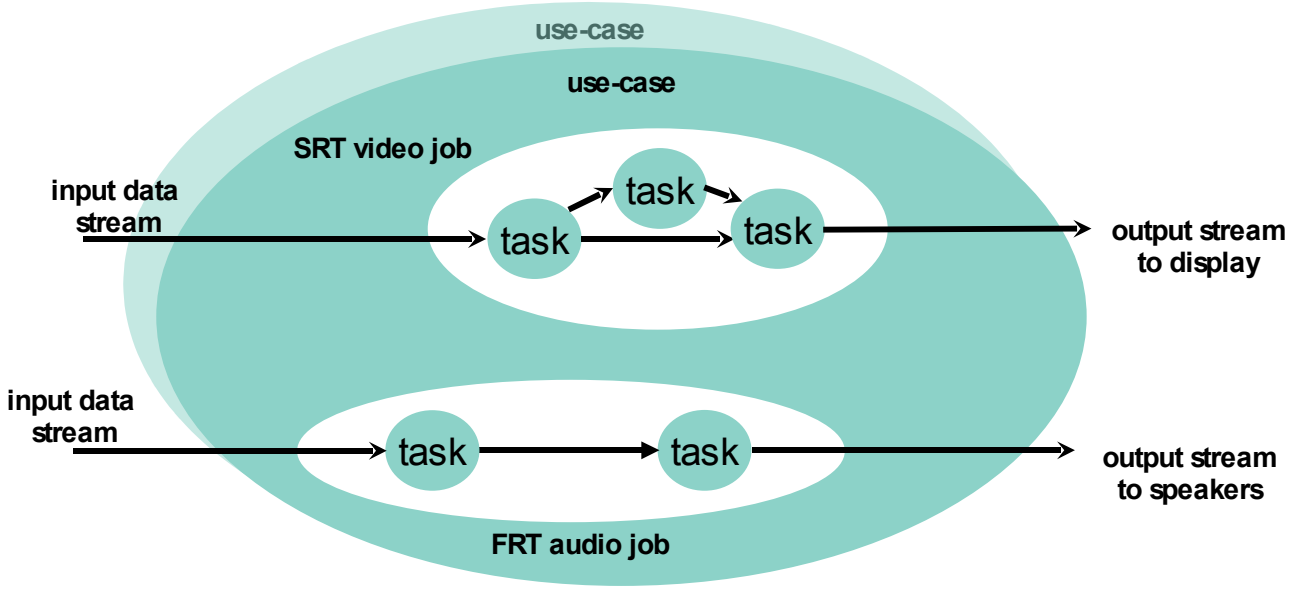
- Multi-stream car-entertainment system
- Objectives & Approach
- Bounding interference with budget schedulers
  - Unsafe worst-case execution time estimates of tasks
- Expressivity analysis model
  - Data dependent execution rates of tasks
- Mapping flow
  - Limitations
- FPGA demonstrator
- Summary

Car entertainment application domain

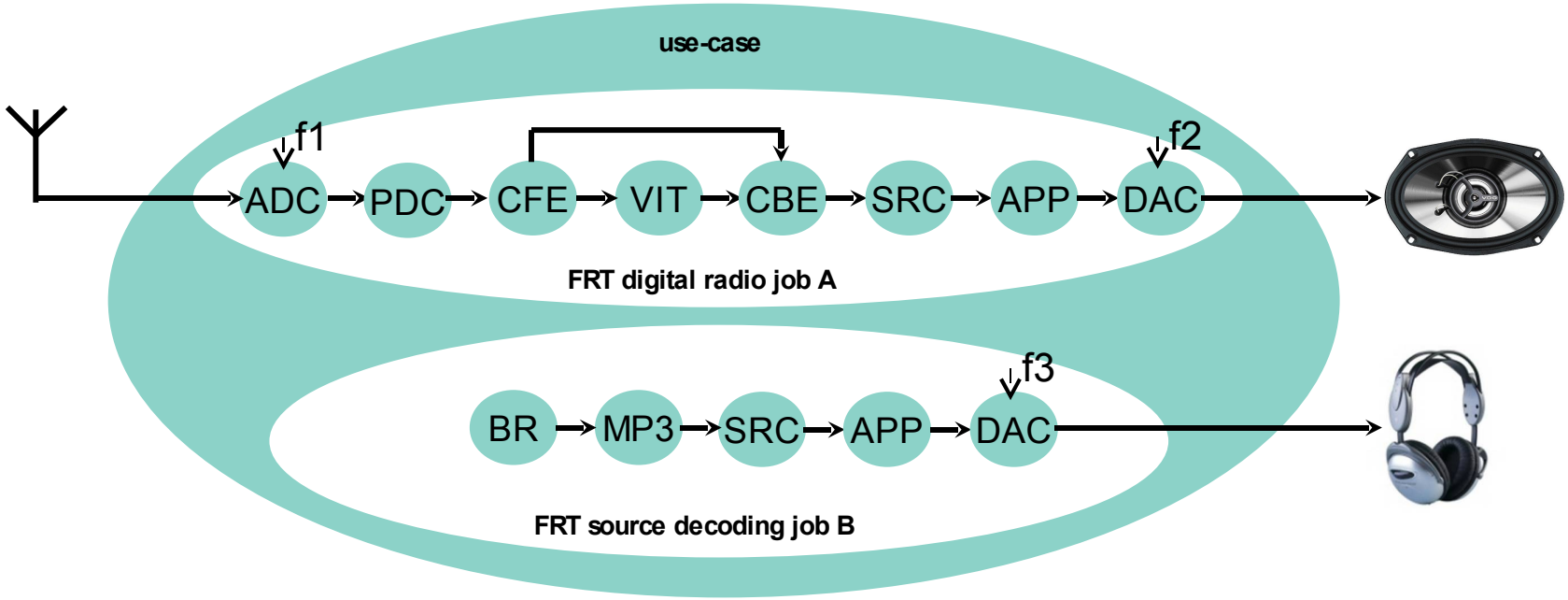
Multi-stream car-entertainment system

Application model

- Jobs are *composed of tasks*
- Simultaneously running jobs *together form use-cases*
- Jobs often have *real-time requirements*
  - Firm (FRT) if deadline misses are *highly undesirable (steep quality degradation)*
  - Soft (SRT) if occasional *deadline misses are tolerable*



Car entertainment use-case

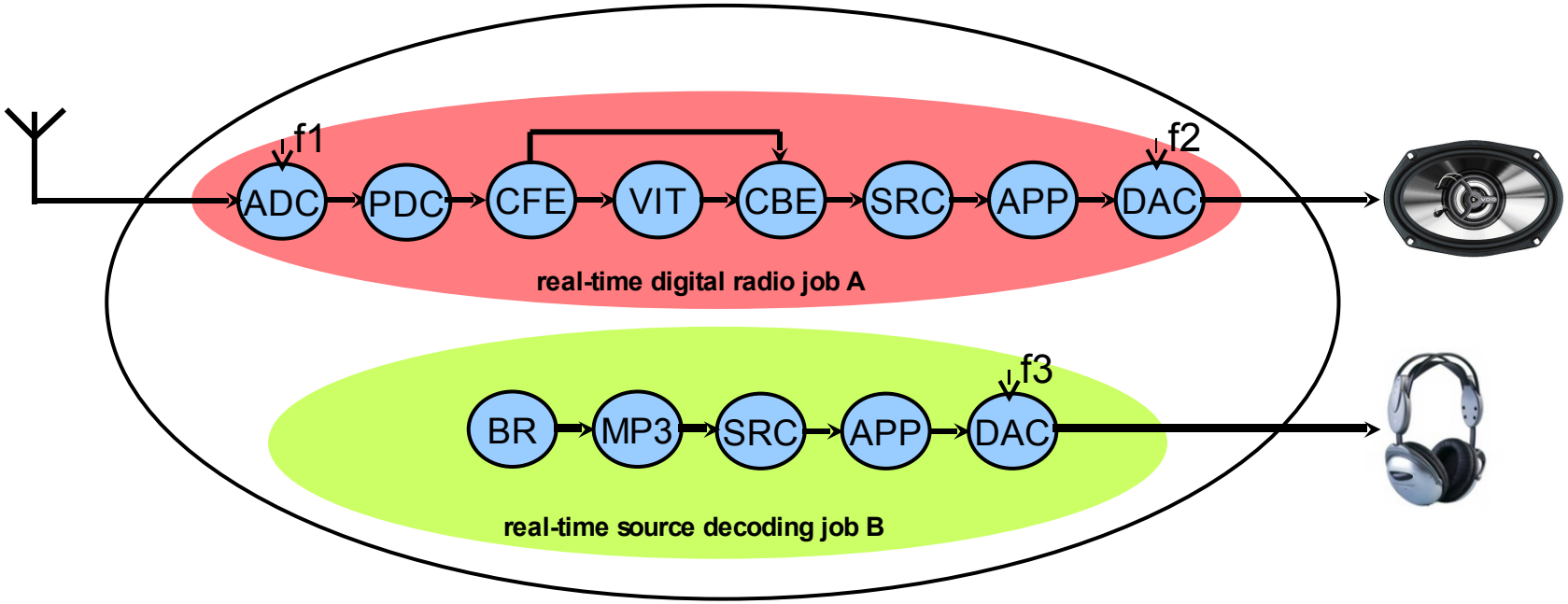


- Observations:
  - Reactive system because stream from transmitter cannot be slowed down
  - Firm real-time jobs because deadline misses are highly undesirable but not catastrophic
  - Both streams are equally important

Our objectives:

- Enable independent development of jobs
- Maintain robustness despite increased resource sharing
- Reduce design and verification effort

Strategy: Divide and conquer

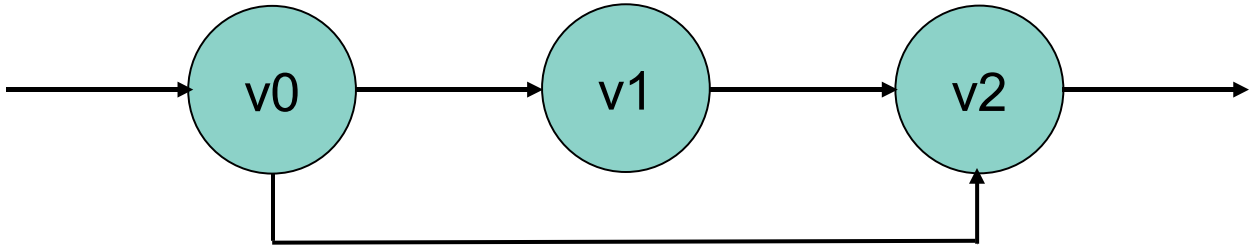


- Bound interference other jobs (guaranteed by measures in hardware)
  - Each job can be designed and characterized independently of other jobs
  - Erroneous behavior of a job has bounded effect on behavior other jobs

Objective 1&2

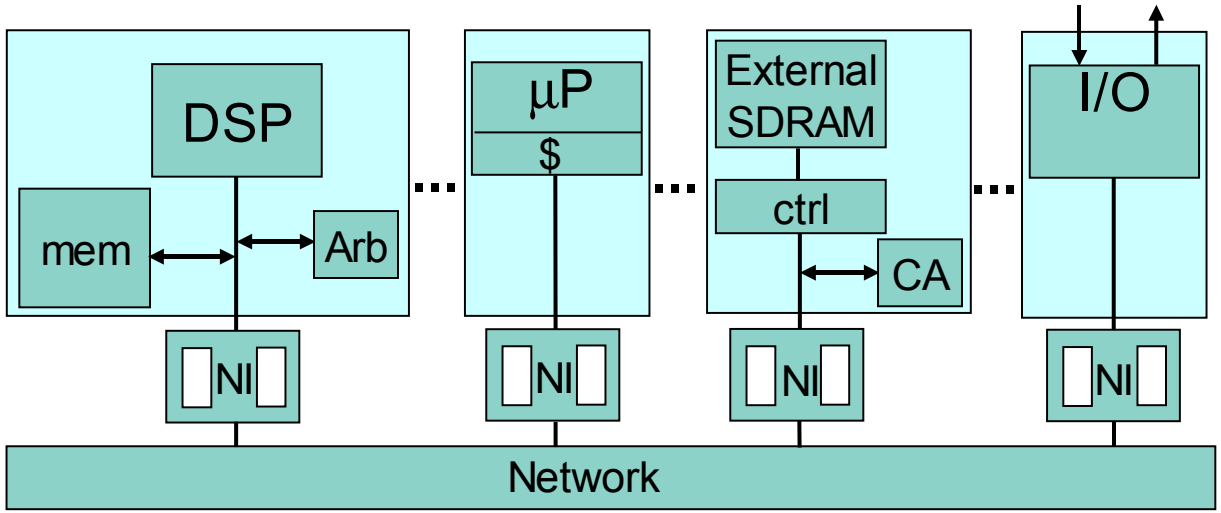
Strategy: Abstraction with guarantees (conservative arrival time data)

Fast (>100Mcc/s) simulation of communicating processes with time (CP-T)



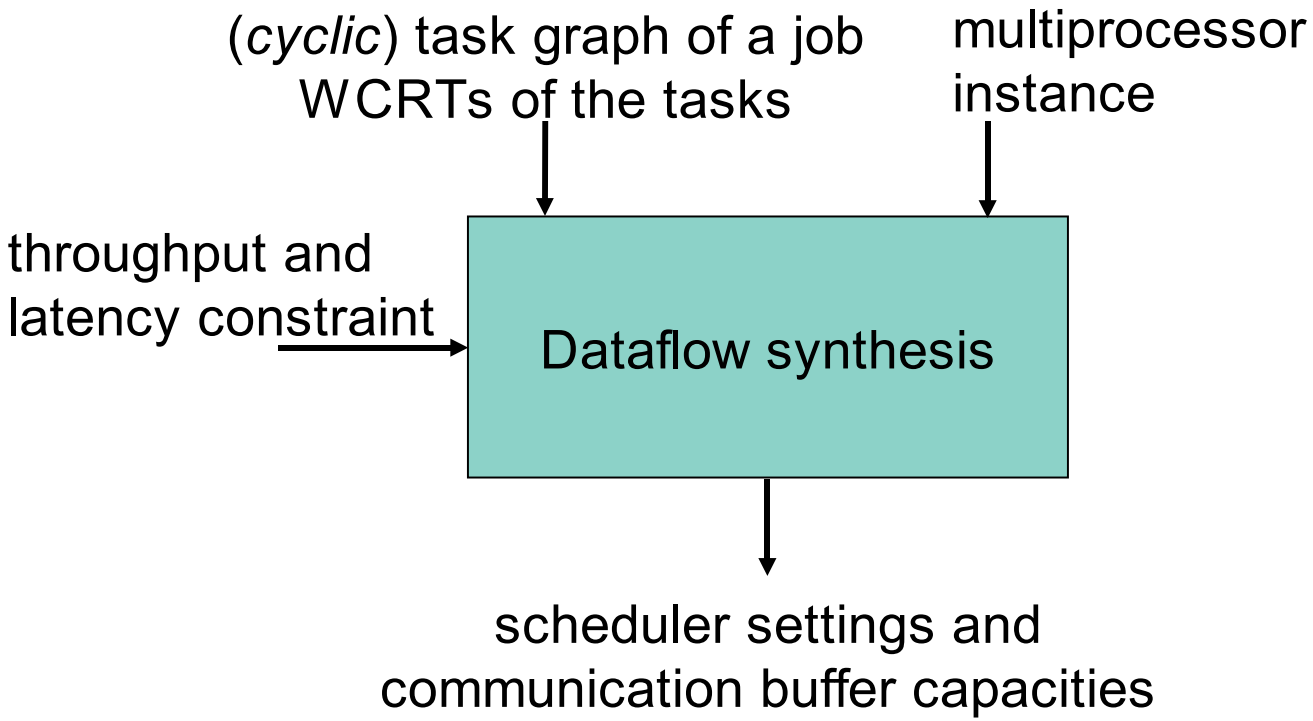
Instead of:

Low-level simulation (e.g. PV-T)

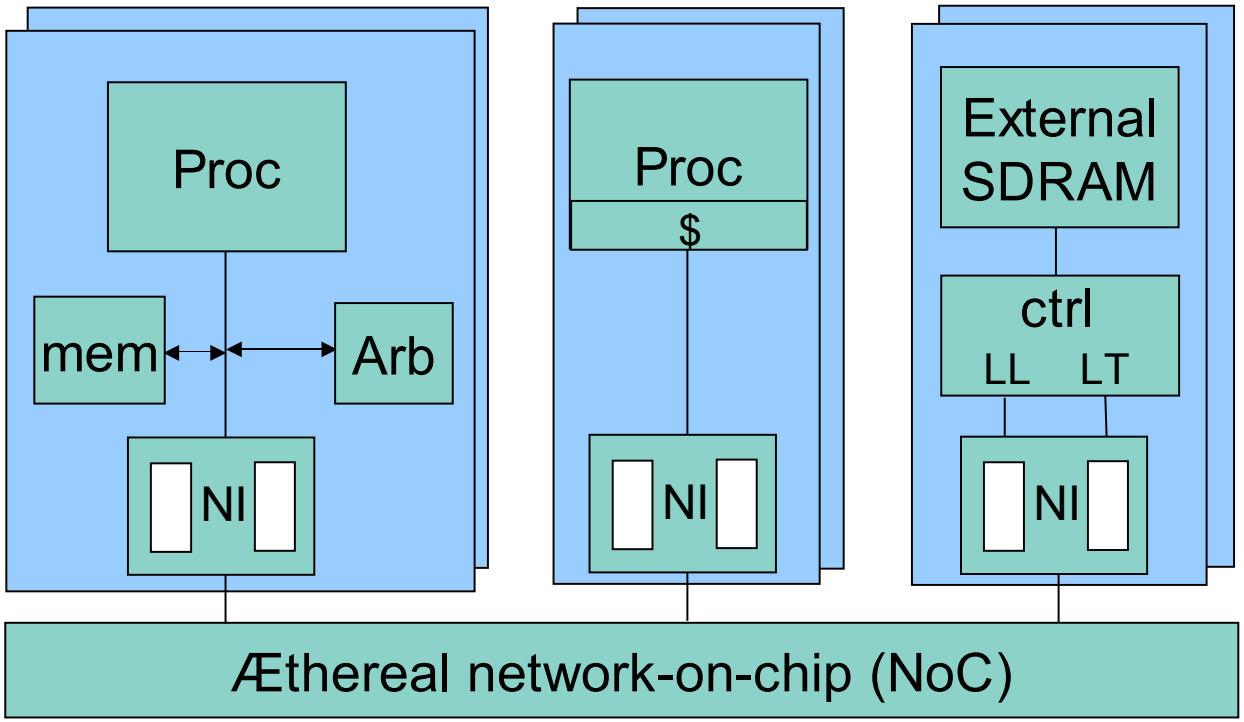


Objective 3

Strategy: Synthesize settings (prevent iterative design space exploration)



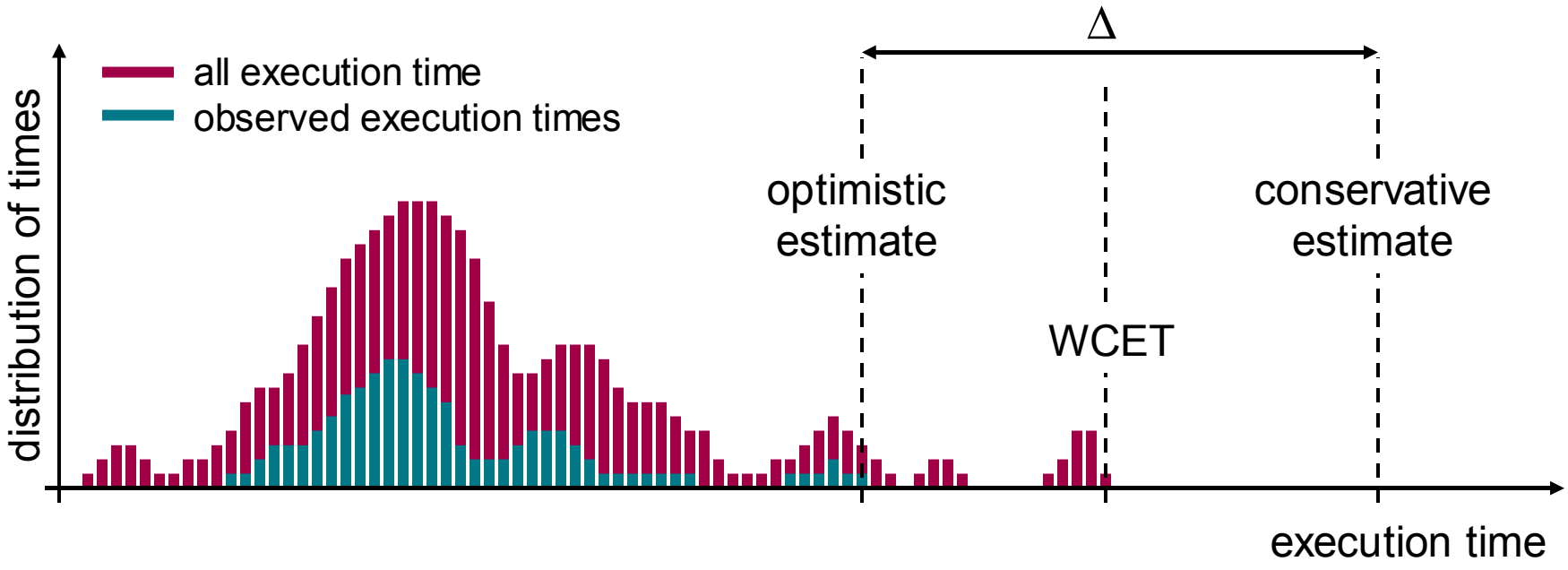
Multiprocessor system under development



- Instructions and data can be stored in external SDRAM
  - lower cost per bit than on-chip SRAM (Digital Radio Mondial channel decoder requires 940 kByte storage)
- Caches hide SDRAM memory access latency
  - large difference between WCET and average execution time

[M. Bekooij et. al.: Bits & Chips 2007]

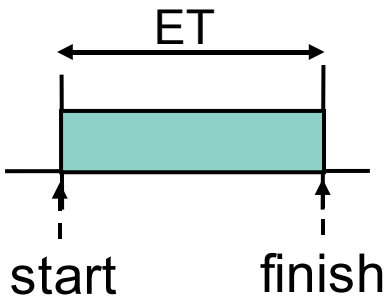
Execution times of tasks



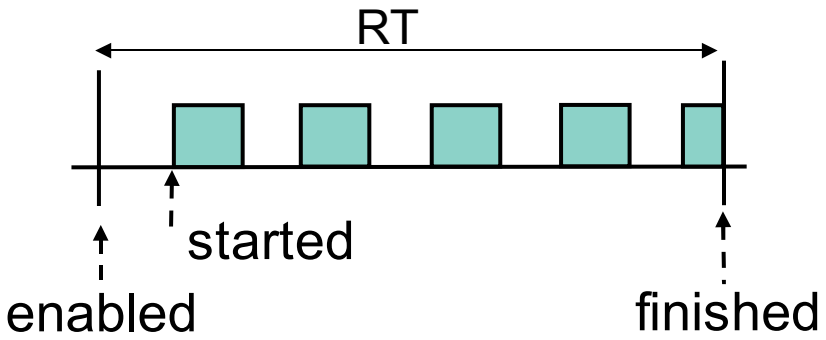
- Why use optimistic-estimated WCETs
  - Distance Δ can be large due to caches and external SDRAM
  - Tight conservative-estimated WCET requires knowledge input data
- Our approach
  - Guarantee no deadline misses for set of input stimuli
  - Fall-back mechanism to cope with deadline misses
  - Worst-case temporal behavior of other jobs should not be affected

Response time

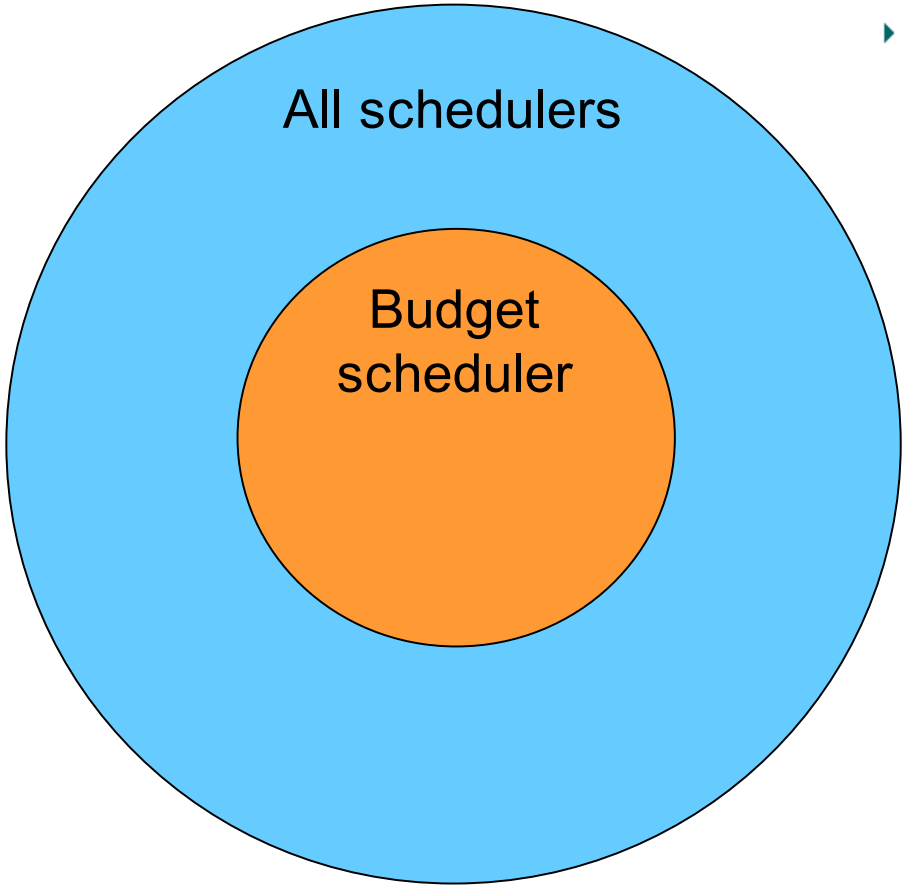
Execution Time (ET)



Response Time (RT)

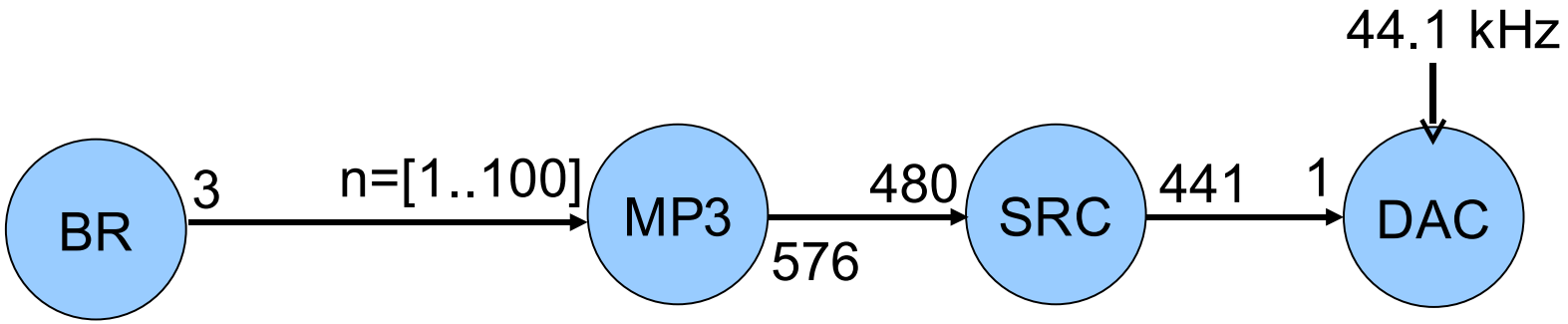


Scheduler/Arbiter characteristics
e.g. memory port arbiter, task scheduler



- **Budget Scheduler (e.g. TDM)**
  - **WCRT independent of**
    - **WCET of tasks other jobs (unsafe WCET!)**
    - **Data arrival/traffic characterization**

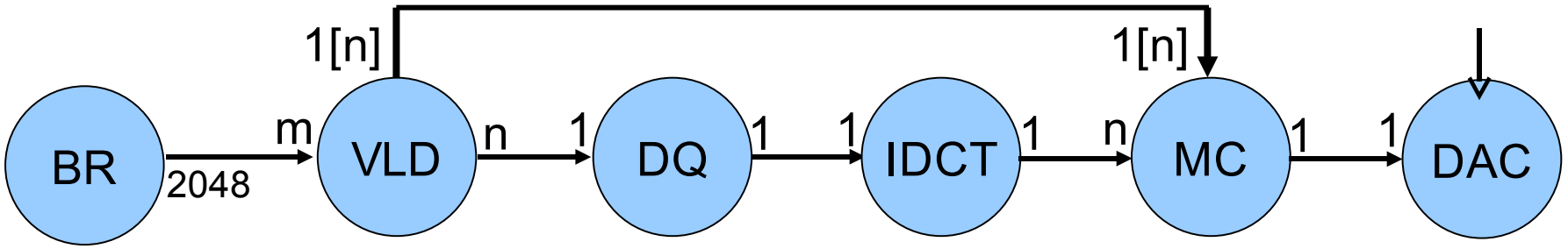
Variable consumption rate



- Digital to analog converter (DAC) determines throughput constraint
- MP3 decoder task consumes variable amount of data
- Block-reader (BR) task must “know” consumption speed MP3 task
  - Implies cyclic dependency that affects the temporal behavior!
  - Block reader task does not execute periodically

[M. Wiggers et.al.,DATE 2008]

Data dependent execution rate

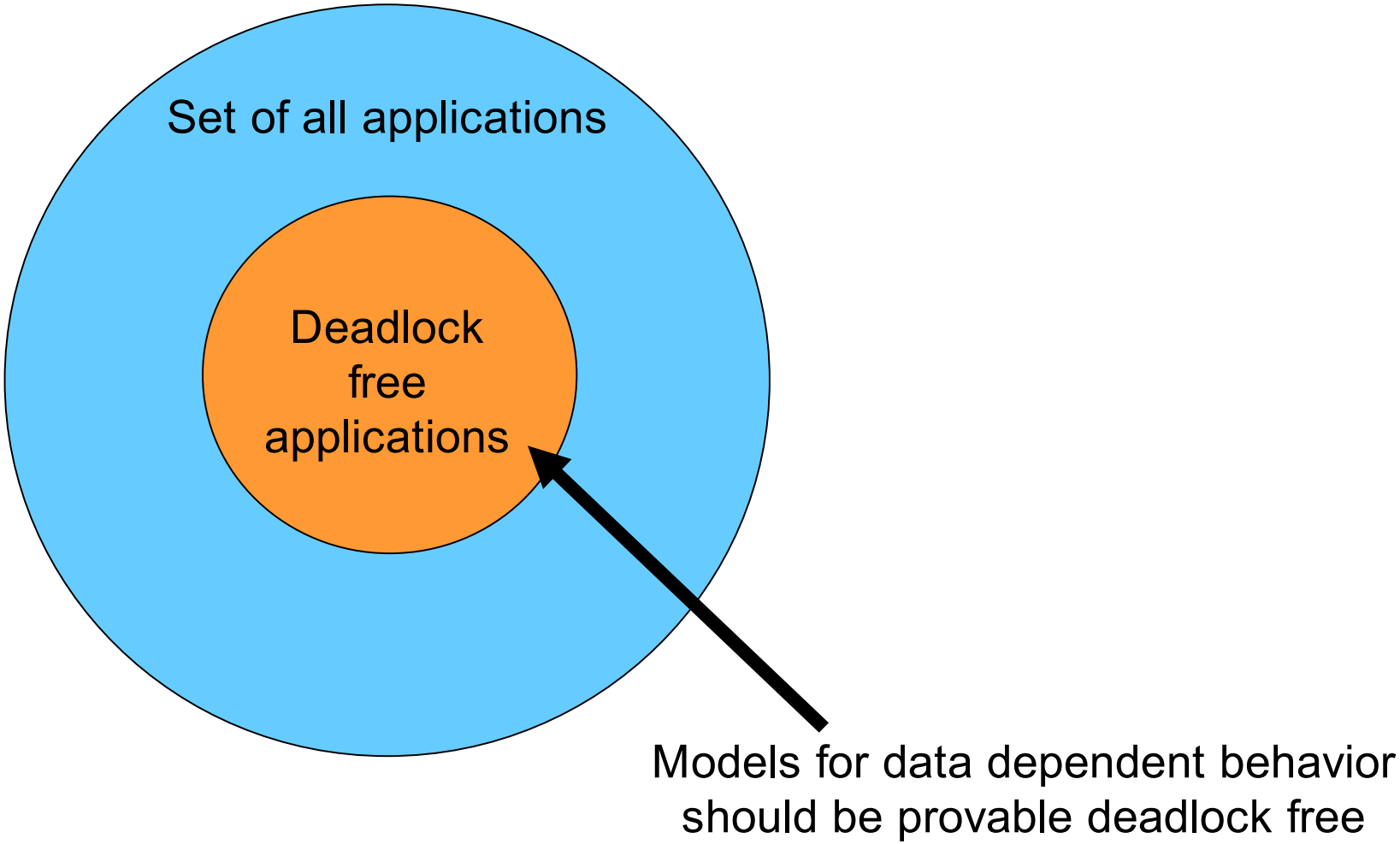


Task graph of an H263 video decoder

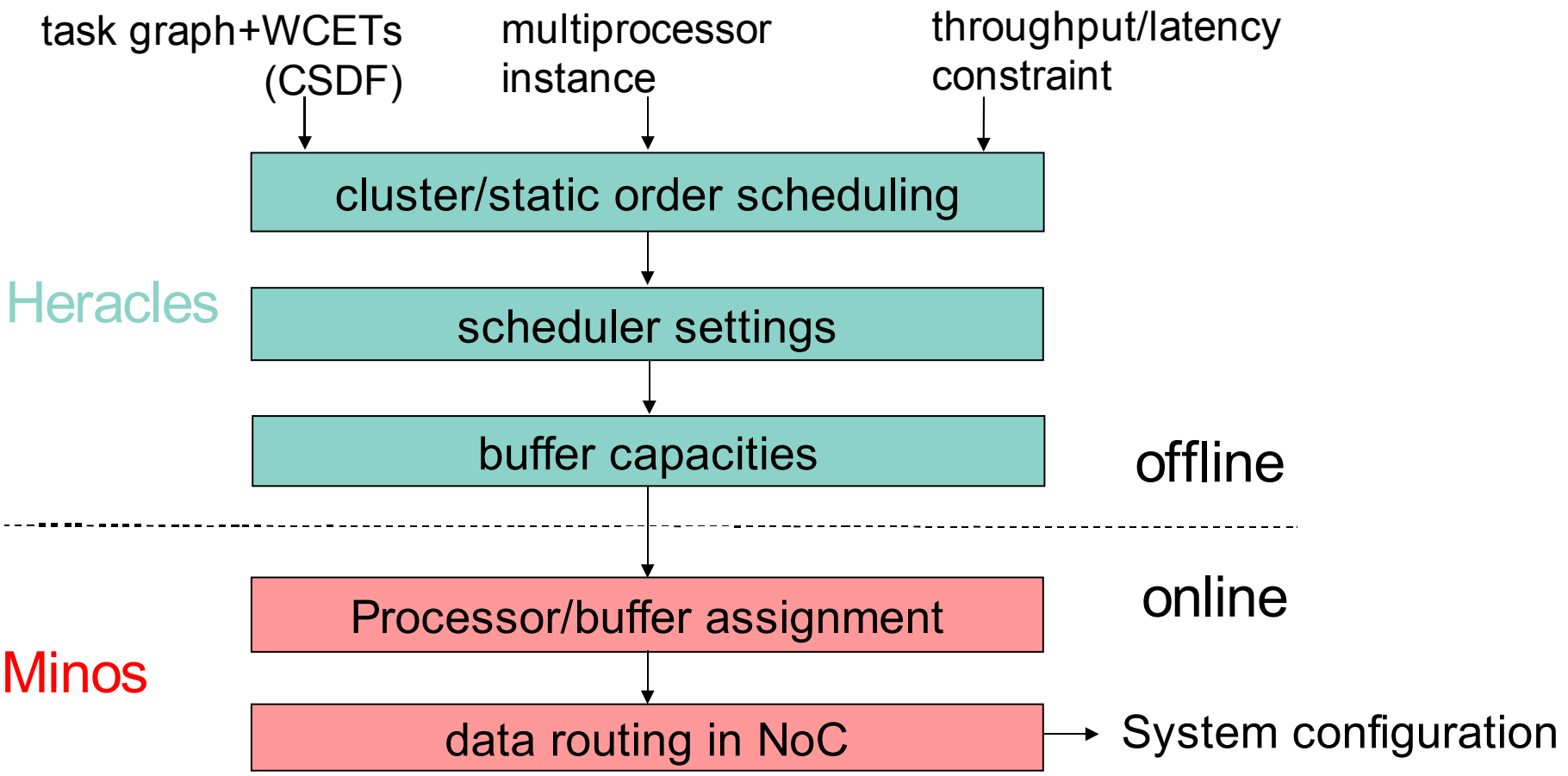
- Number of execution of the DQ and IDCT task is input data dependent

[M. Wiggers et.al.,RTAS 2008]

Expressivity of the model



Tool flow Heracles/Minos (online/offline)



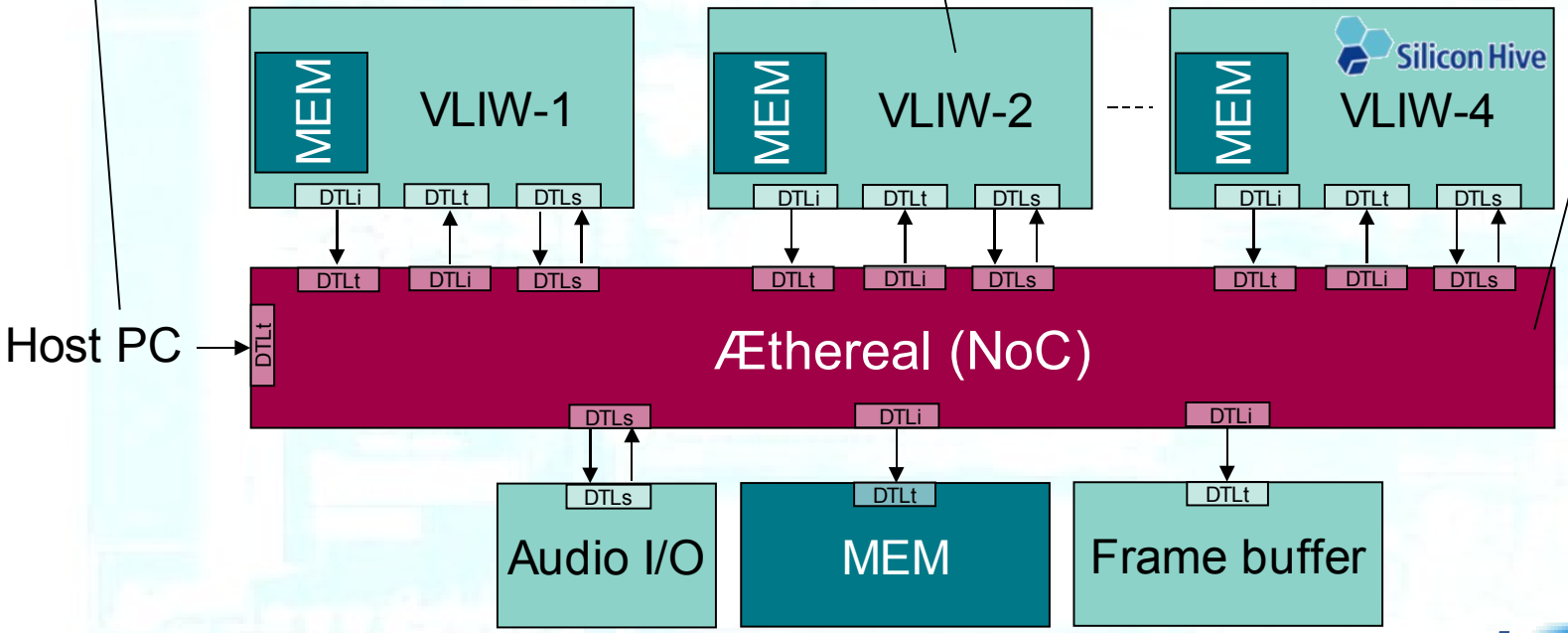
Unsolved issues: phase coupling, maximization online mapping options?

FPGA demonstrator

- PC used as control processor
- High level re-configuration API
  - setup & tear-down connections
  - starting & stopping tasks

- SiHive VLIW core
- Ansi-C compiler

- Only one network in system
  - for control, data, debug
- 2x2 mesh router network
- guaranteed throughput



Differentiators:

- Predictable = upper-bound arrival data can be computed at design time
  - budget scheduler for every shared resource

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Summary

- Car entertainment application characteristics
  - Multi job
  - Tasks with data dependent execution rates
  - Large memory footprint of digital radio applications
- Architecture characteristics
  - Multiprocessor
  - Scratch-pad memories as well as caches together with an external SDRAM
- Approach
  - Bound interference other tasks by making use of budget schedulers
- Tool flow
  - Split in an offline and an online part
- Challenges
  - Phase coupling and maximization of online mapping options
  - Expressive enough analysis model to determine throughput
  - …. and many more.

Questions?

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