



MAPS: An Integrated Framework for MPSoC Application Parallelization

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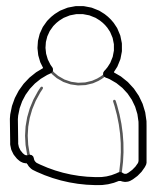
Software for Systems on Silicon
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MAPS - MPSoC Application Programming Studio

- MAPS Project Overview
- MAPS-TCT Framework
- Summary/Outlook

MAPS Project Overview



Multi-App Project

App1

- C
- Hard RT
- DSP
- || 2, X 3

App2

- Threaded C
- Soft RT
- RISC
- || 1

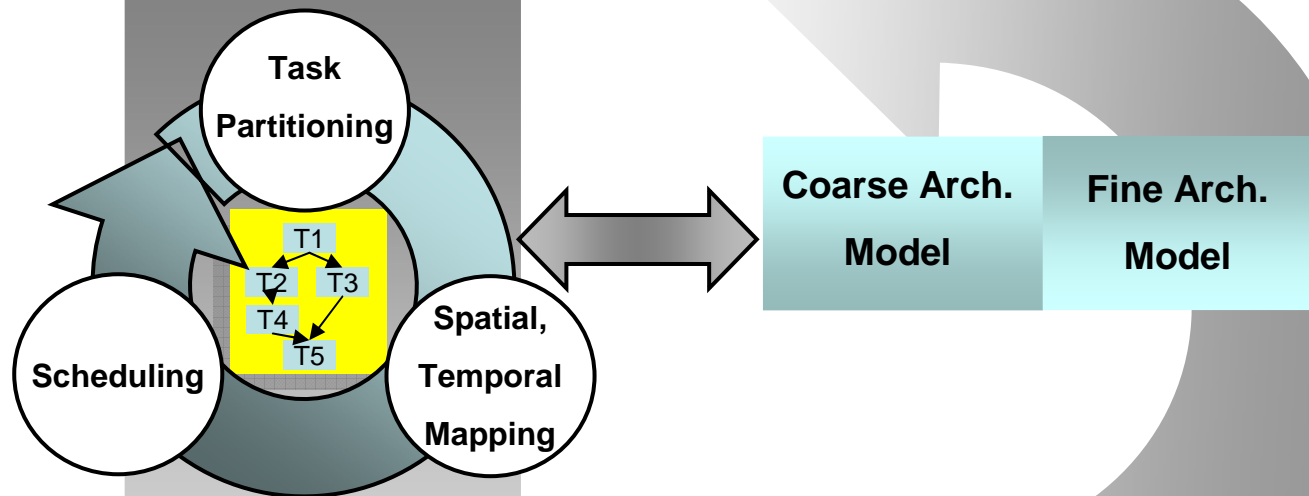
App3

- Mixed
- No RT
- No Pref.
- || 2, X 1

...

App

- Specification
- RT Constraints
- Pref. PE class
- Concurrency



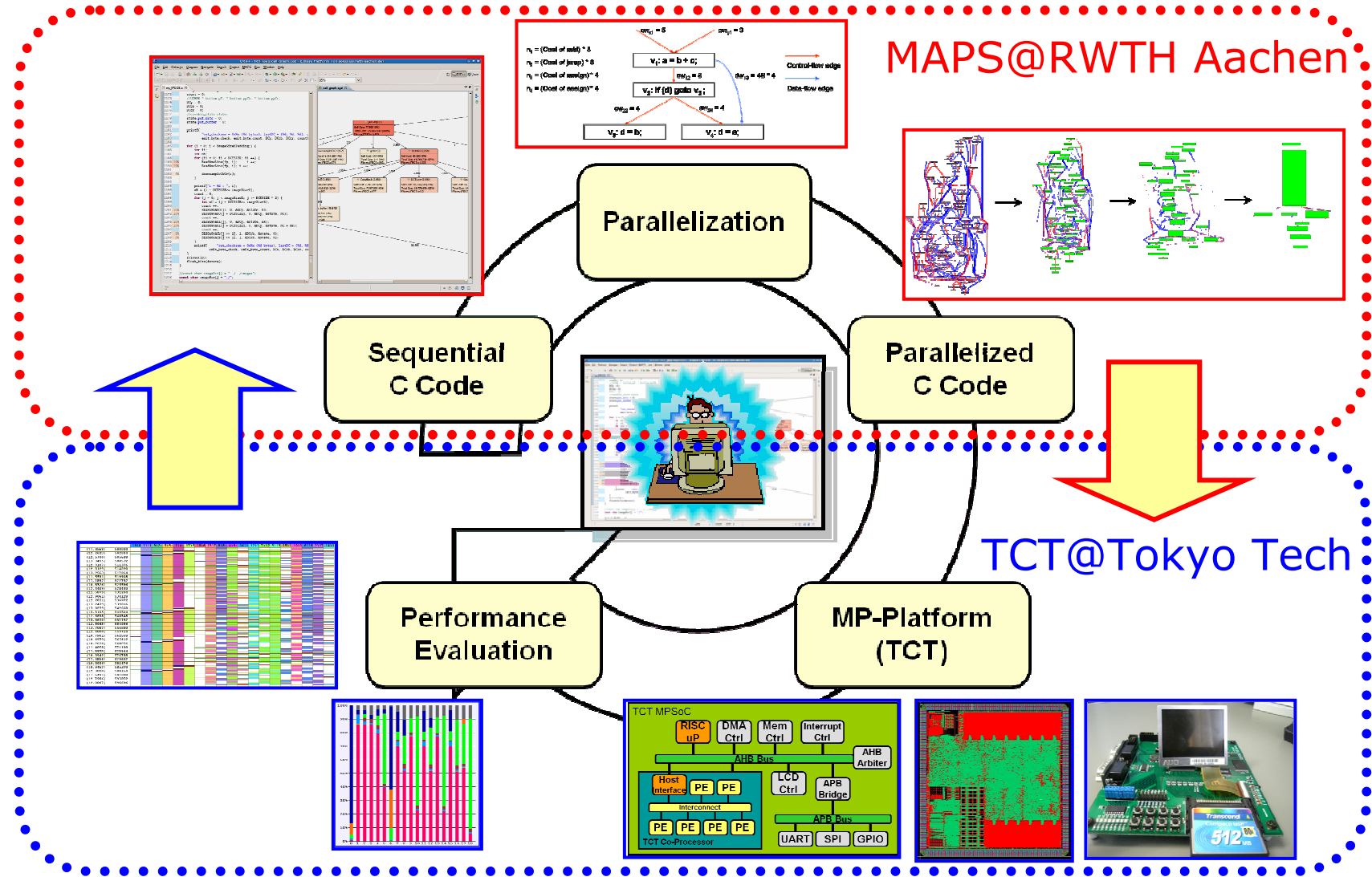
Coarse Arch.
Model

Fine Arch.
Model

MPSoC C Code-gen (CC*, + OS/OSIP services, etc.)

Virtual Platform/Real Hardware Board

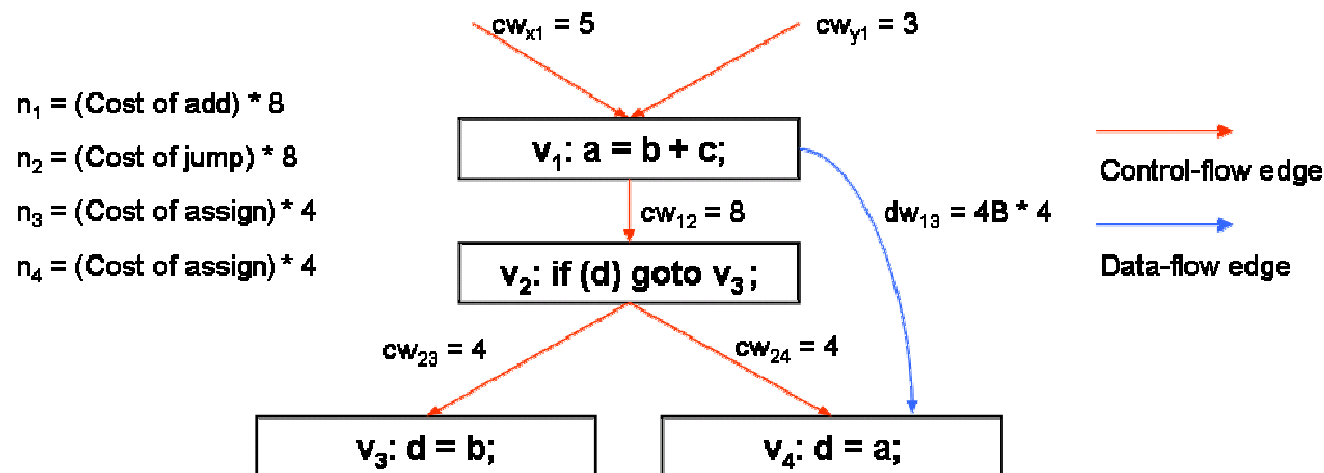
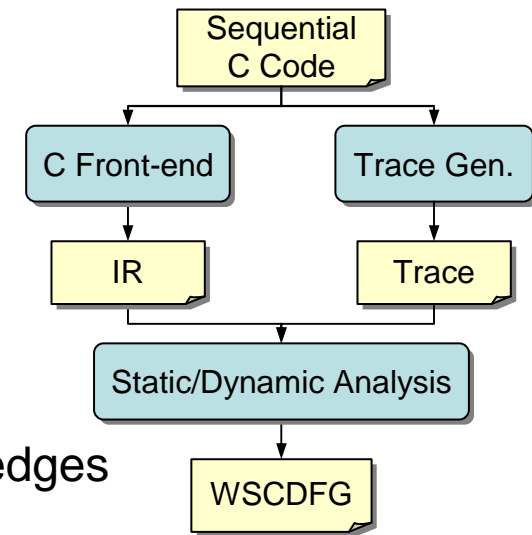
MAPS-TCT Framework



- ***A practical MPSoC software development tool suite***
 - Sequential C (input) → “threaded C” (output)
 - Powerful analysis tools for providing rich feedback to the programmers
 - *Static dependence analysis*
 - *Dynamic profiling*
 - Powerful clustering method for extracting coarse-grain parallelism
 - *Weighted Statement Control Data Flow Graph (WSCDFG)*: annotates dynamic profiling information on CDFG
 - *Coupled Block (CB)*: subgraph of WSCDFG that is schedulable and tightly coupled by data dependence
 - *Constrained Agglomerative Hierarchical Clustering (CAHC)*: iterative clustering for building coarser graphs

Weighted Statement Control/Data Flow Graph (WSCDFG)

- **Definition:** *WSCDFG* is a directed graph defined by $G = (V, CE, DE, CW, DW, N)$, where:
 - V : IR statement nodes
 - CE : set of control flow edges
 - DE : set of data flow edges
 - CW : weights (count) of control edges
 - DW : weights (amount of data, e.g. bytes) of data edges
 - N : weight of IR statement nodes (cost table)



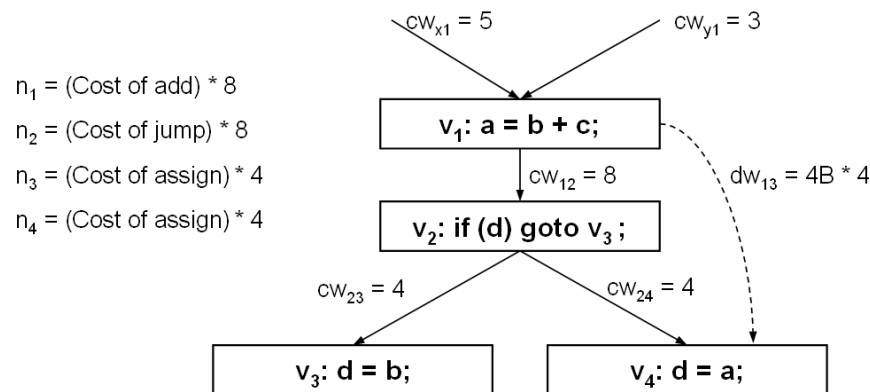
Parallelism Discovery: Granularity - Coupled Block (CB)

- Coarse-grained Task Parallelism in C
- Based on Compiler IR (Intermediate Representation)
- Suitable Granularity of Codes as Atomic code blocks

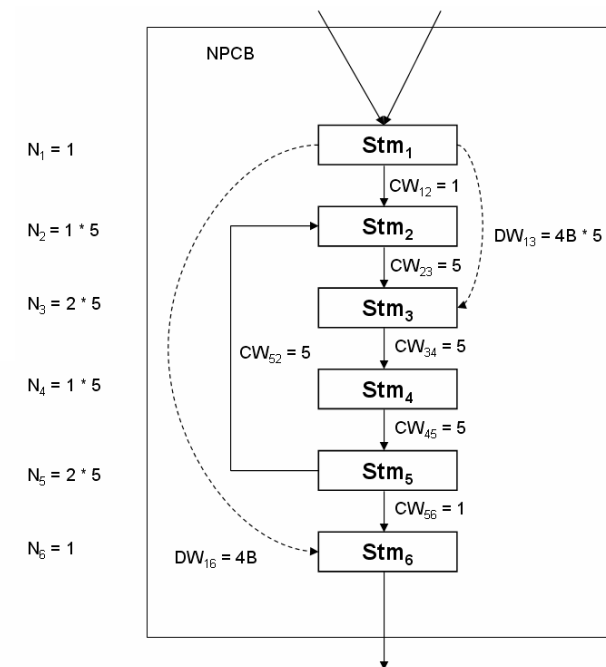
→ **CB** (*Coupled Block*)

■ CB Design Criteria

- Tightly coupled by data-dependence
- Schedulable



Weighted Statement Control/Data-flow Graph (WSCDFG)

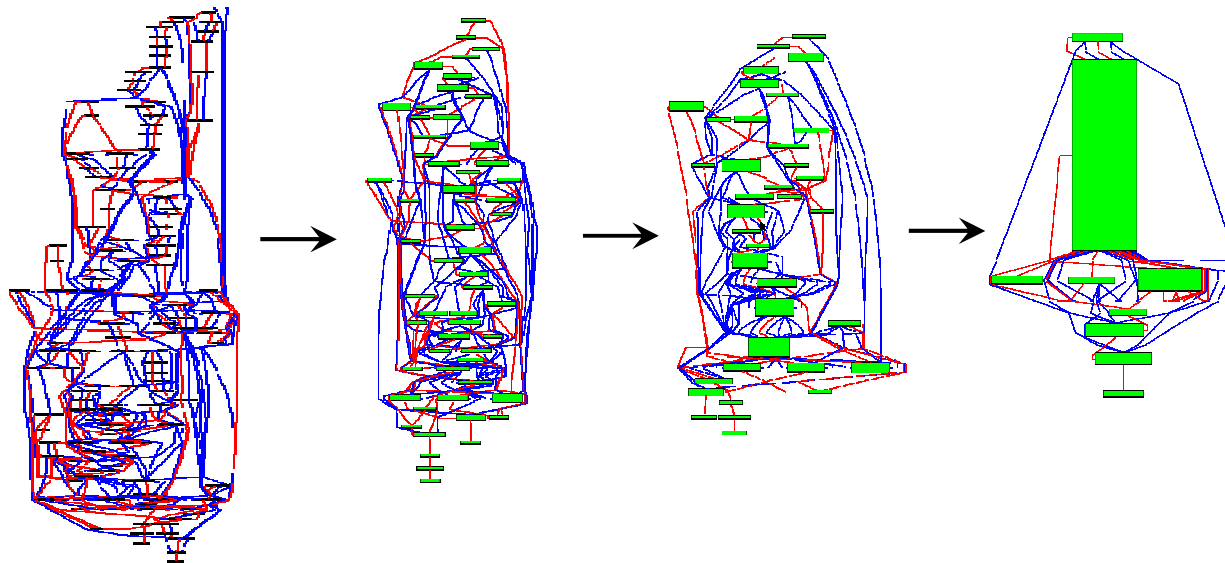


CB Example in WSCDFG

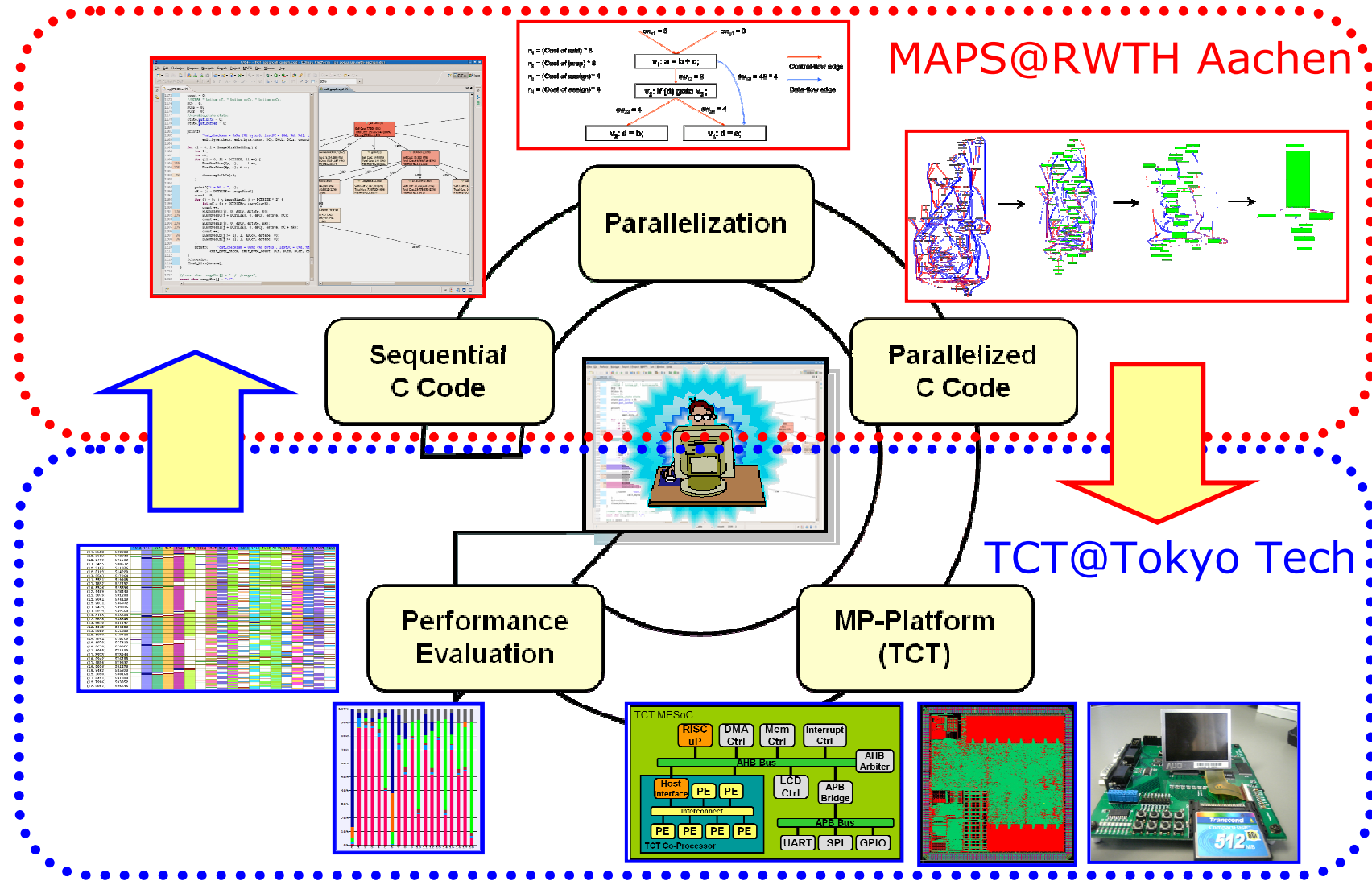
$$\bullet \forall v_i \in V', \frac{w_1 \cdot \sum_{cw_{ij} \in CW'} cw_{ij} + w_2 \cdot \sum_{dw_{ij} \in DW'} dw_{ij}}{D(v_i, V')} > T$$

Parallelism Discovery: CB Generation – CAHC Algorithm

- Optimal generation of CB: **Heuristics needed**
- Based on **Density Boundary Scan algorithm (DBSCAN)** for knowledge discovery in data bases
- **Constrained Agglomerative Hierarchical Clustering – CAHC**
 - **Constrained**: maintain schedulability of CBs
 - **Hierarchical**: several clustering levels with different granularities
 - **Agglomerative**: build coarser graphs iteratively

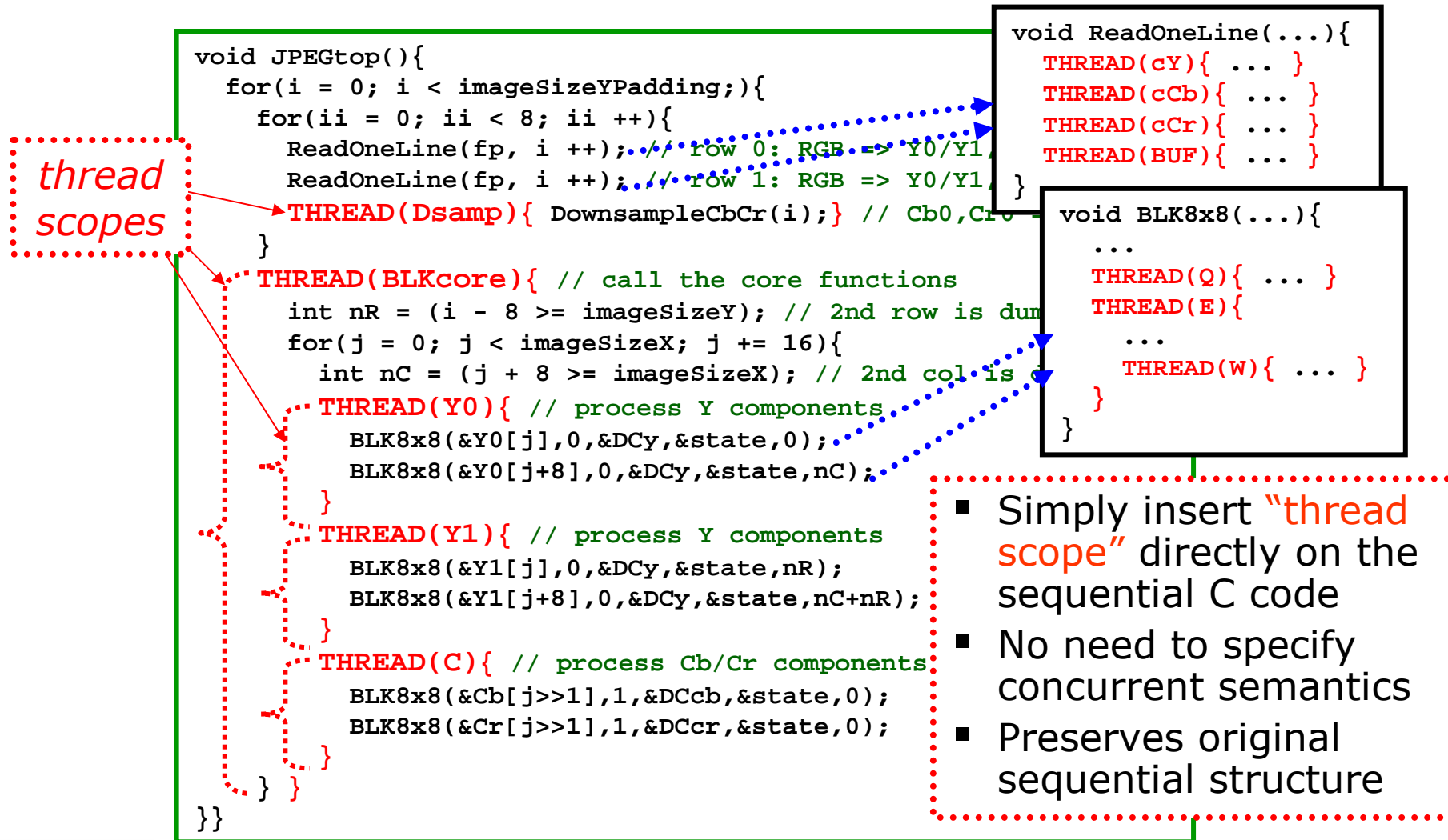


MAPS-TCT Framework



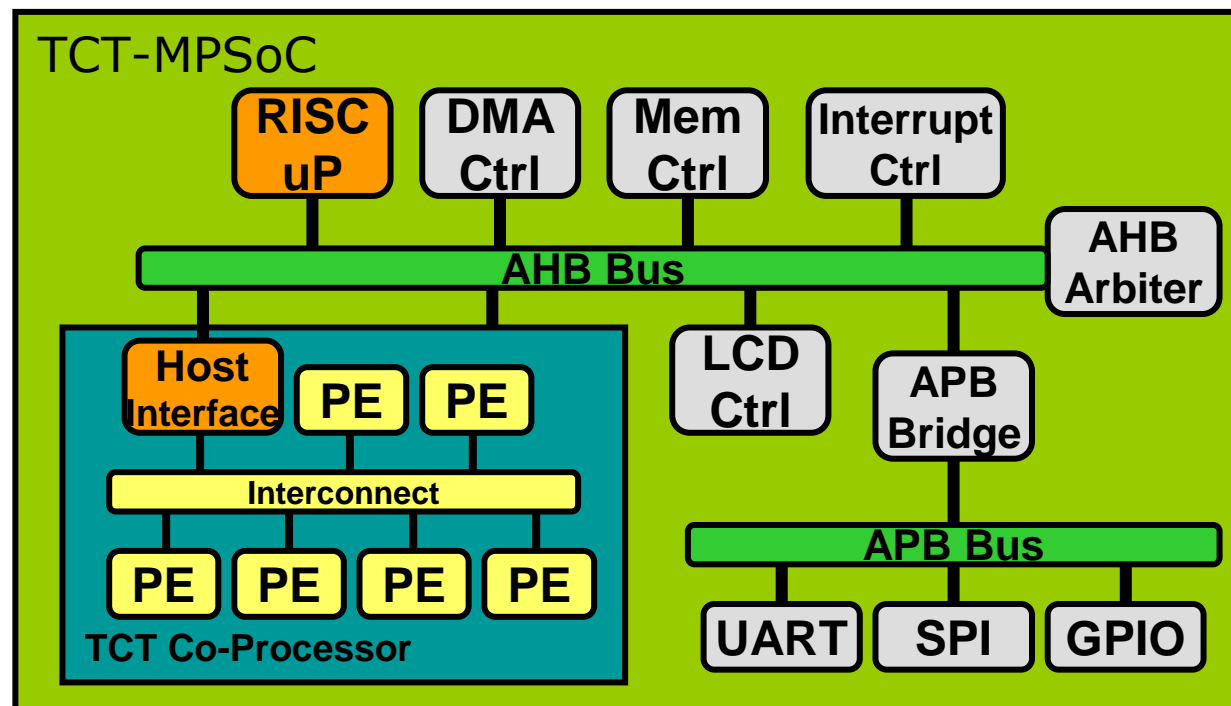
Tightly-Coupled Thread (TCT) Programming Model

Seamless transition from *sequential C codes*



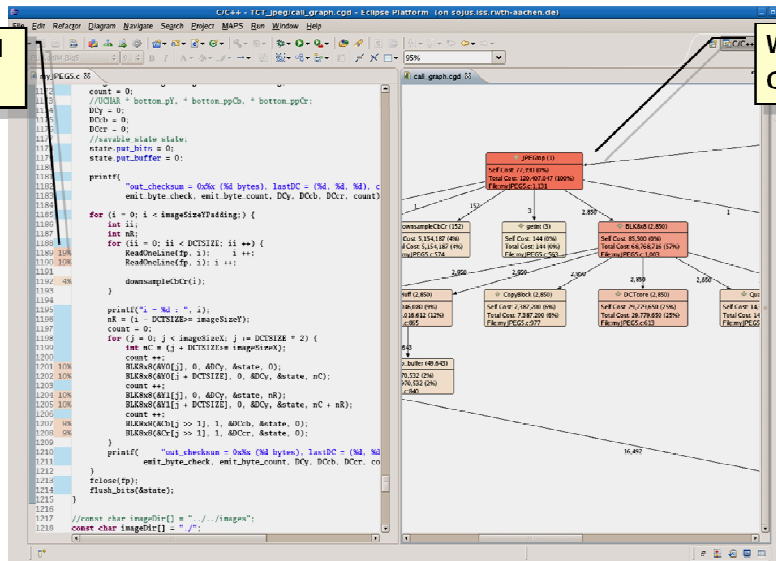
TCT-MPSoC Prototype Chip

- **TCT Coprocessor (TCoP): 6-PE array @ 100 MHz**
 - Full crossbar interconnect
 - Dedicated comm. module in each PE
- **Host RISC core: JANUS200 @ 200 MHz (ARMv4T ISA)**
 - Can be configured as the 7th PE on the PE array interconnect



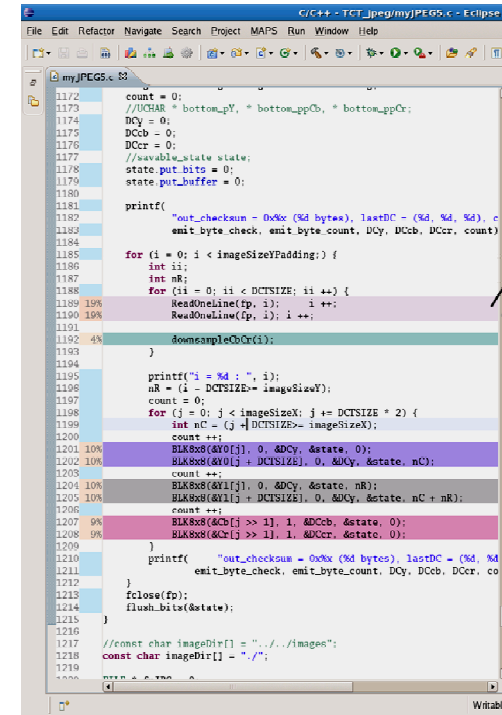
Parallelization Experiment: JPEG Encoder

Source Level Profile



Weighted Call Graph

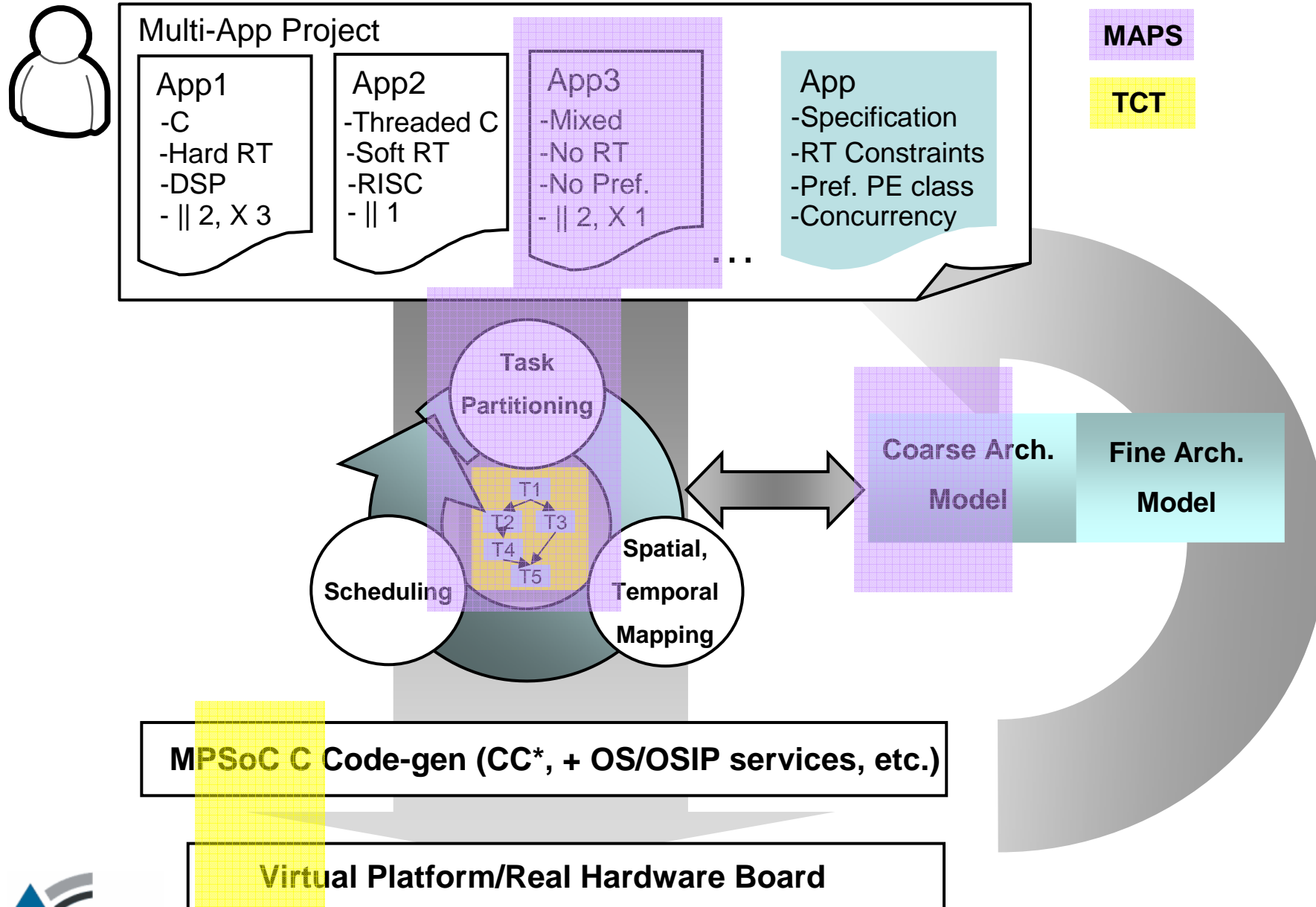
Task Annotation



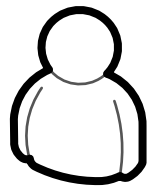
Speedup & efficiency

Step	Speedup	No. of PEs	Parallel Efficiency
1	3.61x	16	22.58%
2	5.48x	17	32.3%
3	5.48x	16	34.3%
manual	9.43x	19	49.6%

Summary: MAPS work-in-progress



Outlook



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- **Multi-App Model**
- **Better Arch. Model**
- **OSIP Scheduling**
- **MPSoC Code-gen**

Task
Partitioning

Scheduling

Spatial,
Temporal
Mapping

Coarse Arch.
Model

Fine Arch.
Model

MPSoC C Code-gen (CC*, + OS/OSIP services, etc.)

Virtual Platform/Real Hardware Board

Thank you!