technische universität
dortmund

fakultät für informatik
informatik 12

1st Workshop on Mapping of Applications to MPSoCs

Schloss Rheinfels
St. Goar, Germany

June 16/17th, 2008

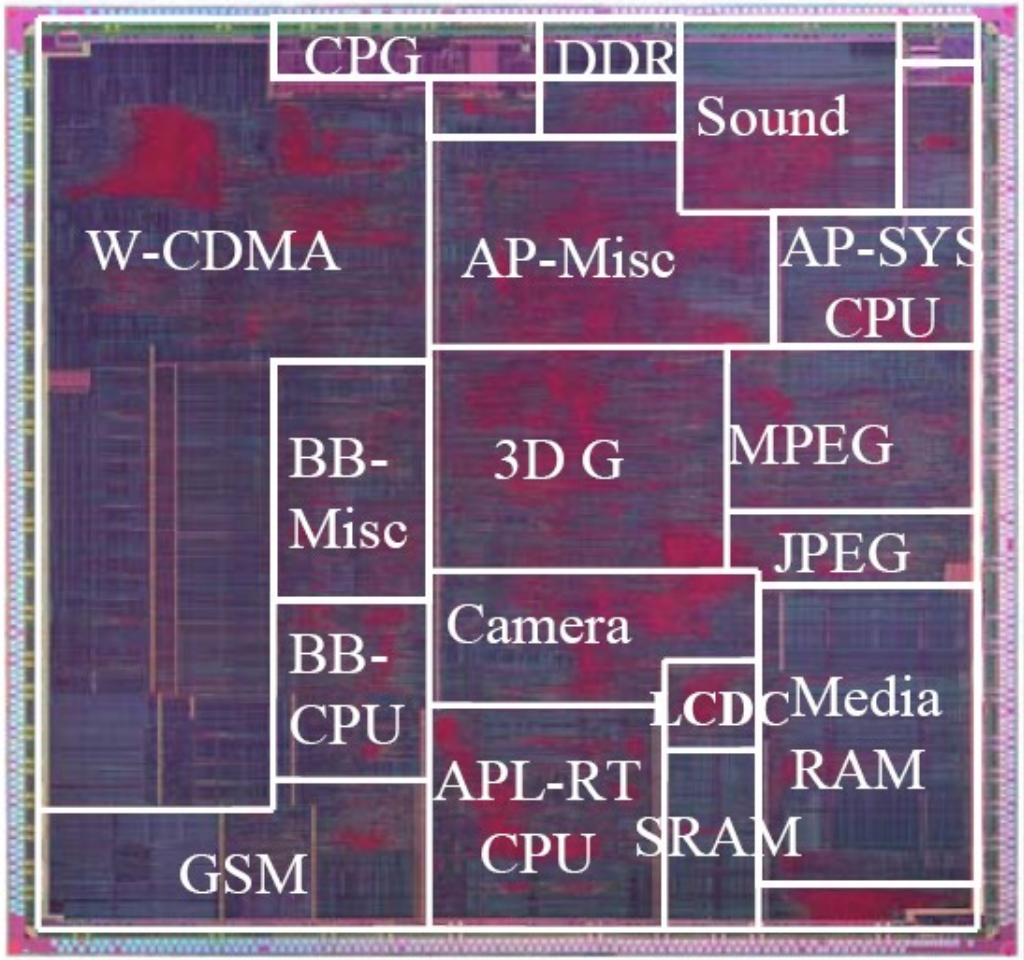
http://www.schloss-rheinfels.de/content/view/113/218/

Trend

Obvious trend toward using many processors in one system: multi-cores, many-cores, MPSoCs

Example

SH-MobileG1: Chip Overview



Die size	11.15mm x 11.15mm
Process	90nm LP 8M(7Cu+1Al) CMOS dual-Vth
Supply voltage	1.2V(internal), 1.8/2.5/3.3V(I/O)
# of TRs, gate, memory	181M TRs, 13.5M Gate 20.2 Mbit mem

http://www.mpsoc-forum.org/2007/slides/Hattori.pdf

Goal

- Traditional applications written as a single thread
- ☞ How to map applications to multiple processors?
- ☞ How to map applications to MPSoCs?
- ☞ Key issue for the ArtistDesign network of excellence
- ☞ Key issue for its cluster on software synthesis, code generation and timing analysis (SSCGTA)

ArtistDesign SSCGTA Partners

- Guillem Bernat (U. York)
- Rainer Leupers (RWTH Aachen)
- Christian Lengauer (Passau U)
- Björn Lisper (Mälardalen U)
- Stylianos Mamagkakis (IMEC)
- Peter Marwedel (TU Dortmund)
- Peter Puschner (TU Wien)
- Reinhard Wilhelm (Saarland U.)

Affiliates:

- Joseph van Vlijmen (ACE/Amsterdam), Björn Franke (U. Edinburgh), Sabine Glesner (TU Berlin), Paul Kelly (London), Alain Darte (ENS/Lyon), Marco Bekooij (NXP/Eindhoven), Bart Kienhuis (Compaan/Leiden), Christian Ferdinand (AbsInt/Saarbrücken), Niklas Holsti (Tidorum/Finland)

Schedule (June 16th)

12:00	Lunch	
12:45	**Global Session I**: Opening (*session chair: Peter Marwedel)*	
13:00	**Future Architectures of MPSoC Platforms** (John Goodacre, ARM)	
14:00	**Mapping Techniques** (Lothar Thiele, ETH Zürich)	
14:55	**Mapping Flow for Car-Entertainment Applications onto Embedded Multiprocessor Systems** (Marco Bekooij, NXP)	
15:30	Break	
16:00	**Global session II** (*session chair: Sander Stuijk)*	
	The MAPS Project - Parallelizing C Compiler for MPSoC- (R. Leupers, W. Sheng, RWTH Aachen)	
16:35	**Requirements for Application Software and Hardware imposed by Temporal Analysis Techniques** (Maarten Wiggers, U. Twente)	
17:10	Brief break	
17:15	**Code Synthesis I** *(session chair: Björn Franke)*	**Timing Analysis I** *(session chair: Björn Lisper)*
17:15	**Overview Over Parallelization Techniques I** (C. Lengauer, U. Passau)	**A Predictable MP Design-Flow for Streaming Applications** (Sander Stuijk, TU Eindhoven)
		Discussions
18:00	Sessions end	
18:30	Departure for social event	
19:00	Social event: wine tasting	

Schedule (June 17th)

9:00	**Global session III** *(session chair: Rainer Leupers)*	
	Future Architectures of MPSoC Platforms II (Gerhard Fettweis, TU Dresden)	
9:50	Brief break	
9:55	**Code Synthesis II** *(session chair: Christian Lengauer)*	**Timing Analysis II** *(session chair: Björn Lisper)*
	Overview Over Parallelization Techniques II (Björn Franke, U. Edinburgh)	**Predictable Timing on MPSoC - A Time-Triggered View Presentation** (Peter Puschner, TU Wien)
10:30	Break (deadline for vacating rooms; returning keys)	
11:00	**Code Synthesis III** *(session chair: Trevor Carlson)*	**Timing Analysis III** *(session chair: Björn Lisper)*
	From Sequential Application Specification to FPGA-based Heterogeneous MPSoC platform execution (Ed Deprettere, U. Leiden)	**Using learning to support the development of embedded systems** (Mark Bartlett, U. York)
11:30	**Mapping to the CELL Processor** (Martino Ruggiero, U. Bologna)	**Discussion on Timing Analysis Issues for MPSoCs**
12:00	**Global session IV** *(session chair: Peter Marwedel)*	
12:00	**Global Road Mapping Discussion**	
12:30	Lunch	
13:30	**Global Road Mapping Discussion** (continued)	
14:00	(-15:00): **ArtistDesign Internal Discussion**	

Logistics

- Workshop fee covered by Artist network
- 2 lunches, 1 dinner + wine tasting and breaks included
- Drinks in the meeting room included
- Some rooms fees also covered through Artist
  (e.g. ArtistDesign affiliates who are not Artist2 members)
  Includes only room fee for 1 night, no extras.
- All other fees to be paid by attendees

Don’t forget: we want an interactive atmosphere!

☞ Keynote

Cooperation

- Mapping: Dresden, Aachen, Zürich, Leiden/Amsterdam, Dortmund? (Azad-) U. Tehran?
- Code generation: Passau, Saarbrücken, Edinburgh, Leiden
- Task graph extraction: Edinburgh, Aachen
- Scenarios: Eindhoven, IMEC, Edinburgh
- Exploration: Dortmund, Zürich
- „Mnemee“: Dortmund, IMEC
- CleanC: IMEC, Edinburgh
- Cell: Leiden, Bologna?
- „Optimma“: K.U.L., Ghent, IMEC
- TA: ArtistDesign Cluster

Meeting

June 2009, Rheinfels
ArtistDesign: Nov. 27/28, 2008 or Nov. 13/14. D‘dorf airport?
Smaller subtask meetings

Other actions

Slides to ArtistDesign web site
Bibliography (bib entries to Peter M).

Next steps