TU/e Technische Universiteit Eindhoven University of Technology

A Predictable Multiprocessor Design-Flow for Streaming Applications Presentation

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Marc Geilen, Bart Theelen and Henk Corporaal

1st Workshop on Mapping of Applications to MPSoCs

Department of Electrical Engineering
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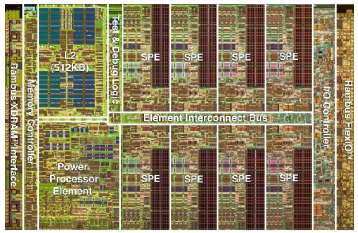

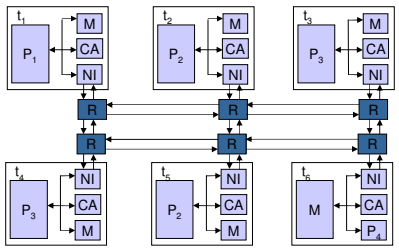

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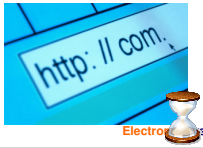
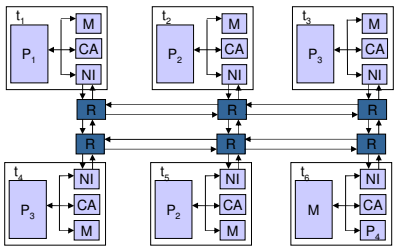
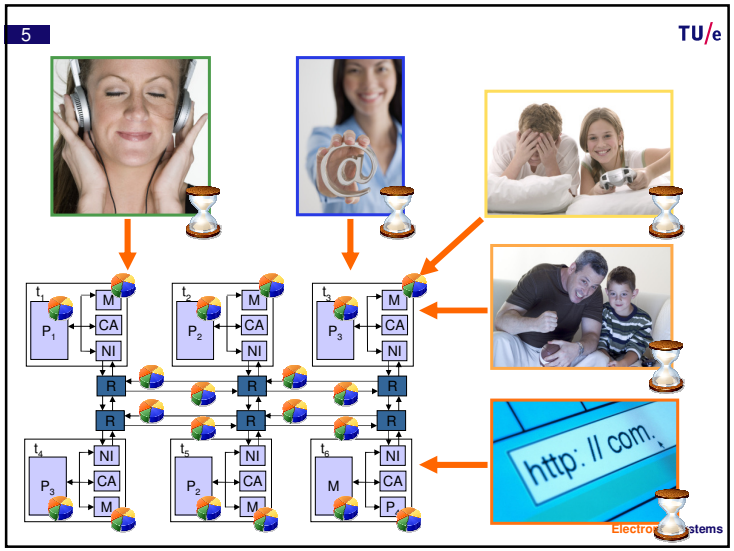




Electro stems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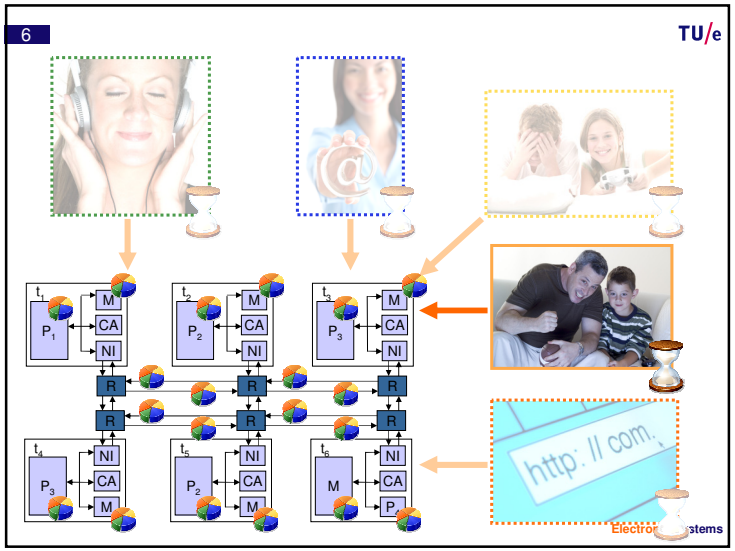
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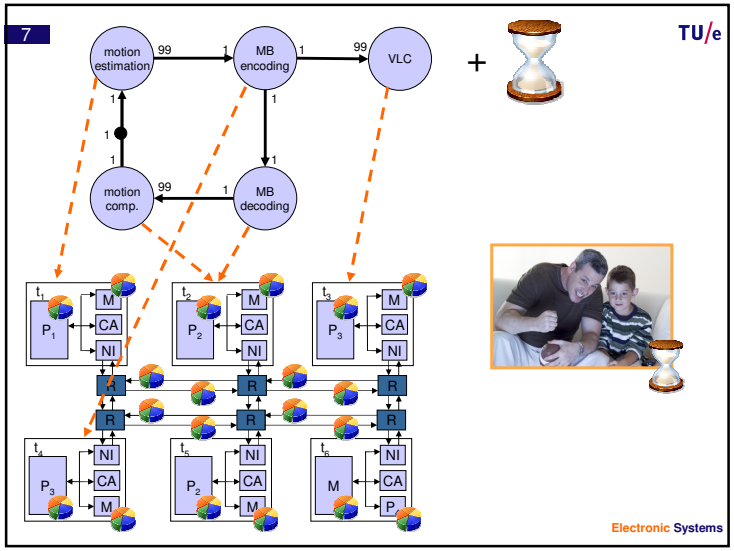
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motion estimation
MB encoding
VLC
motion comp.
MB decoding
99
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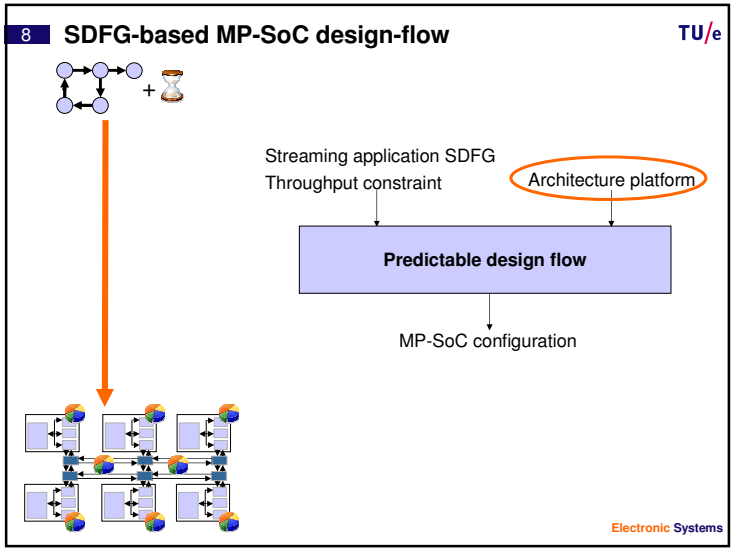
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SDFG-based MP-SoC design-flow
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Streaming application SDFG
Throughput constraint
Architecture platform
Predictable design flow
MP-SoC configuration
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9 Predictable platform

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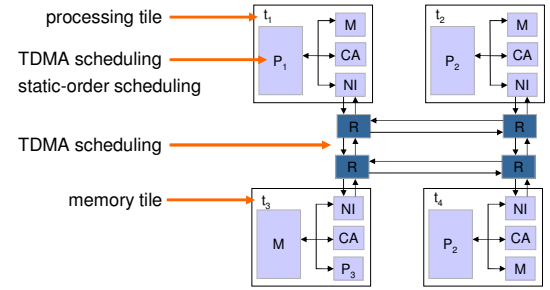

	processor		memory	network interface		
	type	wheelsize	size	#conn	in bw	out bw
t_1	P_1	100	1000	10	96	96
t_2	P_2	100	500	10	96	96
t_3	P_3	100	10000	10	96	96
t_4	P_2	100	500	10	96	96

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10 SDFG-based MP-SoC design-flow

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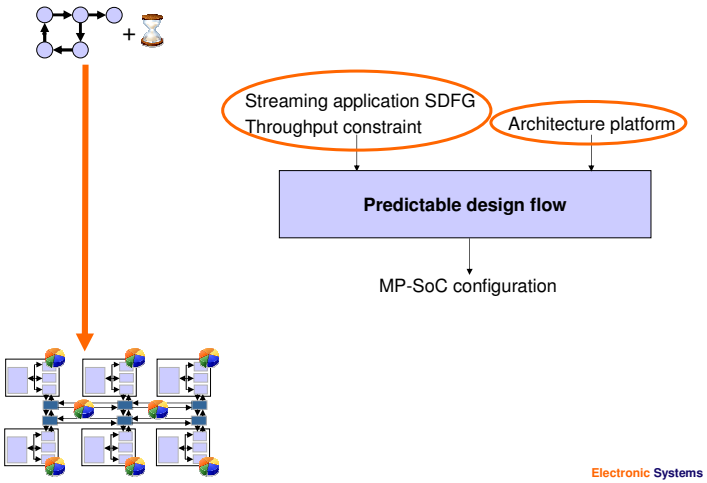

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11 Synchronous Dataflow Graphs

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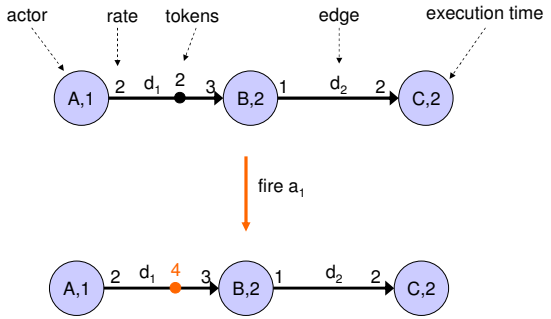

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12 Timed SDF state space

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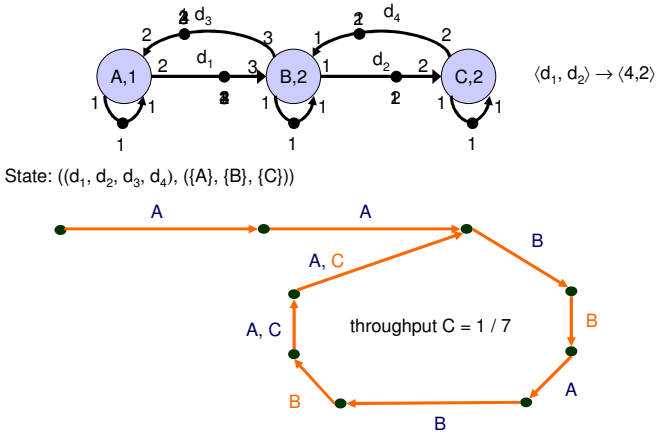

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13 Streaming application SDFG

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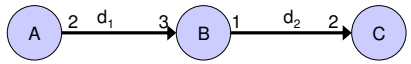

	execution time		memory	
	P_1	P_2	P_1	P_2
A	1	7	200	200
B	2	-	350	-
C	-	2	-	100

	token size
	sz
d_1	128
d_2	64

Throughput constraint: 0.07 firings / time-unit

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14 SDFG-based MP-SoC design-flow

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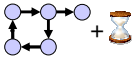
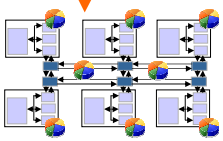


Streaming application SDFG
Throughput constraint

Architecture platform

Predictable design flow

MP-SoC configuration



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15 SDFG-based MP-SoC design-flow

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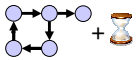


Streaming application SDFG
Throughput constraint

Memory dimensioning (4 steps)

Constraint refinement (2 steps)

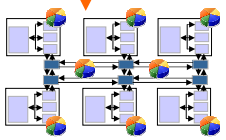
Platform graph

Tile binding and scheduling (4 steps)

Interconnect graph

NoC routing and scheduling (3 steps)

MP-SoC configuration



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16 Memory dimensioning and constraint refinement

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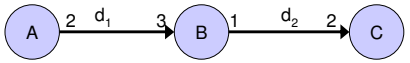
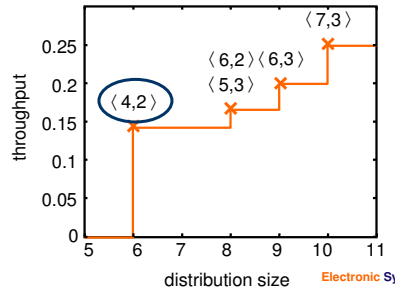


	token size	storage-space			latency	bandwidth
	sz	α_{mem}	α_{src}	α_{dst}	ρ	β
d_1	128	4	2	3	4	109.71
d_2	64	2	1	2	4	18.29

Throughput constraint:
0.07 firings / time-unit



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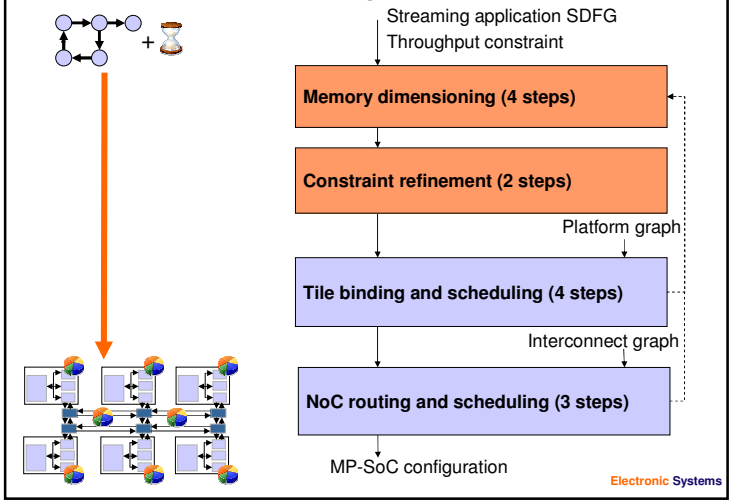
17 SDFG-based MP-SoC design-flow



18 Tile binding

- Actors sorted on "criticality"
  - Related to notion of cycle-mean in HSDF
- Binding considers
  - Processing load
  - Memory load
  - Communication load
  - Communication latency
- Cost function weights alternative tiles

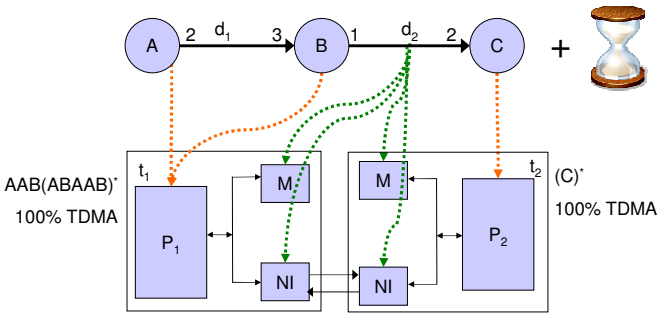
$$\text{cost}(t) = c_1 \cdot l_p(t) + c_2 \cdot l_m(t) + c_3 \cdot l_c(t) + c_4 \cdot l_l(t)$$

- Greedy strategy with one optimization pass after initial binding

19 Scheduling

- Static-order scheduling between actors
  - Order actor firings of an application on a processor
  - List-scheduling algorithm
- TDMA scheduling between applications
  - Provide timing independence between applications
  - Binary search algorithm using fast throughput analysis technique

20 Tile binding and scheduling



Find a binding and scheduling of an SDFG onto an MP-SoC that satisfies the throughput constraint

21 Binding-aware SDFG

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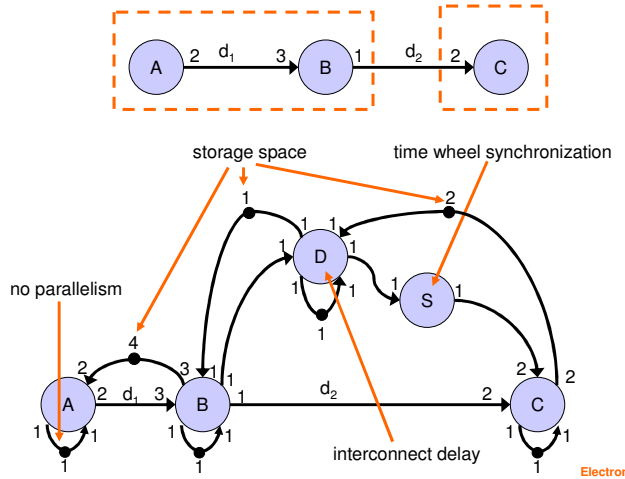

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22 Binding-aware SDFG throughput computation

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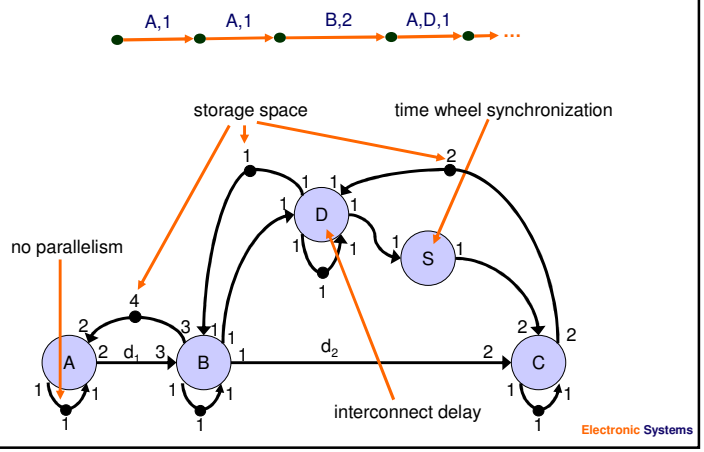

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23 Tile binding and scheduling

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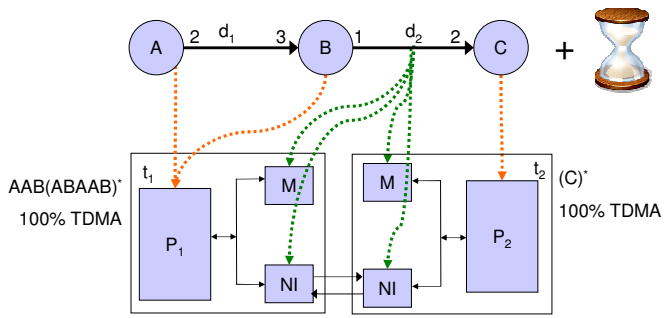

100% time wheels allocated gives throughput of 0.06 < 0.07

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24 SDFG-based MP-SoC design-flow

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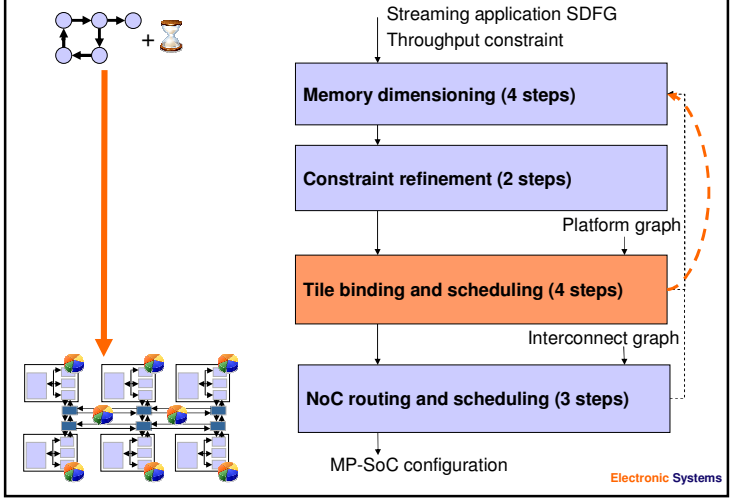

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25 Memory dimensioning and constraint refinement

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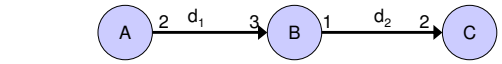
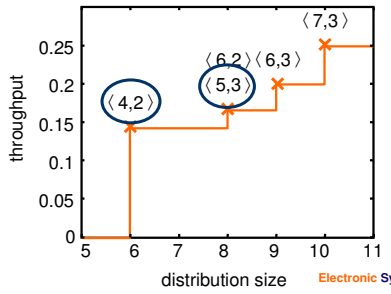


	token size	storage-space			latency	bandwidth
	sz	α_{mem}	α_{src}	α_{dst}	ρ	β
d_1	128	4	3	3	3	128
d_2	64	2	2	2	7	21.33



Throughput constraint:
0.07 firings / time-unit

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26 Tile binding and scheduling

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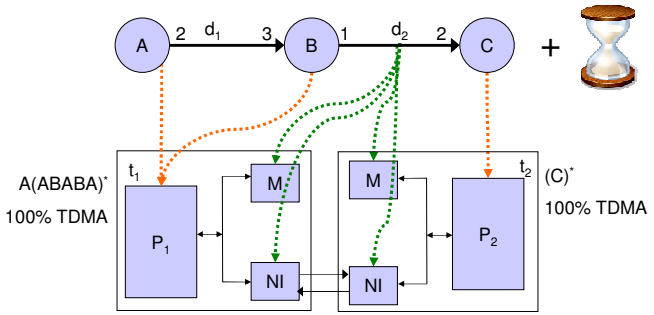

100% time wheels allocated gives throughput of 0.07

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27 SDFG-based MP-SoC design-flow

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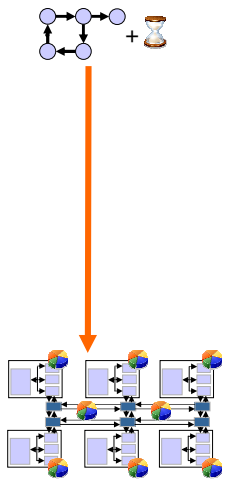

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MP-SoC configuration

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28 NoC routing and scheduling

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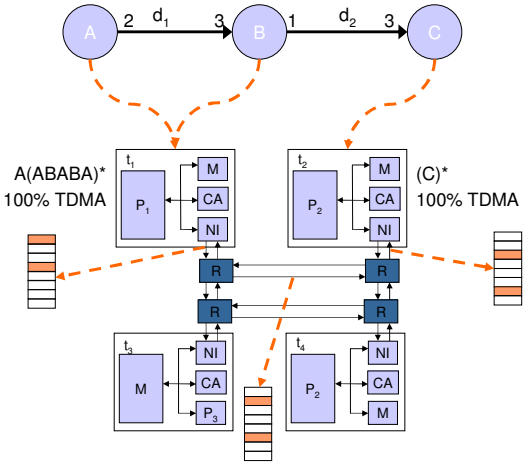

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29 NoC routing and scheduling

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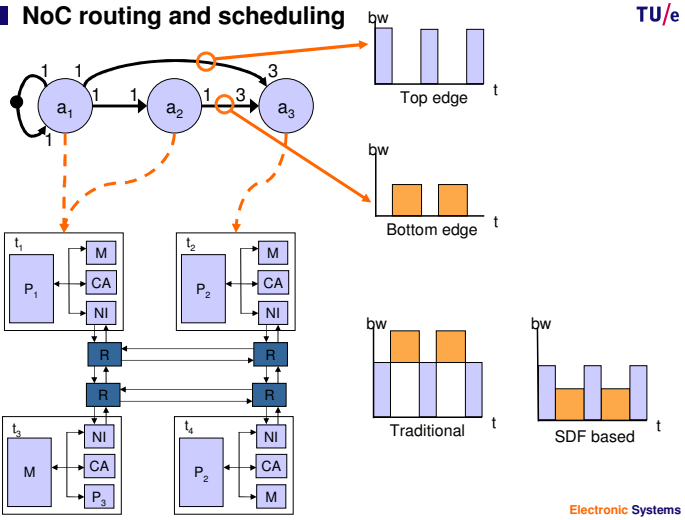

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30 NoC routing and scheduling

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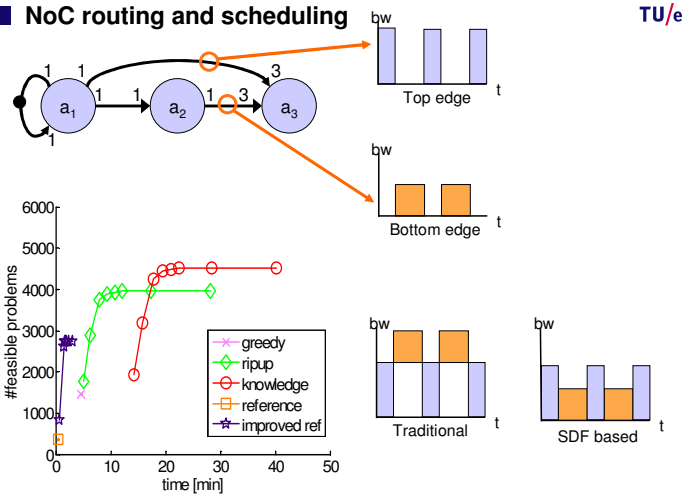

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31 SDFG-based MP-SoC design-flow

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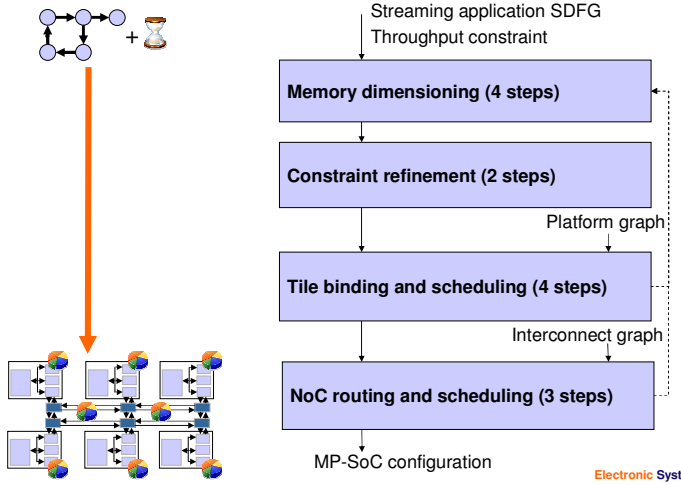

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32 Run-time of the design flow

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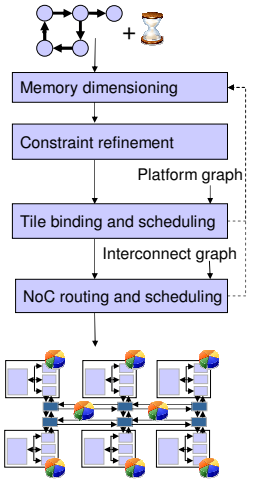

H.263 encoder	H.263 decoder	MP3 decoder
2ms	1611ms	143ms
1ms	0ms	1ms
287ms	816ms	55ms
125ms	261ms	5ms
415ms	**2688ms**	**203ms**

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33 SDF³: SDF For Free

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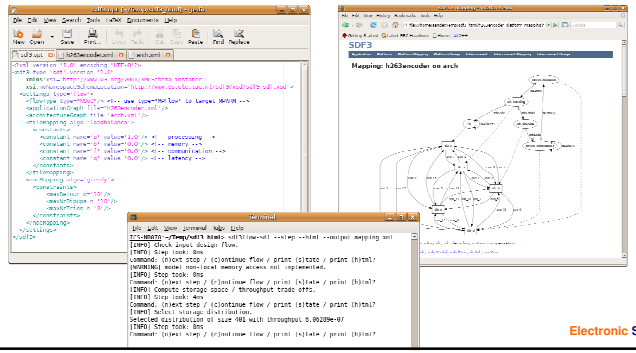
- SDF³ implements the NoC-based MP-SoC design flow
  - Input/output of each step is described in XML
  - XML can be transformed to HTML
  - Command-line tool and C/C++ API available



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34 Conclusions

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- MP-SoC design-flow and SDF³ toolkit available at www.es.ele.tue.nl/sdf3
- First design-flow which maps SDFG to NoC-based MP-SoC
- Considers scheduling on processing, storage and communication resources
- Flow based on trade-offs between storage space, latency and bandwidth
- Most of the steps in the design-flow require milliseconds to complete for realistic applications

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