Dimensioning Heterogeneous MPSoCs via Parallelism Analysis

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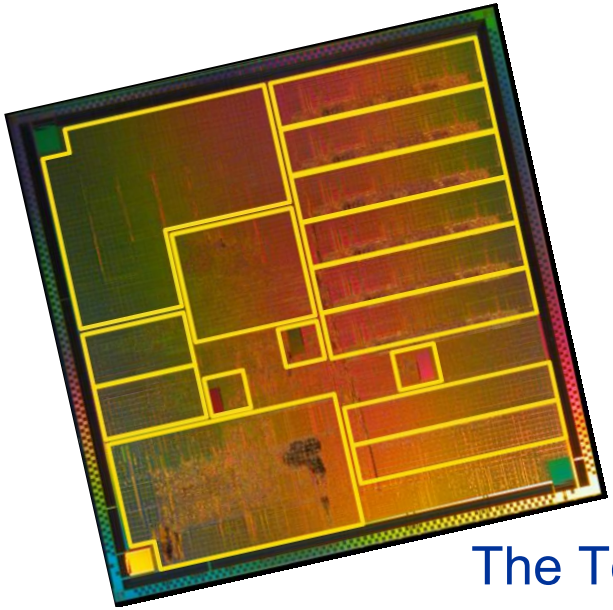
Many Core in Embedded Systems

Trend towards heterogeneous many core systems



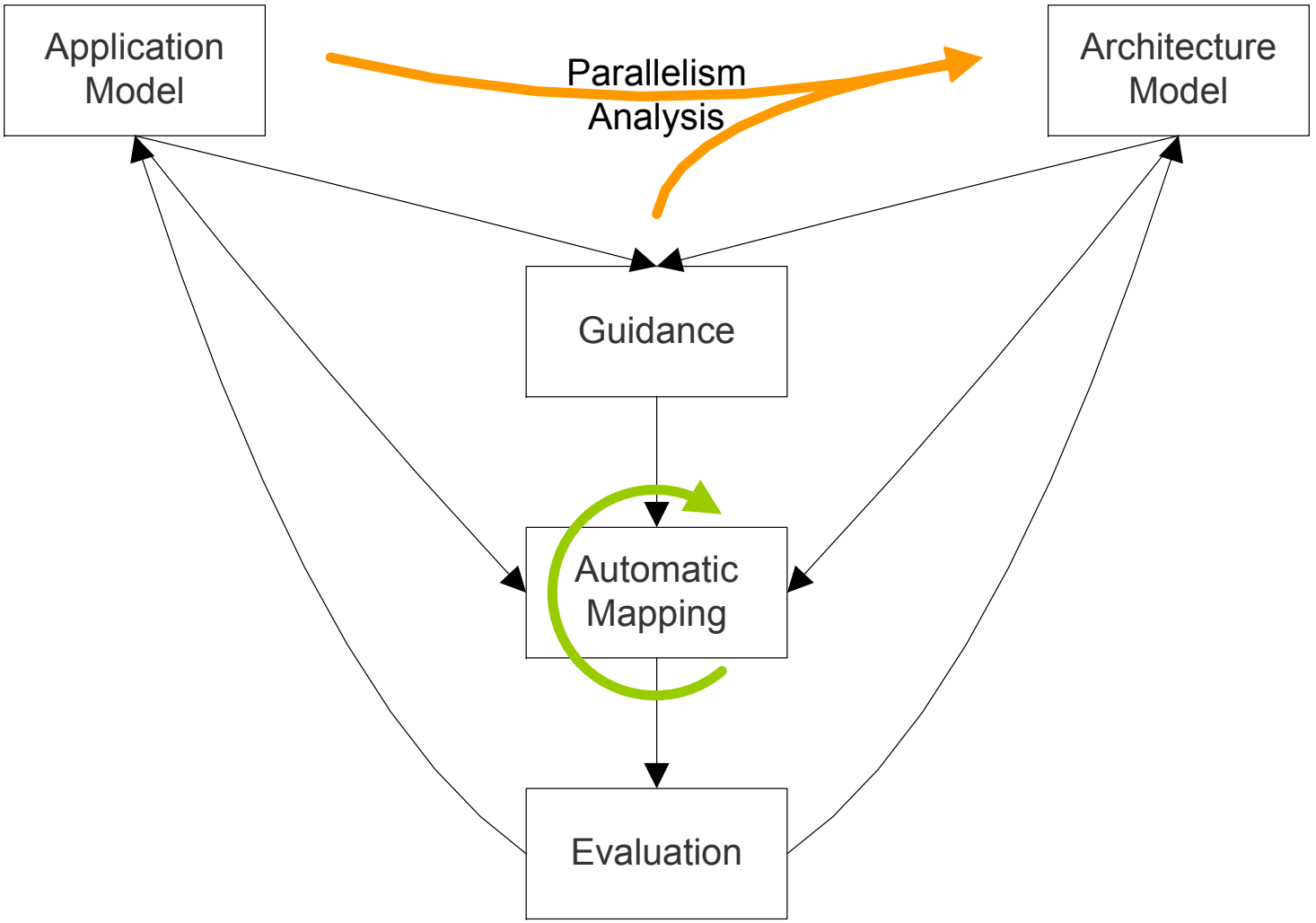
The Tomahawk MPSoC (13 cores, 6 core types)

Challenge: Number of cores ↑, number of core types ↑

→ Number of possible systems ↑ ↑ ↑

→ Fast performance evaluation required

Design Space Exploration Approach



Assumptions / Prerequisites

Given

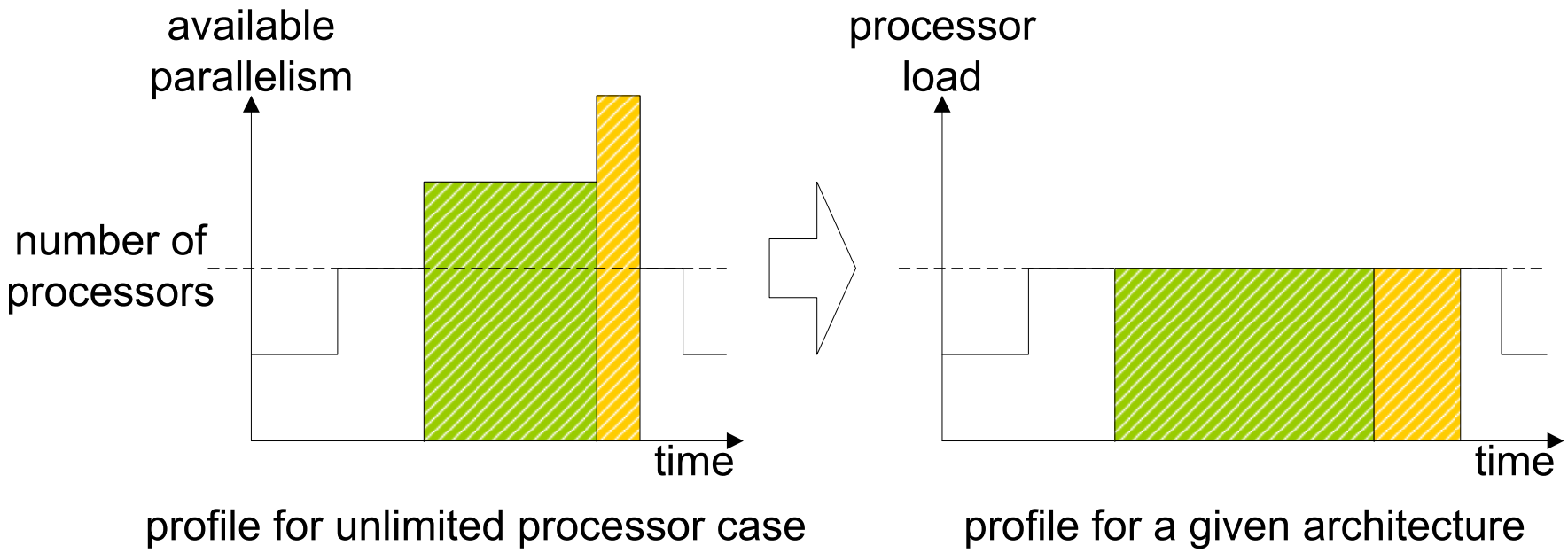
- Task graph
- Performance figures for tasks

Assumptions

- Tasks free of side effects
- Mapping to processor ***type*** given

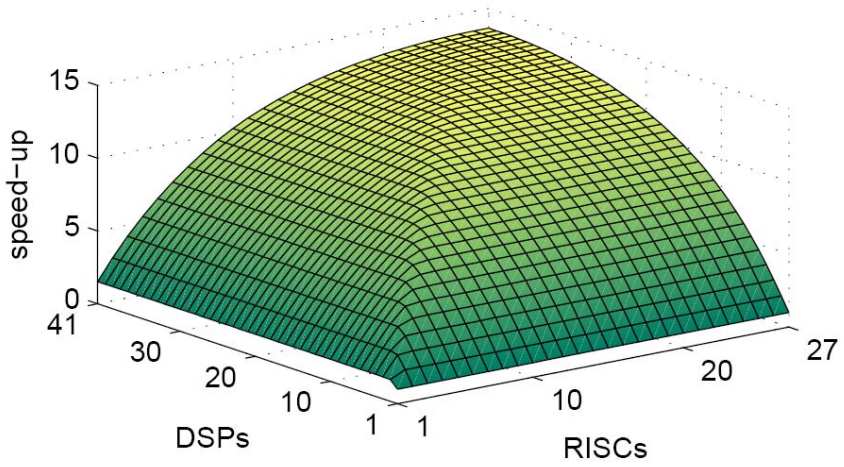
Performance Estimation Principle

Using parallelism profiles for performance estimation

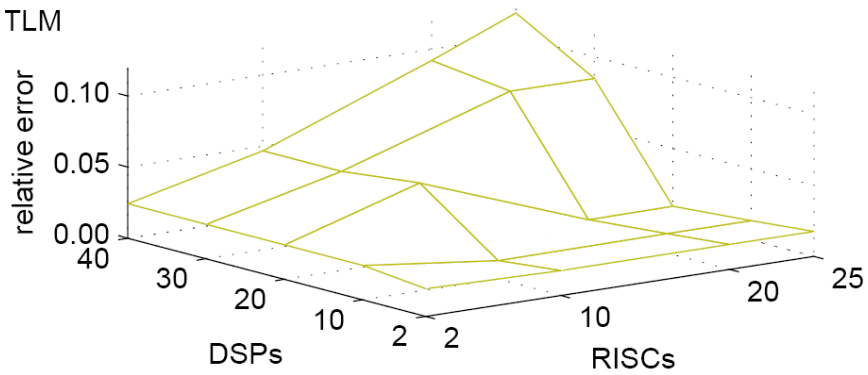


Exemplary Results w/ TGFF

Example: 1000 tasks and 2 core types



relative speed-up curve



estimation error compared to TLM simulation

Estimation vs. Compiler

Target architecture: SAMIRA SIMD VLIW DSP

	blocks	instructions	rel error
iirserial	7	71	0.02
firserial	7	95	-0.11
firparallel	9	131	-0.06
iirparallel	9	140	-0.03
lmsserial	16	194	0.07
dct2d88	74	1018	-0.07
fft648	51	1090	-0.11
fft1288	59	1316	-0.11
fft2568	78	703	-0.11