Y1 review
Brussels, January 23rd, 2009

Network of Excellence

NoE Scientific Management

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SEVENTH FRAMEWORK PROGRAMME

Concepts and Objectives – Main Ideas

Main Idea 1

Embedded systems are essential to ensuring a leading position for Europe in key industrial sectors services.
This is well-recognized in the ICT FP7 priorities, and through the ARTEMIS ETP.

Main Idea 2

Embedded systems design is an emerging scientific discipline, mobilizing a large international community, around a set of fundamental challenging and multi-disciplinary problems.

For this discipline to emerge, a considerable focused research effort by the best teams is needed.

Objectives

Reinforce and strengthen scientific and technological excellence in Embedded Systems Design:

- The NoE acts as a Virtual Center of Excellence
- **Two levels** of integration
  to create critical mass from selected European teams
  - **Strong integration** within selected topics
    by assembling the best European teams,
    to advance the state of the art in the topic.
  - Integration **between** topics
    to achieve the multi-disciplinary excellence and skills required for the development of future embedded technologies.
- Integration is around a Joint Programme of Activities

Core Participants (1/2)

N°	Beneficiary name	Beneficiary short name	Country
1	UJF FILIALE	FLORALIS	France
2	UNIVERSITE JOSEPH FOURIER GRENOBLE 1	UJF/VERIMAG	France
3	RHEINISCH-WESTFAELISCHE TECHNISCHE HOCHSCHULE AACHEN	AACHEN	Germany
4	AALBORG UNIVERSITET	AALBORG	Denmark
5	UNIVERSIDADE DE AVEIRO	AVEIRO	Portugal
6	ALMA MATER STUDORIUM - UNIVERSITA DI BOLOGNA	BOLOGNA	Italy
7	TECHNISCHE UNIVERSITAET BRAUNSCHWEIG	TUBS	Germany
8	UNIVERSIDAD DE CANTABRIA	CANTABRIA	Spain
9	COMMISSARIAT À L'ENERGIE ATOMIQUE	CEA	France
10	DANMARKS TEKNISKE UNIVERSITET	DTU	Denmark
11	UNIVERSITAET DORTMUND	DORTMUND	Germany
12	ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE	EPFL	Switzerland
13	EMBEDDED SYSTEMS INSTITUTE	ESI	Netherlands
14	EIDGENOESSISCHE TECHNISCHE HOCHSCHULE ZUERICH	ETH Zurich	Switzerland
15	INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM VZW	IMEC	Belgium
16	INSTITUT NATIONAL DE RECHERCHE EN INFORMATIQUE ET AUTOMATIQUE	INRIA	France

Core Participants (2/2)

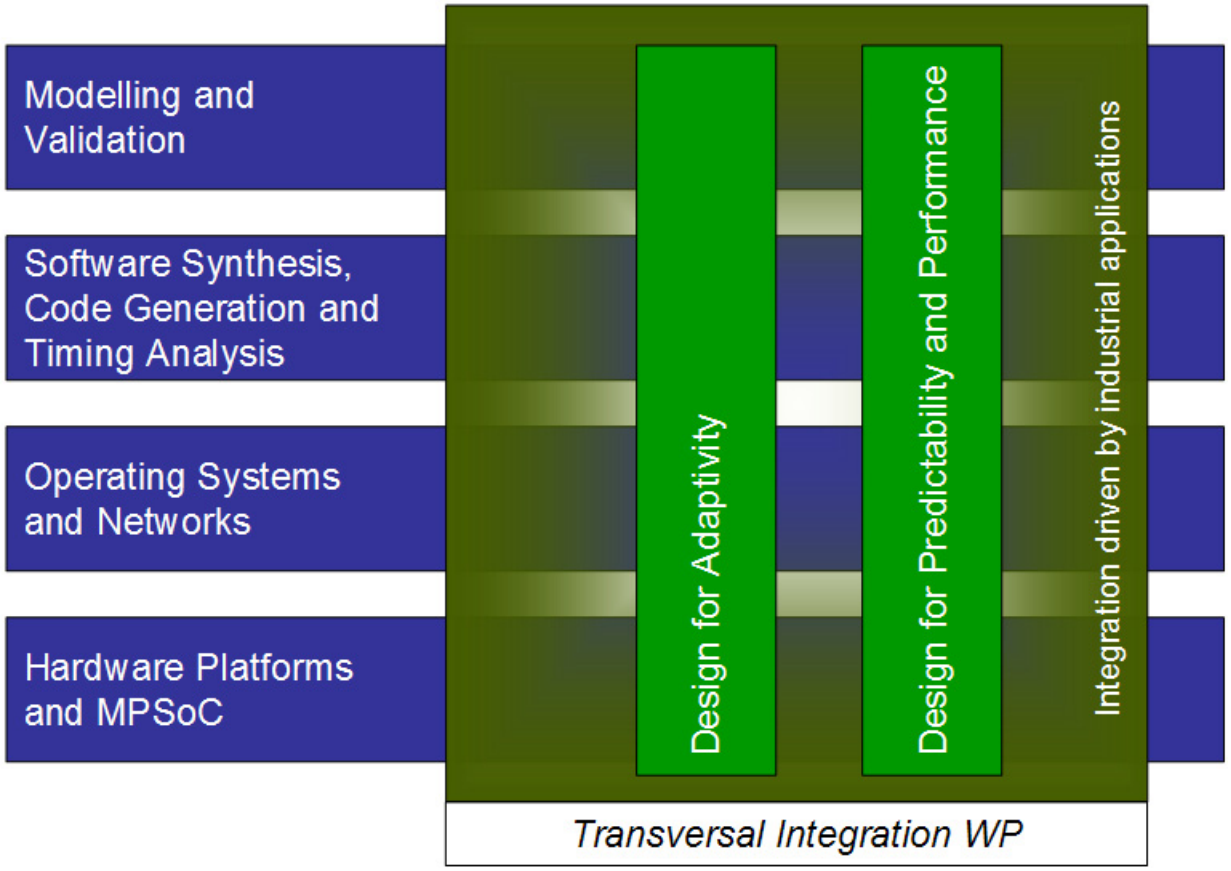
N°	Beneficiary name	Beneficiary short name	Country
17	TECHNISCHE UNIVERSITAET KAISERSLAUTERN	TUKL	Germany
18	KUNGLIGA TEKNIKA HOGSKOLAN	KTH	Sweden
19	LINKÖPINGS UNIVERSITET	LINKOPING	Sweden
20	LUNDS UNIVERSITET	ULUND	Sweden
21	MAELARDALENS HOEGSKOLA	MDH	Sweden
22	OFFIS E.V.	OFFIS	Germany
23	PROJECT FOR ADVANCED RESEARCH OF ARCHITECTURE AND DESIGN OF ELECTRONIC SYSTEMS	PARADES	Italy
24	UNIVERSITAET PASSAU	PASSAU	Germany
25	SCUOLA SUPERIORE DI STUDI UNIVERSITARI E DI PERFEZIONAMENTO SANT'ANNA	SSSA-PISA	Italy
26	INSTITUTO SUPERIOR DE ENGENHARIA DO PORTO	PORTO	Portugal
27	UNIVERSITAET DES SAARLANDES	SAARLAND	Germany
28	UNIVERSITAET SALZBURG	PLU-SALZBURG	Austria
29	UPPSALA UNIVERSITET	UPPSALA	Sweden
30	TECHNISCHE UNIVERSITAET WIEN	VIENNA	Austria
31	UNIVERSITY OF YORK	YORK	UK

Jointly-executed Programme of Research Activities (JPRA)

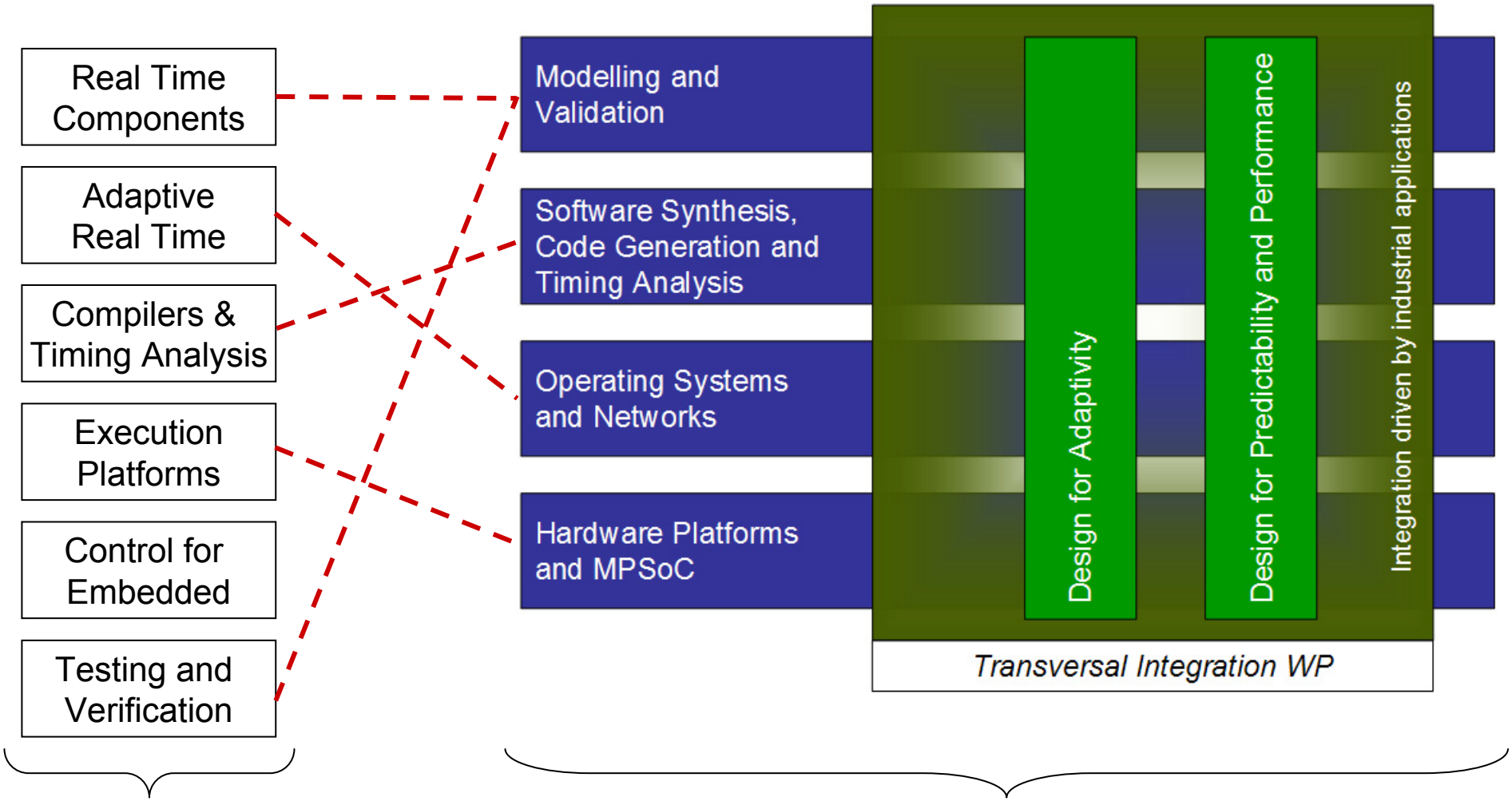
Clusters are autonomous entities, with specific objectives, teams, leaders, and a dedicated yearly budget.

The set of Thematic Clusters cover all the main topics in Embedded Systems Design. The thematic activities in the Transversal Integration workpackage focus on Design methodologies, with specific objectives (Predictability, Adaptivity).

Each cluster may have one or several Activities, as appropriate.



Evolution: tighter integration in ArtistDesign



Theory, Methods and Tools for ES Design

Design flow involves topics leading from initial requirements to a final implementation satisfying them. The objective is to study specific needs for these design activities, as well the possibility of integrating them in a coherent design flow.

We distinguish four essential topics, for which existing techniques should be adapted and extended :

Modelling and Validation: We need formal modelling techniques that take into account the characteristics of a system's external and execution environments. These techniques should support component-based construction for heterogeneous components to be applicable throughout the design process. For embedded systems, validation focuses on testing and verification of non functional properties, including performance and dependability.

Software Synthesis, Code Generation and Timing Analysis: Strong integration should be sought for these interrelated topics. The aim is to study and implement resource-aware synthesis and code generation techniques. These techniques allow the generation of an implementation meeting given user requirements from a functional description of an application (e.g. application software) and a model of a target platform.

Real-Time Operating Systems Scheduling and Networks: The aim is to develop theory methods and tools for new real-time software infrastructures, for the execution and communication between embedded applications. The main problems include adaptive resource management and dependability techniques, in particular to improve robustness to deviations from nominal conditions.

Platforms and MPSoC Design: The aim is implementation of complex applications on multi-core HW platforms. It raises a number of problems for ensuring predictability and efficiency. These include adaptive techniques for resource management, and the study of reliable programming models for multi-core architectures.

Long Term Integration

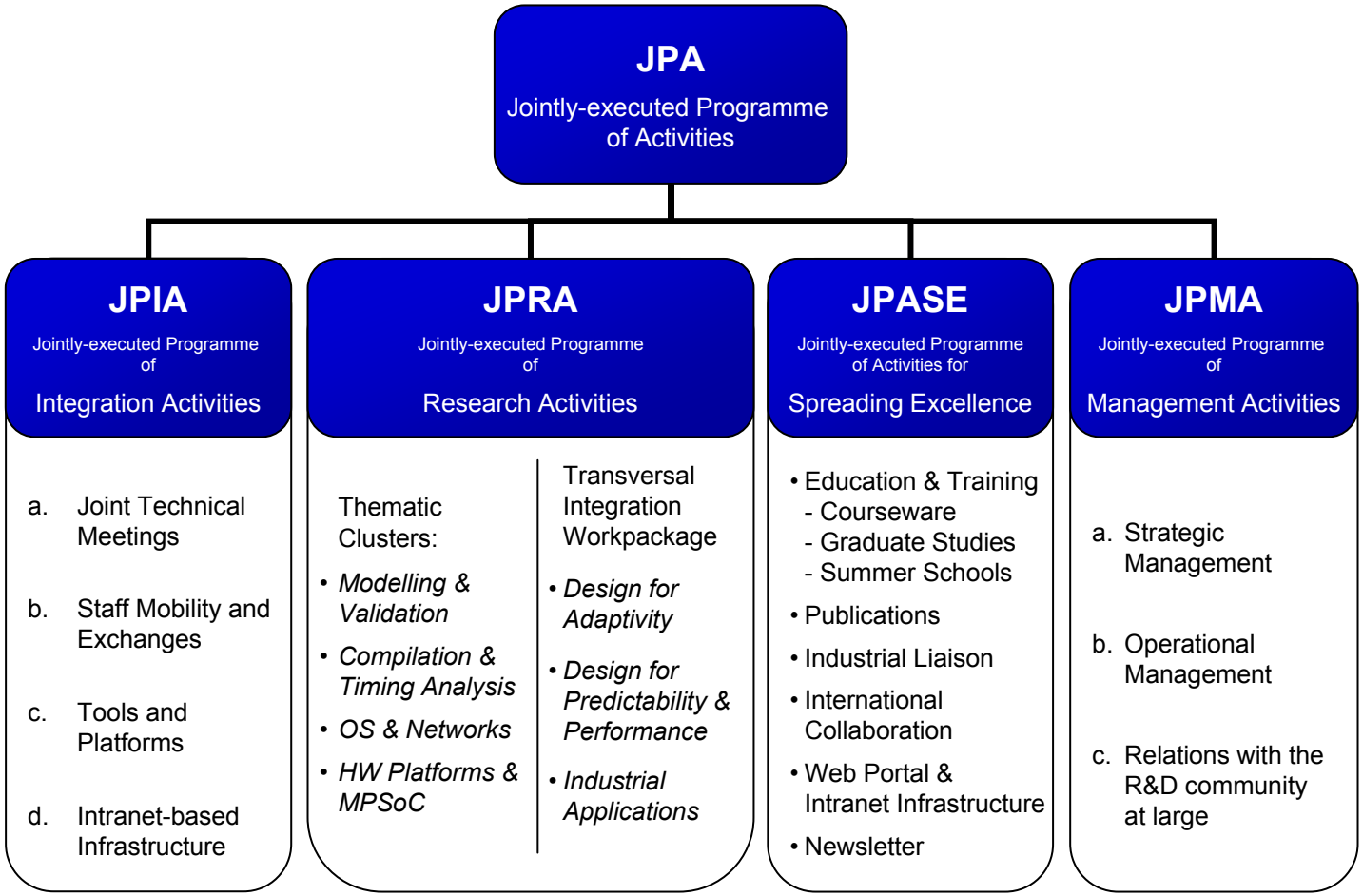
Embedded systems design is a multidisciplinary area requiring competences from hardware engineering, operating systems and networks, programming and compilation, modelling and software engineering, control engineering. The ArtistDesign NoE gathers together leading European teams from all these areas.

ArtistDesign continues and extends these activities, both quantitatively and qualitatively. In setting up the consortium, we have the right balance between critical mass, excellence, and commitment from the core partners.

- **Critical Mass**
  We have a sufficient number of partners, to achieve a fair coverage of the main topics in the area, as well as the capacity to impact the European research landscape. Nonetheless, to ensure efficiency, we have limited the number of core partners, based on previous experience. At the same time, our impact is amplified through the large number of affiliated academic, SME, industrial, and international collaboration partners.
- **Excellence**
  The ArtistDesign core partners include the main European leading teams, as attested by their leadership in their respective areas, as well as their strong involvement in national and European projects and initiatives.
- **Commitment**
  The majority of the ArtistDesign core partners were already involved as core partners in the Artist2 NoE. They have demonstrated a high degree of investment to achieve the workprogramme objectives, by committing the resources needed, which are an order of magnitude larger than those provided by the NoE financing. We estimate that the effort for implementing the JPA is roughly 10 times the financial contribution for integration.

Joint Programme of Activities

ArtistDesign acts as a Virtual Centre of Excellence, composed of a set of virtual teams, called clusters. Each cluster gathers together selected teams from partners, to create the critical mass and expertise in one of the essential topics for embedded systems design.



Jointly-executed Programme of Management Activities (JPMA)

In order to ensure correct integration and coordination of activities, and coordination between the partners, the Consortium carries out a Joint Programme of Management Activities (JPMA). It includes:

- **Strategic Management**
  The Strategic Management Board (SMB) plays a key role in ensuring ongoing integration at 3 levels: I) within the cluster; II) between clusters; III) with the larger European Embedded Systems Design community.
- **Operational Management**
  is ensured by the ArtistDesign Office, and the Executive Management Board (composed of the Cluster Leaders). The ArtistDesign Office ensures that all aspects of the NoE are running smoothly, and that progress is made towards the overall NoE objectives. It is composed of the Scientific Coordinator, the Technical Coordinator, the Financial and Administrative Coordinator from Floralis.
- **Relations with the R&D community at large**
  The NoE has a very strong presence within the embedded systems design community, at all levels. High-level interaction with the main institutions and bodies such as ARTEMIS/ARTEMISIA, professional organisations such as ACM TECS, NSF, DARPA, large conferences, are ensured and supported by various members of the Strategic Management Board, and the Scientific and Technical Coordinators.

Jointly-executed Programme of Integrating Activities (JPIA)

Each ArtistDesign research activity has work within both the JPIA and the JPRA workpackages. Funds for staff mobility are allocated by taking into account the needs for research.

- **Joint Technical Meetings**
  Present, discuss and integrate the ongoing work, and exchange points of view with other teams. They also serve to identify future work directions.
- **Staff Mobility and Exchanges**
  Mobility is justified by and refer to involvement in an activity from the JPRA or JPIA, or one of the following: co-funded scholarships with industry; exchange of students and personnel within the consortium.
- **Tools and Platforms**
  Research platforms lay the groundwork for the JPRA, allowing common research to occur and capitalisation on research results. Platforms are used as the basis for transfer of research results to industry. Some of these have international visibility, and the ambition is for these to serve as world-wide references in their respective topics.

Joint Programme of Activities for Spreading Excellence (JPASE)

These NoE-level activities serve as a relay between the NoE and the international embedded systems design community at large.

- **Education and Training**
  These actions serve as incubators for developing integrated curricula and materials, and to disseminate results and spread excellence well beyond the partners and affiliated partners of ArtistDesign.

- **Publications in Conferences and Journals**
  Implemented through publication in the main conferences on Embedded Systems Design of the area, as well as the active participation for the organization and management of these events.

- **Industrial Liaison**
  This consists of actions oriented towards affiliated industrial partners, to transfer results follow and get feedback on the research and integration activities in the JPA (JPRA, JPIA).

- **International Collaboration**
  These activities play a dual role: showcase the participants' results, and reinforce the NoE's leadership role worldwide. They will also collect relevant information about evolution of the state of the art outside Europe.

- **Web Portal**
  This plays a key supporting role for collaboration and Integration, such as interaction between clusters, management information, such as scholarships, internal events, and progress of the work. The web portal will also be used to disseminate any relevant information to the community at large, and be an essential mechanism for achieving integration and recognition.

JPASE: Extensions to the Web Portal

With respect to the Artist2 web infrastructure, the following improvements and extensions will be implemented to the publicly accessible Web Portal:

- **Calendar of Events**
  A calendar-based view of events in the area will be implemented.

- **Interface with Google Maps**
  An interface based on Google Maps would be provided, showing where the main activities per topic are located. This would cover labs in Europe as well as our International Collaboration partners.

- **Announcements archive**
  The current Artist Mailing List would be expanded, to include automatic archiving, and availability via the Artist Web Portal.

Workpackages

WP0	Jointly-executed Programme of **Management** Activities (JPMA)	MGT	Floralis
WP1	Jointly-executed Programme of **Integration Activities** (JPIA)	RTD	UJF/ VERIMAG
WP2	Joint Programme of Activities for **Spreading Excellence** (JPASE)	OTH ER	UJF/ VERIMAG
WP3	Thematic Cluster: **Modeling and Validation** (JPRA) • *Activity: Modelling* • *Activity: Validation*	RTD	Aalborg
WP4	Thematic Cluster: **Software Synthesis, Code Generation and Timing Analysis** (JPRA) • *Activity: Software Synthesis, Code Generation* • *Activity: Timing Analysis*	RTD	Dortmund
WP5	Thematic Cluster: **Operating Systems and Networks** (JPRA) • *Activity: Resource-Aware OS* • *Activity: Scheduling & Resource Mgt* • *Activity: Embedded RT Networking*	RTD	Pisa
WP6	Thematic Cluster: **Hardware Platforms and MPSoC** (JPRA) • *Activity: Platform and MPSoC Design* • *Activity: Platform and MPSoC Analysis*	RTD	DTU
WP7	**Transversal Integration** (JPRA) • *Activity: Design for Adaptivity* • *Activity: Design for Predictability and Performance* • *Activity: Integration Driven by Industrial Applications*	RTD	PARADES

Thematic Cluster: # Modeling and Validation

cluster leader: Kim Larsen (Aalborg – Denmark)

JPRA Activity: "Modeling"

Suzanne Graf (Verimag - France)

Develop model- and component-based theories, methods, and tools that establish a coherent family of design flows spanning the areas of computer science, control, and hardware. Simultaneously address software, hardware resources, and the physical environment, in a quantitative manner. In order to gain independence from a particular target platform, embedded system design must be model-based. In order to scale to complex applications, embedded system design must be component-based.

JPRA Activity: "Validation"

Kim Larsen (Aalborg - Denmark)

Designing scalable techniques allowing for efficient and accurate analysis of performance and dependability issues with respect to the various types of (quantitative) models considered, covering a range of model-based validation techniques ranging from simulation, testing, model-checking, compositional techniques, refinement and abstract interpretation.

Thematic Cluster:

Software Synthesis, Code Generation and Timing Analysis

cluster leader:
Peter Marwedel (Dortmund – Germany)

JPRA Activity: "Software Synthesis, Code Generation "

Peter Marwedel (Dortmund - Germany)

Software generation has evolved to a level where compilers are key components, but not the only components that are useful for generating executable code. New models of computations such as data-flow based models aim at avoiding the well-known disadvantages of imperative programming styles. It can also be expected that the link between software engineering and embedded systems will become stronger.

JPRA Activity: "Timing Analysis"

Björn Lisper (Mälardalen - Sweden)

Timing analysis of MPSoC systems is a new scientific field, and is very timely from an application perspective as MPSoC and Multicore architectures rapidly are becoming mainstream. A research effort in this area will thus establish European dominance in a field that rapidly is becoming very important.

Thematic Cluster:

Operating Systems and Networks

cluster leader:
Giorgio Buttazzo (Pisa - Italy)

JPRA Activity: "Resource-Aware Operating Systems" *Giorgio Buttazzo (Pisa - Italy)*

Investigate how RTOS have to be extended or modified to support emerging RT embedded systems (high complexity, highly variable resource requirements and parallel processing). Hence, another objective is to investigate kernel mechanisms that can efficiently manage the available resources, taking multiple constraints into account, while guaranteeing isolation properties.

JPRA Activity: "Scheduling and Resource Management" *Alan Burns (York - UK)*

Provision of models of embedded platform resources and policies, and the necessary analysis for undertaking the run-time scheduling of these resources and policies. A key scientific challenge is to link this resource-centred analysis with models of the application (and their resource usage policies) and the performance profiles of the hardware platform itself.

JPRA Activity: "Real-Time Networks" *Luis Almeida (U. Aveiro – Portugal)*

This activity addresses numerous research challenges in the frameworks of Networked Embedded Systems (NESs), Wireless Sensor Networks (WSNs) and Mobile Ad-hoc Networks (MANETs).

Thematic Cluster:

Hardware Platforms and MPSoC

cluster leader:
Jan Madsen (DTU - Denmark)

JPRA Activity: "Platform and MPSoC Design"

Luca Benini (U. Bologna - Italy)

The main scientific challenges addressed in this activity are focused on how to map complex applications onto multi-core hardware platforms. This includes addressing allocation and scheduling issues like: scalability, flexibility, composability, predictability, design-time reduction and increased dynamism. The problem is complex and multi-faceted. On one hand, we have static (design/compile time) approaches, where applications are analyzed and optimal mapping decisions are taken before the platform is deployed in the field. On the other hand, we have dynamic, runt-time approaches where mapping decisions are taken online, and they are triggered by environmental and workload variations.

JPRA Activity: "Platform and MPSoC Analysis"

Jan Madsen (DTU - Denmark)

Establish a set of models and analysis methods that scales to massively parallel and heterogeneous multiprocessor architectures, is applicable to distributed embedded systems as well, allows for the analysis of global predictability and efficiency system properties and takes the available hardware resources and the corresponding sharing strategies into account.

Transversal Integration

cluster leader:
Alberto Sangiovanni (PARADES - Italy)

JPRA Activity: "Design for Adaptivity"

Karl-Erik Årzén (Lund University – Sweden)

An embedded hardware-software system is adaptive, if it can modify its behaviour and/or architecture to changing requirements. Adaptivity is increasingly important as the complexity and autonomy of embedded systems increases. Adaptivity is required both off-line at design-time and on-line at run-time. Off-line adaptivity is required to handle changing system specifications and to support platform-based or product-family based development.

JPRA Activity: "Design for Predictability and Performance"

Bengt Jonsson (Uppsala - Sweden)

The technical achievements contribute to a suite of techniques across the abstraction levels of embedded system design, including application modelling and analysis, scheduling support, compilers, and platform design techniques. The achievements will also entail interfacing of existing tools for design of embedded systems.

JPRA Activity: "Integration Driven by Industrial Applications"

Alberto Sangiovanni (PARADES - Italy)
Ed Brinksma (ESI - Netherlands)

The ultimate goal of this activity is to provide the "meta rules" according to which the design transformations are carried out and interfaces are built and hence to provide strong guidance to the clusters to make their results more relevant and applicable.

Budget

7% **WP0: Jointly-executed Programme of Management Activities (JPMA)**

36% **WP1: Jointly-executed Programme of Integration Activities (JPIA)**
- 12% Transversal Integration
- 6% Each Thematic Cluster

12% **WP2: Joint Programme of Activities for Spreading Excellence (JPASE)**

9% **WP3: JPRA/Thematic Cluster: Modeling and Validation**
- Activity: Modelling
- Activity: Validation

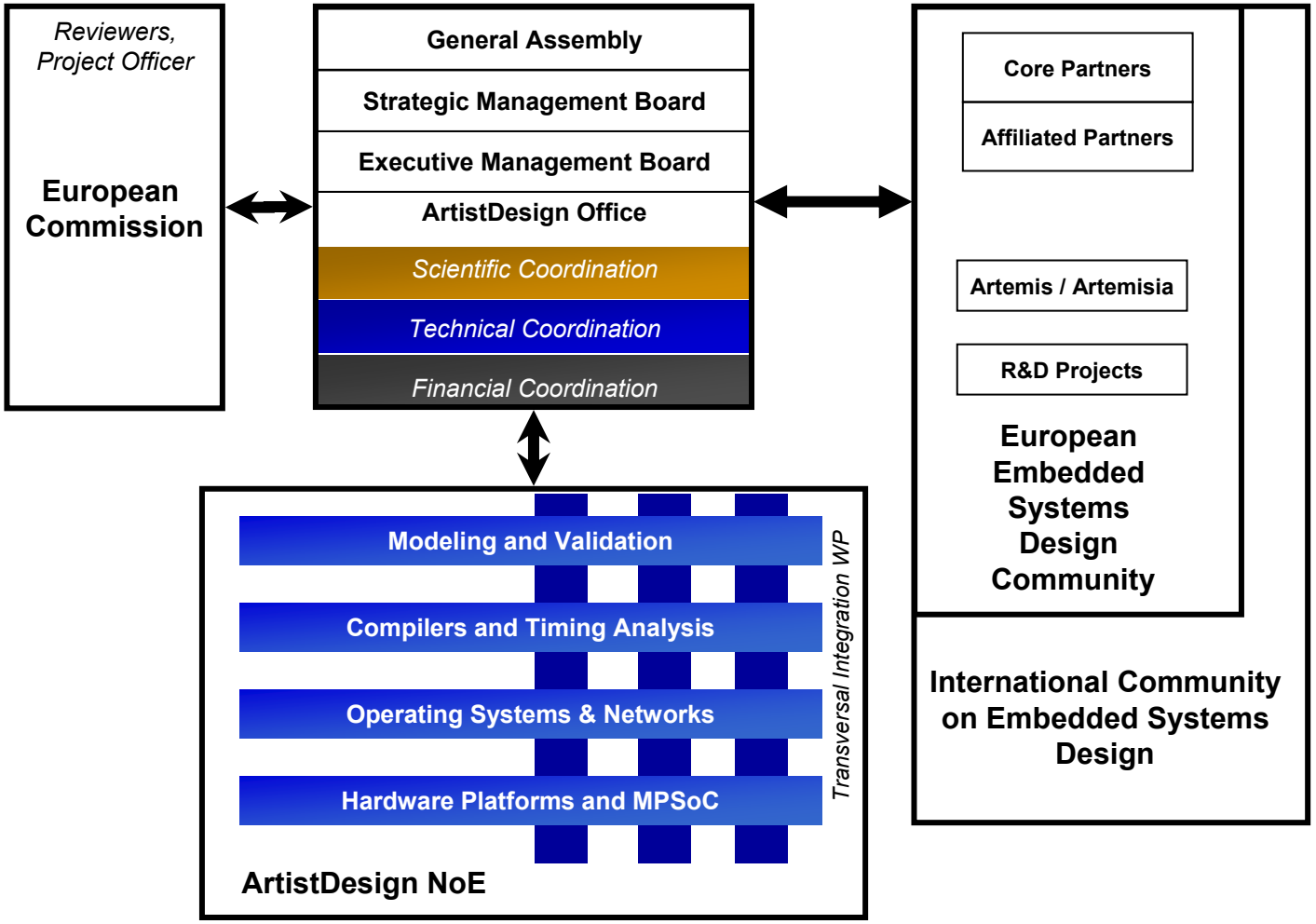
9% **WP4: JPRA/Thematic Cluster: Compilers and Timing Analysis**
- Activity: Software Synthesis and Code Generation for Embedded Systems
- Activity: Timing Analysis

9% **WP5: JPRA/Thematic Cluster: Operating Systems and Networks**
- Activity: Real-Time Operating Systems
- Activity: Scheduling and Resource Management
- Activity: Embedded Real-Time Networking

9% **WP6: JPRA/Thematic Cluster: Hardware Platforms and MPSoC**
- Activity: Execution Platform and MPSoC Analysis
- Activity: Platform and MPSoC Design

9% **WP7: Transversal Integration Activities**
- Activity: Design for Predictability
- Activity: Design for Adaptivity
- Industrial Integration

Management Structure



Management of the NoE

We believe that the current two-tiered Management structure - dividing the management amongst cluster leaders and the Strategic Management Board composed of both cluster leaders and a limited number of other selected prominent core partners – has been the right one for managing such a large research entity.

It provides the right combination of flexibility and accountability, while leaving room for innovation and evolution.

These “best practices” were initiated in Artist2, and continue in ArtistDesign. The partners are working well and efficiently together to achieve the aims.

Executive Summary

Y1 Activity Report

Modeling and Validation: Modeling

Significant achievements on Component-based Modeling:

- Work by INRIA, PARADES, and VERIMAG, on the theory of tagged systems provides conditions for correct implementation of synchronous systems on “less synchronous” architectures.
- Work by INRIA on new models of computation, the Kahn-extended Event Graph (KEG), which adds “static control” in the Model of Computation of Marked Graphs.
- Work on the BIP component framework, introduces a notion of expressiveness for component-based formalisms, which provides a basis for their comparison. This notion drastically differs from the usual one, as it takes into account the expressive power of composition operators (glue operators).

Significant progress has been achieved in methods for distributed implementation of non-distributed specifications.

- VERIMAG studied a method for the automatic generation of distributed implementations of BIP models.
- INRIA, PARADES and VERIMAG studied the concept of loosely time-triggered architectures, implementing time-triggered architectures. Finally, fully asynchronous implementations of synchronous systems have been studied.
- Other results on distributed implementations include reliability, new heuristics in scheduling for reliability, design of communication architectures and time-triggered system-on-chip architectures.

Modeling and Validation: Validation

Significant results on Interfaces and Compositionality:

- Development of interface theories supporting component reuse (EPFL).
- Contract-based verification techniques for the heterogeneous rich component (HRC) model (INRIA, PARADES, VERIMAG), in the framework of the SPEEDS project.
- ETHZ and Uppsala propose modular performance analysis techniques, based on the real-time calculus and timed automata.
- VERIMAG has continued the work on compositional deadlock verification of BIP programs, and its implementation in the DeadlockFinder tool.

On qualitative validation, work has been carried out in the following directions:

- Significant contributions to game-theoretic approaches to real-time system testing.
- Games for different extensions of timed automata such as weighted timed automata, priced timed automata, multi-priced timed automata.
- Extended and improved the functionality of the UPPAAL tools, including the use of slicing techniques for model optimization as well as features supporting interface theory for real-time systems.
- Studied quantitative testing techniques. In particular, we have developed a theory allowing testing of systems in the presence of measurement imprecisions.
- Studied quantitative model checking techniques for timed models, including timed automata, linear hybrid automata and general non-linear hybrid systems.
- Studied compositional synthesis and verification techniques. These include modular supervisory control, as well as the verification of component-based systems.

SW Synthesis, Code Gen. and Timing Analysis: SW Synthesis and Code Generation

- Studied the influence of scratchpad memory allocation techniques on worst case execution times (WCET). First experiments show WCET reductions of more than 50% for several benchmarks.
- Investigated WCET-aware register allocation techniques, by extending existing techniques based on graph colouring.
- Continued work on scalable source-level analysis and annotation-based timing analysis methods. This allows a significant increase in productivity, by requiring the user to annotate the relevant timing information that cannot be automatically computed.
- Studied polyhedral loop parallelisation techniques for multi-core systems.

Regarding tools and platforms, we developed work in the following directions:

- Designed a Static Loop Analyzer, allowing to estimate loop iteration bounds.
- Demonstrated the applicability of the analyser on benchmarks taken from the benchmark suites MRTC, DSPStone, MiBench, UTDSP and MediaBench. Our loop analyser was the only tool able to answer all questions related to flow fact during the WCET tool challenge 2008.
- Developed a new WCET-aware procedure positioning and cloning technique. The compiler optimisations obtained were exploited for WCET reduction. Results on real-world benchmarks show WCET reductions of 10% on average, while ACET is reduced by 2 on average.
- Continued the cooperation between ACE and Aachen on the retargetable code optimizations. The conditional execution engines have been extended by a strong retargeting formalism.

SW Synthesis, Code Gen. and Timing Analysis: Timing Analysis

Theory

- Studied a notion of time predictability of cache architectures, which is the first precise notion found in the literature. Four different cache replacement strategies were compared and the LRU strategy was found to be optimal. This research is related to work within the PREDATOR FP7 project, which attempts to reconcile performance and predictability.
- Studied Timing anomalies, where local worst-case choices may not lead to the global worst-case scenario, is essential for time predictability. We have studied techniques for handling timing anomalies for efficient WCET analysis, as well as for measuring the impact of timing anomalies on WCET analysis.

Other work on Timing Analysis includes:

- Parametric Timing Analysis, where some parameters of the program can remain unknown until execution.
- Developed Timing Analysis techniques, in collaboration with BOSCH, taking into account operating modes of programs, computed semi-automatically.
- Developed WCET analysis for systems with preemptive scheduling.

Tools

- Work on the AIR format has continued. The format was extended and adapted to the needs of the partners. The attribute database was extended with new attributes.
- We also worked on the development and improvement of formats for ensuring the interoperability of the tools. The work on formats includes ALF for computation semantics representation, conversion of the ABSINT AIR format to SWEET format, and the definition of common flow description attributes.
- As was the case last year, the WCET Challenge 2008 consisted of a set of benchmark programs and analysis tasks to be performed by the contestants. http://www.artist-embedded.org/artist/-WCET-08-.html

Operating Systems and Networks

Resource-aware Operating Systems

In addition to work done in Artist2, we developed work in the following directions:

- Modeling and analysis of control-driven tasks. The standard design of control is based on the periodic sampling. We studied a model which saves a considerable amount of computational resources which samples the inputs when needed.
- Implementation of a flexible scheduling framework called FRSH that is capable of handling multiple concurrent activites with different criticality and timing in the same system. The framework has been designed to be implemented on different platforms.
- ERIKA support for the EasyBee radio transceiver has been developed.
- We studied issues relating to the operating system support needed by advanced users of a real-time specification for Java. In particular, two issues have been addresses: how to handle systems that contain a large number of events; and how to measure blocking time.

Operating Systems and Networks

Scheduling and Resource Management

We have had a large volume of activity on this topic:

All the partners, under the leadership of York, have worked for establishing a taxonomy of resource usage. The taxonomy distinguishes between different classes of resources - each class being subdivided into a number of resource types.

The architectural model of a Flexible Scheduling Framework developed in the FRESCOR and FIRST EU-IST projects has been extended to include a contract model. Contracts represent complex requirements of the applications which can be managed by the underlying system to provide the required level of service.

Several activities on scheduling, in particular multi-resource scheduling for multi-core platforms, schedulability for CAN-based control applications, sensitivity analysis, flexible scheduling on low-cost microcontrollers.

Other work related to the Transversal Activity: “Design for Adaptivity” has been carried out, including dynamic runtime adaptability, optimal period selection and scheduling for embedded controllers.

Operating Systems and Networks

Real-Time Networks

We have carried out work on:

- Analysis techniques, including Worst Case analysis and dimensioning of cluster-tree Wireless Sensor Networks, as well as analysis for specific networks.
- We studied techniques for supporting real-time communication and QoS for Wireless Sensor Networks. These include work around the use of IEEE 802.15.4 and ZigBee as federating communication protocols for Wireless Sensor Network applications, as well as supporting real-time communication of the Erika real-time operating system.
- We have also furthered work, started in Artist2, on student design competitions in the scope of the IEEE Real Time Systems symposium.

Hardware Platform and MPSoC Design

Platform and MPSoC Design

- Study of system design methodologies handling the dynamic nature of embedded systems and allowing predictability and optimal use of resources.
- Bologna, with ETHZ, has studied optimalisation-centric MPSoC design techniques. The main goal of this work was to establish a common understanding of the MPARM framework developed in Bologna, and the DOL framework developed at ETHZ.
- Bologna and Linkoping have studied a temperature power-optimization system. A temperature-aware dynamic voltage selection technique has been developed for energy minimisation.

- Design optimization for fault-tolerant distributed embedded systems is developed by Linkoping and DTU.
- Bologna and ETHZ have improved the design of a scavenger prototype, to perform automatic maximum power point tracking.

- Studied programming models for MPSoC architectures as well as investigated the hardware/software interface between the processing elements and the interconnect network.
- Studied a component-based service model for early design space exploration and performance estimation.

Hardware Platform and MPSoC Design

Platform and MPSoC Analysis

Focus on modelling and performance analysis for multi-processor and/or networked systems.

- Techniques for performance estimation of distributed real-time systems, based on simulation, in particular for applications using heterogeneous task scheduling policies. We also studied performance analysis techniques for a MPSoC in collaboration with ST Microelectronics.
- Studied relations between simulation-based and analytical methods for performance evaluation of distributed real-time systems. Based on experimental simulation results, we were able to draw interesting conclusions regarding the pessimism of formal approaches. The experiments were performed on FlexRay and CAN-based distributed systems.
- Studied interesting relations between MPA (Modular Performance Analysis) and Timed Automata.
- Extended the fault-tolerant process model, to consider a combination of hardware and software fault-tolerant techniques. We have proposed a method for computing the reliability of a system, taking into account: a) hardening levels in hardware; b) the re-execution levels in software; c) scheduling for sharing recovery slacks.
- Studied scheduling-based energy optimisation techniques for energy-scavenging wireless sensor networks.

Design for Adaptivitty (Transversal Integration activity)

- Studied a symbolic quality control technique for multi-media applications. Adaptivity is ensured by using a controller, which monitors system execution and adapts quality parameters of its functions so as to meet hard real-time constraints.
- Studied adaptive energy management techniques in clusters of wireless sensor nodes. They allow tuning the application parameters according to the time-varying amount of harvested energy.
- Studied a reference architecture for self-configuring embedded systems in collaboration with Volvo. Algorithms suitable for runtime configuration management, load balancing, and quality of service have been developed and adapted to automotive applications.
- Designed adaptive techniques to enhance real-time support of IEEE 802.11.e networks. For such networks, we developed protocols to enhance the resilience to interference, and to provide an estimation of a relative localisation based on the radio frequency signal.
- Studied techniques allowing the design and performance analysis for multi-mode systems. We also studied online performance analysis techniques for distributed systems. A novel distributed algorithm for control of the global analysis flow has been proposed.
- Contributions in the STREP projects FRESCOR and ACTORS to develop an infrastructure for adaptive scheduling of real-time applications.

Design for Predictability (Transversal Integration activity)

Modeling and Validation of component –based systems

- Studied the concept of predictability in relation with robustness, and identified two major challenges in embedded systems design. These challenges require a rethinking of the conventional, purely discrete and purely functional foundation of computing.
- We worked on modular performance analysis techniques, based on real-time calculus for systems with cyclic dependencies. We integrated a contract-based scheduling framework with a component-based technology.

Timing Analysis and Compiler Techniques

- Work on relations between Timing Analysis and Timing Predictability. A definition of predictability for cache architectures has been proposed, and the relative competitiveness of 4 different cache replacement strategies has been analysed.
- Investigated WCET analysis techniques for cooperative task scheduling. A method guiding developers of an embedded system to select optimal pre-emption points is under development.
- Studied parametric timing analysis techniques that overcome usual limitations of analysis techniques requiring the maximum number of loop iterations to be known statically.

OS/MW/Networks

- Work addressed various issues, including: Integrating scheduling analysis and model checking; influence of abstractions on the schedulability analysis of distributed real-time systems, time-predictable operating systems.

Architecture and System Design

- Studied techniques allowed predictability for fault-tolerant embedded systems and predictability for multi-processor MPSoC architectures.
- Developed a set of parameterisable models of L2 Caches and integrated them in an accurate virtual platform environment.
- Designed a Precision Timed (PRET) architecture based on a reactive processor, coupled with a MicroBlaze general purpose processor.

Industrial Integration (Transversal Integration activity)

- This activity groups a set of industrial interactions and collaborations with ArtistDesign teams. The long-term goal is to understand industrial design methodologies and identify the research results that could be applied in these methodologies.

- The work this year has consisted in organising a few high-profile meetings with industry (eg: Embedded Systems: Industrial Applications ’08) as well as joint workshops and technical meetings.

- At this point, these constitute a rich set of events and interactions, which need to be structured and which need a more specific focus.

Deliverables (1/2)

WP0: Joint Programme of Management Activities (JPMA)

Floralis	D1-(0.1)-Y1	**Project Management Report**
	D2-(0.2)-Y1	Project Activity Report
UJF/Verimag	D2-(0.2a)-Y1	*ch. 1* - **Executive Summary and Overview**
Aalborg	D2-(0.2b)-Y1	*ch. 2* - **Modelling and Validation**
Dortmund	D2-(0.2c)-Y1	*ch. 3* - **SW Synthesis, Code Generation and Timing Analysis**
Pisa	D2-(0.2d)-Y1	*ch. 4* - **Operating Systems and Networks**
DTU	D2-(0.2e)-Y1	*ch. 5* - **Hardware Platforms and MPSoC Design**

WP1: Joint Programme of Integration Activities (JPIA)

UJF/Verimag	D3-(1.0)-Y1	**Integration Activities Report**

WP2: Joint Programme of Activities for Spreading Excellence (JPASE)

UJF/Verimag	D4-(2.0)-Y1	**Spreading Excellence Report**

WP3: Modeling and Validation (JPRA)

EPFL	D5-(3.1)-Y1	**Modelling**
Aalborg	D6-(3.2)-Y1	**Validation**

Deliverables (2/2)

WP4: Software Synthesis, Code Generation and Timing Analysis (JPRA)

Dortmund	D7-(4.1)-Y1	**Software Synthesis, Code Generation**
Saarland	D8-(4.2)-Y1	**Timing Analysis**

WP5: Operating Systems and Networks (JPRA)

Pisa	D9-(5.1)-Y1	**Resource-aware Operating Systems**
York	D10-(5.2)-Y1	**Scheduling and Resource Management**
Aveiro	D11-(5.3)-Y1	**Embedded Real-Time Networking**

WP6: Hardware Platforms and MPSoC (JPRA)

Bologna	D12-(6.1)-Y1	**Platform and MPSoC Design**
DTU	D13-(6.2)-Y1	**Platform and MPSoC Analysis**

WP7: Transversal Integration (JPRA)

Lund	D14-(7.1)-Y1	**Design for Adaptivity**
Uppsala	D15-(7.2)-Y1	**Design for Predictability**
PARADES	D16-(7.3)-Y1	**Integration Driven by Industrial Applications**

Current Results – Integration within the NoE

Within the NoE, we have achieved a strongly integrated community,

- Through joint projects, publications, collaborations
- Recognised internationally that has a significant impact on European R&D on Embedded systems.

Acted to integrate the area of Embedded Systems Design, and promote the emergence of the discipline:

- Organization of major conferences (Embedded Systems Week, Date, RTSS) as well as in IEEE and the ACM.
- International Collaboration activities (high-level meetings and schools)
- Triggering numerous and significant R&D projects (national and European)
- Many teams play a leading role in their own countries, by participating in setting up and leading national centers of excellence and major projects.
- The European embedded systems community is now a reality, through a structured constituency. Active role in ARTEMIS (2 Steering Board members, Contribution to SRA)

Changes to the Consortium

- ESI change of representative
- EPFL transfer to IST Austria (effective Sept 1st)
  Giovanni De Micheli will be the new EPFL representative
  Susanne Graf will lead the Modeling activity
- Aveiro transfer to Porto (effective July 2009)
- PARADES => ASV becomes a consultant

THANK YOU