Year 1 Review
Brussels, January 23rd, 2008

Cluster

Achievements and Perspectives :

Hardware Platforms and MPSoC Design

leader : Jan Madsen

Technical University of Denmark (DTU)

SEVENTH FRAMEWORK PROGRAMME

Cluster Participants

- Jan Madsen (DTU – Denmark)
- Luca Benini (UNIBO – Italy)
- Lothar Thiele (ETHZ – Switzerland)
- Rolf Ernst (TUBS – Germany)
- Petru Eles (LiU – Sweden)
- Stylianos Mamagkakis (IMEC – Belgium)
- Axel Jantsch (KTH – Sweden)
- Thierry Collette (CEA/LIST – France)

- Volvo –Sweden
- SymTAVision – Germany
- Robert Bosch – Germany
- Intel – Germany
- Prevas – Denmark
- Bang & Olufsen ICEpower – Denmark
- Telecom Italia Lab – Italy
- NTUA – Greece
- EPFL – Switzerland
- NTNU - Norway
- Duke University - USA
- Virginia Tech - USA

High-Level Objectives

- Focus on Design and Analysis
- Hardware architecture and software components in their interaction
  - Less hardware platform design
  - More hardware platform configuration

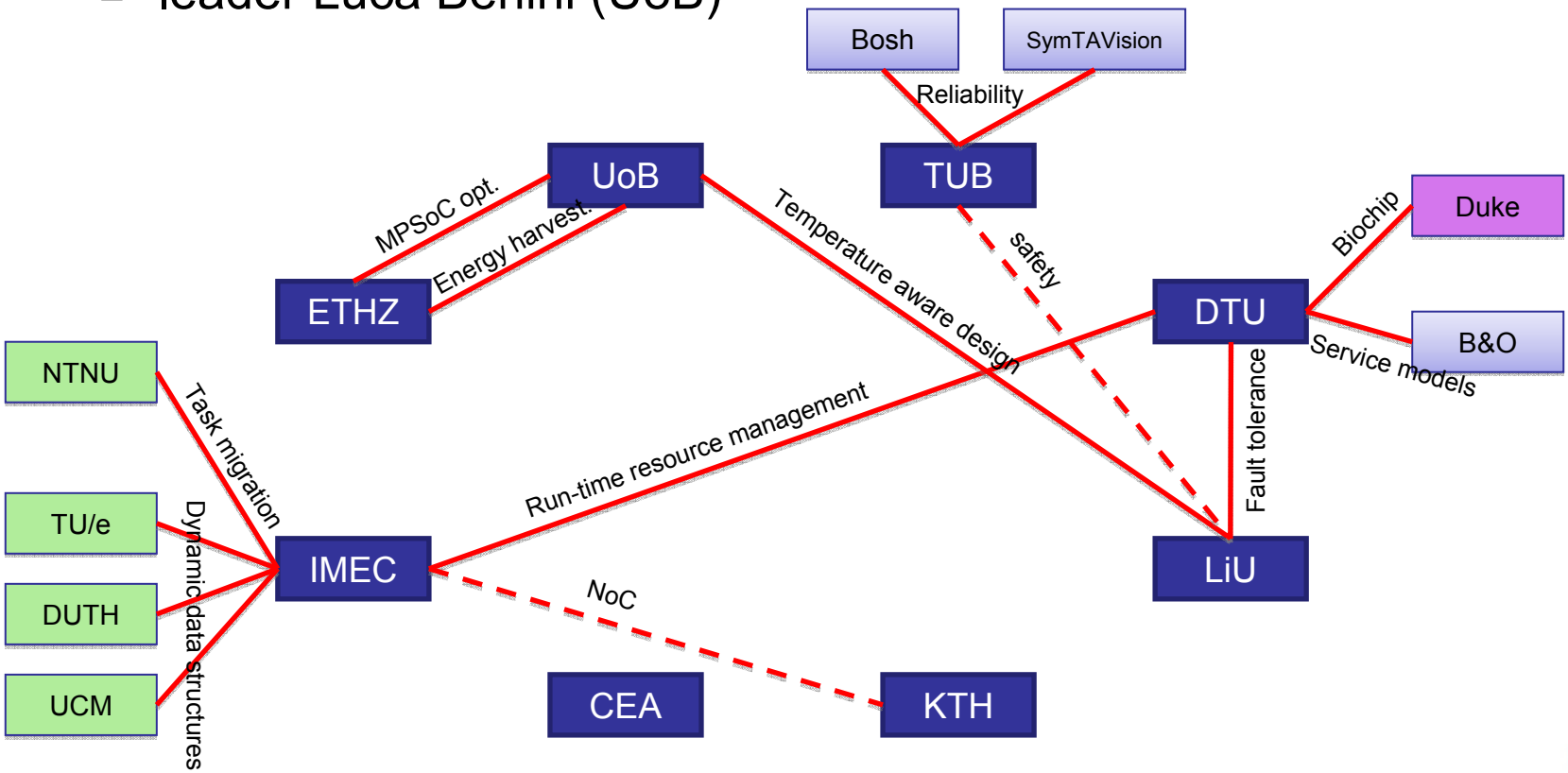
  } Focus on resource management
- Tools for accurate estimation
- Design space exploration and optimization
  - Task mapping (design-time and run-time)
  - Energy minimization / management
- Adaptability
  - Robustness
  - Life-time management
  - Resilience

State of the Integration in Europe

- Distributed, communication-centric embedded systems
  - Multi-core System-on-Chip (MPSoC)
  - Networked embedded systems
  - Wireless sensor networks
- Hardware platforms for embedded applications will continue to be multi-core
- Programming models, design-time and run-time application environments are less clear
- Growing maturity of scalable performance analysis algorithms and tools
- New challenges, platform robustness and adaptivity

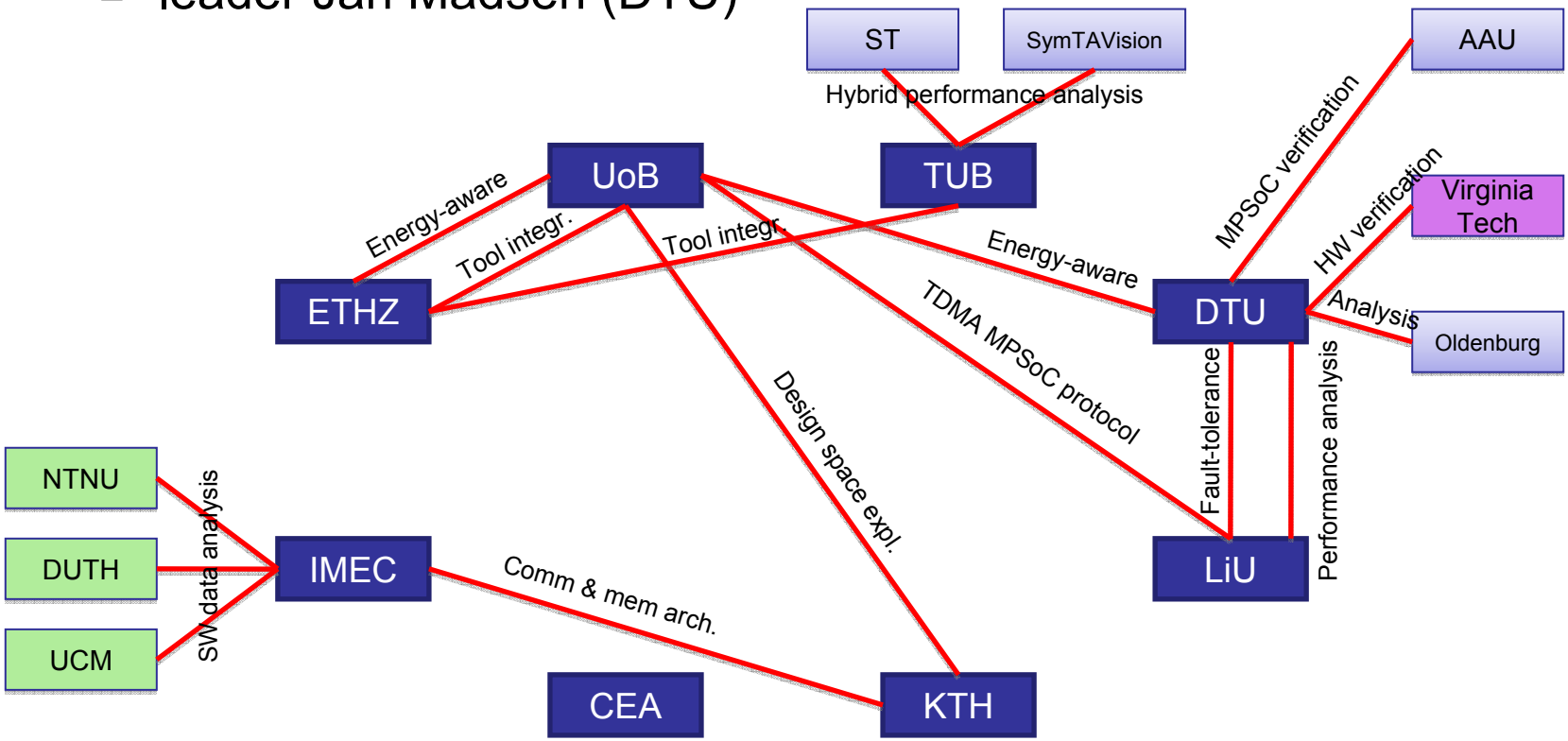
Building Excellence

- Design Activity
  - leader Luca Benini (UoB)



Building Excellence

- Analysis Activity
  - leader Jan Madsen (DTU)



Building Excellence

- Joint publications
  - 22 (9 journals and 13 conferences)
- Joint organization of workshops, tutorials, and special sessions
  - 6th IEEE ESTIMEDIA
  - Castness 2008
  - DATE'08 (Embedded Software Track, Special Sessions, PhD forum)
  - MPSoC'08 (4 invited talks)

Building Excellence

- Summer schools and training activities
  - PhD course DTU, “Advanced Topics in Embedded Systems”
  - Summer school Brazil, “Embedded Systems”
  - ALARI “Embedded Systems”
- New EU research projects
  - MNEMEE, COMBEST, PREDATOR (FP7)
  - SYSMODEL, SCALOPES (ARTEMIS JU)
- Cooperation with other research groups
  - Duke, Virginia Tech, Ecole Polytechnique Montreal
  - UCM, TU/e, NTNU, NTUA, Gent

Building Excellence

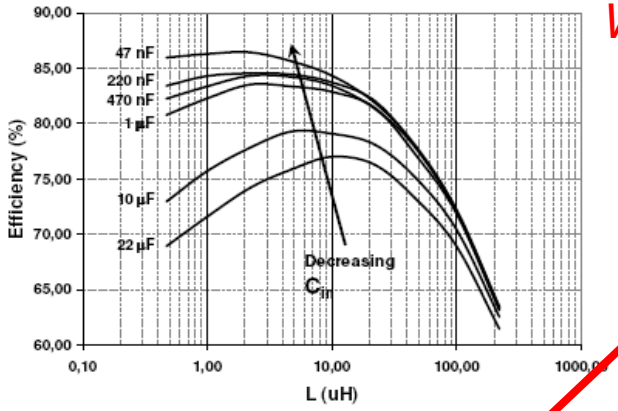
- Cluster workshops
  - Industrial Collaboration, Copenhagen, June 5-6, 2008
  - 6 focused meetings
- Mobility
  - 6 PhD visits
  - 4 faculty/researcher visits
- Impact on industrial practice
  - 2 Industry seminars
  - 3 PhD students are working with industry partners
  - Active participation to ARTEMIS JU Call1
  - Participation in several industry funded project

Overall Assessment and Vision at Y0+1

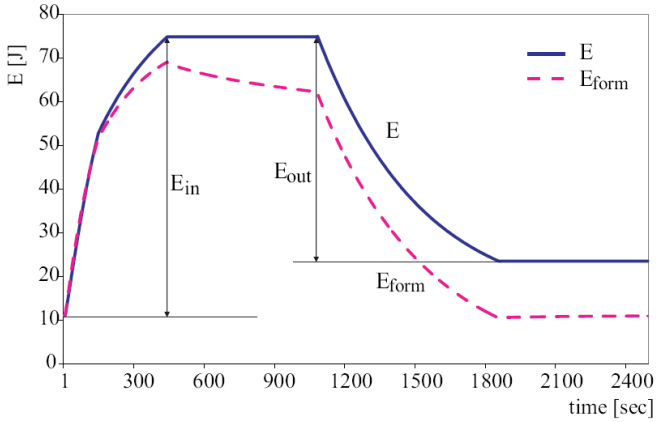
- Good continuation from ARTIST2
- Numerous research activities
- Several industrial contacts and applications
- Explored approached for upcoming embedded systems
  - to increase predictability and adaptability for multi-core platforms
  - energy-aware embedded systems
  - fault-tolerance in distributed embedded systems
  - new technologies – e.g. biochips

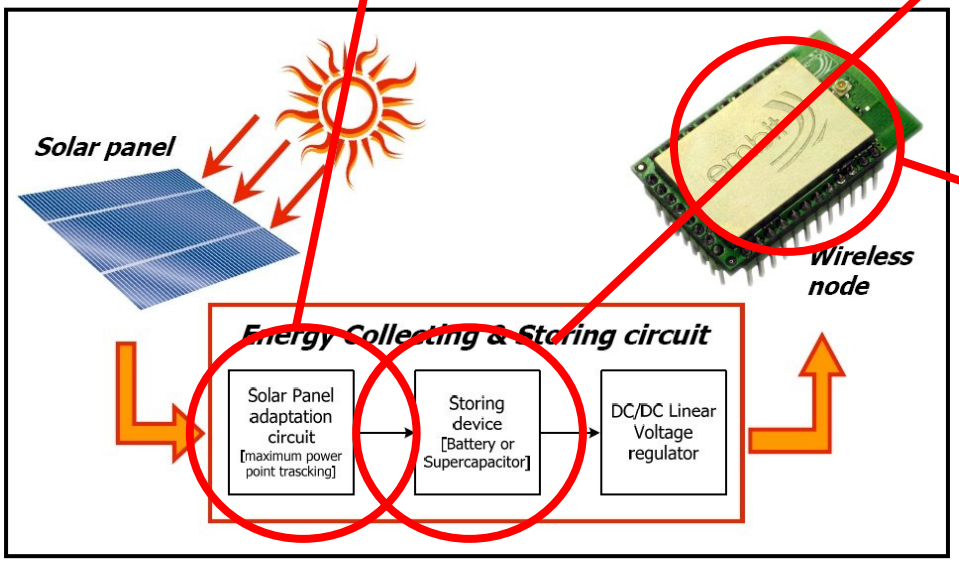
Scientific Highlights: HW/SW Power Management for Energy Harvesting Sensor Nodes (UNIBO, ETHZ)

Improved harvester design through parametric design space exploration (UNIBO)

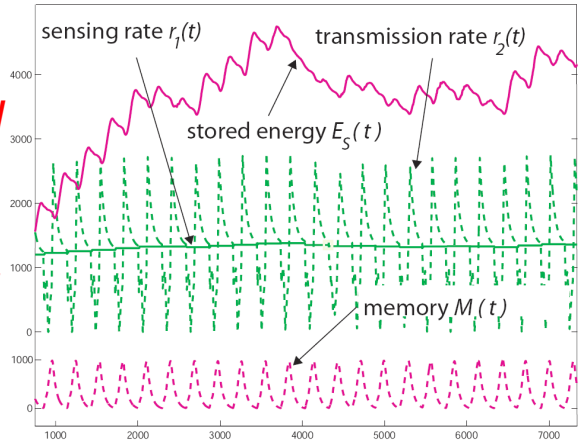


We analyzed and modeled the non-ideal behavior of supercapacitors as energy storage devices (ETHZ).

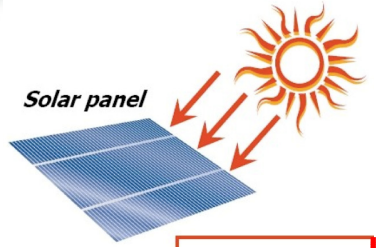


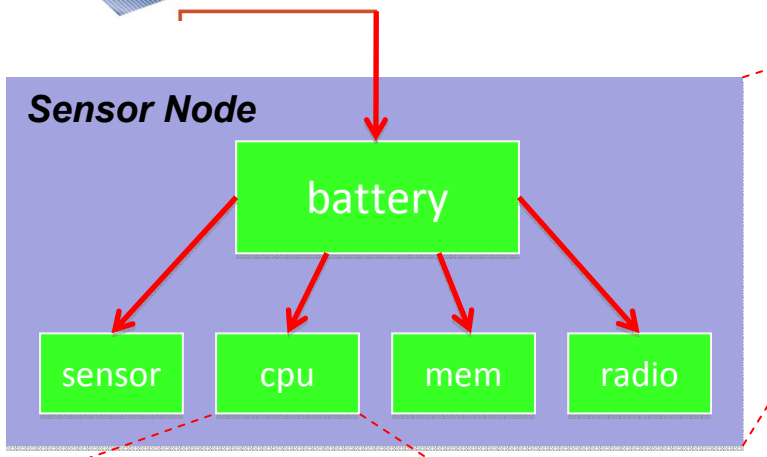


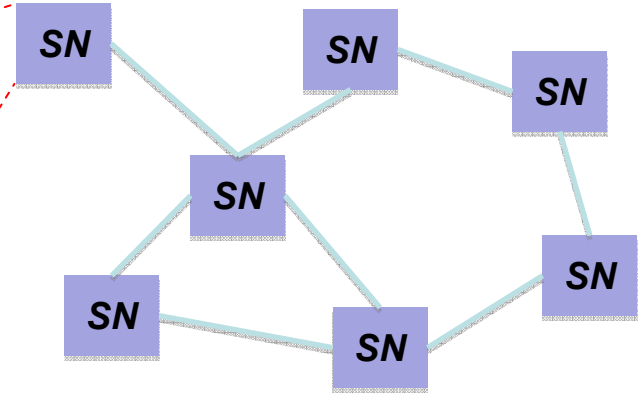
Predictive adaptive control approaches to increase robustness and autonomy (ETHZ, UNIBO)

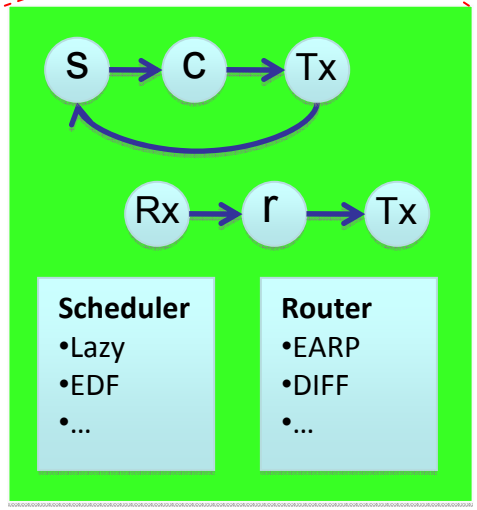


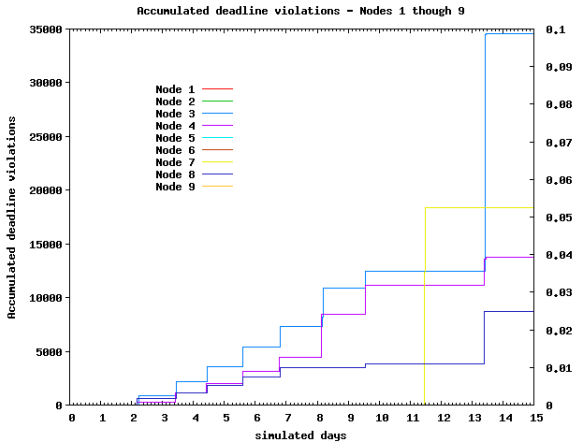
Scientific Highlights
Energy harvesting WSN (UoB, DTU)

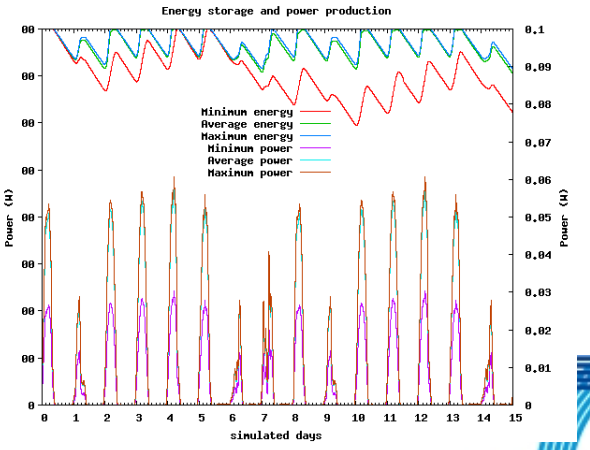




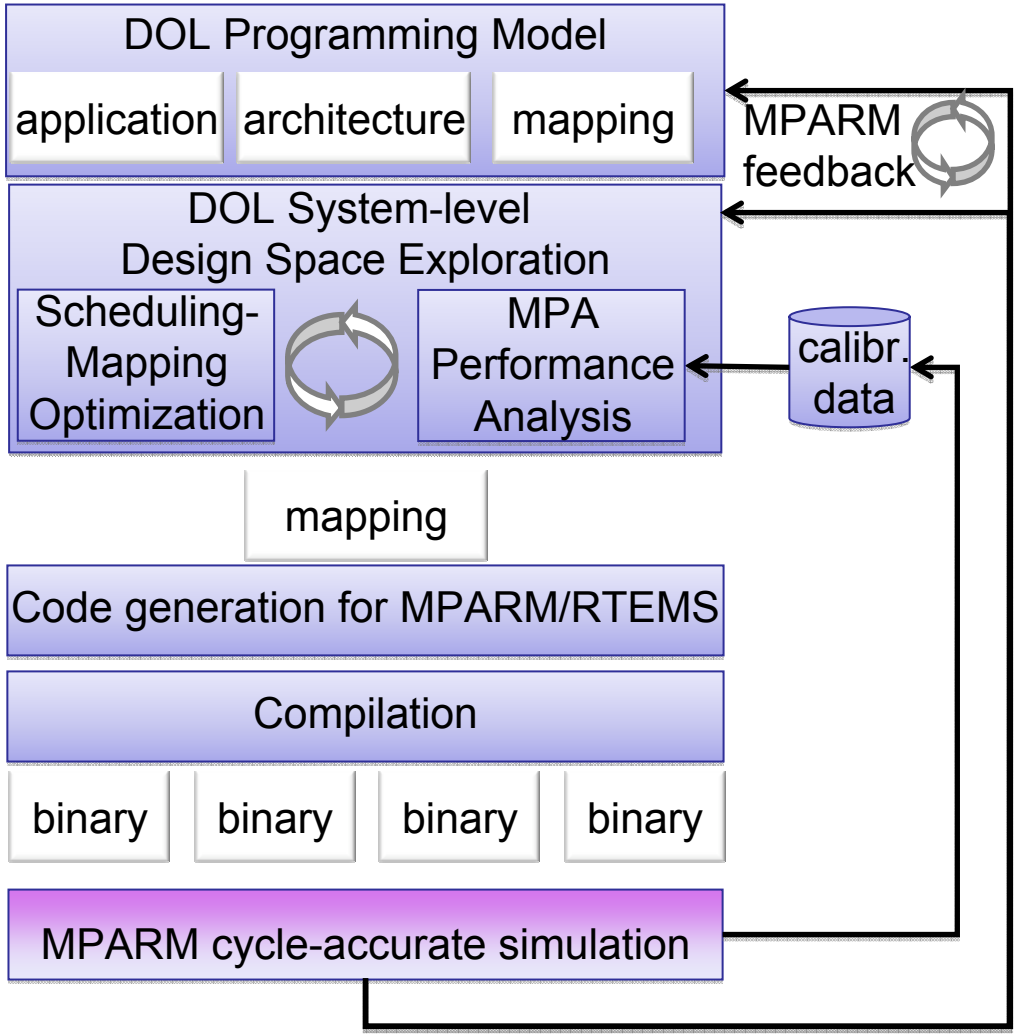








Scientific Highlights: Performance Analysis and Mapping Optimization of MPSoCs (UNIBO, ETHZ)



The programming model and high-level API of DOL were ported to the MPARM simulation platform ***– first prototype ready***

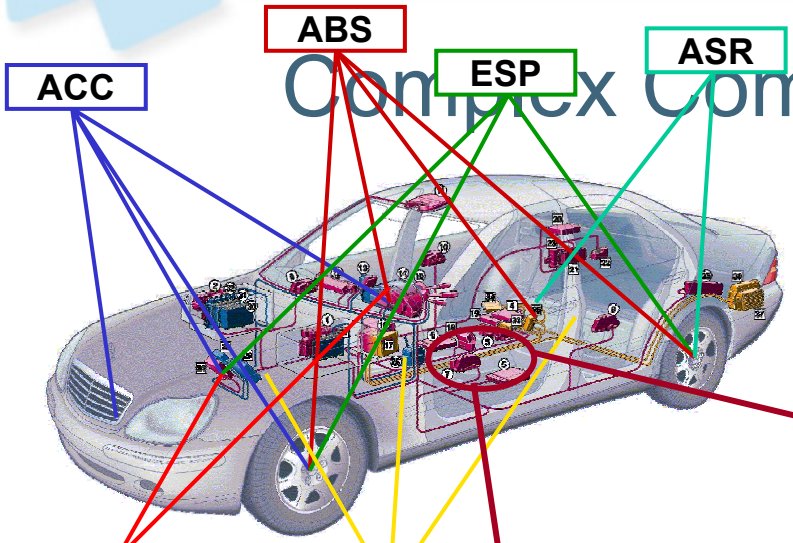
- Alignment of semantics
- Code generation (hardware-dependent software layer)

On-going work:

- MPA analysis of MPSoC design, and comparison with MPARM simulation results
- Address predictability issues from both sides:
  - Build predictable platform
  - Build MPA model which accurately matches the platform features

SEVENTH FRAMEWORK PROGRAMME

Complex Communication Timing

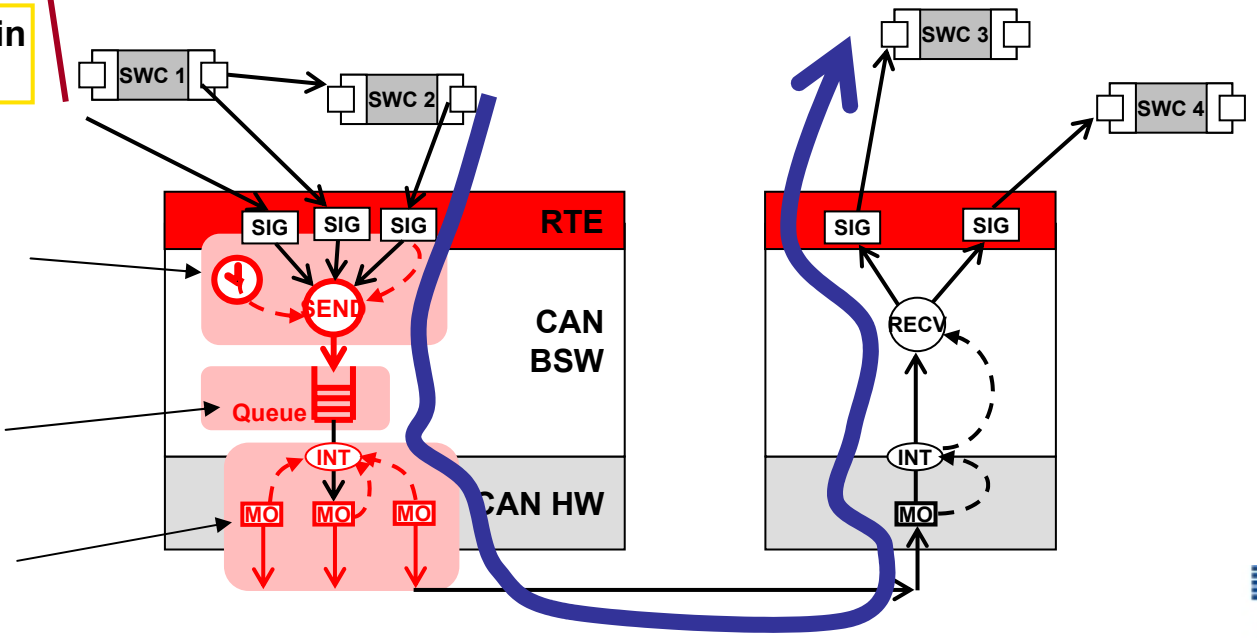


SIG	signal register
SEND/ RCV	COM layer tasks or interrupts
INT	driver interrupt
MO	message object (HW buffer)

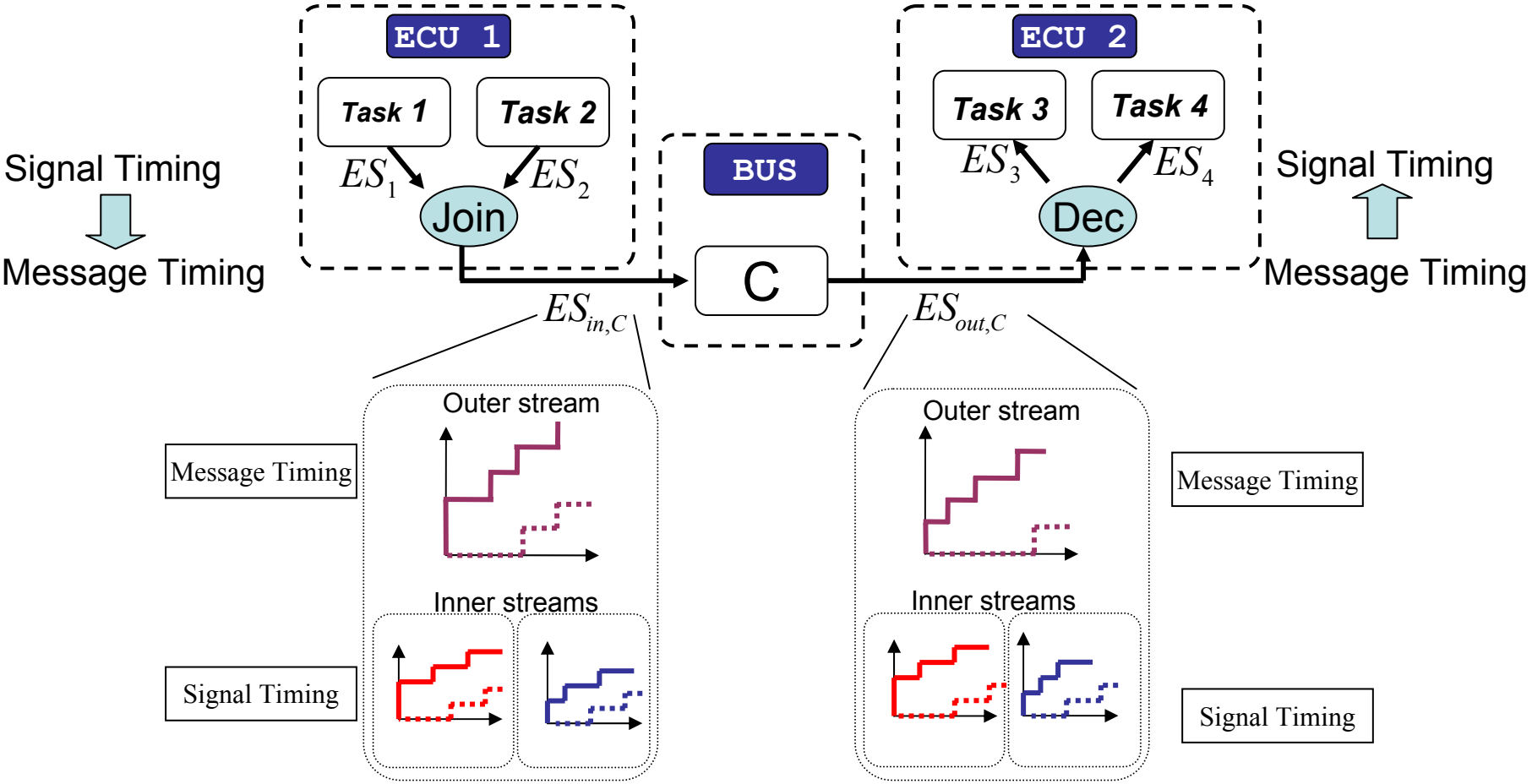
Frame generation timing
(cyclic and/or event+driven)

Buffering strategy
(FIFO, priority ordered, hybrid)

Nachrichten Objekte
(hardware buffers)



Modeling the Communication Layer



ETHZ – TUBS: Combining Different System Abstractions

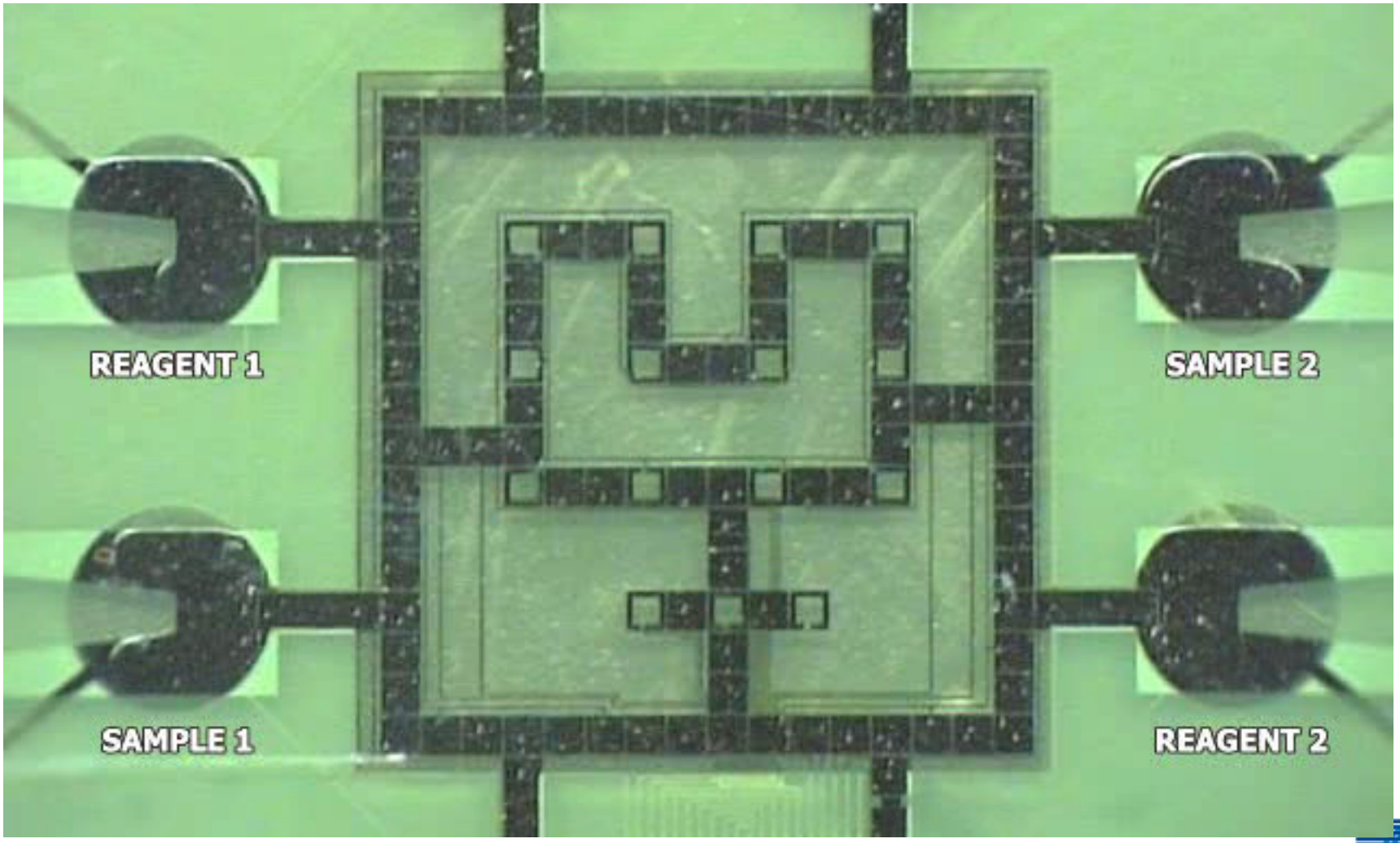
- MPA and SymTA/S use different abstractions for modeling merged event streams.
  - MPA uses event count curves (ECC) and SymTA/S uses a hierarchical event model (HEM).
- Both approaches have their strengths and weaknesses:
  - E.g. merging event streams with a high variability (with high jitter) favors the HEM, while long paths favor the ECCs.
- The integration of the MPA-Tool and SymTA/S allows to transform from one abstraction into the other

⇨ It is possible to always use the more favorable abstraction

Plans for Y2

- Refined performance analysis for MPSoC
- Predictability for MPSoC
- Programming multi-core paltforms
- Reliability
- Integrating different levels of safety requirements on networks and multi-core platforms
- Moving from energy-aware to energy neutral distributed embedded systems
- Exploring new technologies
  - Biochip

Bio-Computation



(courtesy Chakrabarty, Duke University)