PROJECT PERIODIC REPORT

Grant Agreement number: 214373

Project acronym: ARTISTDESIGN

Project title: ArtistDesign – Design for Embedded Systems

Funding Scheme: Full cost

Date of latest version of Annex I against which the assessment will be made: 01/21/09

Periodic report: **1st** ☒ **2nd** ☐ **3rd** ☐ **4th** ☐

Period covered: **from 1st January 2008 to 31st December 2008**

Name, title and organisation of the scientific representative of the project's coordinator[1]:

Mr Joseph SIFAKIS – UJF VERIMAG (partner n°2)

Tel: +33 (0)4 56 52 03 51

Fax: +33 (0)4 56 52 03 50

E-mail: Joseph.Sifakis@imag.fr

Project website[2] address: http://www.artist-embedded.org/artist/-Home-Page-.html

CONTENTS

1. Declaration by the scientific coordinator

Declaration by the Scientific Coordinator

I, as scientific coordinator of the ArtistDesign NoE and in line with the obligations as stated in Article II.2.3 of the Grant Agreement declare that:

- The attached periodic report represents an accurate description of the work carried out in this project for this reporting period;
- The project (tick as appropriate):
  - ☑ has fully achieved its objectives and technical goals for the period;
  - ☐ has achieved most of its objectives and technical goals for the period with relatively minor deviations[1];
  - ☐ has failed to achieve critical objectives and/or is not at all on schedule[2].
- The public website is up to date, if applicable.
- To my best knowledge, the financial statements which are being submitted as part of this report are in line with the actual work carried out and are consistent with the report on the resources used for the project (section 6) and if applicable with the certificate on financial statement.
- All beneficiaries, in particular non-profit public bodies, secondary and higher education establishments, research organisations and SMEs, have declared to have verified their legal status. Any changes have been reported under section 5 (Project Management) in accordance with Article II.3.f of the Grant Agreement.

Name of Scientific Coordinator: Joseph Sifakis

Date: March 31st 2008

Signature of the Scientific Coordinator: 

[1] If either of these boxes is ticked, the report should reflect clearly and explain why the objectives were not achieved.
[2] If either of these boxes is ticked, the report should reflect clearly and explain why the objectives were not achieved, and any remedial actions taken.

2. Publishable summary

1. Overview

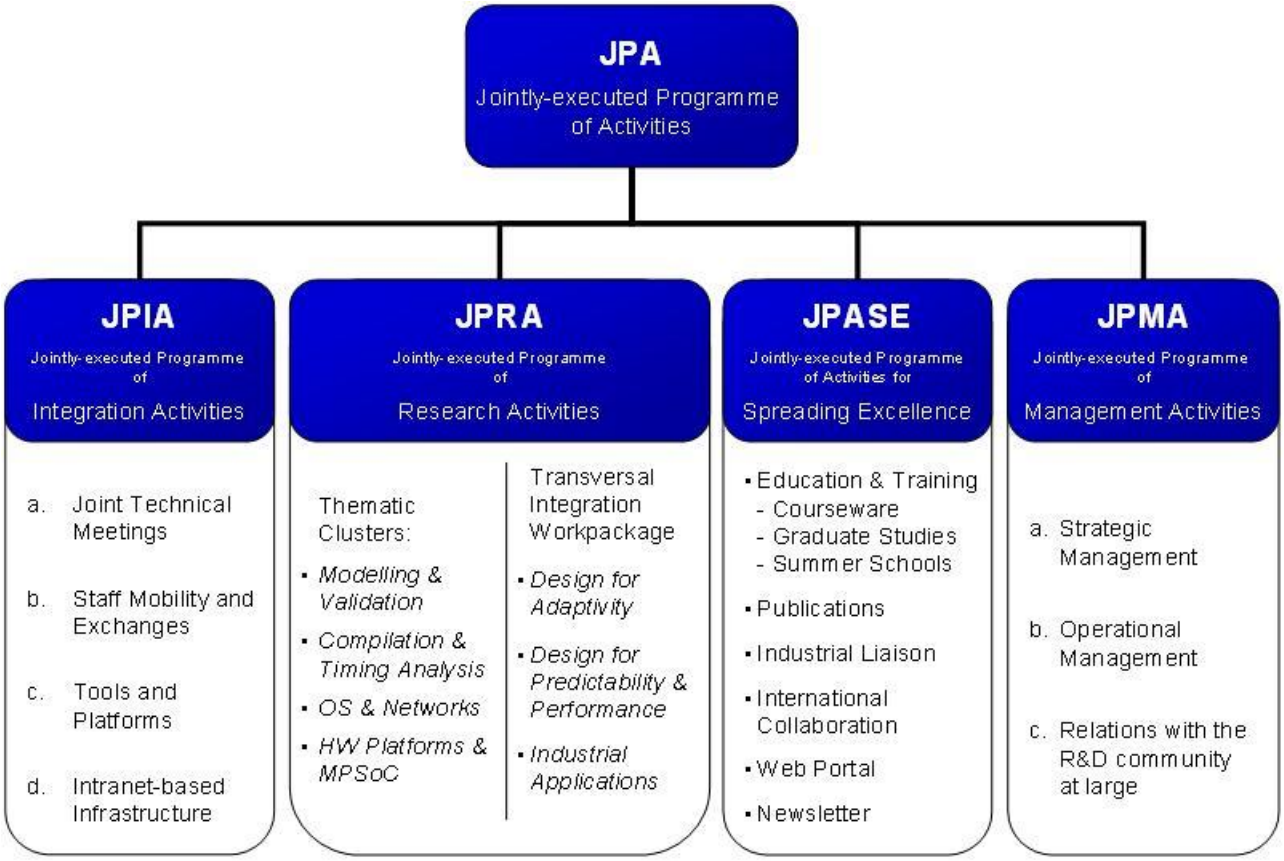
ArtistDesign finances durable integration between teams and not the concrete elements of the JPA which most often belong to other projects. These specific technical objectives may or may not be attained (this is the essence of research as opposed to development), but we feel that the main product of ArtistDesign is the emergence of a lasting European research community, that has a significantly enhanced capacity for preparing Europe's future.

The research is completed by work in the JPIA (Jointly Executed Programme of Integration Activities) workpackage, which aim to transform research results in tangible tools and components, and bring teams closer together on a day to day basis.
We believe that the topics chosen provide a good coverage of the area, for embedded software and systems.

The ArtistDesign NoE is a complex construction assembled from world-leading communities, teams, and individuals. This is certainly an asset, but also a source of complexity in management. Each team has two essential characteristics: world-class excellence and strong interaction with top industrial players. ArtistDesign partners play a leading role in the different communities in embedded systems design, and they advance the state of the art in each of these.

It is difficult to abstract out a global synthesis of the overall technical achievements. This is due to the diversity and the low granularity of the actions to be covered (meetings, publications, attendance at workshops, visits, and platforms).

The following is a certainly non-exhaustive assessment of the work in the Joint Programme of Activities' 4 main branches.

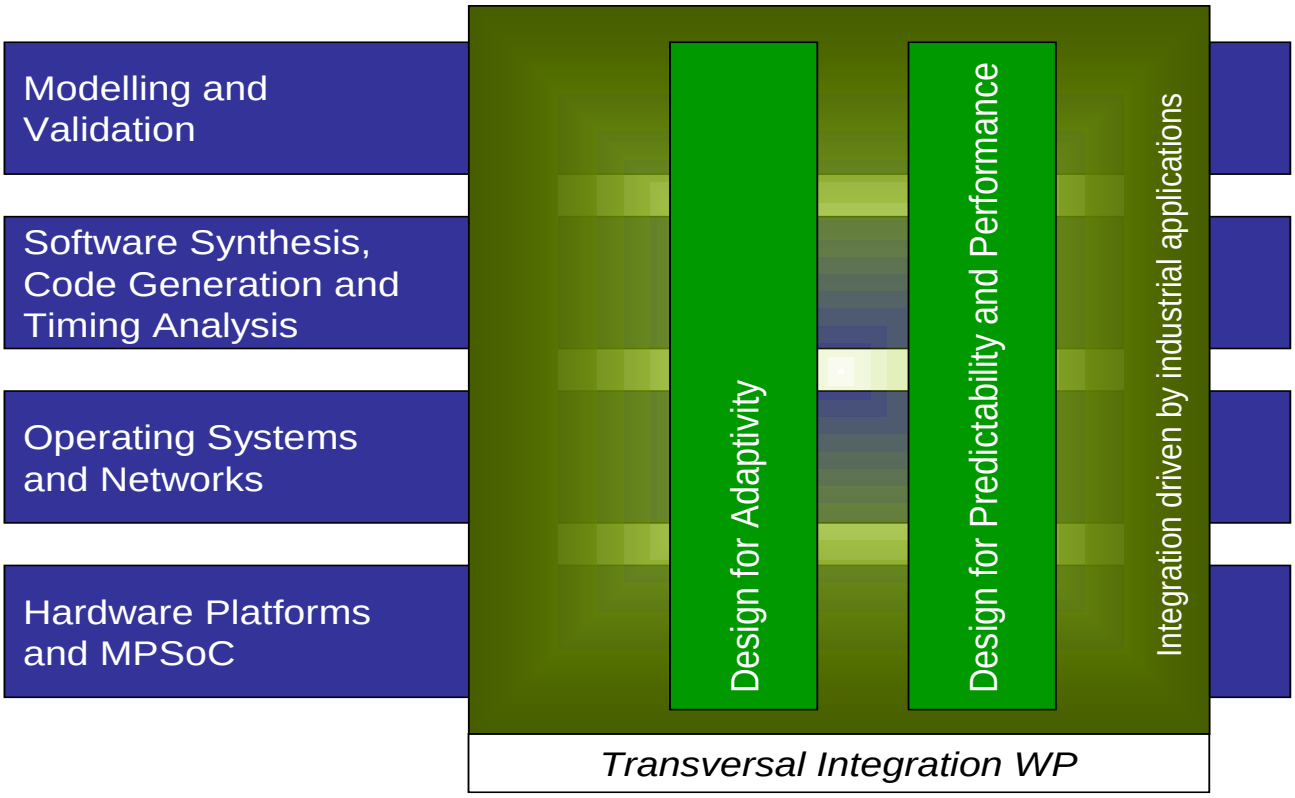


2. Joint Programme of Research Activities (JPRA)

The JPRA is composed of intra and inter-cluster research activities on cutting-edge topics in embedded systems design. While the main bulk of financing for these activities is taken up by outside programmes (Integrated Projects, National Programmes, Industrial Contracts, etc), the ArtistDesign NoE finances the extra burden due derived from integrating these into a single coherent research programme.

Thus, the essential ingredient within ArtistDesign is the JPRA, which motivates the participating research teams far more than the actual financing, which is tiny in comparison with the overall research aims. It is completed by the Joint Programme of Integrating Activities (JPIA), and the Joint Programme of Activities for Spreading Excellence (JPASE), and overseen by the Joint Programme of Management Activities (JPMA).

The structure of the research activities reflects the following decomposition of the embedded systems design flow.
This design flow is composed of the following cooperating activities, starting with component based modeling and leading to implementation. These activities must be well coordinated, and supported by tools and methods to ensure satisfactory levels of productivity and quality.
Accordingly, we have structured the area of embedded systems design into the following topics.



Modeling and Validation. Unlike other computer systems, embedded systems are strongly connected with a physical environment. A scientific foundation for embedded systems must therefore deal simultaneously with software, hardware resources, and the physical environment, in a quantitative manner. In order to gain independence from a particular target platform, embedded system design must be model-based. In order to scale to complex applications, embedded system design must be component-based. The overall objective of this activity is develop model and component based theories, methods, and tools that establish a coherent family of design flows spanning the areas of computer science, control, and hardware. The activity brings together the most important teams in the area of model and component based design in Europe.

SW Synthesis, Code Generation and Timing Analysis. There is a continuing demand for higher performance of information processing, which stimulates using a growing amount of parallelism (including using multiple processors). This trend affects the design of embedded systems. We address issues related to multiple heterogeneous processors on a chip, also containing memory hierarchies and communication interfaces. Such processors can only be exploited if (sets of) applications can be efficiently mapped to heterogeneous processors.

Timing analysis is also affected by the trend toward the new platforms. Timing analysis has to cope with the kind of memory hierarchies found in MPSoCs. Also, timing analysis beyond the single processor is required. Hence, timing analysis will also consider the timing of communication. The overall objective is to provide safe timing guarantees for systems consisting of local memories hierarchies and multiple processors.

Operating Systems and Networks. We investigate how current real-time operating systems have to be extended or modified to support emerging real-time embedded systems characterized by a high degree of complexity, highly variable resource requirements and parallel processing such as multicores. Most embedded systems are often characterized by scarce resources in terms of processing power, memory, space, weight, energy, and cost.

Hence, another objective is to investigate kernel mechanisms that can efficiently manage the available resources, taking multiple constraints into account, whilst guaranteeing isolation properties. Also, to support dynamic applications with variable resource requirements or to cope with

unpredictable resource availability, feedback control techniques for resource management at the operating system and application level are also investigated.

Hardware Platforms and MPSoC Design. While hardware platforms for embedded applications will continue to be multi-core, with increasing degrees of parallelism, the evolution trajectory on programming models, design-time and run-time application environments is much less clear. The consequence is fragmentation: while many research teams are working on one or more of these domains, there is little communication and integration, this leads to duplication of results and overall slow progress. The teams involved in this activity have a wide-ranging research experience which covers all the key areas in MPSoC application specification mapping. The integration activity supported by ArtistDesign will help the participants to the cluster in strengthening the coherency of their approaches and focus on addressing complementary issues in a synergistic fashion.

Design for Adaptivity. An embedded hardware-software system is adaptive, if it can modify its behavior and/or architecture to changing requirements. Adaptivity is increasingly important as the complexity and autonomy of embedded systems increases. Adaptivity is a cross-cutting system characteristic that affects both hardware and software. At the software-level adaptivity is mainly concerned with flexible and adaptive resource scheduling, e.g., CPU time scheduling. At the hardware-level adaptivity includes both adaptation of operation modes, e.g., supply voltage and clock frequency, processor instruction sets, and dynamic management of hardware resources, e.g., processing elements and memory.

Design for Predictability and Performance. Many applications have strict requirements on timing, and limited resources (memory, processing power, power consumption, etc.). All systems also have increasing demands on (average) performance, which has motivated the introduction of features such as caching, pipelining, and (now becoming very prominent) multiprocessor platforms. Almost all such efficiency-increasing features drastically increase variability and decrease analyzability of response-times, etc. and thus have a detrimental effect on predictability. Since the introduction of new architectural features is inevitable, it is important to: a) develop technology and design techniques for achieving predictability of systems built on modern platforms, and b) investigate the trade-offs between performance and predictability.

Integration Driven by Industrial Applications. To have a strong impact on industry and society at large, the results of the Thematic Clusters need to be harmonized in an overall design flow that can sustain the embedded design chain from conception of the product to its implementation. The design chains vary in length and players according to the industrial segment addressed: for example, the design chain in automotive electronics starts with the car maker (e.g., BMW, Daimler Chrysler, Peugeot, Fiat), goes through the Tier 1 suppliers (e.g.,Contiteves, Bosch, Magneti Marelli) and connects to the Tier 2 suppliers (e.g., FreeScale, ST, Infineon, Hitachi). It often includes IP providers such as programmable cores, RTOS and software development tool providers and design service companies. In the mobile communication domain, the chain starts with the application developers (e.g., gaming and video content), includes the telecommunication operators (e.g., Telecom Italia and Telefonica), the device makers (e.g., Nokia and Ericsson), the silicon makers (e.g., TI, Qualcomm and ST) and outsourcing manufacturing companies (e.g., Flextronics). Today, there is stress in the chain as the technology advances may create opportunities to redefine the roles of the various players. In addition, the system integrators are often faced with an almost impossible task of composing their design out of parts supplied by companies whose design methods and standards are widely different and about which they have limited or no information. There is a need for an all-encompassing approach to system design that can make an entire industrial segment work as a virtual vertically integrated company.

3. Joint Programme of Integration Activities (JPIA)

The JPIA activities promote integration of geographically dispersed team sand have long lasting effects:
Joint Technical Meetings. Joint Technical meetings aim to present, discuss and integrate the ongoing work, and exchange points of view with other teams. They also serve to identify future work directions.
Staff Mobility and Exchanges. This is essential for integration within the NoE, including mobility of students and/or researchers, between core teams, or between core teams and affiliated teams. Mobility is justified by and refers to involvement in an activity from the JPRA or JPIA, or one of the following: co-funded scholarships with industry; exchange of students and personnel within the consortium.
Tools and Platforms. A research platform is composed of competencies, resources, and tools targeting specific technical and scientific objectives around a chosen topic. These are at the state-of-the-art, and are made available to the R&D community for experimentation, demonstration, evaluation, and teaching.
The research platforms, tools and facilities are an essential tool for implementing the JPIA. They will lay the groundwork for the JPRA, allowing common research to occur and capitalization on research results. Platforms are used as the basis for transfer of research results to industry. They allow teaching practical knowledge of the concepts and techniques.
ArtistDesign platforms are not defined from scratch – they integrate the results of long-term efforts, and are meant to be durable, evolving with the state of the art. The partners are committed to durability, and have invested significant resources into their development. The construction of ArtistDesign has provided the opportunity to assemble existing pieces into a rationally-structured set of platforms, covering the area of embedded systems design.
Some of the ArtistDesign platforms have international visibility, and the ambition is for these to serve as world-wide references in their respective topics.

4. Jointly-executed Programme of Activities for Spreading Excellence (JPASE)

ArtistDesign leverages on the worldwide visibility of the ARTIST2 NoE. It is progressively creating a European embedded systems design community and spreading the "Artist culture" in all major research institutions.
To ensure that the next generation of researchers will continue in this direction we, as a consortium, devote a great deal of effort to Spreading Excellence, in both academic and industrial circles. Furthermore, through our links with both core and affiliated partners, we actively set up permanent links between industry and public research, based on existing partner collaborations with major industrial players in the area.
The JPASE activities are intended to spread excellence and structure the community at large. They are planned by the Strategic Management Board, and are implemented by ArtistDesign core and affiliated partners.
The NoE will leverage on its members and teams, who play a main role in the organization of world-class scientific events, to disseminate results in the area. We expect that the NoE's structured and authoritative dissemination will have a strong effect on the community as a whole, for orienting and creating synergy for research.

5. Managing the Network of Excellence (JPMA)

We believe that the current two-tiered Management structure - dividing the management amongst cluster leaders and the Strategic Management Board composed of both cluster leaders and a limited number of other selected prominent core partners – has been the right one for managing such a large research entity. It has provided the right combination of flexibility and accountability, while leaving room for innovation and evolution.
This management structure is reproduced with adaptations in the ArtistDesign NoE. The adaptations reflect the greater cohesion between partners, and move to capitalize on and strengthen the integration achieved in Artist2.

3. Project objectives for the period

The ArtistDesign NoE is the visible result of the ongoing integration of a community.

The central objective for ArtistDesign is to build on existing structures and links forged in the ARTIST2 NoE, to become a virtual Centre of Excellence in Embedded Systems Design. This is achieved through tight integration between the central players of the European research community. Also, the consortium is smaller, and integrates several new partners. These teams have already established a long-term vision for embedded systems in Europe, which advances the emergence of Embedded Systems as a mature discipline.

ArtistDesign is becoming the main focal point for dissemination in Embedded Systems Design, leveraging on well-established infrastructure and links. It will extend its dissemination activities, including Education and Training, Industrial Applications, as well as International Collaboration. ArtistDesign will establish durable relationships with industry and SMEs in the area.

ArtistDesign builds on existing international visibility and recognition, to play a leading role in structuring the area.

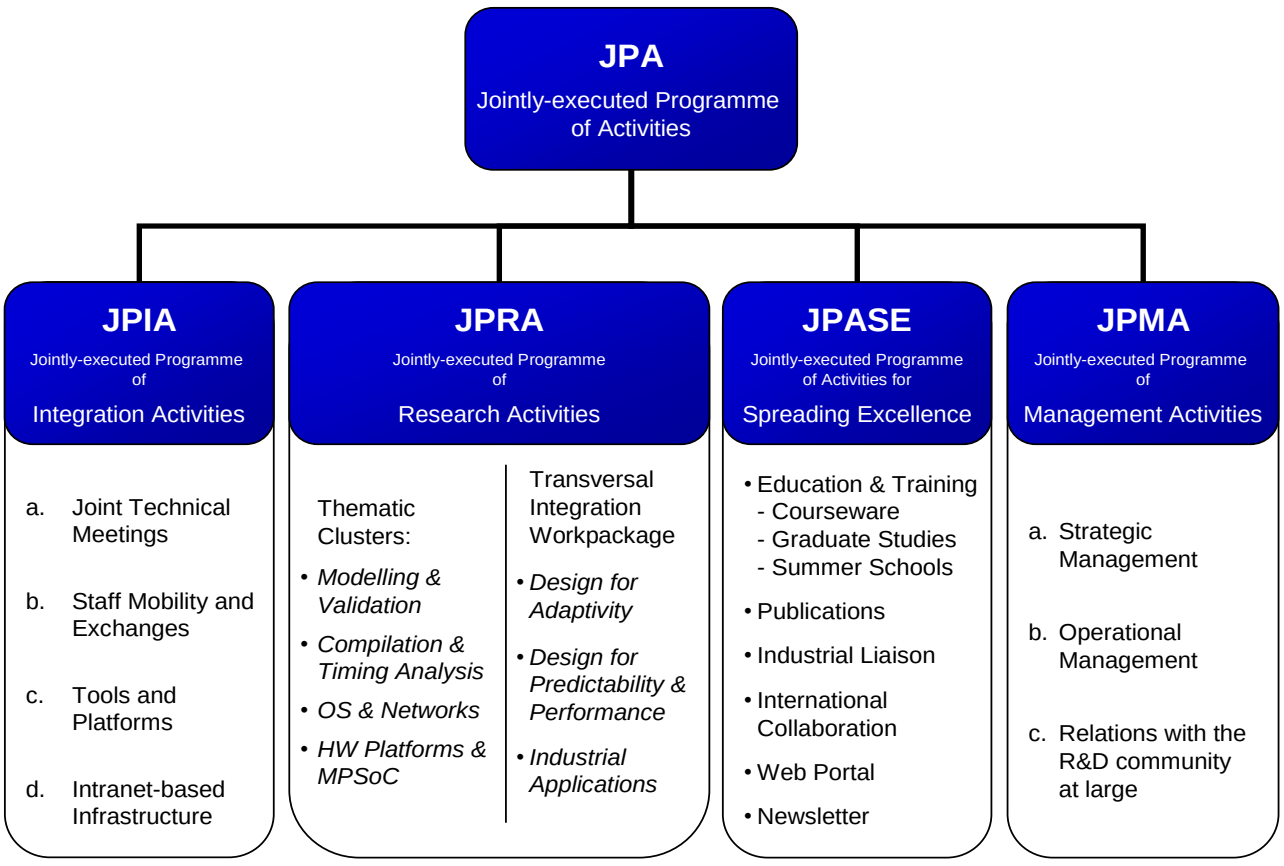
The research effort aims to integrate topics, teams, and competencies, grouped into 4 Thematic Clusters: “Modeling and Validation”, “Software Synthesis, Code Generation, and Timing Analysis”, “Operating Systems and Networks”, “Platforms and MPSoC”. “Transversal Integration” covering both industrial applications and design issues aims for integration between clusters.

4. Work progress and achievements during the period

ArtistDesign finances durable integration between teams and not the concrete elements of the JPA which most often belong to other projects. These specific technical objectives may or may not be attained (this is the essence of research as opposed to development), but we feel that the main product of ArtistDesign is the emergence of a lasting European research community, that has a significantly enhanced capacity for preparing Europe's future.
The research is completed by work in the JPIA (Jointly Executed Programme of Integration Activities) workpackage, which aim to transform research results in tangible tools and components, and bring teams closer together on a day to day basis.
We believe that the topics chosen provide a good coverage of the area, for embedded software and systems.

The ArtistDesign NoE is a complex construction assembled from world-leading communities, teams, and individuals. This is certainly an asset, but also a source of complexity in management. Each team has two essential characteristics: world-class excellence and strong interaction with top industrial players. ArtistDesign partners play a leading role in the different communities in embedded systems design, and they advance the state of the art in each of these.

It is difficult to abstract out a global synthesis of the overall technical achievements. This is due to the diversity and the low granularity of the actions to be covered (meetings, publications, attendance at workshops, visits, and platforms).
The following is a certainly non-exhaustive assessment of the work in the Joint Programme of Activities' 4 main branches.



4.1 Joint Programme of Research Activities (JPRA)

We present an overall vision integrating aspects from both the Artist2 European Network of Excellence (ended Sept 30th 2008) and ArtistDesign. This more complete vision is not necessarily followed in the Cluster and Activity deliverables, to avoid "double reporting".

Modelling and Validation

Modelling

On modelling heterogeneous systems, we have obtained some very significant results:

- Work by INRIA, PARADES, and VERIMAG, on the theory of tagged systems provides conditions for correct implementation of synchronous systems on "less synchronous" architectures. Work by INRIA on new models of computation, the Kahn-extended Event Graph (KEG), which adds "static control" in the Model of Computation of Marked Graphs.
- Work on the BIP component framework, introduces a notion of expressiveness for component-based formalisms, which provides a basis for their comparison. This notion drastically differs from the usual one, as it takes into account the expressive power of composition operators (glue operators).
- Significant progress has been achieved in methods for distributed implementation of non-distributed specifications. VERIMAG studied a method for the automatic generation of distributed implementations of BIP models. INRIA, PARADES and VERIMAG studied the concept of loosely time-triggered architectures, implementing time-triggered architectures. Finally, fully asynchronous implementations of synchronous systems have been studied.
- Other results on distributed implementations include reliability, new heuristics in scheduling for reliability, design of communication architectures and time-triggered system-on-chip architectures.

Validation

At the crossroads between Modelling and Validation, we have obtained significant results on Interfaces and Composability, including:

- The development of interface theories supporting component reuse (EPFL). We have shown that existing interface theories provide no formal support for component reuse. We enriched interface theories with a new operation allowing the same component to implement several different interfaces in a design.
- The development of contract-based verification techniques for the heterogeneous rich component (HRC) model (INRIA, PARADES, VERIMAG), in the framework of the SPEEDS project. The techniques allow handling multiparty interaction, as well as many different languages for describing notions of refinement under contexts. These results found application in the verification and analysis of HRC models.
- In joint work, ETHZ and Uppsala propose modular performance analysis techniques, based on the real-time calculus and timed automata. A prototype tool name CATS for compositional timing and performance analysis has been developed.

- VERIMAG has continued the work on compositional deadlock verification of BIP programs, and its implementation in the DeadlockFinder tool. Other results include the enhancement of existing component models, such as the synthesis of controllers from specifications and the generation of component models from their observed behaviour.
-

On qualitative validation, work has been carried out in the following directions:

- Significant contributions to game-theoretic approaches to real-time system testing. By modelling the systems as timed game automata and specifying the test purposes as formulas, we developed a timed game solver Tiga to synthesize testing strategies.

  We studied games for different extensions of timed automata such as weighted timed automata, priced timed automata, multi-priced timed automata. The results relate to the complexity of decision problems for these automata, as well as model checking and synthesis algorithms. The notion of timed parity games has been studied, with a focus on robustness and complexity. We have also studied reach ability in timed games.

- Continuing on work from previous years, we have extended and improved the functionality of the UPPAAL tool, including the use of slicing techniques for model optimization as well as features supporting interface theory for real-time systems.

- We have studied quantitative testing techniques. In particular, we have developed a theory allowing testing of systems in the presence of measurement imprecision. We also studied testing methods for probabilistic processes.

- We have studied quantitative model checking techniques for timed models, including timed automata, linear hybrid automata and general non-linear hybrid systems. The work on verification has been applied to non-trivial case studies and systems, in particular in collaboration with industry.

Finally, we have studied compositional synthesis and verification techniques. These include modular supervisory control, as well as the verification of component-based systems.

Software Synthesis, Code Generation and Timing Analysis

Software Synthesis and Code Generation

We developed research in the following directions:

- We studied the influence of scratchpad memory allocation techniques on worst case execution times (WCET). We developed integer linear programming models to decide which parts of a program's code or data can be moved onto the highly predictable scratchpad. First experiments show WCET reductions of more than 50% for several benchmarks.
  We also investigated WCET-aware register allocation techniques, by extending existing techniques based on graph colouring.
- We continued work on scalable source-level analysis and annotation-based timing analysis methods. The SATIrE infrastructure allows building analysers that take source code annotations as additional input, and generate output as annotations. This allows a significant increase in productivity, by requiring the user to annotate the relevant timing information that cannot be automatically computed. The integration of PAG was instrumental in investigating the scalability of analyses.

- We studied polyhedral loop parallelisation techniques for multi-core systems.

Regarding tools and platforms, we developed work in the following directions:

- We designed a Static Loop Analyzer, allowing estimating loop iteration bounds. This information is essential for a large number program analyses. Our analyser improves analysis techniques based on conventional abstract interpretation by integrating a new static polytope-based loop evaluation method.
  We have demonstrated the applicability of the analyser on benchmarks taken from the benchmark suites MRTC, DSPStone, MiBench, UTDSP and MediaBench. Our loop analyser was the only tool able to answer all questions related to flow fact during the WCET tool challenge 2008.
- In continuation of work performed in Year 3, we developed a new WCET-aware procedure positioning and cloning technique. The compiler optimisations obtained were exploited for WCET reduction. Results on real-world benchmarks show WCET reductions of 10% on average, while ACET is reduced by 2 on average.

The cooperation between ACE and Aachen on the retargetable code optimizations has been continued. The conditional execution engines have been extended by a strong retargeting formalism.

Timing Analysis

In addition to experimental work, we developed important results on Timing Analysis.
We have studied a notion of time predictability of cache architectures, which is the first precise notion found in the literature. Four different cache replacement strategies were compared and the LRU strategy was found to be optimal. This research is related to work within the PREDATOR FP7 project, which attempts to reconcile performance and predictability.
The study of Timing anomalies, where local worst-case choices may not lead to the global worst-case scenario, is essential for time predictability. We have studied techniques for handling timing anomalies for efficient WCET analysis, as well as for measuring the impact of timing anomalies on WCET analysis.

Other work on Timing Analysis includes parametric Timing Analysis, where some parameters of the program can remain unknown until execution. We also developed Timing Analysis techniques, in collaboration with BOSCH, taking into account operating modes of programs, computed semi-automatically. Finally, we developed WCET analysis for systems with preemptive scheduling.

Work on the AIR format has continued. The format was extended and adapted to the needs of the partners. The attribute database was extended with new attributes.
We also worked on the development and improvement of formats for ensuring the interoperability of the tools. The work on formats includes ALF for computation semantics representation, conversion of the ABSINT AIR format to SWEET format, and the definition of common flow description attributes.
As was the case last year, the WCET Challenge 2008 consisted of a set of benchmark programs and analysis tasks to be performed by the contestants.
http://www.artist-embedded.org/artist/-WCET-08-.html

Operating Systems and Networks

Resource-aware Operating Systems
In addition to work done in Artist2, we developed work in the following directions:

- Modeling and analysis of control-driven tasks. The standard design of control is based on the periodic sampling. We studied a model which saves a considerable amount of computational resources which samples the inputs when needed.
- Implementation of a flexible scheduling framework called FRSH that is capable of handling multiple concurrent activites with different criticality and timing in the same system. The framework has been designed to be implemented on different platforms.
- ERIKA support for the EasyBee radio transceiver has been developed.
- We studied issues relating to the operating system support needed by advanced users of a real-time specification for Java. In particular, two issues have been addresses: how to handle systems that contain a large number of events; and how to measure blocking time.

Scheduling and Resource Management
We have had a large volume of activity on this topic:

- All the partners, under the leadership of York, have worked for establishing a taxonomy of resource usage. The taxonomy distinguishes between different classes of resources - each class being subdivided into a number of resource types.
- The architectural model of a Flexible Scheduling Framework developed in the FRESCOR and FIRST EU-IST projects has been extended to include a contract model. Contracts represent complex requirements of the applications which can be managed by the underlying system to provide the required level of service.
- Several activities on scheduling, in particular multi-resource scheduling for multi-core platforms, schedulability for CAN-based control applications, sensitivity analysis, flexible scheduling on low-cost microcontrollers.
- Other work related to the Transversal Activity: “Design for Adaptivity” has been carried out, including dynamic runtime adaptability, optimal period selection and scheduling for embedded controllers.

Real-Time Networks
We have carried out work on:

- Analysis techniques, including Worst Case analysis and dimensioning of cluster-tree Wireless Sensor Networks, as well as analysis for specific networks.
- We studied techniques for supporting real-time communication and QoS for Wireless Sensor Networks. These include work around the use of IEEE 802.15.4 and ZigBee as federating communication protocols for Wireless Sensor Network applications, as well as supporting real-time communication of the Erika real-time operating system.
- We have also furthered work, started in Artist2, on student design competitions in the scope of the IEEE Real Time Systems symposium.

Hardware Platform and MPSoC Design

Platform and MPSoC Design
The work has included:

- Study of system design methodologies handling the dynamic nature of embedded systems and allowing predictability and optimal use of resources.
  Bologna, with ETHZ, has studied optimalisation-centric MPSoC design techniques. The main goal of this work was to establish a common understanding of the MPARM framework developed in Bologna, and the DOL framework developed at ETHZ.
  Bologna and Linkoping have studied a temperature power-optimization system. A temperature-aware dynamic voltage selection technique has been developed for energy minimisation.
  Other work on design optimization for fault-tolerant distributed embedded systems is developed by Linkoping and DTU.
- Bologna and ETHZ have improved the design of a scavenger prototype, to perform automatic maximum power point tracking. They developed a compact model for small solar modules that accurately describes their behaviour over a wide range of irradiance conditions. Furthermore, they improved the efficiency of the DC-CD converter at the solar harvester.
- We (DTU) have studied programming models for MPSoC architectures as well as investigated the hardware/software interface between the processing elements and the interconnect network. We also have studied a component-based service model for early design space exploration and performance estimation.

Platform and MPSoC Analysis
Work on analysis complete the design techniques above, with simulation, and performance analysis techniques:

- We studied techniques for performance estimation of distributed real-time systems, based on simulation, in particular for applications using heterogeneous task scheduling policies. We also studied performance analysis techniques for a MPSoC in collaboration with ST Microelectronics.
- An important work direction is modelling and performance analysis for multi-processor and/or networked systems.

  We studied relations between simulation-based and analytical methods for performance evaluation of distributed real-time systems. Based on experimental simulation results, we were able to draw interesting conclusions regarding the pessimism of formal approaches. The experiments were performed on FlexRay and CAN-based distributed systems.

  We also studied interesting relations between MPA (Modular Performance Analysis) and Timed Automata.
- We have extended the fault-tolerant process model, to consider a combination of hardware and software fault-tolerant techniques. We have proposed a method for computing the reliability of a system, taking into account: a) hardening levels in hardware; b) the re-execution levels in software; c) scheduling for sharing recovery slacks.
- We have worked on modelling and optimisation of a miniaturized solar energy harvester. We focused on the optimisation of two important metrics: a) maximisation of the energy harvesting efficiency and b) the minimisation of the energy used for ineffective operations. A hierarchical control solution has been designed which overcomes several drawbacks of

previously proposed approaches. A novel algorithm for approximate multi-parametric linear programming has also been proposed.

- We studied scheduling-based energy optimisation techniques for energy-scavenging wireless sensor networks.

Design for Adaptivity (Transversal Integration activity)

We have worked mainly in two complementary directions: a) Study of architectures and algorithms for ensuring adaptivity; b) Study of modelling and analysis techniques for adaptive systems:

- We studied a symbolic quality control technique for multi-media applications. Adaptivity is ensured by using a controller, which moniotors system execution and adapts quality parameters of its functions so as to meet hard real-time contraints.
- We studied adaptive energy management techniques in clusters of wireless sensor nodes. They allow tuning the application parameters according to the time-varying amount of harvested energy.
- We studied reference architecture for self-configuring embedded systems in collaboration with Volvo. Algorithms suitable for runtime configuration management, load balancing and quality of service have been developed and adapted to automotive applications.
- We designed adaptive techniques to enhance real-time support of IEEE 802.11.e networks. For such networks, we developed protocols to enhance the resilience to interference, and to provide an estimation of a relative localisation based on the radio frequency signal.
- We studied techniques allowing the design and performance analysis for multi-mode systems. We also studied online performance analysis techniques for distributed systems. A novel distributed algorithm for control of the global analysis flow has been proposed.
- Several partners have collaborated in the STREP projects FRESCOR and ACTORS to develop an infrastructure for adaptive scheduling of real-time applications.

Design for Predictability (Transversal Integration activity)

The technical work on Predictability has intersected work in all the Thematic Clusters.

<u>Modeling and Validation of component –based systems</u>

- We studied the concept of predictability in relation with robustness, and identified two major challenges in embedded systems design. These challenges require a rethinking of the conventional, purely discrete and purely functional foundation of computing.
- We worked on modular performance analysis techniques, based on real-time calculus for systems with cyclic dependencies. We integrated a contract-based scheduling framework with a component-based technology.

<u>Timing Analysis and Compiler Techniques</u>

- The main contribution is work on relations between Timing Analysis and Timing Predictability. A definition of predictability for cache architectures has been proposed, and the relative competitiveness of 4 different cache replacement strategies has been analysed.

- We also investigated WCET analysis techniques for cooperative task scheduling. A method guiding developers of an embedded system to select optimal pre-emption points is under development.
- We also studied parameteric timing analysis techniques that overcome usual limitations of analysis techniques requiring the maximum number of loop iterations to be known statically.

OS/MW/Networks
Our work addressed various issues, including: Integrating scheduling analysis and model checking; influence of abstractions on the schedulability analysis of distributed real-time systems, time-predictable operating systems.

Architecture and System Design

- We studied techniques allowed predictability for fault-tolerant embedded systems and predictability for multi-processor MPSoC architectures.
- We also developed a set of parametyerisable models of L2 Caches and integrated them in an accurate virtual platform environment.
- Finally, we are designing a Precision Timed (PRET) architecture based on a reactive processor, coupled with a MicroBlaze general purpose processor.

Industrial Integration (Transversal Integration activity)

This activity groups a set of industrial interactions and collaborations with ArtistDesign teams. The long-term goal is to understand industrial design methodologies and identify the research results that could be applied in these methodologies.
The work this year has consisted in organising a few high-profile meetings with industry (eg: Embedded Systems: Industrial Applications ’08) as well as joint workshops and technical meetings.
At this point, these constitute a rich set of events and interactions, which need to be structured and which need a more specific focus.

4.2 Joint Programme of Integration Activities (JPIA)

Structure of the Integration Effort

The JPIA activities promote integration of geographically dispersed teamsand have long-lasting effects:
Joint Technical Meetings. Joint Technical meetings aim to present, discuss and integrate the ongoing work, and exchange points of view with other teams. They also serve to identify future work directions.
Staff Mobility and Exchanges. This is essential for integration within the NoE, including mobility of students and/or researchers, between core teams, or between core teams and affiliated teams. Mobility is justified by and refers to involvement in an activity from the JPRA or JPIA, or one of the following: co-funded scholarships with industry; exchange of students and personnel within the consortium.
Tools and Platforms. A research platform is composed of competencies, resources, and tools targeting specific technical and scientific objectives around a chosen topic. These are at the state-of-the-art, and are made available to the R&D community for experimentation, demonstration, evaluation, and teaching.

The research platforms, tools and facilities are an essential tool for implementing the JPIA. They will lay the groundwork for the JPRA, allowing common research to occur and capitalisation on research results. Platforms are used as the basis for transfer of research results to industry. They allow teaching practical knowledge of the concepts and techniques.
ArtistDesign platforms are not defined from scratch – they integrate the results of long-term efforts, and are meant to be durable, evolving with the state of the art. The partners are committed to durability, and have invested significant resources into their development. The construction of ArtistDesign has provided the opportunity to assemble existing pieces into a rationally-structured set of platforms, covering the area of embedded systems design.
Some of the ArtistDesign platforms have international visibility, and the ambition is for these to serve as world-wide references in their respective topics.
The detailed information regarding the JPIA activities is available in the JPIA deliverable.

Assessment

The ArtistDesign Network of Excellence is a significant evolutionary step for integrating the leading embedded systems design research teams in Europe. The clusters are more tightly woven together, and each represents a significantly greater critical mass than did the clusters in the Artist2 Network of Excellence, which ended Sept 30th 2008, and has nearly the same consortium.
Despite this strong overlap with the Artist2 NoE, the overall assessment for the WP at the end of ArtistDesign Y1 (Jan–Dec 2008) is positive - both in terms of impact on the overall structuring and lasting integration within the consortium and more generally within the area in Europe.

- The ArtistDesign clusters have been actively pursuing operational integration through joint meetings, staff mobility, and shared platforms and tools.
- The level of activity shows that the Cluster / Activity structure and research topics defined for ArtistDesign make sense, and are viable vehicles for integrating the area. In operational terms, they generate sufficient interest for the partners and individual researchers to participate actively in the joint meetings, to exchange personnel, and to orient the tools and platforms developed to make sense within this structure.
- There is clearly a greater level of maturity for tools and platforms than had been the case at the start of the Artist2 NoE – and the partner teams are actively pursuing a policy of implementing tools, demonstrators, and in many cases their accompanying methodologies.
- Nonetheless, it is important to remember that these are tools and platforms for research. The aim is not necessarily always for these to lead to commercially viable tools and start-up companies. In general, they are the concrete realisation of the state-of-the-research, allowing to explore possibilities for future research and later tools (some of which may in turn lead to commercially viable products).
- The level of activity varies according to individual clusters / activities, which is normal. We believe this is partly due to the remaining overlap with Artist2 – which should no longer be the case in Y2.

4.3 Jointly-executed Programme of Activities for Spreading Excellence (JPASE)

ArtistDesign leverages on the worldwide visibility of the ARTIST2 NoE. It is progressively creating a European embedded systems design community and spreading the "Artist culture" in all major research institutions.
To ensure that the next generation of researchers will continue in this direction we, as a consortium, devote a great deal of effort to Spreading Excellence, in both academic and industrial circles. Furthermore, through our links with both core and affiliated partners, we actively set up permanent links between industry and public research, based on existing partner collaborations with major industrial players in the area.
The JPASE activities are intended to spread excellence and structure the community at large. They are planned by the Strategic Management Board, and are implemented by ArtistDesign core and affiliated partners.
The NoE will leverage on its members and teams, who play a main role in the organisation of world-class scientific events, to disseminate results in the area. We expect that the NoE's structured and authoritative dissemination will have a strong effect on the community as a whole, for orienting and creating synergy for research.

Education and Training

- Courseware – The NoE has the ambition to serve as a resource and point of reference for the area, including by collecting and disseminating course materials for teaching embedded systems design.
- Graduate Studies – The NoE will provide support for selected graduate studies programmes, as the means for training engineers and researchers in embedded systems design.
- Summer Schools – The NoE will actively support and participate in summer schools and seminars in embedded systems design.
- International Workshop on Embedded Systems Education – We will continue this series of international workshops, started in ARTIST2. York has accepted to lead this activity.
- Implement a high-visibility International Summer School. The ArtistDesign NoE will organise each year a high-visibility international Summer School, drawing top European lecturers in Embedded Systems Design. The audience is researchers, PhD students, and engineers. The following group of core partners will lead this activity: Luca Benini (Bologna), Giorgio Buttazzo (SSSA-Pisa), Petru Eles (Linkoping), Kim Larsen (Aalborg), Peter Marwedel (Dortmund).
- Training Engineers – Many partners are already active in this area, such as IMEC, EPFL, ESI, and Aalborg's CSI. The ArtistDesign NoE will provide logistical, financial dissemination through the Web Portal and newsletter.

Publications in Conferences and Journals

The ArtistDesign consortium is very active in publishing in scientific journals and conferences, as attested by the list of significant publications by the partners' teams.
The NoE leverages on its members and teams, who are strongly implicated in collaboration with industry, to organize and structure industrial relations, and develop mutually beneficial interactions. Furthermore, through Industrial Liaison, ArtistDesign receives useful feedback about the relevance of work directions and priorities.

Links to Artemisia

ArtistDesign seeks a tight interaction with the Artemis community, through the **Artemisia Liaison Task Force**. This is composed of the following prominent ArtistDesign members, also active in ARTEMIS/ARTEMISIA: Luca Benini, Ed Brinksma, Werner Damm, Jean-Luc Dormoy, Rudy Lauwereins, and Joseph Sifakis. Amongst these, 3 are elected members of the ARTEMIS Steering Board. Joseph Sifakis is the chair of ARTEMISIA's Chamber B.

ArtistDesign partners will be encouraged to join ARTEMISIA.

International Collaboration

The ArtistDesign "*International Collaboration*" activities allow ArtistDesign to be visible internationally, and to monitor the evolution of the state of the art in the area worldwide.
International Collaboration fits into a global win-win strategy for achieving the participants' long-range aims. Examples of activities include:

- **High-level meetings** gathering top representatives from industry, funding agencies, and research, to discuss avenues for International Collaboration, including on R&D and standards e.g. IST/NSF Workshop on Component-based Engineering (Paris, June 05).
- International Collaboration **Working Groups** for exploring possible avenues for research and education in a chosen topic and producing white papers and reports e.g. joint EU/US Working Groups: on Timing Validation, Adaptive Real-Time Systems for Dynamic Applications, Semantic Platform for Hard Real Time (2002 – 2003).
- Organization and sponsoring of international conferences and schools, to disseminate recent research results, and promote the emergence of embedded systems as a discipline e.g. Embedded Systems Week, New Jersey, October 2005.
- International Collaboration **Publications**.
- **Joint international projects**. Set up joint collaborative projects e.g. Columbus project or extend existing projects, by allotting them an extra budget.

International Collaborations is implemented mainly in collaboration with the USA, building on existing links between IST and the US funding agencies (mainly NSF).
ArtistDesign leverages on and extend the successful International Collaboration activities initiated in the ARTIST2 NoE.

The following table shows the consumption of manmonths by partner and by work package.

ARTISTDESIGN - Breakdown of manmonth / year1

	TOTAL		WP10		WP11		WP12		WP13		WP14		WP15		WP16		WP17		Total Project in Person-Months
	Actual / PF total:	7.29	Actual / PF total:	6.93	Actual / PF total:	17.30	Actual / PF total:	9.07	Actual / PF total:	6.75	Actual / PF total:	11.76	Actual / PF total:	9.43	Actual / PF total:	19.91	Actual / PF total:	17.13	Actual total:	98.64
	Planned / PF total:	51.00	Planned / PF total:	37.50	Planned / PF total:	320.50	Planned / PF total:	106.75	Planned / PF total:	87.25	Planned / PF total:	79.25	Planned / PF total:	73.00	Planned / PF total:	80.50	Planned / PF total:	109.00	Planned total:	907.25
Partner 1 FLORALI$				0.38															6.93
Partner 2 UJF Verimag						2.38		2.35		2.59									8.52
Partner 3 Aachen												2.00							2.00
Partner 4 Aalborg														1.87					4.80
Partner 5 Aveiro						1.47	0.50	0.83	0.50								0.93	1.25	3.50
Partner 6 Bologna															1.25	2.50			3.75
Partner 7 TUBS																	0.84		4.98
Partner 8 Cantabria						0.01		0.10	0.60					1.53				3.34	2.44
Partner 9 CEA										1.60								0.24	6.00
Partner 10 DTU												1.00			6.00				1.51
Partner 11 Dortmund					0.10	0.10	0.30	0.10		0.50								0.11	0.80
Partner 12 EPFL					0.41	1.20	5.04	0.75				1.87		0.88	3.75	2.31			1.24
Partner 13 E$I										0.75								0.83	6.96
Partner 14 ETH Zurich												3.00						2.00	12.96
Partner 15 IMEC																		1.31	2.02
Partner 16 INRIA												0.76							0.00
Partner 17 TUKL																			0.00
Partner 18 KTH															4.10			1.40	5.50
Partner 19 Linkoping																			0.00
Partner 20 Ulund										0.50	0.25							1.00	4.00
Partner 21 MDH																		1.12	0.50
Partner 22 OFFIS																			1.43
Partner 23 Parade$												0.76						1.00	0.76
Partner 24 Passau														2.00	3.16				6.00
Partner 25 $$$A PI$A																			6.20
Partner 26 Porto																			2.25
Partner 27 Saarland										0.66								0.13	1.50
Partner 28 PLU Salzburg																			1.27
Partner 29 Uppsala																			0.00
Partner 30 Vienna																		0.38	2.33
Partner 31 YORK																			0.00

At project level, there is no significant deviation of consumption of manmonths to claim. We can also point out that the global rate of consumption is quite low.

Some partners did not declare any personnel costs (no manmonths allocated to the project over the first year) with any adjustments planned retrospectively for next year. The reason given to the coordinator to explain why this is the case is that personnel time and personnel costs had already been claimed on the Artist 2 project which stopped on August 2008.

In a nutshell, 10.87% of global estimated manmonths had been consumed over the first year of the project.

At each WP level, the rate of consumption goes from 5 to 24%. The following table explains the global consumption of manmonth by WP.

		TOTAL	% of manmonth consumption by WP
WP00	Actual WP total:	7,29	14,29%
	Planned WP total:	51,00	
WP01	Actual WP total:	17,30	5,40%
	Planned WP total:	320,50	
WP02	Actual WP total:	9,07	8,50%
	Planned WP total:	106,75	
WP03	Actual WP total:	6,75	7,74%
	Planned WP total:	87,25	
WP04	Actual WP total:	11,76	14,84%
	Planned WP total:	79,25	
WP05	Actual WP total:	9,43	12,92%
	Planned WP total:	73,00	
WP06	Actual WP total:	19,91	24,73%
	Planned WP total:	80,50	
WP07	Actual WP total:	17,13	15,72%
	Planned WP total:	109,00	
Total Project in Person-Months	Actual total:	98,64	10,87%
	Planned total:	907,25	

5. Deliverables and milestones tables

Table 1.Deliverables - Year 1

Del N°	Deliverable name	WP N°	Lead participant	Nature	Dissemination level	Due delivery date from Annex 1	Delivered Yes/No	Actual / Forecast delivery date	Deliverable ID on Artistdesign website
WP0 : Joint Programme of management activities (JPMA)									
D-0.1	Project management report	0	Floralis UJF/Verimag	Report	Public	T0+12	YES	Actual delivery date	Floralis D1-(0.1)-Y1
D-0.1	Project activity report	0	UJF/Verimag	Report	Public	T0+12	YES	Actual delivery date	UJF/VERIMAG D2-(0.2)-Y1
WP1 : Joint programme of integration activities (JPIA)									
D-1.0	Integration activities report	1	UJF/Verimag	Report	Public	T0+12	YES	Actual delivery date	UJF/Verimag D3-(1.0)-Y1
WP2 : Joint programme of activities for spreading excellence (JPASE)									
D-2.0	Spreading excellence report	2	UJF/Verimag	Report	Public	T0+12	YES	Actual delivery date	UJF/Verimag D4-(2.0)-Y1
WP3 : Thematic cluster : modeling and validation (JPRA)									
D-3.1	Modelling report	3	Aalborg	Report	Public	T0+12	YES	Actual delivery date	EPFL D5-(3.1)-Y1
D-3.2	Validation report	3	Aalborg	Report	Public	T0+12	YES	Actual delivery date	Aalborg D6-(3.2)-Y1
WP4 :Thematic cluster : Software synthesis, code generation and timing analysis (JPRA)									
D-4.1	Software synthesis, code generation	4	Dortmund	Report	Public	T0+12	YES	Actual delivery date	Dortmund D7-(4.1)-Y1
D-4.2	Timing analysis	4	Dortmund	Report	Public	T0+12	YES	Actual delivery date	Saarland D8-(4.2)-Y1
WP5 :Thematic cluster : Operatng systems and networks (JPRA)									
D-5.1	Resource-aware operating systems	5	Pisa	Report	Public	T0+12	**YES**	Actual delivery date	PISA D9-(5.1)-Y1
D-5.2	Scheduling and ressource management	5	Pisa	Report	Public	T0+12	**YES**	Actual delivery date	York D10-(5.2)-Y1
D-5.3	Embedded real-time networking	5	Pisa	Report	Public	T0+12	**YES**	Actual delivery date	Aveiro D11-(5.3)-Y1
WP6 : Thematic cluster : Hardware platforms and MPSoC design									
D-6.1	Platform and MPSoC design	6	DTU	Report	Public	T0+12	YES	Actual delivery date	Bologna D12-(6.1)-Y1
D-6.2	Platform and MPSoC analysis	6	DTU	Report	Public	T0+12	YES	Actual delivery date	DTU D13-(6.2)-Y1
WP7 : Transversal Integration (JPRA)									
D-7.1	Design for adaptivity	7	PARADES	Report	Public	T0+12	YES	Actual delivery date	Lund D14-(7.1)-Y1
D-7.2	Design for predictability	7	PARADES	Report	Public	T0+12	YES	Actual delivery date	Uppsala D15-(7.2)-Y1
D-7.3	Industrial integration	7	PARADES	Report	Public	T0+12	YES	Actual delivery date	PARADES D16-(7.3)-Y1

Milestones

Table 2. Milestones - Year 1

Milestone N°	Milestone name	Due achievement date from Annex 1	Achieved Yes/No	Actual / Forecast achievement date	Comments
M-Indus-Y1	Industrial liason : ARTEMISIA - Y1	T0+12	YES	Actual achievement date	ArtistDesign seeks a tight interaction with the Artemis community, through the Artemisia Liaison Task Force. This is composed of the following prominent ArtistDesign members, also active in ARTEMIS/ARTEMISIA: Luca Benini, Ed Brinksma, Werner Damm, Jean-Luc Dormoy, Rudy Lauwereins, and Joseph Sifakis. Amongst these, 3 are elected members of the ARTEMIS Steering Board. Joseph Sifakis is the chair of ARTEMISIA's Chamber B. ArtistDesign partners will be encouraged to join ARTEMISIA.
M-Web-Y1	Web Y1	T0+12	YES	Actual achievement date	The ArtistDesign Web Portal is a major tool for Spreading Excellence within the Embedded Systems Community. It aims to be the focal point of reference for events and announcements of interest to the embedded systems community. This will play a key supporting role for collaboration and Integration, such as interaction between clusters, management information, such as scholarships, internal events, and progress of the work. The web portal will also be used to disseminate any relevant information to the community at large. We believe the web portal will be an essential mechanism for achieving integration. It acts as a repository of knowledge in the area, including courseware, information about standards, methods and tools, research publications and results. This web portal will be made available within the NoE core and affiliated partners, and to other parties.
M-Web-Y1	International Collaboration Y1	T0+12	YES	Actual achievement date	The ArtistDesign "International Collaboration" activities allow ArtistDesign to be visible internationally, and to monitor the evolution of the state of the art in the area worldwide. International Collaboration fits into a global win-win strategy for achieving the participants' long-range aims. Examples of activities include: • High-level meetings gathering top representatives from industry, funding agencies, and research, to discuss avenues for International Collaboration, including on R&D and standards e.g. IST/NSF Workshop on Component-based Engineering (Paris, June 05). • International Collaboration Working Groups for exploring possible avenues for research and education in a chosen topic and producing white papers and reports e.g. joint EU/US Working Groups: on Timing Validation, Adaptive Real-Time Systems for Dynamic Applications, Semantic Platform for Hard Real Time (2002 – 2003). • Organization and sponsoring of international conferences and schools, to disseminate recent research results, and promote the emergence of embedded systems as a discipline e.g. Embedded Systems Week, New Jersey, October 2005. • International Collaboration Publications. • Joint international projects. Set up joint collaborative projects e.g. Columbus project or extend existing projects, by allotting them an extra budget. International Collaborations is implemented mainly in collaboration with the USA, building on existing links between IST and the US funding agencies (mainly NSF). ArtistDesign leverages on and extend the successful International Collaboration activities initiated in the ARTIST2 NoE.

6. Project management

6.1 Consortium Management Tasks

The consortium management is carried out by the ArtistDesign Strategic Management Board (http://www.artist-embedded.org/artist/-Strategic-Management-Board,938-.html): Joseph Sifakis – chair (UJF/VERIMAG), Luis Almeida (Univ Porto), Karl-Erik Årzén (Lund), Luca Benini (Bologna), Albert Benveniste (INRIA), Bruno Bouyssounouse (UJF/VERIMAG), Alan Burns (York), Giorgio Buttazzo (Pisa), Tom Henzinger (EPFL), Bengt Jonsson (UPPSALA), Kim Larsen (Aalborg), Jan Madsen (DTU), Peter Marwedel (TU Dortmund), Alberto Sangiovanni (PARADES), Lothar Thiele (ETH Zurich), Reinhard Wilhelm (Saarland University).

The Scientific Coordinator is Joseph Sifakis; the Technical Coordinator is Bruno Bouyssounouse, the Administrative and Financial Coordinator is Olivier Guérard.

The management tasks include (but are not limited to):

- Organize the technical work and meetings
- Ensure that work progresses on track
- Organize, collect and finalize the technical reporting
- Organize, collect and finalize the financial and administrative reporting
- Organize the Spreading Excellence Activities (see the deliverable), and implement the main ones (others are implemented by the partners).
- Take care of management issues (evolution of the budget, changes to the consortium, etc).

At the end of the first year of the project, an amendment has been required by the coordinator in order to update the financial situation between partner n°1 (Floralis) and partner n°2 (UJF/Verimag). The technical coordinator (Bruno Bouyssounouse) was not employed by Floralis but by UJF/Verimag so we had to transfer provisional budget in order to ensure that key tasks were effectively carried out.

The first amendment, the new version of Annex 1 (DoW) has been approved by the Commission on the 21st of January, 2009.

The management achievements include:

- A successful Year 1 (all of the points above).

6.2 Problems that have occurred

- No particular problems occurred over the course of year 1.

6.3 Changes in the consortium

Only points 2, 3 and 6 require amendments to the EC Contract.

The following changes are implemented at the end of year 1:

1. The main representative for the Embedded Systems Institute (ESI), Ed Brinksma, is leaving to become Rector Magnificus at the University of Twente. He is replaced by Boudewijn Haverkort.

The following changes are anticipated in Year 2:

2. It is possible that PARADES will cease to exist, and thus implicitly withdraw from the project. In this case, PARADES' responsibilities would be taken up by other partners, with corresponding shifts in the budget structure.
3. Tom Henzinger, leader for EPFL will be moving to a new institute he is creating, called IST Austria. IST will become a new partner to the ArtistDesign project. EPFL remains a partner too.
4. Suzanne Graf will replace Tom Henzinger as leader of the "Modelling" activity, and will be co-leader of the "Modelling and Validation" cluster.
5. The new representative for EPFL will be Giovanni De Micheli.
6. Luis Almeida will be moving to University of Porto. University of Aveiro becomes an affiliated partner, and the University of Porto (distinct legal entity from ISEP) becomes a new partner, with Aveiro's budget - effective July 1st 2009.

6.4 Project Meetings, Dates, Venues

The ArtistDesign Kickoff meeting was held January 29-30th, 2008 in Paris.
Joint Technical meetings aim to present, discuss and integrate the ongoing work, and exchange points of view with other teams. They also serve to identify future work directions.

They are often organized around the annual General Assembly and Review, or around some of the main conferences in the area (most of which are piloted by a majority of ArtistDesign partners).

Depending on the context and in particular on the maturity of the topics under discussion, these Joint Technical Meetings may be open to the public, or by invitation (which implicitly includes all interested ArtistDesign partners).

Joint technical meetings for the Modelling and Validation Cluster

Organization of the workshop: Veronique Bruyere and Jean-Francois Raskin. "Automata and Verification", University of Mons-Hainaut, Belgium, August 25-26, 2008.

Summer school: Movep 08: Co-organization of the Movep school (http://www.univ-orleans.fr/movep2008/) about modelling and verifying parallel processes in June 2008, partially funded by Artist 2.

RTSS08 track on Design and Verification of Embedded Real-Time Systems, the 29th IEEE Real-Time Systems Symposium. Barcelona, Spain. November 30 - December 3, 2008.

This is one of the four tracks of RTSS 2008.
The objective is to promote research on design and analysis, and verification of embedded real-time systems. It intends to cover the whole spectrum from theoretical results to concrete applications with an emphasis on practical and scalable techniques and tools providing the designers with automated support for obtaining high-quality software and hardware systems. A particular goal is to provide a forum for interaction between different research communities, such as scheduling, hardware/software co-design, and formal techniques. http://www.rtss.org

Workshop : SafeCert 2008, International Workshop on the Certification of Safety-Critical Software Controlled Systems, ETAPS 2008 Budapest, Hungary, 29 March, 2008, organized by TU Braunschweig and OFFIS.
The need for certification, like for instance in the rail sector, imposes the burden of not only validating a system, but also proving in a juridical sense, that the validation can be trusted. The major question addressed in the workshop was how to embed formal methods and tools in a seamless design process which covers several development phases and which includes an efficient construction of a safety case for the product. http://safecert08.offis.de/

Workshop FIT 2008: Foundation of Interface Theories ETAPS 2008 Budapest, Hungary, 29 March, 2008, organized by CISS, Aalborg University and ITU, Copenhagen. Invited presentations from INRIA, Rennes, and Twente U.
Component-based design is widely considered as a major approach to developing systems in a time and cost effective way. Central in this approach is the notion of an interface. Interfaces summarize the externally visible properties of a component and are seen as a key to achieving component interoperability and to predict global system behavior based on the component behavior. To capture the intricacy of complex software products, rich interfaces have been proposed. These interfaces do not only specify syntactic properties, such as the signatures of methods and operations, but also take into account behavioral and extra-functional properties, such as quality of service, security and dependability. Rich interfaces have been proposed for describing, e.g., the legal sequences of messages or method calls accepted by components, or the resource and timing constraints in embedded software. The development of a rigorous framework for the specification and analysis of rich interfaces is challenging. The aim of this workshop is to bring together researchers who are interested in the formal underpinnings of interface technologies.

Workshop: 1st International Workshop on Model Based Architecting and Construction of Embedded Systems
Toulouse -- September 29th, 2008
This ARTIST workshop is held in conjunction with MODELS 2008 as a follow-up workshop of the SVERTS and MARTE workshops organised in previous years, the objective of this workshop is to bring together researchers and practitioners interested in model-based software engineering for real-time embedded systems. We are seeking contributions relating to this subject at different levels, from modelling languages and semantics to concrete application experiments, from model analysis techniques to model-based implementation and deployment. Given the criticality of the application domain, we particularly focus on model-based approaches yielding efficient and provably correct designs. Concerning models and languages, we welcome contributions presenting novel modelling approaches as well as contributions evaluating existing ones. The organisers of this workshop are partners from the ASSERT and SPICES project; the ARTIST partners are CEA and Verimag.
http://www.artist-embedded.org/artist/ACES-MB-08.html

Workshop SLA++P 2008: Model-driven High-level Programming of Embedded Systems
European Joint Conference on Theory and Practice of Software ETAPS 2008
Budapest, Hungary – April 5th, 2008
SLA++P is a workshop dedicated to synchronous languages and the model-driven high-level programming of reactive and embedded systems. Firmly grounded in clean mathematical semantics, synchronous languages are receiving increasing attention in industry ever since they emerged in the 80s. Lustre, Esterel, Signal are now widely and successfully used to program real-time and safety critical applications, from nuclear power plant management layer to Airbus air flight control systems. At the same time, model-based programming is making its way in other fields of software engineering, too, often involving cycle-based synchronous paradigms. The purpose of the SLA++P workshop is to bring together researchers and practitioners who work in the field of languages and tools for the model-driven development of embedded applications both in hardware and software. The workshop is not limited to synchronous approaches but open to other engineering design approaches with strong semantical foundations providing a way to go from a high-level description to provable executable code. http://www.artist-embedded.org/artist/SLA-P-2008,1231.html

Workshop : ACESMB 2008, 1st Int. Workshop on Model Based Architecting and Construction of Embedded Systems
ACM/IEEE 11th Int. Conf. on Model Driven Engineering Languages and Systems
Toulouse, France - September 29th, 2008
New real-time systems have increasingly complex architectures because of the intricacy of the multiple interdependent features they have to manage. They must meet new requirements of reusability, interoperability, flexibility and portability. These new dimensions favour the use of an architecture description language that offers a global vision of the system, and which is particularly suitable for handling real-time characteristics. Due to the even more increased complexity of distributed, real-time and embedded systems (DRE), the need for a model-driven approach is more obvious in this domain than in monolithic RT systems. The purpose of this workshop is to provide an opportunity to gather researchers and industrial practitioners to survey existing efforts related to behaviour modelling and model-based analysis of DRE systems. This workshop sought contribution from researchers and practitioners interested in all aspects of the representation, analysis, and implementation of DRE system behaviour and/or architecture models.
http://www.artist-embedded.org/artist/ACES-MB-08.html

Workshop: UML & AADL 2008
13th IEEE International Conference on Engineering of Complex Computer Systems
Belfast, Northern Ireland - April 2nd, 2008
New real-time systems have increasingly complex architectures because of the intricacy of the multiple interdependent features they have to manage. They must meet new requirements of reusability, interoperability, flexibility and portability. These new dimensions favour the use of an architecture description language that offers a global vision of the system, and which is particularly suitable for handling real-time characteristics. Due to the even more increased complexity of distributed, real-time and embedded systems (DRE), the need for a model-driven approach is more obvious in this domain than in monolithic RT systems. The purpose of this workshop is to provide an opportunity to gather researchers and industrial practitioners to survey existing efforts related to behaviour modelling and model-based analysis of DRE systems. This workshop sought contribution from researchers and practitioners interested in all aspects of the representation, analysis, and implementation of DRE system behaviour and/or architecture models.
http://www.artist-embedded.org/artist/Topics,1199.html

Joint technical meetings for the Software Synthesis, Code Generation and Timing Analysis cluster

Course: Peter Marwedel, Rainer Leupers: Retargetable Compilation

Lugano, Switzerland, Feb. 25-29., 2008

The course consisted of two parts: the first part (by Peter Marwedel) focused on memory-architecture aware compilation. The second part (by Rainer Leupers, RWTH Aachen) focused on processor retargetability. The course was supported by ALARI. http://www.alari.ch

Tutorial: Peter Marwedel, Embedded Systems in a Nutshell, Spring School on Knowledge Discovery in Ubiquitous Systems,

Porto, Portugal, March 2, 2008

This tutorial provided a brief overview over specification techniques, hardware, scheduling and optimization of embedded systems for a community without any pre-existing knowledge on embedded systems. http://www.kdubiq.org

Tutorial: Rainer Leupers, Gerd Ascheid (RWTH Aachen), Wilfried Verachtert, Tom Ashby, Arnout Vandecappelle (IMEC): System-Level Design and Application Mapping for Wireless and Multimedia MPSoC Architectures

DATE 2008

Munich, Germany, March 10, 2008

Advanced embedded devices such as multi-standard mobile terminals demand ever-increasing performance and energy efficiency. Simultaneously, a high degree of flexibility and programmability is required due to increasing software complexity and fast changing protocol and codec standards. This has led to the concept of MPSoC (Multi-Processor System-on-Chip) platforms. In many cases, MPSoCs are simply assembled in "best effort" manner from existing legacy IP components, and programming the platform presents a major bottleneck. As Moore´s Law permits us to enter the "many core" MPSoC area, what is needed is a systematic approach that builds on well-proven technologies, but also innovates with novel classes of electronic system-level (ESL) design automation tools.

This tutorial discussed several key questions with significant impact on the future of MPSoC: What are the MPSoC killer applications? Is homogeneous or heterogeneous architecture the right choice? What are the key tools, methodologies and programming models for successfully designing and programming MPSoC platforms? In the end, will there be only a few survivor platforms that everyone has to accept? Based on their extensive research and industry experience, the presenters provided their answers from a practical, application-oriented perspective.

http://www.date-conference.com/archive/conference/proceedings/PAPERS/2008/DATE08/PDFFILES/TUTORIALS.PDF

Workshop: Software & Compilers for Embedded Systems (SCOPES) 2008

Munich, Germany – March 13-14, 2008

SCOPES focuses on the software generation process for modern embedded systems. Topics of interest include all aspects of the compilation process, starting with suitable modelling and specification techniques and programming languages for embedded systems. The emphasis of the workshop lies on code generation techniques for embedded processors. The exploitation of specialized instruction set characteristics is as important as the development of new optimizations for embedded application domains. Cost criteria for the entire code generation and optimization process include runtime, timing predictability, energy dissipation, code size and others. Since today's

embedded devices frequently consist of a multi-processor system-on-chip, the scope of this workshop is not limited to single-processor systems but particularly covers compilation techniques for MPSoC architectures.

In addition, this workshop puts a spotlight on the interactions between compilers and other components in the embedded system design process. This includes compiler support for e.g. architecture exploration during HW/SW codesign or interactions between operating systems and compilation techniques. Finally, techniques for compiler aided profiling, measurement, debugging and validation of embedded software were also covered by this workshop, because stability of embedded software is mandatory.

SCOPES 2008 was the 11th workshop in a series of workshops initially called "International Workshop on Code Generation for Embedded Processors". The name SCOPES has been used since the 4th workshop. The scope of the workshop remains software for embedded systems with emphasis on code generation (compilers) for embedded processors.

SCOPES 2008 was organized by Heiko Falk from TU Dortmund and was held as DATE Friday Workshop. There were many discussions between cluster members at SCOPES (starting already on the eve before the sessions), at DATE and during an Artist2 meeting during the same week, making the entire week the key joint event in spring. http://www.scopesconf.org/scopes-08

Keynote: Rainer Leupers: ESL Design Technologies for Wireless and Multimedia MPSoC Architectures

3rd International Symposium on Industrial Embedded Systems (SIES 2008)

La Grande Motte, June 11-13, 2008 http://www.lirmm.fr/SIES2008/

Meeting: 1st Workshop on Mapping Applications to MPSoCs, 2008

St. Goar, *Germany – June 16-17, 2008*

Objectives for the meeting: The goal of the ArtistDesign workshop was to identify requirements and partial solutions for the problem of mapping applications to MPSoCs. It was considered to be the starting point for more intensive cooperations in the ArtistDesign framework. Also, members of other projects (hipeac2, ACOTES) were invited.

Organizer: Peter Marwedel (TU Dortmund)

Other participants: there were a total of 37 participants.

Conclusions: The topic was partitioned into two related areas: mapping and code generation. Working groups were formed and it was agreed to have joint follow-up workshops.

http://www.artist-embedded.org/artist/Mapping-of-Applications-to-MPSoCs.html

Meeting: Working Meeting IFIP 2.11 (Program Generation)

Passau, *Germany – Jun. 19-21, 2008*

Objectives for the meeting: General discussion on the future of program generation.

Organizer: Christian Lengauer (U. Passau)

Other participants: IFIP 2.11.

Forum: 8th International Forum on Application-Specific Multi-Processor SoC, 2008
Aachen, Germany, 23 - 27 June 2008,

MPSoC is a pluridisciplinary forum bringing together key R&D actors from the different fields required to design heterogeneous multiprocessor SoC (MPSoC). MPSoC '08, 8th event of the forum series, was held on 23-27 June 2008 at Château St. Gerlach (near Aachen) and was organized by ISS/SSS, RWTH Aachen University. Rainer Leupers from RWTH Aachen was one of the general co-charis of this premier event. The full week format and the quality of both attendees and speakers made MPSoC '08 a unique occasion for executives and senior managers to explore new ideas and refine strategic thinking. The program brought together key actors from IP, fabless, semiconductor, system houses and design industry to build a vision of the next step in integrated system design. More than 50 world class R&D speakers discussed fundamental and strategic issues to master multi-processor SoC design. This year's technical sessions presented strategic directions and state-of-the-art research, covering topics like MPSoC Architecture, MPSoC Application Platforms, MPSoC Programming, MPSoC Design methodologies, etc. The detailed program and the slides from the speakers can be found in the event's website.

Organizer: Rainer Leupers, Heinrich Meyr (RWTH Aachen)

http://www.mpsoc-forum.org

Workshop: 8th Int'l Workshop on Worst-Case Execution Time Analysis (WCET'08)
Prague, Czech Republic – July 1st, 2008

The 8th International Workshop on Worst-Case Execution Time Analysis (WCET 2008) was held as a satellite event to the 20th Euromicro Conference on Real-Time Systems (ECRTS 2008). The goal of the workshop is to bring together people from academia, tool vendors and users in industry that are interested in all aspects of timing analysis for real-time systems. The workshop fosters a highly interactive format with ample time for in-depth discussions. It provides a relaxed forum to present and discuss new ideas, new research directions, and to review current trends in this area. The presentations are kept short to leave plenty of time for interaction of attendees.

The WCET 2008 event of this workshop has gained on popularity, it had 45 registered participants. This tendency may be interpreted that the real-time community becomes increasingly aware of the importance of WCET analysis. The workshop program included four regular sessions with 13 talks on WCET analysis. Additionally an invited talk on timing analysis at system level was given by Prof. Rolf Ernst and the current results of the WCET Tool Challenge 2008 were presented by the organizer, Niklas Holsti.

http://www.artist-embedded.org/artist/WCET-08.html

Keynote: Constructing Time-Critical Embedded Systems: Use Your Intelligence before Runtime
6th Workshop on Intelligent Solutions in Embedded Systems
Regensburg, Germany – July 10-11, 2008

This presentation, given by Peter Puschner, examined the complexity of contemporary hardware and software architectures and demonstrated how the sophisticated mechanisms used lead to difficulties in understanding and analysing the timing of embedded real-time applications. It was argued that a new trend towards simplicity is needed that avoids speculation and minimizes the number of dynamic decisions taken at runtime. Following these principles one can eliminate timing variations, system timing becomes easy to understand, and proofs for temporal correctness turn out to be almost trivial. http://fbim.fh-regensburg.de/~wises08/index.htm

Tutorial: Timing Analysis and Timing Predictability
Embedded Networked Systems: Theory and Applications
Heraklion, Crete – July 21–25, 2008
The 2008 Lectures in Computer Science of the Onassis Foundation were dedicated to theory and applications of Embedded Systems. Among the talks by leading researchers was a two-part tutorial by Reinhard Wilhelm on Timing Analysis and Timing Predictability.
http://www.forth.gr/onassis/lectures/2008-07-21/lecturers.html

Invited Course: Peter Marwedel, Heiko Falk, Embedded Systems with Emphasis on the Exploitation of the Memory Hierarchy
Advanced Institute of Information Technology
Seoul, Korea – August 11-15, 2008
The goal of this course is to provide an overview over key areas in embedded system design which should be taught at Universities. After attending the course, the attendees should be able to compare different approaches to embedded system design education and their advantages and limitations. The attendees will also become familiar with the contents of a course on embedded system design which aims targets second or third year students. The course should enable attendees to design the structure of embedded system education at their universities. In the last third of the course, attendees will be introduced to research topics regarding embedded system optimization. In particular, this last third will address the so-called memory wall problem (the problem resulting from the small performance improvements of memories). This problem is frequently seen as the key problem for further performance enhancements of future systems. This material would be appropriate for an advanced course in embedded system design.

Peter Marwedel and Heiko Falk from TU Dortmund lectured this one-week course for Korean professors (CS and EE) after an invitation by the (South) Korean Advanced Institute of Information Technology. http://ttt.aiit.or.kr

Tutorial: Peter Marwedel: Memory architecture aware compilation for Embedded Systems
Artist South American Summer School
Florianopolis, Brazil, Aug. 25.-29., 2008
The tutorial focused on compilation techniques exploiting descriptions of the memory architecture.
http://www.artist-embedded.org/artist/Objectives,1365.html

ARTIST2 Summer School 2008 in Autrans:
Autrans, France, Sept. 8th-12th, 2008

- **Tutorial/Invited Talk: Peter Marwedel, Heiko Falk: Memory architecture aware compilation**
  This talk gave an overview over compilation for scratchpad memories and linked it to worst case execution time aware compilation.
- **Tutorial/Invited Talk: Reinhard Wilhelm: Timing Analysis and Timing Predictability**
  This talk gave an overview over recent techniques for timing analysis.

http://www.artist-embedded.org/artist/ARTIST2-Summer-School-2008.html

Invited talk: Peter Marwedel: Mapping of Applications to MPSoCs
4th Compiler Assisted SoC Assembly Workshop (CASA08)
Atlanta, USA – Oct. 19th, 2008
The talk summarized the presentations of the "1st workshop on the mapping of applications to MPSoCs" for a wider audience. http://www.esweek.org/

Workshop: 4th Workshop on Embedded Systems Education, 2008
Atlanta, US, – October 23rd, 2008
Embedded system education is still a very young area and frequently restricted to teaching the details of microcontroller programming. A long-term objective of this workshop is to stimulate the introduction of broader curricula. Also, there will be more emphasis on publishing the results of the workshop online and in journals. http://www.esweek.org/

Meeting: Working Meeting on Mapping Applications to MPSoCs (*Fall Activity meeting*).
Düsseldorf, *Germany – Nov. 27th-28th, 2008*
Objectives for the meeting: The goal of the ArtistDesign meeting was to intensify the discussions started at the Rheinfels workshop and to advance the cooperation between the partners.
Organizer: Peter Marwedel (TU Dortmund)
Other participants: there were a total of 25 participants.
Conclusions: Details of the cooperation between the partners were fixed.

Keynote: Rainer Leupers: Advanced MPSoC design technologies in the UMIC project
J-CING (Japan – CoWare Innovators Group) 2007
Tokyo, Nov. 30th, 2007 http://www.coware.co.jp/J-CING/keynote2.html

Joint technical meetings for the Operating Systems and Networks cluster

Meeting: APRES 2008: Workshop on Adaptive and Reconfigurable Embedded Systems
St. Louis, MO, USA – April 21st, 2008
Objectives for the meeting: The purpose of the workshop was to discuss new and on-going research that is centered on the idea of adaptability as first class citizen and consider the involved tradeoffs. The workshop provided an open forum to discuss ideas and approaches, and intended to give the attendees a chance to discuss them in a relaxed environment. The target audience included people from academia, tool vendors, system suppliers, and users in industry interested in the all aspects of the mentioned topics. The workshop was based on presentations of selected works with sufficient time for feedback from the audience and discussions. Participants have been encouraged to submit short papers, workin-progress reports, or position papers.
Organizers:

- Luis Almeida, Univ. of Aveiro, Portugal
- Sebastian Fischmeister, Univ. of Pennsylvania, USA
- Insup Lee, Univ. of Pennsylvania, USA
- Julian Proenza, Univ. of the Balearic Islands, Spain

URL: http://www.artist-embedded.org/artist/APRES08.html

Meeting: Training Course on Real-Time Kernels for Microcontrollers: Theory and Practice
Pisa, Italy – June 23-25, 2008
Objectives for the course: The course was aimed at:

1. providing the fundamentals concepts of real-time computing systems, including scheduling, resource management and timing analysis;
2. introducing the OSEK/VDX standards, taking as a reference implementation the Erika Enterprise kernel;
3. showing how to apply such concepts in practice, with examples based on the Altera Nios II and the Microchip dsPIC DSC microcontrollers;
4. teaching participants how to develop simple control applications using Erika Enterprise with code generation from functional models.

Organizers:

- Giorgio Buttazzo - Scuola Superiore Sant'Anna, Italy
- Paolo Gai, Evidence Srl
- Tullio Facchinetti, University of Pavia, Italy
- Ettore Ricciardi – ISTI-CNR, Pisa

http://www.artist-embedded.org/artist/Real-Time-Kernels-for.html

Meeting: Operating Systems and Networks
Pisa, Italy – October 2-3, 2008
Objectives for the meeting: The purpose of the meeting was to refine the research objectives of the cluster on Operating Systems and Networks and coordinate the collaboration among the different groups. Discussed topics included: architecture effects on worst-case execution times, taxonomy of resources, real-time networks, and real-time and control issues.
Organizers:

- Giorgio Buttazzo - Scuola Superiore Sant'Anna, Italy
- Alan Burns – University of York, UK
- Luis Almeida, Univ. of Aveiro, Portugal

Meeting: OSPERT 2008 - Fourth International Workshop on Operating Systems Platforms for Embedded Real-Time Applications
Prague, Czech Republic – July 1st, 2008
Objectives for the meeting: This workshop was intended as a forum for researchers and practitioners of RTOS to discuss the recent advances in RTOS technology and the challenges that lie ahead. The workshop consisted of submitted papers as well as invited presentations about academic state-of-the-art and industrial state-of-practice within the area of real-time operating systems architectures and services.
Organizers:

- Jim Anderson, University of North Carolina, Chapel Hill, USA

http://www.cs.unc.edu/~anderson/meetings/ospert08/OSPERT.html

Meeting: WCET 2008: Worst Case Execution Time Analysis
Prague, Czech Republic – July 1st, 2008
Objectives for the meeting: The goal of the workshop was to bring together people from academia, tool vendors and users in industry interested in all aspects of timing analysis for real-time systems. The workshop fostered a highly interactive format with ample time for in-depth discussions. It provided a relaxed forum to present and discuss new ideas, new research directions, and to review

current trends in this area. The presentations were kept short to leave plenty of time for interaction of attendees.
Organizers:

- Jim Anderson, University of North Carolina, Chapel Hill, USA

http://www.cs.unc.edu/~anderson/meetings/ospert08/OSPERT.html

Meeting: RTN 2008: Real-Time Networks
Prague, Czech Republic – July 1st, 2008
Objectives for the meeting: The Real Time Networks (RTN, formerly RTLIA) workshop was the seventh on the series of workshops that started at the 2002 ECRTS conference. RTN focuses on the current technological challenges of developing communication infrastructures that are real-time, reliable, pervasive and interoperable. The goal of this workshop was to bring together people from industry and academia that are interested in all aspects of real-time communication. The workshop provided a relaxed forum to present and discuss new ideas, new research directions and to review current trends in this area.
Organizers:

- Anis Koubâa, IPP-HURRAY Research Group, ISEP-IPP, Portugal.

http://www.hurray.isep.ipp.pt/rtn08/index.php

Meeting: Course on Real-Time Control Systems: Theory and Practice
Pisa, Italy – April 2-18, 2008
Objectives: The objective of the course was to introduce classical control notions applied to real-time computing systems. Topics included Discrete time systems, Exact Real-time simulation, period selection, delayed models, controllability, observability and performance of discrete time controllers, real-time computing of control systems, timing and implementation, control of real-time systems, event-driven systems, scheduling of event driven systems.
Organizers:

- Giorgio Buttazzo - Scuola Superiore Sant'Anna, Italy
- Manel Velasco – University of Catalonia, Spain

Meeting: A Multi-Processor Architectural Simulator (MPARM)
Pisa, Italy – November 5-6, 2008
Objectives: The objective of the meeting was to discuss how to use the MPARM simulator developed at the University of Bologna for evaluating the effects of sheduling and cache memories on task execution times. Martino Ruggiero, who participated in the development of the simulator, gave a tutorial to explain the MPARM architecture, the available hardware modules, their profiling features, possible power models, how add new modules to MPARM, the software development flow, the application profiling, debugging features, the operating system interface, the communication library, and a few examples.
Organizers:

- Giorgio Buttazzo - Scuola Superiore Sant'Anna, Italy
- Luca Benini – University of Bologna, Italy
- Martino Ruggiero – University of Bologna, Italy

Joint technical meetings for the Hardware Platforms and MPSoC cluster

Workshop: Industrial Collaboration
Copenhagen, Denmark – June 5-6, 2008.
Objectives for the meeting: Main objective is to get the affiliated industrial partners of the cluster involved in the activities of the cluster.
Organizer: Jan Madsen (DTU)
Other participants: Matthias Gries (Intel), Daniel Karlsson (Volvo), Anders Tranberg-Hansen (B&O ICEpower), Michael R. Hansens (DTU), Sven Karlsson (DTU), Michael R. Boesen (DTU), Peter Sørensen (DTU), Elena Maftei (DTU), Petru Eles (LiU), Soheil Samii (LiU), Jakob Rosen (LiU), Rolf Ernst (TUBS), Simon Schliecker (TUBS), Simon Perathoner (ETHZ), Clemens Moser (ETHZ), Mamagkakis Stylianos (IMEC), Renaud De Landtsheer (IMEC), Luca Benini (UNIBO), David Brunelli (UNIBO), Thierry Collette (CEA), Huimin She (KTH).

Conclusions: The meeting consisted of three parts; an industrial session, where the industrial partners presented the challenges of Embedded systems design as seen from their perspective. A Partner session, where each Partner presented their current research related to the cluster. Finally, a discussion session with the topic interaction with companies. The conclusion from the discussions was that it is very difficult to have the companies reveal their design flows, which would be of great interest for the academic partners. What would be possible is to 1) have the companies defining industry cases for academia to study, and 2) to have design flows developed in academia to be reviewed by industry partners.

Meeting: Cluster meeting on Analysis
Munich, Germany – March, 2008
Objectives for the meeting: Short status and planning meeting for the Analysis activity.
Organizer: Jan Madsen (DTU)
Other participants: Matthias Gries (Intel), Petru Eles (LiU), Rolf Ernst (TUBS), Mamagkakis Stylianos (IMEC), Luca Benini (UNIBO), Thierry Collette (CEA), Axel Jantsch (KTH)
Conclusions : Main conclusion was to have a joint cluster and industry meeting in Copenhagen late spring or early summer. Also possible exchange visits were discussed.

Meeting: Cluster meeting on Design
Munich, Germany – March, 2008
Objectives for the meeting: Short status and planning meeting for the Design activity.
Organizer: Luca Benini (UNIBO)
Other participants: Petru Eles (LiU), Rolf Ernst (TUBS), Mamagkakis Stylianos (IMEC), Jan Madsen (DTU), Thierry Collette (CEA), Axel Jantsch (KTH)

Workshop: Tools and Design Methodologies
Eindhoven, the Netherlands – March, 2008
On March 27, 2008, a two day workshop tool place in TU/e where the ICD, IMEC, DUTH/ICCS and TU/e presented their individual tools and design methodologies. A common design and tool flow was drafted as a result of the workshop.

Workshop: IMEC Tools
Athens, Greece – May, 2008
During May 9, 2008, a one day workshop took place in ICCS, where IMEC researcher Dr. Stylianos Mamagkakis presented and discussed with the main ICCS and DUTH researchers the the MPSoC parallelization (MPA) and memory hierarchy mapping (MH) tools of IMEC

Meeting: Scenario Cluster
Leuven, Belgium – April and November, 2008
There were 2 meetings of the scenario cluster in April'08 and November'08 taking place in IMEC and Uni. Gent, respectively. The interaction focused on further improvements of the scenario extraction, identification, exploitation, and switching and calibration steps.

Meeting: Bologna
Bologna, Italy – March 6-7, 2008
Objectives for the meeting: Discussing dynamic adaptation to changes in system behaviour and requirements. Use of appropriate resource abstractions and interfaces.
Organizer: University Bologna
Other participants: University Bologna, SSSA, ETHZ, University Dortmund, University Saarland.
Conclusions: The meeting lead to cooperation between SSSA and ETHZ in the area of dynamic adaptations and hard real-time systems.

Meeting: Application Model
Bologna, Italy – June 5, 2008
Objectives for the meeting: Discussing an appropriate application model that serves as a basis for the joint work on adaptive changes.
Organizer: University Bologna
Other participants: University Bologna, SSSA, ETHZ.
Conclusions: A joint application model has been defined. It is the basis of the ongoing cooperation between University Bologna, SSSA (PISA) and ETHZ (Zurich).

Meeting: BIP – DOL
Grenoble, France – September 15-16, 2008
Objectives for the meeting: The main goal of this meeting was to define the collaboration between ETHZand VERIMAG on coupling DOL (Distributed Operation Layer) and BIP (Behavior Interaction Priority) frameworks.
Organizer: Verimag
Other participants: Veriamg, ETHZ
Conclusions: The main outcome of this meeting was the definition of a design flow as well as establishing the basic modeling aspects.

Joint technical meetings for the Design for Adaptivity in Embedded Systems (Transversal Integration WP)

Meeting: Lund May 13-14, 2008
City, Country – Lund, Sweden
Objectives for the meeting: Provide the kick-off meeting for this activity. Present the work that is currently done by the individual partners. Discuss the ontology of adaptivity in embedded systems. Plan the work for the coming year.
Organizer: Karl-Erik Årzén (ULUND)
Other participants: Mälardalen, IMEC, York, SSSA, Aveiro, CEA, TUKL, NXP, Ericsson, KTH, IPP, UPC, UPM, UCatania (20 persons in all)

Conclusions

- The interpretation of the work adaptivity can be very wide depending on the community. Hence there is substantial need for strong definitions of the terminology used. This was initiated at the meeting
- The next formal meeting for the entire activity will be held in at SSSA, Pisa, 2-3 April 2009.
- A Wiki will be defined to act both as the platform for the internal work within the activity as well as the interface to the rest of the community. The wiki has been set up and is currently being filled with content. (http://www2.control.lth.se/ArtistAdapt/)
- It was decided to use the APRES workshop series to promote the work within the activity. It was decided to aim for organizing the next instance of APRES (Workshop on Adaptive and Reconfigurable Embedded Systems) in connection with ECRTS in Dublin in July 2009.
- Existing collaborations among the partners were identified. They include FRESCOR, ACTORS, MOSART, REALITY, and PREDATOR.

Meeting web: http://www.artist-embedded.org/artist/Design-for-Adaptivity.html

Meeting: Bologna March 6-7, 2008
City, Country – Bologna, Italy
Objectives for the meeting: Discussing dynamic adaptation to changes in system behavior and requirements. Use of appropriate resource abstractions and interfaces.
Organizer: University Bologna
Other participants: University Bologna, SSSA, ETHZ, University Dortmund, University Saarland.
Conclusions: The meeting lead to cooperation between SSSA and ETHZ in the area of dynamic adaptations and hard real-time systems.

Meeting: Application Model, June 5, 2008
City, Country – Bologna, Italy
Objectives for the meeting: Discussing an appropriate application model that serves as a basis for the joint work on adaptive changes.
Organizer: University Bologna
Other participants: University Bologna, SSSA, ETHZ.
Conclusions: A joint application model has been defined. It is the basis of the ongoing cooperation between University Bologna, SSSA (PISA) and ETHZ (Zurich).

Meeting: BIP – DOL, 15th-16th Sept. 2008
City, Country – Grenoble, France
Objectives for the meeting: The main goal of this meeting was to define the collaboration between ETHZ and VERIMAG on coupling DOL (Distributed Operation Layer) and BIP (Behavior Interaction Priority) frameworks.
Organizer: Verimag
Other participants: Verimag, ETHZ
Conclusions: The main outcome of this meeting was the definition of a design flow as well as establishing the basic modeling aspects.

Joint technical meetings for the Design for Predictability (Transversal Integration WP)

Meeting: ArtistDesign meeting mapping of applications for MPSoCs
*Düsseldorf, Germany; date: 27th and 28th of November 2008***:**
Within the frame of this ArtistDesign meeting which addresses the mapping of applications to MPSoCs, ETHZ presents an overview and a SW demonstration of the Distributed Operation Layer framework.

Joint technical meetings for the Integration Driven by Industrial Applications (Transversal Integration WP)

Meeting: Workshop: From Embedded Systems to Cyber-Physical Systems: a Review of the State-of-the-Art and Research Needs, RTAS in St. Louis at the Renaissance Grand Hotel Saint Louis, USA, April 21st, 2008
Objectives for the meeting:
To presentment an overarching view of methodologies and theories for the design of embedded and critical systems as it has emerged in the past five years and discuss the future in terms of the extension of the notion of embedded systems to Cyber-Physical Systems (CPS).

Organizers: Tom Henzinger (Berkeley, EPFL), Alberto Sangiovanni-Vincentelli (Berkeley, PARADES Roma), Jonathan Sprinkle (University of Arizona), Janos Sztipanovits (Vanderbilt)
Other participants: Werner Damm, OFFIS, EPFL, Roberto Passerone, U. Trento. Henzinger and Sangiovanni-Vincentelli were among the organizers of the meeting. All presented talks in their area of expertise and reflected the research work carried out in COMBEST and ArtistDesign.
Conclusions: In the overview of the present status of the discipline, the workshop addressed heterogeneous system composition, design methods based on abstraction and refinement, interface theories, mapping of abstract entities to implementation platforms and industrial applications. The presentations also featured industry representatives who gave their perspective of what are the gaping holes in the state of the art in their business segment and how to bridge academic accomplishments with industrial practice. The discussion about the extension of the theories and methodologies to the new generation of CPS reviewed the necessary steps and a possible roadmap for research. The discussion included public research organizations. European Community representatives provided the state-of-the-art and the research initiatives on embedded systems in the EU..Alberto Sangiovanni Vincentelli summarized the meeting and the conclusions. He called for the next steps in the EU-US collaboration to be coordinated between NSF and the EU research agencies.
http://ike.ece.cmu.edu/twiki/bin/view/CpsNCO/WebHome

Meeting: Industrial Integration: Industrial Challenges and Design Drivers Selection, PARADES Offices, Rome, November 12 and 13, 2008
Objectives for the meeting:

- To review with industrial partners and affiliates the challenges to be faced in embedded system design in several vertical industrial segments;
- Based on these inputs, to select the design drivers for the integration activity;
- To plan for next year activities choosing the leaders for each vertical industrial segment.

Organizers: Alberto Sangiovanni Vincentelli (PARADES), Ed Brinksma (ESI)

Other participants: 33 participants of which 27 were representing Artist Design partners (PARADES, OFFIS, ESI, University of Trento, University of Bologna, TU Braunschweig, TU Dortmund, Universidad de Cantabria, TU Wien, IMEC, Uppsala University, TU Denmark). Others were industrial participants working in international corporations (UTC) or in Artist Design affiliated companies (Danfoss, Phillips, Thales, Carmeq, Real-Time-at-Work and IAI). The participants are available on the Artist Design Web site.

Conclusions: After the two-day presentations, the following areas were selected as design drivers for the activity of the industrial integration transversal activity:

1. Transportation with emphasis on automotive and avionic. These two areas were combined since from a design flow point of view they shared enough common features to warrant a unified approach. The link to CESAR was emphasized as the Artemis project had exactly the same characteristics.OFFIS will drive and coordinate the activities in this area.
2. Health care with emphasis on equipments. Health care is one of the core research areas of the EU for the foreseeable future. Since we are using the applications as drivers, we decided to focus on well-developed products to demonstrate the use of Artist Design technology. ESI will drive and coordinate this activity.
3. Zero-energy buildings. This area is a growth domain for traditional industry such as construction, HVAC, monitoring and energy optimization. There is a strong push from the EU and the technical problems are challenging. The level of understanding of the academic partners in this domain is limited as it is a new area to most of them. PARADES will lead this effort.

We recommended having one-two yearly meetings per area at topical conferences and one-two plenary meetings at the annual Artist Design meeting and at one of the topical conferences such as Formal Methods where it is likely that most of the partners and a substantial contingent from industry will be present.
http://www.artist-embedded.org/artist/Agenda,1532.html

6.5 Project planning and status

The project has fully achieved its objectives and technical goals for the period.
All milestones had been reached for the first year and all deliverables had been produced and accepted by the Commission after the review meeting (which took place on the 23rd of January, 2009 in Brussels).

6.6 Impact of possible deviations from the planned milestones and deliverables, if any

There were no significant deviations from the planned milestones or deliverables.

6.7 Any changes to the legal status of any of the beneficiaries, in particular non-profit public bodies, secondary and higher education establishments, research organisations and SMEs;

During Year 1, there were no changes in legal status for any of the beneficiaries.

6.8 Development of the Project website

The ArtistDesign Web Portal (http://www.artist-embedded.org/) is a major tool for Spreading Excellence within the Embedded Systems Community. It aims to be the focal point of reference for events and announcements of interest to the embedded systems community.
This will play a key supporting role for collaboration and Integration, such as interaction between clusters, management information, such as scholarships, internal events, and progress of the work. The web portal will also be used to disseminate any relevant information to the community at large. We believe the web portal will be an essential mechanism for achieving integration.
It acts as a repository of knowledge in the area, including courseware, information about standards, methods and tools, research publications and results. This web portal will be made available within the NoE core and affiliated partners, and to other parties.

This repository is to be the reference for the embedded systems design community. It builds on the existing ARTIST2 Portal, which includes several features that help keep it coherent and up to date:

- Authorised users (principally, the ARTIST2 partners) can access the back end of the site to modify and update information directly. The changes are immediately visible on the site, which greatly streamlines the updating process.
- It's possible to track changes and go back to previous versions of individual web pages.
- Events are automatically sorted by date, and transferred to 'Past Events'. When appropriate.
- Structural information (hierarchy of pages) is maintained automatically.
- Ergonomics are set for the entire site. The "look and feel" of the site is always homogeneous throughout the site. It's possible to change these ergonomics, and these changes are applied homogeneously throughout the site, via automated mechanisms.

The ArtistDesign Web Portal offers information about:

- **Workshops, Conferences, Schools and Seminars**
  Provide information about the main scientific events in the area, and in particular those organised by ArtistDesign.
- **International Collaboration**
  Advertise the ArtistDesign International Collaboration events, and provide pointers to the most visible International Projects (either about significant projects outside Europe, or joint International Collaboration projects.
- **Publications**
  Publications from core partners, with emphasis on Position Papers, White Papers, etc. that may have a particularly deep impact.
- **Course Materials Available Online**
  The web portal will centralize course materials from as many sources as possible, to make them available to the general public.

7. Explanation of the use of the resources

For the first year of the project, there is no significant financial deviation to take into account. Most of the partners had spent a small part of his provisional personnel budget for year 1. The amounts claimed on personnel cost are closely linked with the effort in terms of manmonth claimed in the project.

Some partners did not declare any personnel costs (no manmonths allocated to the project over the first year) with any adjustments planned retrospectively for next year. As previously explained, personnel time and personnel costs had already been claimed on the Artist 2 project which stopped on August 2008.

.

For IMEC (partner n°15), his high personnel cost is due to the fact that they have a new tax on salary to pay. That tax has not been previously planned for in the provisional budget.

The following table explains the costs claimed by partners per type of expenditures.

Table - ESTIMATED ELIGIBLE COSTS PER TYPE OF EXPENDITURES

Participant	Cost Model	Manpower	Equipment	Consumable	Travel	Subcontracting	Other costs	Overhead	Total
FLORALIS	FC	26 940,00 €			10 030,00 €		1 991,00 €	7 791,00 €	46 752,00 €
UJF/Verimag	FC	46 575,00 €						27 944,00 €	74 519,00 €
Aachen	FC	6 469,00 €			10 300,00 €			10 061,00 €	26 830,00 €
Aalborg	FC	0,00 €			4 145,00 €			2 487,00 €	6 632,00 €
Aveiro	FC	23 065,00 €			7 483,00 €		1 500,00 €	19 228,00 €	51 276,00 €
Bologna	FC	12 347,00 €			5 446,00 €			10 675,00 €	28 468,00 €
TUBS	FC	18 327,00 €			7 262,00 €			15 353,00 €	40 942,00 €
Cantabria	FC	20 822,00 €			2 334,00 €			13 893,00 €	37 049,00 €
CEA	FC	12 898,00 €		30,00 €				7 826,00 €	20 754,00 €
DTU	FC	23 531,00 €			16 519,00 €			24 030,00 €	64 080,00 €
Dortmund	FC	4 834,00 €			5 205,00 €		2 009,00 €	7 228,00 €	19 276,00 €
EPFL	FC	15 826,00 €		53,00 €				9 527,00 €	25 406,00 €
ESI	FC	13 405,00 €			3 451,00 €			10 113,00 €	26 969,00 €
ETH Zurich	FC	14 260,00 €			3 382,00 €			10 585,00 €	28 227,00 €
IMEC	FC	94 763,00 €			7 256,00 €			64 157,00 €	166 176,00 €
INRIA	FC	11 431,00 €						11 014,00 €	22 445,00 €
TUKL	FC	0,00 €			6 366,00 €		2 000,00 €	5 019,00 €	13 385,00 €
KTH	FC	0,00 €			10 131,00 €			6 078,00 €	16 209,00 €
Linköping	FC	27 632,00 €			4 365,00 €			19 198,00 €	51 195,00 €
ULund	FC	0,00 €			6 887,00 €			4 132,00 €	11 019,00 €
MDH	FC	24 764,00 €			1 491,00 €			15 753,00 €	42 008,00 €
OFFIS	FC	3 084,00 €			9 169,00 €			7 351,00 €	19 604,00 €
Parades	FC	14 466,00 €					1 976,00 €	6 734,00 €	23 176,00 €
Passau	FC	4 696,00 €			828,00 €			3 314,00 €	8 838,00 €
SSSA-Pisa	FC	43 014,00 €			10 303,00 €			31 990,00 €	85 307,00 €
Porto	FC	13 008,00 €			9 368,00 €			13 425,00 €	35 801,00 €
Saarland	FC	13 666,00 €			440,00 €			8 463,00 €	22 569,00 €
PLU-Salzburg	FC	5 500,00 €			9 892,00 €		9 722,00 €	15 068,00 €	40 182,00 €
Uppsala	FC	0,00 €			4 078,00 €			2 446,00 €	6 524,00 €
Vienna	FC	1 314,00 €			8 672,00 €			5 991,00 €	15 977,00 €
York	FC	0,00 €			10 383,00 €			6 229,00 €	16 612,00 €
TOTAL		496 637,00 €	0,00 €	83,00 €	175 186,00 €	0,00 €	19 198,00 €	403 103,00 €	1 094 207,00 €

The following table has more details on the different work packages with explanations on the tasks performed related to the costs claimed above:

ARTISTDESIGN - YEAR 1			
Table - COMMENTS ON WORK PERFORMED			
Participants	WPs	person months	Comments
Partner 1 Floralis	WP00	6,93	**Coordinator of the project** - technical follow up Travel expenses: Kick off meeting - Brussels meeting (dec 2008)
	WP02	0,00	Other expenses: Cylab workshop (WP2 spreading excellence)
TOTAL		6,93	
Partner 2 UJF/Verimag	WP00	0,36	Scientific and Technical coordinators of the NoE. No travel expenses.
	WP01	2,38	VERIMAG has co-organized workshops with CEA related to model-based development of real-time and embedded systems (1st International Workshop on Model Based Architecting and Construction of Embedded Systems - Toulouse -- September 29th, 2008 http://www.artist-embedded.org/artist/ACES-MB-08.html). VERIMAG is collaborating intensely with INRIA +OFFIS + PARADES in the SPEEDS project where for developing a modelling framework, a design methodology and system level validation techniques. Alberto Sangiovanni Vincentelli has visited VERIMAG. VERIMAG researchers spent significant amount of time visiting Rome to carry out research work in the area of methodologies and tools for embedded system design. Alberto Ferrari has visited Grenoble and other locations to maintain connectivity with the rest of the research community.
	WP02	2,35	Organized the main Spreading Excellence events of the NoE, wrote the deliverable (see deliverable for details http://www.artist-embedded.org/docs/Events/2009/ArtistDesign_Y1Review/deliverables/D4-2-0-Y1_Spreading_Excellence.pdf). Managed the website (with inputs from all partners).
	WP03	2,59	VERIMAG has worked on the expressiveness of BIP and defined a new notion of expressiveness for components. VERIMAG has applied BIP to modelling of architectures of autonomous robots, in collaboration with the AMAES project. VERIMAG has worked on a distributed semantics for BIP and enhanced the BIP execution engines to multithreaded execution. VERIMAG has worked on the modelling of quantitative extrafunctional properties for software intensive embedded product lines. Verimag has worked on modelling platform properties with AADL and BIP.
	WP07	0,84	Started work on integrating MPA and DOL, in particular the semantics of DOL will be modelled in BIP to verify additional important system properties.
TOTAL		8,52	
Parnert 3 Aachen	WP04	2,00	Research work on the project MAPS, which targets the MPSoC programming challenge by providing a tool-set to help software developers to parallelize and efficiently map/schedule the applications to the multiprocessor platform.
TOTAL		2,00	
Partner 4 Aalborg		0,00	
TOTAL		0,00	
Partner 5 Aveiro	WP01	1,47	Joint work towards: server-based traffic scheduling for composable communication systems; using DC-powerline communications in the automotive domain; improving robustness of CAN-based distributed embedded systems with star topologies; using the service-based paradigm in distributed real-time systems for improved functional flexibility.
	WP02	0,83	Participation in the ARTIST Summer Schools in Autrans/France and in Shanghai/China; several seminars and tutorials; CiberMouse@RTSS2008 students design competition.
	WP05	1,87	Dynamic QoS management in distributed multimedia and control systems; Networks and middlewares to support dynamic reconfiguration; Wireless communication for autonomous agents.
	WP07	0,63	Contributions in the scope of the activity on Design for Adaptivity: organization of APRES 2008 (Int. Workshop on Adaptive and Reconfigurable Embedded Systems), participation in meetings and in the editing of joint documents.
TOTAL		4,80	
Partner 6 Bologna	WP01	0,50	Prof. Benini participate on a number of Artist-Design meetings to promote the integration of geographically dispersed teams
	WP02	0,50	Prof. Benini participate on a number of meetings to disseminate Artist-Design results and concepts
	WP06	1,25	Short-term research internships set up with Dr Francesco Paterna on energy-efficient variation tolerant allocation strategies for multi-core platforms. Prof. Luca Benini is UNIBO group leader in all project activities.
	WP07	1,25	Short-term research internships set up with Dr Sabry Mohamed on predictable memory hierarchies for multi-cores. Prof. Luca Benini is UNIBO group leader in all project activities.
TOTAL		3,50	
Partner 7 TUBS	WP06	2,50	Travel expenses: Cluster and integration meetings (Copenhagen, Rome)- Dissemination ESWEEK 2008 - Integration of tools and methods (TUBS and ETHZ) for MpSoC analysis - Study of method for hybrid performance analysis for MpSoC
	WP07	1,25	Online performance control and predictability of MpSoC architectures Industrial case study on MpSoC performance analysis
TOTAL		3,75	

Partner 8 Cantabria	WP01	0,01	Preparation and participation in kickoff meeting
	WP02	0,10	Participation in international workshops and conferences
	WP05	1,53	Participation in Pisa meeting, preparation of deliverables, participation in remote discusions, presentation of WP-specific results at international conferences and workshops
	WP07	3,34	Participation in Rome meeting, preparation of deliverables, participation in standardization committees, presentation of WP-specific results at international conferences and workshops
TOTAL		4,98	
Partner 9 CEA	WP02	0,60	Travel expenses: Kickoff meeting (Jan08) Organization and participation to the ACES-MB workshop in the context of the MODELS conference.
	WP03	1,60	Modeling Activity: Work on MARTE under three point of views: resource modeling, modeling of Model of Compuation and Model Analysis of real-time features.
	WP07	0,24	CEA is working with KTH on EAST-ADL.
TOTAL		2,44	
Partner 10 DTU	WP06	6,00	Travel expenses: technical meetings at Duke University, Bologna and Linkoping WP6.1 Component-based service model framework (3 MM), work done in relation to affiliated industry partner B&O ICEpower WP6.2 Energy harvesting aware routing with scheduling optimization (2 MM), work done in colaboration with Bologna WP6.2 Analysis tool addressing decidability and model-checking results for fragments of interval logics (1 MM), work done in collaboartion with Oldenburg
TOTAL		6,00	
Partner 11 Dortmund	WP01	0,10	Travel expenses: the first Rheinfels workshop - summer school at Autrans - working meeting at Düsseldorf Dortmund integrated the MPARM simulator from Bologna and its own Memory Simulator.
	WP02	0,30	Dortmund participated in the South American Summer School on Embedded Systems and presented the summary of the first Rheinfels Workshop at the Embedded Systems Week in Atlanta. Also, Dortmund provides one of the chairs of the Workshop on education in Embedded System Design.
	WP04	1,00	Dortmund organized the 1st workshop on Mapping Applications to MPSoCs at Rheinfels Castle in June 2009, and also organized the 1st working meeting in Düsseldorf in November 2009. Also, Dortmund organized the writing of deliverables and participated in the review.
	WP07	0,11	Dortmund reported about its work on design for predictability in the context of worst case execution time aware compilation.
TOTAL		1,51	
Partner 12 EPFL	WP01	0,10	Travel expenses: Kick off meeting Work with Salzburg on Timed Languages
	WP02	0,10	Workshop on Foundations of Component Based Design
	WP03	0,50	Cluster coordination "Modeling activity" Work on quantitative modeling and verification
	WP07	0,10	Work on Parades on Determinism
TOTAL		0,80	
Partner 13 ESI	WP01	0,41	Travel expenses: Kickoff meeting (Jan08) - Meeting 'Integration drive by industrial applications (Nov) - Rome workshop on industrial applications (Nov). Contribution especially as co-leader on intercluster activity: Integration Driven by Industrial Applications;
	WP07	0,83	Co-leader on intercluster activity: Integration Driven by Industrial Applications; Organization and contribution to workshop on Embedded Systems: Industrial Applications '08
TOTAL		1,24	
Partner 14 ETH Zurich	WP01	1,20	Travel expenses: ETH Zurich participated in several meetings concerning the areas of Hardware Platforms and MPSoC. In addition, student exchanges took place to support mobility.
	WP06	3,75	JPRA Activity: "Platform and MPSoC Design": ETH Zurich and Bologna continued collaborations on optimal management of smart sensor with energy harvesting capabilities. JPRA Activity: "Platform and MPSoC Analysis": ETH Zurich worked with Bologna and TU Braunschweig on joint efforts to support predictability and efficiency.
	WP07	2,00	ETH Zurich worked together with Uppsala and Saarland on System Architectures and Hardware Platforms.
TOTAL		6,95	

Partner 15 IMEC	WP01	5,04	Travel expenses :Artist meeting @ DATE'08 (Munchen) - ArtistDesign about sandwich PhDs (Athens) - Adaptivity kick-off meeting (Lund) - ArtistDesign-MPSoC cluster regular meeting (Copenhagen) - 1st workshop on Mapping of Applications to MPSoCs and ArtistDesign synchronization (St Goar) - Artist Summer School (Grenoble) - meeting & presentation for the RTOS cluster of ArtistDesign NoE (Pisa) - "Integration Driven by Industrial Applications" Transversal Activity (Rome) - project meeting SSCG cluster (Dusseldorf) - PhD and Sandwich PhD teams scientific and technical coordination
	WP02	1,55	Dissemination and Use activities
	WP04	1,87	PhD and Sandwich PhD Compiler team coordination
	WP05	0,88	Sandwich PhD MPSoC team coordination
	WP06	2,31	PhD MPSoC team coordination
	WP07	1,31	Cross Design Layer technical coordination
TOTAL		12,96	
Partner 16 INRIA	WP01	0,75	Travel expenses: all such expenses shall be declared as adjustments in the next Financial Statement. Work on design for predictability of reactive programming languages
	WP02	0,52	Work on component based design
	WP03	0,75	Work on quantitative modeling and verification (reliability)
TOTAL		2,02	
Partner 17 TUKL		0,00	Travel expenses : WP2: Spreading Excellence Multicore workshop
TOTAL		0,00	
Partner 18 KTH		0,00	
TOTAL		0,00	
Partner 19 Linkoping	WP06	4,10	Energy efficient design of embedded real-time systems: We have addressed the problem of energy-efficient design for time constrained multiprocessor systems. In particular, the problem of thermal aware energy optimisation has been tackled. Timing analysis of distributed real-time systems: Analysis of heterogeneous systems using various task scheduling policies and heterogeneous communication protocols with static and dynamic phases. Both formal and simulation based approaches were developed.
	WP07	1,40	Predictable, Fault-tolerant Embedded Systems Design:generating predictable (fault-tolerant) and efficient schedules for embedded applications with soft and hard real-time constraints. Predictable for Multiprocessor SoC Architectures: We have developed an overall strategy and framework for predictable multiprocessor applications.
TOTAL		5,50	
Partner 20 ULund		0,00	Leader for the Design for Adaptivity transversal activity. Organized meeting, graduate course, editing deliverable, preparing review, setting up wiki, Participating in the OS and Network cluster (participating at meetings). Travel expenses for Kick off meeting and workshop meeting in Lund (May)
TOTAL		0,00	
Partner 21 MDH	WP04	3,00	Research on timing analysis for MPSoC systems
	WP07	1,00	Research on parametric timing analysis for adaptive systems
TOTAL		4,00	
Partner 22 OFFIS	WP03	0,50	Modelling activity - Interaction with partners on compositional analysis techniques regarding safety and real, as well as on deployment synthesis; Interaction with partners on meta models for heterogeneous rich components; Active in interaction with industries on ES topics. 5 researchers are involved in ArtistDesign, two of them are permanent stuff and three are non-permanent. personal costs are only claimed for non-permanent stuff. Travel expenses: Kick-off Meeting; Interaction meetings with partners and industry; Artist Workshop Embedded Systems: Industrial Applications 08 (Rome); Interaction with the US: Presentation at National Workshop for Research on High-confidence Transportation Cyber-physical Systems: Automotive, Aviation & Rail (Washington, DC)
TOTAL		0,50	
Partner 23 Parades	WP02	0,06	Travel expenses: Meeting 'Integration drive by industrial applications (Nov) - Rome workshop on industrial applications (Nov) - Meeting of partners for Industrial Applications activity. Dinner in Atlanta (Oct)
	WP03	0,25	Work on quantity management and scheduling mechanisms.
	WP07	1,12	Work with EPFL-Salzburg on Timed Languages. Work with EPFL on characteristics of design: determinism, predictability, and abstract semantics
TOTAL		1,43	
Partner 24 Passau	WP04	0,76	travel expenses: Kick-off-Meeting in Paris - workshop MPSOCs in St Goar Automatic Parallelization and Optimization of Loop Programs for Multicores and GPUs with Scratchpad Memories
TOTAL		0,76	

Partner 25 SSSA PISA	WP01	2,00	Travel expenses :Kick off meeting - workshop for Adaptivity in Lund - ECRTS08 conference in Prague - IARIA conference in Cap Esterel- Workshop on Foundations of Component Based Design - WFCD08 in Atlanta - Organisation of ArtistDesign Meeting in Pisa - Consumables (Sparkfun) - Consumables (Embedded Solutions). - Activity focusing on resource management to produce a taxonomy of system resources and to discuss the real-time scheduling algorithms for multi-core platforms
	WP02	1,00	Organization of a graduate course in Pisa on real-time kernels for microcontrollers
	WP05	2,00	Development of a real-time kernel to be used as a shared platform for embedded applications
	WP07	1,00	Development of feedback scheduling algorithms and schedulabilitu analysis for adaptive reasource managements on multicore architectures
TOTAL		6,00	
Partner 26 PORTO	WP01	2,35	Travel expenses: Kickoff Meeting in Paris Participation in the kick-off meeting and contributions to the year one tuning of objectives of concerned clusters and transversal activities.
	WP02	0,50	Travel expenses: Artist Summer School Participation in Artist summer school 2008
	WP05	3,15	Travel expenses: Cluster Meeting in York in conjunction with PC meeting ECRTS; Research Meetings with Pisa; Workshop Controlo 2008; ECRTS 08 Conference; RTCM Seminar; Meeting - Thematic Cluster: Operating Systems and Networks. Contributions to the 3 activities, namely in terms of the efforts concerning taxonomy (resource management activity) and roadmaps (networks activity). Work together with Pisa on implementing OpenZB on Flex platforms.
	WP07	0,20	Travel expenses: Artemisia Event Contributions to both Design for adaptivity and industrial integration.Organization of the CPS (cyber-physical systems) event associated with DCOSS
TOTAL		6,20	
Partner 27 SAARLAND	WP02	0,25	Travel expenses: kick-off meeting in Paris + workshop
	WP04	2,00	Cooperation with TU Vienna on static analysis for mode detection
TOTAL		2,25	
Partner 28 PLU SALZBURG	WP01	0,45	Overall ESWEEK 2008 organization, general co-chair (Including EMSOFT, WFCD), work with EPFL on timed languages
	WP02	0,13	ESWEEK 2008 sponsoring, Artist Summer School 2008 in Shanghai
	WP03	0,56	Research papers on compositional HTL semantics (with EPFL and Porto), helicopter test platform, runtime patching (with Porto)
	WP07	0,13	Research paper on SSD/HDD integration (with Hitachi GST, San Jose)
TOTAL		1,27	
Partner 29 UPPSALA	WP01	0,00	Participation in ArtistDesign plenary meeting, January 2008. - Hosting visiting researchers from: Brno Technical University, Technical Univ. of Dortmund, Chinese Academy of Sciences
	WP02	0,00	Participation in key conferences of the area: - Embedded Systems Week 2008 in Atland, Georgia, - Real Times Systems Sumposium 2008, Barcelona, Spain.
	WP03	0,00	Research work on: - Verification and testing of timed and infinite-state systems, partly contributing to Ph.D. theses of Mayank Saksena, Lisa Kaati, Nommene Ben Henda, Ahmed Rezine - Generation of models for components of embedded systems, resulting in two Ph.D. theses during the period (Therese Bohlin and Olga Grinchtein)
	WP07	0,00	Coordination of trasversal cluster on Predictability, including coordination of meetings and writing of annual report
TOTAL		0,00	
Partner 30 Vienna	WP01	0,54	Travel expenses: Project meetings (Kick-off) - Workshop in St. Goar; dissemination (ISOLA Symposium, SEUS Workshop, Echtzeit 2008) - Project cooperation with York on Timing Analysis & Hardware Architecture;
	WP02	0,28	direction of WCET workshop; steering committee SEUS workshop; visit to TU Brno; conference and workshop presentations
	WP05	1,13	MPSoC architectures for time predictability and composability; composability, compositionality and stability of timing;
	WP07	0,38	time-predictable OS: prototype implementation and experiments
TOTAL		2,33	
Partner 31 YORK		0,00	Travel expenses: workshop & conference:Majorca (Feb) - Prague (July) - Mineapolis (July) - Grenoble (Sept) - Hamburg (Sept) - San Jose (Sept) - Pisa (Oct) - Madrid (Oct) - Porto (Oct) - Barcelona (Dec) - Brussels (Dec) - Scientific and Technical coordinators of an activities with the cluster and involvement in other clusters and activities, and cross cluster activities.
TOTAL		0,00	

8. Financial statements – Form C and Summary financial report

A separate financial statement from each beneficiary (FormC) is available on the NEF session and is not yet validated by the Commission at the moment.

A summary financial report which consolidates the claimed Community contribution of all the beneficiaries is provided here:

Artist

Financial board

n°	Name	Provisionnal budget				TOTAL	Theoretical EC $	Requested EC Contribution
		RTD (A)	Demo	Mngt (C)	Other (D)			
1	FLORALIS	349		248 400	484 953	733 702	733528	733 530
2	UJF/Verimag	285 417		66 600	15 578	367 595	296241	296 239
3	Aachen	119 762				119 762	89822	89 821
4	Aalborg	191 922				191 922	143942	143 941
5	Aveiro	163 404			2 400	165 804	124953	124 953
6	Bologna	219 350				219 350	164513	164 512
7	TUBS	138 048			1 472	139 520	105008	105 008
8	Cantabria	148 996				148 996	111747	111 747
9	CEA	133 226				133 226	99920	99 919
10	DTU	246 778			6 401	253 179	191485	191 484
11	Dortmund	255 016			4 000	259 016	195262	195 262
12	EPFL	143 996				143 996	107997	107 997
13	ESI	102 228				102 228	76671	76 671
14	ETH Zurich	164 492				164 492	123369	123 369
15	IMEC	296 771				296 771	222578	222 578
16	INRIA	104 812				104 812	78609	78 609
17	TUKL	122 552			6 400	128 952	98314	98 314
18	KTH	216 416			3 200	219 616	165512	165 512
19	Linköping	136 159				136 159	102119	102 119
20	ULund	97 518			3 201	100 719	76340	76 339
21	MDH	119 762			6 401	126 163	96223	96 222
22	OFFIS	78 368				78 368	58776	58 776
23	Parades	153 342			1 528	154 870	78199	78 199
24	Passau	91 428				91 428	68571	68 571
25	SSSA-Pisa	212 163				212 163	159122	159 122
26	Porto	122 552				122 552	91914	91 914
27	Saarland	209 302				209 302	156977	156 976
28	PLU-Salzburg	78 368			4 466	82 834	63242	63 242
29	Uppsala	131 258				131 258	98444	98 443
30	Vienna	114 672		2 400		117 072	88404	88 404
31	York	309 610				309 610	232208	232 207
	TOTAL	**4 908 037**	**0 €**	**317 400**	**540 000**	**5 765 437**	**4500005**	**4 500 000**
Cost declared Year 1								
1	FLORALIS	333	0 €	44 030	2 389	46 752		46 585
2	UJF/Verimag	74 519	0 €	0	0	74 519		55 888
3	Aachen	26 830	0 €	0	0	26 830		20 122
4	Aalborg	6 632	0 €	0	0	6 632		4 974
5	Aveiro	48 876	0 €	0	2 400	51 276		39 057
6	Bologna	28 468	0 €	0	0	28 468		21 351
7	TUBS	40 942	0 €	0	0	40 942		30 706
8	Cantabria	37 049	0 €	0	0	37 049		27 786
9	CEA	20 754	0 €	0	0	20 754		15 565
10	DTU	64 080	0 €	0	0	64 080		48 060
11	Dortmund	16 062	0 €	0	3 214	19 276		15 260
12	EPFL	25 406	0 €	0	0	25 406		19 054
13	ESI	26 969	0 €	0	0	26 969		20 226
14	ETH Zurich	28 227	0 €	0	0	28 227		21 170
15	IMEC	166 176	0 €	0	0	166 176		124 632
16	INRIA	22 445	0 €	0	0	22 445		16 833
17	TUKL	10 185	0 €	0	3 200	13 385		10 838
18	KTH	16 209	0 €	0	0	16 209		12 156
19	Linköping	51 195	0 €	0	0	51 195		38 396
20	ULund	11 019	0 €	0	0	11 019		8 264
21	MDH	42 008	0 €	0	0	42 008		31 506
22	OFFIS	19 604	0 €	0	0	19 604		14 703
23	Parades	21 200	0 €	0	1 976	23 176		12 576
24	Passau	8 838	0 €	0	0	8 838		6 628
25	SSSA-Pisa	85 307	0 €	0	0	85 307		63 980
26	Porto	35 801	0 €	0	0	35 801		26 850
27	Saarland	22 569	0 €	0	0	22 569		16 926
28	PLU-Salzburg	24 627	0 €	0	15 555	40 182		34 025
29	Uppsala	6 524	0 €	0	0	6 524		4 893
30	Vienna	15 649	0 €	328	0	15 977		12 064
31	York	16 612	0 €	0	0	16 612		12 459
	total	**1 021 115**	**0 €**	**44 358**	**28 734**	**1 094 207**		**833 533**

At project level, less than 19% of the provisional budget has been consumed. 18.52% of the global requested EC contribution has been requested via the FormCs on the NEF session.

This low rate of consumption in the NoE is due to the fact that the Artist 2 project was still active till the end of August 2008, thus there was an overlap with the previous year's project and most of the partners on the ArtistDesign project were also partners on Artist 2 project.

9. Certificates

Any certificates are due for this period, in accordance with Article II.4.4 of the Grant Agreement.