



IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Activity - Progress Report for Year 1

Platform and MPSoC Design

Cluster:

Hardware Platforms and MPSoC

Activity Leader:

Prof. Luca Benini (UNIBO)

<http://www-micrel.deis.unibo.it/>

Policy Objective (abstract)

The main objective of the activity is to build a common research environment and a wide basis of technical and scientific competences on embedded platforms, with special emphasis on Multi-processor Systems-on-Chip (MPSoCs). The main challenges are the significant fragmentation and lack of integration in this area. The consensus on the fact that hardware platforms for embedded applications will be multi-core, with increasing degrees of parallelism, is not matched at the software and system design level. The teams involved in the activity aim at building stronger common techniques for modeling, analysis and run-time management of embedded hardware platforms. The expected impact will be a faster and more consistently focused development of methods and tools in support of application development and mapping.

Versions

number	comment	date
1.0	First version delivered to the reviewers	December 19 th 2008

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1. Overview of the Activity

1.1 *ArtistDesign Participants and Roles*

Team leader: Prof. Lothar Thiele – TIK, ETH Zürich (Switzerland). Role: design methods for MPSoC that combine performance analysis with multi-objective application mapping strategies. To this end, an available programming environment DOL (distributed operation layer) will be enhanced and combined with tools from other partners.

Team leader: Prof. Petru Eles – Linköping University (Sweden). Roles: (i) Analysis and Optimization of real-time and fault-tolerant applications implemented on distributed Platforms and MPSoC. (ii) Analysis and Optimization of energy efficient, time constrained embedded systems.

Team Leader: Prof. Luca Benini – University of Bologna (Italy). Roles: (i) Development of power modeling and estimation framework for systems-on-chip. (ii) Development of optimal allocation and scheduling techniques for energy-efficient mapping of multi-task applications onto multi-processor systems-on-chips. (iii) Development of energy-scavenging techniques for ultra-low power sensor network platforms.

Team Leader: Prof. Jan Madsen – IMM, Technical University of Denmark (Denmark) Areas of his team's expertise: abstract RTOS and NoC models for multiprocessor system simulation and verification. Modeling and analysis of fault-tolerant embedded systems.

Team Leader: Prof. Rolf Ernst – TU Braunschweig (Germany) Roles: TU Braunschweig contributes methods to deal with variability and reliability issues for systems built from unreliable components.

Team Leader: Dr. Stylianos Mamagkakis – Interuniversity Microelectronics Centre, IMEC vzw. (Belgium) This team will introduce novel design-time and run-time resource management optimizations for MPSoC platforms

1.2 *Affiliated Participants and Roles*

Dr. Daniel Karlsson, Volvo Technology Corporation
Architecture and Design of Automotive Embedded Systems.

Dr. Valter Bella, Telecom Italia Lab
Architecture and Design of Wireless Sensor Networks and Embedded Systems for Ambient Intelligence.

Bjørn Sand Jensen – Bang & Olufsen ICEpower (Denmark)
Areas of his team's expertise: chip design for audio signal processing

CTO Rune Domsteen – Prevas (Denmark)
Areas of his team's expertise: platform design for embedded systems

Prof. Krish Chakrabarty - Duke University (USA).
Areas of his team's expertise: first to develop droplet-based biochips that use electrowetting on dielectric for droplet transport. Design methods and tools for droplet-based biochips

Prof. Dimitrios Soudris – Democritus Uni. of Thrace, DUTH (Greece)
This team will introduce novel dynamic data type and data allocation optimizations for MPSoC platforms.

Prof. David Atienza – Uni. Complutense de Madrid, UCM (Spain)

This team will introduce novel run-time memory management optimizations for MPSoC platforms.

Prof. Per Gunnar Kjeldsberg - Norges Teknisk-Naturvitenskapelige Uni., NTNU (Norway)

This team will introduce novel task migration methodologies for MPSoC platforms utilizing hardware accelerators.

1.3 Starting Date, and Expected Ending Date

Starting date: January 2008.

Ending date: the activity will span the duration of the project, and continue beyond the end of the project. This is because all current trends indicate that MPSoC and platform design will increasingly become a primary concern and focus of action for researchers, designers and developers working on embedded systems.

Moreover, the integration achieved by this activity is creating the know-how and the skills required for the definition of new research and development initiatives. As a result, all partners are already actively involved in long term funded research programs in MPSoC and embedded design, whose end-date is beyond the duration of ArtistDesign.

1.4 Objective

While there is wide consensus on the fact that hardware platforms for embedded applications will continue to be multi-core, with increasing degrees of parallelism, the evolution trajectory on programming models, design-time and run-time application environments is much less clear. The consequence is fragmentation: while many research teams are working on one or more of these domains, there is little communication and integration, this leads to duplication of results and overall slow progress. The teams involved in this activity have a wide-ranging research experience which covers all the key areas in MPSoC application specification mapping. The integration activity supported by ARTIST-DESIGN will help the participants to the cluster in strengthening the coherency of their approaches and focus on addressing complementary issues in a synergistic fashion. In particular, there will be an initial effort in reaching a common consensus on the most critical issues to be addressed, define common terminology and decide the operational strategy to address them in a collaborative fashion. The expected impact will be a faster and more consistently focused development of methods and tools in support of application development and mapping.

1.5 Background

The partners involved in this activity have very active ongoing cooperations on a number of topics. A non-exhaustive set of examples of background cooperation activities is given here.

IMEC, University of Bologna, University of Madrid and DUTH have ongoing collaboration on dynamic memory management optimizations at the system level for single processor systems, which they plan to extend in the domain of multiprocessor systems.

ETHZ and Bologna have ongoing collaborations on optimal management of smart sensor with energy harvesting capabilities. Wireless sensor networks are a very relevant example hardware platforms with very tight energy constraints. The limited battery lifetime can be extended indefinitely if the node is equipped with energy harvester that collect and store energy from the environment. However, given the erratic nature of environmental energy sources, the rate at which sensing, computation and storage operations can be performed

should be dynamically adjusted to the energy availability using a closed-loop optimal control policy

KTH and Bologna have cooperated on the development of optimal static mapping strategies for real-time biomedical application onto multi-core platforms. This work has demonstrated that workload allocation is not sufficient to obtain energy-optimal mappings, as a very significant contribution to the power budget is spent in memory transfers. Hence synergistic memory and computation allocation approach is required.

Linköping and Bologna have cooperated on allocation and scheduling policies for low power systems, where clock frequency and voltage setting are also degrees of freedom for optimization.

DTU and Linköping have cooperated on optimisation of distributed embedded systems

1.6 Technical Description: Joint Research

The main scientific challenges addressed in this activity are focused on how to map complex applications onto multi-core hardware platforms. This includes addressing allocation and scheduling issues like: scalability, flexibility, composability, predictability, design-time reduction and increased dynamism. The problem is complex and multi-faceted. On one hand, we have static (design/compile time) approaches, where applications are analyzed and optimal mapping decisions are taken before the platform is deployed in the field. On the other hand, we have dynamic, run-time approaches where mapping decisions are taken online, and they are triggered by environmental and workload variations. While these approaches start from different premises, they should not be regarded as alternative, rather they are synergistic.

Design time analysis and decisions can help in providing a good starting point for run-time adaptation, moreover off-line pre-computation can reduce the overhead of the online policies making them more reactive and less resource-hungry. One important requisite for any mapping strategy is to ensure predictability AND efficiency. Note that online adaptation is not adverse to predictability: if online adaptation is based on feedback control (e.g. finite horizon), it can be used to “stabilize” the system, and make it more robust (predictable) in response to environmental variations (e.g. temperature).

Another scientific challenge addressed in this activity is the development innovative reliable multicore programming models and architecture platform able to address computation and control oriented applications. One key building block is the development of efficient synchronization & communication abstractions that are required for successfully deploying MPSoCs in embedded application domains. Efficiency is inherently related to both power and performance, hence it is an energy metric. In embedded systems, productivity-enhancing abstractions are acceptable only if they do not compromise efficiency, so the focus is on how to enable fast development (debugging, tuning) without losing efficiency. It is also extremely important to take into account variability of both hardware fabrics and application workloads, which is deemed to rapidly increase. Hence, the concurrency management layer should provide means for dynamically managing workload variations, as well as hardware unpredictability sources.

1.7 Problem Tackled in Year 1

A number of problems were tackled in Year 1, through several cooperations involving two or more partners. In the following paragraphs, we briefly summarize the problems tackled and the partners involved.

ETHZ has been mainly involved in cooperations with University Bologna and University Dortmund. In particular, we looked at new approaches to map algorithms onto highly parallel

MPSoC platforms. To this end, we linked the specification and mapping environment DOL (distributed operation layer) from ETHZ to the MPARM simulation platform from University Bologna. Major efforts have been invested into the corresponding alignment of the semantics, the generation of appropriate hardware-dependent software and the implementation of predictable communication fabrics. This work just started and will continue during the next phase of ARTISTDesign. Together with University Dortmund, we are starting to investigate the influence of memory mapping on the whole MPSoC design process. A first visit of a PhD student from Dortmund to ETHZ took place which resulted in a first problem specification.

The **Linköping** group has addressed two major issues: *Design optimisation of fault tolerant distributed real-time systems* and *Energy efficient design of embedded real-time systems*. Linköping has addressed the problem of energy-efficient design for time constrained multiprocessor systems. In particular, the problem of thermal aware energy optimisation has been tackled. The major challenge was to integrate temperature modelling into the framework of energy efficient system level scheduling and voltage selection.

DTU and Linköping have addressed problems related to the design and optimisation of fault tolerant mixed hard/soft real-time systems. In future technology generations the ongoing trends of technology downscaling, rising system complexity and power reduction will have various effects on the reliability of microelectronic systems. These effects include device variations within single chips or circuits, an increasing sensitivity to soft errors, and device degradation due to aging. As a consequence, microprocessors as well as communication devices will become more and more susceptible to the occurrence of internal errors, i.e. the system designer will be faced with increasing error rates. The usage of appropriate fault-tolerance mechanisms is necessary to counteract these errors and thus preventing them from originating a system failure. The application of fault tolerance mechanisms has an impact on the overall reliability of a system. On the one hand fault tolerance normally increases the ability of a system or a component to operate correctly w.r.t. its specification. However the application of such techniques can have critical side effects which may cause violations of non-functional system constraints. This is particularly the case for real-time systems, where the overhead that is generated by fault tolerance mechanisms can lead to timing failure due to deadline misses.

Braunschweig is currently addressing the need for characterizing the reliability of real-time systems with two different methods: one is a simulation-based approach that introduces errors into the simulation of the system and observes the run-time effects, and the other is a formal analysis. The analysis improves on previous approaches to the point that the results now closely match the results of the simulation. This method has the additional benefit of being much faster

Moreover, **DTU** has also addressed issues related to the following macro-topics: (i) *MPSoC design and architectures*. In this context, the emphasis has been on methods to develop MPSoC platforms, covering application specific platforms as well as platforms for dynamic reconfiguration. (ii) *MPSoC programming*. In this context, the emphasis has been on exploring high-level programming models for multi-core architectures and on understanding the dynamic behavior of run-time reconfigurable systems with the aim of developing efficient run-time management algorithms. (iii) *Synthesis for Biochips*. This is a new activity which aims at using principles from MPSoC design to design biochips based on digital microfluidics. Emphasis has been on understanding the biochip platform and identifying the design problems related to it.

University of **Bologna** has addressed, in cooperation with ETHZ, the modelling of miniaturized energy harvesting devices for perpetually powered systems. In particular we optimized the design of photovoltaic energy harvester for distributed embedded systems and wireless sensor networks focusing on energy harvesting efficiency as primary design metric. We proposed a methodology for optimizing the design of a solar harvester with maximum-power point tracking defining guidelines for developers. The proposed methodology is not limited to self powered WSN nodes, but it can be easily applied to embedded systems in order to extend battery

lifetime. Furthermore it can be used to optimize the design of harvesting ICs; to this end we proposed an inductor-less architecture, suitable for on-chip integration, which permits to increment the conversion process efficiency at the minimum power consumption.

The main problem tackled between **IMEC** and its affiliated partners (ie, DUTH, UCM and NTNU) was the establishment of a common profiling and run-time MPSoC resource management exploration framework. More specifically, the existing MATISSE and MATADOR frameworks were used as foundation and extended using the software metadata and system scenario approaches. Additionally, in collaboration with DUTH, KTH, TU/e and TU Dortmund a common design flow and tool flow was investigated in order to link the run-time memory optimization methodologies and tools with the design-time memory optimization and source code parallelization methodologies and tools. This work was performed in cooperation with the Software, Synthesis, Code Generation and Timing Analysis cluster and involved additional teams outside the ArtistDesign network.

2. Summary of Activity Progress

2.1 Technical Achievements

The main achievements obtained by the partners involved in this activity are summarized below. While most of the achievement were obtained through cooperation, we also refer to a number of achievement by individual partners, which may in the future build the basis for additional cooperation.

Optimization-centric MPSoC Design (University Bologna together with ETHZ)

The technical achievements are based on a set of joint meetings and visits:

- Luca Benini (Bologna), Visit at ETH Zurich, May 20, 2008; attendees: ETHZ, UNIBO: Talk and intense discussion about Optimization-centric embedded systems design: addressing the multi-core challenge. As a result of this meeting, a plan to combine DOL (distributed operation layer framework) with MPARM (multi-processor ARM) simulation was agreed upon.
- Meeting on combining DOL with MPARM, July 22, 2008; attendees: UNIBO, ETHZ: PhD students of ETH were in Bologna to study the application of the MPARM Platform for ETHs experiments. Following that, DOL was ported to MPARM. Efforts are taking place to implement mapping algorithms and other experiments on this platform.
- ArtistDesign cluster meeting in Pisa, October 2-3, 2008; attendees: UNIBO, SSSA, USAAR, ABSINT, AIRBUS, BOSCH, ETHZ: Meeting on scheduling methods for MPSoC. Discussion with industrial partners about the application model and what kind of real-life example applications they could provide. A wish-list, with descriptions of the application and hardware model used so far, was handed over.

The primary goal of this activity was to establish a mutual understanding of the MPARM framework (developed at University of Bologna), on one hand, and the DOL framework (developed at ETHZ), on the other hand.

One main outcome of the meetings was to establish the design of the Modular Performance Analysis (MPA) analytic model for the MPARM platform. For this goal, the input specification and the API of the Distributed Operation Layer (DOL) framework, developed by ETHZ, was ported to the MPARM environment. This work is still under way. In particular, further phone conferences on the 22nd and 24th of October have been devoted to a refinement of the approach. This phone meetings had as main goal the identification of the basic design factors impacting on predictable communication fabrics.

Design optimisation of fault tolerant distributed embedded systems (Linköping, DTU)

Linköping University and DTU have developed an approach to the analysis and design of safety critical, fault tolerant embedded applications with soft and hard real-time constraints (for the analysis aspects see "Platform and MPSoC Analysis" activity report). The goal is to guarantee the deadlines for the hard processes even in the case of faults, while maximizing the overall utility. Time/utility functions are used to capture the utility of soft processes. Process re-execution is employed to recover from multiple faults. A single static schedule computed off-line is not fault tolerant and is pessimistic in terms of utility, while a purely online approach, which computes a new schedule every time a process fails or completes, incurs an unacceptable overhead. Thus, a quasi-static scheduling strategy is used, where a set of schedules is synthesized off-line and, at run time, the scheduler will select the right schedule based on the occurrence of faults and the actual execution times of processes. An optimisation technique for the generation of schedule tables supporting such a quasi-static scheduling

approach has been developed and implemented. Moreover, a preemption technique is elaborated as a method to generate flexible schedules that maximize the overall utility for the average case while guarantee timing constraints in the worst case. The scheduling algorithm determines off-line when to preempt and when to resurrect processes.

Temperature Aware System-level Power Optimization (Linköping, University Bologna together)

Linköping and UoB have cooperated on system-level design issues, focusing on energy optimization, and more specifically on the optimization of energy-efficient time constrained multiprocessor systems. In particular, the problem of thermal aware energy optimisation has been tackled.

The major challenge was to integrate temperature modelling into the framework of energy efficient system level scheduling and voltage selection.

High power densities in current SoCs result in both huge energy consumption and increased chip temperature. We have elaborated a temperature-aware dynamic voltage selection technique for energy minimization and performed a thorough analysis of the parameters that influence the potential gains that can be expected from such a technique, compared to a voltage selection approach that ignores temperature. We have also made a study regarding the relevance of taking into consideration transient temperature effects at optimization, the impact of the percentage of leakage power relative to the total power consumed and of the degree to which leakage depends on temperature. Moreover, we have also proposed a temperature-aware task mapping technique for energy optimization in systems with dynamic voltage selection capability.

Photovoltaic scavenging systems from the model to the optimized desing (University Bologna, ETHZ, together)

University of Bologna and ETHZ have improved the design of a scavenger prototype which exploits miniaturized photovoltaic modules to perform automatic maximum power point tracking. We propose a detailed model of the solar cell that predicts the instantaneous power collected by the panel and improves the simulation of harvester systems. Furthermore, we focused on a methodology for optimizing the design of MPPT solar harvesters for self-powered embedded systems and presented innovations in the circuit architecture with respect to our previous implementation. We verified that energy consumption and efficiency of the MPP tracker are very important design criteria in energy scavengers for sensor nodes, therefore we analyzed two important metrics: (i) maximization of the energy harvesting efficiency; (ii) minimization of the energy used for ineffective operations.

To this end the technical achievements can be summarized as follow:

- (a) We presented a compact model for small solar modules that accurately describes the behaviour over a wide range of irradiance conditions, cell temperature variation and incident angle with out numerical approaches typically adopted;
- (b) We improved the design process of the DC–DC converter at the solar harvester input stage boosting its efficiency
- (c) We addressed the powering a sensor node with miniaturized photovoltaic modules of a few mm² proposing a new inductor-less architecture for the harvesting process suitable for on-chip integration.

Synthesis of digital microfluidic biochips (DTU, Duke)

DTU has conducted research on the synthesis of droplet-based microfluidic biochips (also known as labs-on-a-chip). Microfluidic-based biochips are replacing the conventional

biochemical analyzers, and are able to integrate on-chip all the necessary functions for biochemical analysis using microfluidics. The “digital microfluidic” biochips are based on the manipulation of liquids not as a continuous flow, but as discrete droplets (hence the term “digital”), and thus are highly reconfigurable and scalable.

Biochips are becoming increasingly complex and are likely become multifunctional and adaptive “biochemical processing” devices integrating hematology, pathology, molecular diagnostics, cytology, microbiology, and serology onto the same platform. Consequently, the biochip designs will become larger and more complex, and new top-down computer-aided design tools are required, which can offer the same level of support as the one taken for granted currently in the semiconductors industry.

The modeling of a biochemical application is performed using an abstract model consisting of a sequencing graph. The digital biochip is modeled as a two-dimensional array of cells, where each cell can hold a droplet. DTU has proposed an integer linear programming (ILP) synthesis methodology [MPMS08] that, starting from a biochemical application and a given biochip, determines the allocation, placement, resource binding, and scheduling of the operations in the application. The research has shown that taking the placement into account during synthesis can lead to better results. The placement step takes into account potentially faulty cells, reconfiguring the biochip to provide fault-tolerance.

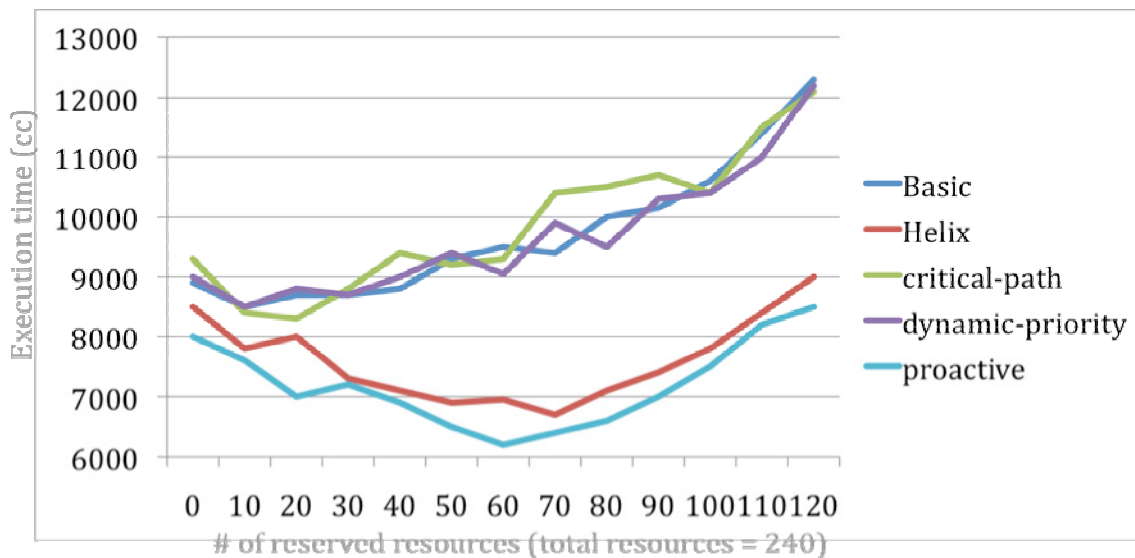
MPSoC architectures and programming models (DTU)

The multi-core research efforts are focused on network-on-a-chip based architectures. Currently the work of DTU is conducted in two themes: i) exploring high-level programming models focusing on programmer productivity and ii) investigating the hardware/software interface between the processing elements and the interconnect network. The wide use of multi-core architectures has led to a situation where programmers not accustomed to parallel programming will have to adapt their programs to parallel architectures. This means that easy to use, high productivity parallel programming models need to be explored. We are developing a task-based shared memory programming model where inter-task communication is made explicit. The second theme is on the hardware/software interface between the processors and the interconnection network. We believe that the interconnection network will have to support applications with radically different requirements. Thus, we are working on developing an interface that 1) provides very low communication latency and 2) can support a plethora of programming models and application requirements. The first studies has focused on supporting shared memory programming models efficiently both in terms of performance and hardware resource utilization. This have been done through a case study of an embedded image processing application [RaStKa08], for which parallelism and scalability has been investigated. The major challenges faced when parallelizing the application were to extract enough parallelism from the application and to reduce load imbalance. The application had limited immediately available parallelism. It was difficult to further extract parallelism since the application had small data sets and parallelization overhead were relatively high. There was also a fair amount of load imbalance, which was made worse by a non-uniform memory latency. Even so, we have shown that with some tuning relative speedups in excess of 9 on a 16-core system can be reached.

Run-time resource management (DTU, IMEC)

Understanding the dynamic behavior of run-time reconfigurable systems is a very complicated task, due to the often very complicated interplay between the application, the application mapping, and the underlying hardware architecture. However, it is a key issue to determine the right reconfigurable architecture and a matching optimal on-line resource management policy.

Although architecture selection, application mapping and run-time system have been studied intensively in the past, they have not been thoroughly studied and modelled in the context of run-time reconfigurable system. DTU has extended its simulation framework COSMOS to study the dynamic behavior of run-time reconfigurable systems. COSMOS is an extension of the ARTS multiprocessor simulation framework which were developed during ARTIST2.



Through a number of design space exploration experiments, they have pinpointed the critical design issues in the reconfigurable architecture study and analyze their impact on the architecture performance. Experiments with various run-time resource management policies have shown that it is possible to gain performance from such architectures and have suggested some general guidelines for obtaining efficient run-time resource management [WuHaMa08].

Component-based service model (DTU, B&O ICEpower)

DTU has together with B&O ICEpower developed a component-based service model which allows for early exploration and performance estimation of MPSoC based systems. A service execution model is a behavioural implementation of the services offered by a component. Depending on the level of abstraction used to describe the service execution model, a service can represent anything from the execution of a task or a function to arithmetic operations or actual instructions. The service execution model defines, which services are provided, how their behaviour is implemented and their latency.

The service execution models uses a simulation based approach, that enables designers to extract detailed quantitative information regarding the runtime properties of the components being modelled e.g. execution profiles, resources utilization, memory usage, communication channel utilization, stalls and their causes, etc., and, thus, directs the designer to the best suited configuration of a given system. The work has resulted in two publications [THMJ08, THM08].

Modelling and Evaluation of Reliability Analysis for MpSoCs (TU Braunschweig)

TU Braunschweig has taken several steps to address the prediction of performance implications of errors in systems with unreliable components and fault-tolerance mechanisms. The main focus is the impact of these factors on real-time performance. For this purpose initial timing models have been developed to reflect the performance of such systems in the error-free case as well as in case of errors. These models enable an exact specification of the timing

effects different fault-tolerance mechanisms may have. In this context we currently restrict our consideration to transient errors, such that systematic design failures can be excluded.

We have developed two methods to evaluate the reliability, i.e. the ability of a system or a component to perform its intended function. For this, we obtain a time-dependant function that describes the probability of correct operation during a period of time. The first approach is Monte-Carlo simulation ([SE08]). Based on a given system configuration the timing behaviour of a component is simulated, whereas errors are randomly inserted corresponding to the specified error model. Because Monte-Carlo simulation is based on random events a large number of simulation runs has to be performed, what leads to long runtimes until accurate results are obtained.

To remove the limitation of long simulation runtimes a formal analysis procedure has been developed (to be published). It is based on priority-driven environments with strictly period activation of tasks. In contrast to existing methods which consider only dedicated situations of a fault-tolerant component for its timing behaviour our approach realizes a load-dependant analysis, thus we do not constrain the analysis to only a worst-case situation of transient overload. The results of this new analysis methodology are compared with those obtained from Monte-Carlo simulation. The good compliance of these results shows that the proposed analysis is an accurate technique for reliability estimation which is much faster than simulation.

http://www.ida.ing.tu-bs.de/en/research/projects/autonomous_integrated_systems_ais/

System Scenarios for Embedded System Design (IMEC, TU/e, DUTH, UCM)

This work focuses on a generic and systematic design-time/run-time methodology for handling the dynamic nature of modern embedded systems, which can be utilized by existing design methodologies to increase their efficiency. It is based on the concept of system scenarios, which group system behaviours that are similar from a multi-dimensional cost perspective, such as resource requirements, delay, and energy consumption, in such a way that the system can be configured to exploit this cost similarity. At design-time, these scenarios are individually optimized. Mechanisms for predicting the current scenario at run-time and for switching between scenarios are also derived. This design trajectory is augmented with a run-time calibration mechanism, which allows the system to learn on-the-fly during its execution, and to adapt itself to the current input stimuli, by extending the scenario set, changing the scenario definitions, and both the prediction and switching mechanisms.

www.es.ele.tue.nl/~vali/scenarios/

Dynamic Data Type Design Search Space Exploration (IMEC, DUTH, UCM)

IMEC has developed a methodology and library for automated Dynamic Data Type (DDT) optimization under the MATISSE framework. DUTH has modularized the DDT library to increase the size design search space and to investigate optimizations for MPSoC platforms. UCM has developed Vector Evaluated Genetic Algorithm to speed up the automatic exploration of the extended design search space.

Task migration to Hardware Accelerators (IMEC, NTNU)

IMEC has developed the Task Concurrency Methodology for run-time scheduling of tasks on MPSoC platforms. NTNU is extending the methodology to include task migration capabilities to Hardware Accelerators realized on FPGAs.

2.2 *Individual Publications Resulting from these Achievements*

Several publications were obtained in this year, which are closely related to the activity. We group them on a partner-by-partner basis.

ETHZ:

- Jian-Jia Chen, Lothar Thiele: Expected System Energy Consumption Minimization in Leakage-Aware DVS Systems. International Symposium on Low Power Electronics and Design, August, 2008.
- Jian-Jia Chen, Lothar Thiele: Energy-Efficient Task Partition for Periodic Real-Time Tasks on Platforms with Dual Processing Elements. 14th Intl Conference on Parallel and Distributed Systems, IEEE, December, 2008.

Linköping

- Min Bao, Alexandru Andrei, Petru Eles, Zebo Peng, "Temperature-Aware Voltage Selection for Energy Optimization", Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, pp. 1083-1086.
- Min Bao, Alexandru Andrei, Petru Eles, Zebo Peng, "Temperature-Aware Task Mapping for Energy Optimization with Dynamic Voltage Scaling", The IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems (DDECS'08), Bratislava, Slovakia, April 16-18, 2008, pp. 44-49.

UoB

- D. Dondi, A. Bertacchini, D. Brunelli, L. Larcher and L. Benini, "Modelling and Optimization of a Solar Energy Harvester System for Self Powered Wireless Sensor Networks". IEEE Transactions on Industrial Electronics, 55:7(2759-2766), 2008.
- D. Brunelli, "Miniaturized Solar Scavengers for Ultra-low Power Wireless Sensor Nodes". Workshop on Energy in Wireless Sensor Networks (WEWSN 2008), Greece, 2008.

DTU

- [MPMS08] Elena Maftai, Paul Pop, Jan Madsen, Thomas K. Stidsen, "Placement-Aware Architectural Synthesis of Digital Microfluidic Biochips using ILP", in Proceedings of International Conference on Very Large Scale Integration (in press), 2008
- [MPPV08] Elena Maftai, Paul Pop, Florin Popentiu-Vladicescu, "Synthesis of reliable digital microfluidic biochips using Monte Carlo simulation" in Safety, Reliability and Risk Analysis: Theory, Methods and Applications (Martorell et al., eds.), 2008, Taylor & Francis Group, London, ISBN 978-0-415-48513-5, pages 2333—2341
- [RaStKa08] M. Rasmussen, M. Stuart and S. Karlsson "Parallelism and Scalability in an Image Processing Application", In proceedings of 4th International Workshop on OpenMP, IWOMP'2008, volume 5004 of LNCS, pages 158-169, May 2008.
- [WHM08] Kehuai Wu, Esben Rosenlund Hansen, Jan Madsen, Towards Understanding and Managing the Dynamic Behavior of Run-Time Reconfigurable Architectures, in the proceedings of the Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA'08), July 2008.
- [THM08] Anders Tranberg-Hansen, Jan Madsen, A Service Based Component Model for Composing and Exploring MPSoC Platforms, in the proceedings of the 1st International Symposium on Applied Science in Biomedical and Communication Technologies, October 2008.

TU Braunschweig

- [SE08] M. Sebastian and R. Ernst. Modelling and Designing Reliable On-Chip Communication Devices in MPSoCs with Real-Time Requirements. In 13th IEEE International Conference on Emerging Technologies and Factory Automation, 2008.

IMEC vzw.

- 'Run-time management of a MPSoC containing FPGA tiles', Nollet, V.; Avasare, P.; Eeckhaut, H.; Verkest, D. and Corporaal, H., Journal IEEE Trans. Very Large Scale Integration Systems (TVLSI), 2008
- 'Fast multi-dimension multi-choice Knapsack heuristic for MP-SoC run-time management', Couvreur, C.; Nollet, V.; Catthoor, F. and Corporaal, H., Journal ACM Transactions on Embedded Computing Systems (TECS), 2008
- 'A Safari Through the MPSoC Run-Time Management Jungle', Nollet, V.; Verkest, D. and Corporaal, H., Journal of Signal Processing Systems, 2008
- 'Power dissipation of the network-on-chip in multi-processor system-on-chip dedicated for video coding applications', Milojevic, D.; Montperrus, L. and Verkest, D., Journal of Signal Processing Systems, 2008
- 'An automatic scratch pad memory management tool and MPEG-4 encoder case study', Baert, R.; De Greef, E.; Brockmeyer, E.; Vanmeerbeeck, G.; Avasare, P.; Mignolet, J. and Cupak, M., 45th Design Automation Conference (DAC), 2008
- 'Exploring Parallelizations of Applications for MPSoC platforms using MPA', Baert, R.; Brockmeyer, E.; Wuytack, S. and Ashby, T., Design, Automation, and Test in Europe (DATE), 2009
- 'Simulation framework for early phase exploration of SDR platforms: a case study of platform dimensioning', Trautmann, M.; Mamagkakis, S.; Bougard, B.; Declerck, J.; Umans, E.; Dejonghe, A.; Van der Perre, L. and Catthoor, F., Automation, and Test in Europe (DATE), 2009

2.3 Interaction and Building Excellence between Partners

Optimization-centric MPSoC Design (University Bologna together with ETHZ)

The interaction between ETHZ and University Bologna was based on various face-to-face meetings in Zurich and in Bologna. In addition, various phone meetings took place for clarifying technical issues during the tool integration of DOL and MPARM. As a result of the close cooperation, a PhD student exchange currently takes place (Michele Magno from Bologna currently stays at ETHZ).

Energy efficient embedded system design (Linköping, UoB)

The interaction in this activity has been between Linköping and UoB.

- Meeting/discussion at the conference "Design, Automation and Test in Europe (DATE08)", Munich, Germany, March 10-14, 2008.
- The MPARM platform from Bologna has been extensively used for the thermal aware energy minimisation experiments at Linköping. This has led to frequent interactions between the groups.

Design of fault tolerant distributed embedded systems systems (Linköping, DTU)

The interaction in this activity has been between Linköping and DTU.

- Meeting/discussion at the conference "Design, Automation and Test in Europe (DATE08)", Munich, Germany, March 10-14, 2008.
- Paul Pop from DTU has visited Linköping several times during 2008.

System-level design framework with cycle-accurate simulator (UoB, ETHZ)

The interaction in this activity has been between ETHZ and UoB.

- Several phone meetings/discussions between UoB and ETHZ during 2008.
- Iuliana Bacivarov, Wolfgang Haid and Kai Huang from ETHZ have visited UoB during 2008.
- The MPARM platform from Bologna has been extensively used by ETHZ. This has led to frequent interactions between the groups.

Photovoltaic scavenging systems from the model to the optimized desing (UoB, ETHZ)

The interaction in this activity has been between UoB and ETHZ. This is part of a close cooperation between the two groups in the area of Power Management for Energy Harvesting Sensor Nodes.

- Meeting/discussion at the conference "Design, Automation and Test in Europe (DATE08)", Munich, Germany, March 10-14, 2008.

Dynamic Data Type Design Search Space Exploration

Two PhD candidates, namely Miguel Peon from UCM and Alexandros Bartzas from DUTH, visited Imec for 2 months in the beginning of 2008 to work on DMA and Memory assignment optimizations for MPSoC with the use of Software metadata.

System Scenarios for Embedded System Design

One PhD candidate, namely Elena Hammani from NTNU, visited Imec for 3 months in the end of 2008 to work on task migration extensions on the Task Concurrency Management (TCM) methodology.

There were 2 meetings of the scenario cluster in April'08 and November'08 taking place in IMEC and Uni. Gent, respectively. The interaction focused on further improvements of the scenario extraction, identification, exploitation, switching and calibration steps.

The partners from IMEC, TU Dortmund (at ICD), DUTH and TU/e are jointly working on the MNEMEE project funded through the 7th framework (see <http://www.mnemee.org>). Under this project design-time tools and run-time resource management components are integrated in a single environment. The focus is the memory subsystem of MPSoC.

The partners from IMEC, DUTH and KTH are jointly working on the MOSART project funded through the 7th framework (see <http://www.mosart-project.org>). Under this project design-time tools and run-time resource management components are integrated in a single environment. The focus is the interconnect, namely the Network-on-Chip (NoC) subsystem of MPSoC.

Synthesis of digital microfluidic biochips (DTU, Duke)

DTU and Duke University has started a collaboration on digital microfluidic biochips. A PhD student from DTU working on microfluidic biochips is currently visiting Prof. Krish Chakrabarty's group at Duke University, USA, for a period of 6 months. Duke University is an affiliated partner

in ArtistDesign, and has been the first to develop droplet-based biochips that use electrowetting on dielectric for droplet transport.

Run-time resource management (DTU, IMEC)

DTU and IMEC have started discussions on possible collaboration in the area of run-time resource management. Plans for a joint cluster workshop on the theme has been initiated.

Component-based service model (DTU, B&O ICEpower)

DTU and B&O ICEpower are working closely together to develop a new design methodology and support tools for the design flow of B&O ICEpower. A PhD student from DTU is spending 10-20% of his time in the company. B&O ICEpower is an affiliated partner in ArtistDesign.

2.4 Joint Publications Resulting from these Achievements

Even though there are some Joint publications already obtained this year (see list below), this is only the first year of the activity and sustained stream of joint publications is expected every year.

Linköping, DTU

1. Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng, "Synthesis of Flexible Fault-Tolerant Schedules with Preemption for Mixed Soft and Hard Real-Time Systems", 11th EUROMICRO CONFERENCE on DIGITAL SYSTEM DESIGN (DSD 2008), Parma, Italy, September 3-5, 2008, pp. 71-80.
2. Petru Eles, Viacheslav Izosimov, Paul Pop, Zebo Peng, "Synthesis of Fault-Tolerant Embedded Systems", Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, pp. 1117-1122.
3. Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng, "Scheduling of Fault-Tolerant Embedded Systems with Soft and Hard Timing Constraints", Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, 915-920.

DTU, Braunschweig, Bologna

1. Wu, K., Madsen, J., Kanstein, A., Mladen, B., *MT-ADRES: Multithreading on Coarse-Grained Reconfigurable Architecture*, Intel. Journal of Electronics (IJE), Volume 95, Issue 7, July 2008. Page(s): 761-776.
2. Anders Tranberg-Hansen, Jan Madsen, Bjørn Sand Jensen, A Service Based Estimation Method for MPSoC Performance Modelling, to appear in the proceedings of the 3rd International Symposium on Industrial Embedded Systems, June 2008.
3. A Reactive and Cycle-True IP Emulator for MPSoC Exploration Mahadevan, S.; Angiolini, F.; SparsSparso, J.; Benini, L.; Madsen, J. Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Volume 27, Issue 1, Jan. 2008 Page(s):109 – 122

IMEC vzw. & DUTH & UCM

- 'Enabling run-time memory data transfer optimizations at the system level with automated extraction of embedded software metadata information', Bartzas, A.; Peon-Quiros, M.; Mamagkakis, S.; Catthoor, F.; Soudris, D. and Mendias, J., Asia and South Pacific Design Automation Conference - ASP-DAC, 2008

- 'Optimization Methodology of Dynamic Data Structures based on Genetic Algorithms for Multimedia Embedded Systems', Baloukas, C.; Risco Martin, J.; Atienza, D.; Poucet, C.; Papadopoulos, L.; Mamagkakis, S.; Soudris, D.; Hidalgo, J.; Catthoor, F. and Lancars, J., Elsevier Journal of Systems and Software (JSS), 2008

IMEC vzw. & TU/e

- 'A System Scenario based Approach to Dynamic Embedded Systems', S.V. Gheorghita, M. Palkovic, J. Hamers, A. Vandecappelle, S. Mamagkakis, T. Basten, L. Eeckhout, H. Corporaal, F. Catthoor, F. Vandeputte, K. De Bosschere, ACM Transactions on Design Automation of Electronic Systems, ToDAES. To appear in 2009.

IMEC vzw. & TU/e & DUTH & TU Dortmund (at ICD)

- 'MNEMEE: Memory management technology for adaptive and efficient design of embedded systems' S.Mamagkakis, P.Lemmens, D.Soudris, T.Basten, P.Marwedel, D.Kritharidis, G.Guilmin, 16th IFIP/IEEE International Conference on Very Large Scale Integration - VLSI-SOC, 2008.

IMEC vzw. & KTH & DUTH

- 'MOSART: Mapping Optimisation for Scalable multi-core ARchiTecture', B. Candaele, A. Jantsch, T. Ashby, K. Tiensyrjä, F. Ieromnimon, B. Vanthournout, P. Di Crescenzo, D. Soudris, 16th IFIP/IEEE International Conference on Very Large Scale Integration - VLSI-SOC, 2008.

2.5 *Keynotes, Workshops, Tutorials*

Invited Talk L. Thiele (ETHZ): MPSOC Conference. Aachen, Germany, June 23-27, 2008: Lothar Thiele described a new approach for mapping algorithms onto MPSoC architectures. It is a result of a cooperation between ARTISTDesign partners from Aachen, TIMA and LETI. The design methodology is named DOL (distributed operation layer) and targets real-time and efficient multiprocessor systems and applications.

Summer School: Course on Embedded Systems (ETHZ, L. Thiele), Florianopolis, Brasil, August 25-2, 2008. The summer school was dedicated to promote the interaction between the embedded system communities in Europe and South America. Lothar Thiele was presenting a wide range of subjects, starting from basic methods to design embedded software for embedded systems. In addition, he presented methods for real-time scheduling and performance analysis of distributed embedded systems.

ARTIST Summer School: Invited talk on design space exploration and performance analysis (ETHZ, L. Thiele), Grenobles, France, Sept 8-12, 2008. During the ARTIST Summer School in Grenobles, Lothar Thiele presented interface-based design techniques for stream-based embedded systems. Real-time behavior is obtained by extending the usual component interfaces by resource-aware guarantee-assume predicates. This way, constraints and properties of single components propagate through the whole system and define the relation between the component-based and system-based properties.

Tutorial L. Thiele (ETHZ): Analysis of Distributed Embedded Systems. CASTENESS WORKSHOP ROMA, Jan. 15-18, 2008. During the CASTENESS Workshop, ETHZ gave a tutorial on the different methods to estimate the performance of distributed embedded systems, including computation, communication and resource sharing.

Invited Talk L. Thiele (ETHZ): Workshop Mapping Algorithms onto MPSOC. Germany, June 16-17, 2008. Lothar Thiele presented the current state-of-the art in mapping algorithms onto multi-processor platforms. Different approaches have been compared and a classification based on the application domain and estimation methods has been provided.

ArtistDesign meeting (upcoming meeting), location: Düsseldorf, Germany; date: 27th and 28th of November 2008: Within the frame of this ArtistDesign meeting which addresses the mapping of applications to MPSoCs, ETHZ presents an overview and a SW demonstration of the Distributed Operation Layer framework.

Castness 2008 Workshop; location: Rome, Italy; date: 15th-18th of January 2008: The objectives of CASTNESS workshops and schools are, first, to provide training about the future of multi-processor/adaptable embedded systems (system SW, HW architectures, applications) and second, the cross-dissemination among European projects. ETHZ presented an overview and a SW demonstration of the Distributed Operation Layer framework, included in a complete MPSoC design flow, as well as detailed information about the design space exploration and mapping optimization steps within this framework.

Invited talk: Petru Eles - Synthesis of Fault-Tolerant Embedded Systems DATE 2008 Conference, Munich, Germany - March 10, 2008 As part of the special day on Dependable Embedded Systems: With this occasion several results obtained in the ARTIST context have been made accessible to an international audience. They are related, in particular, to fault tolerance aspects of distributed real-time systems like those used in automotive applications.

Industrial Invited talk: “Energy Scavenging Techniques”

Cesena, Italy – September 11, 2008

Speaker: Luca Benini

Technogym spa, is a world leader in the design of fitness equipment for private homes, fitness clubs, hotels, spas, rehabilitation centers, corporate gyms, universities, professional sports facilities and beyond was very interested on the emerging opportunities available from MPSoC and energy harvesting technologies.

Luca Benini gave a talk on the system challenges of designing wireless sensor networks, particular emphasizing the challenges of making these systems self-powered using energy harvesting techniques. The seminar was attended by approximately 50 people.

Industrial Invited talk: “Wireless Sensor Networks for Smart Home Environments”

Turin, Italy – November 24, 2008

Speaker: Luca Benini

Telecom Italia Lab, is a dedicated research centre for Telecom Italia, that is Italy's domestic leader for telecommunication, supplying about 21 million fixed lines and 36 million mobile lines. Luca Benini is invited to give a talk about the platforms for developing smart home environments. The talk covered research front-ends of Wireless Sensor Networks and low power system design, including (1) energy harvesting policies; (2) multimedia streaming over WSN and wearable devices. The seminar was attended by approximately 20 people.

Opening Keynote : Networks, multicore, and systems evolution - facing the timing beast (R. Ernst)

Emerging Technologies and Factory Automation Conference

Hamburg, Germany – September 16, 2008

Abstract: Embedded systems rapidly grow in several dimensions. They grow in size, from local isolated networks with simple protocols to network hierarchies to large open heterogeneous networks with complex communication behaviour. They grow in performance, from simple microcontrollers to superscalar to multicore systems with many levels of memory hierarchy. And, they expand in the time dimension by moving from static system functions to open and evolutionary functions that change over time and require new design methods and autonomous system functions. All these development contribute to an ever increasing behavioural complexity with equally complex timing. Nevertheless, the fundamental requirements to reliability and performance predictability have stayed and even been enhanced. Embedded system technology has responded with new integration methods and software architectures supported by platform control methods using new service quality metrics, and with composable formal methods that scale with system size. The talk gave an overview on this exiting scientific field and will give practical examples

http://www.etfa2008.org/ETFA_2008/Keynote_Talks.html

**Keynote : Platform trends for software defined radio: Heterogeneity at its best
FETCH 2008**

Montebello, Canada – January 7, 2008

Software defined radios rely on intensive use of heterogeneity at various levels. The baseband section is built-up of multiple heterogeneous cores and hardware accelerators; the required low power consumption demands a precious equilibrium between hardware and software implementation of the inner and outer modem algorithms and a stringent trade-off analysis at all levels of implementation abstraction .

<http://fetch2007.googlepages.com/programme>

Workshop : ‘International Workshop on Object-Oriented Software Development for the Embedded World - OOSDEW’

European Conference on Object-Oriented Programming - ECOOP 2008

Paphos, Cyprus – July 7, 2008

The purpose of the IMEC organized OOSDEW workshop is to bring hardware and software communities closer together in order to explore the current and future challenges in application development and integration in different embedded system domains. We examined software engineering technologies for addressing those challenges, without neglecting the often stringent constraints imposed by hardware.

<http://www.imec.be/SE4ES/ECOOP08/>

Workshop : ‘7th Workshop on Optimizations for DSP and Embedded Systems

IEEE/ACM International Symposium on Code Generation and Optimization - CGO 2008

Seattle, USA – March 22, 2009

The aim of the IMEC organized ODES workshop is to give the opportunity to researchers and practitioners to share their findings and get feedback on optimizations for performance, power and cost of DSP and embedded systems. Topics of interest include, but are not limited to: Algorithmic transformations and code/software optimization, Hardware and software optimizations for low-power consumption and/or code density, Coprocessor and hardware accelerators, Compiler techniques and code generation for media processing etc..

<http://www.imec.be/odes/>

Conference: Industrial Embbed Systems**3rd International Symposium on Industrial Embedded Systems (SIES)***Montpellier, France – 11-13 June, 2008*

Anders Tranberg-Hansen from DTU gave a talk on “A Service Based Estimation Method for MPSoC Performance Modelling”. The talk presented an abstract service based estimation method for MPSoC performance modeling, which allows fast, cycle accurate design space exploration of complex architectures including multi processor configurations at a very early stage in the design phase. To illustrate the method, a small MPSoC system, developed at Bang & Olufsen ICEpower was modelled and performance estimates were produced for various configurations of the system implementation.

Mini-keynote: Codesign**8th International Forum on Application-Specific Multi-Processor SoC (MPSoC)***St. Gerlach, The Netherlands, June 23-27, 2008.*

Jan Madsen from DTU gave a talk on “*Adaptive Embedded Systems Challenges of Run-Time Resource Management*”. The mini-keynote addressed some of the challenges of run-time resource management in adaptive embedded systems. The challenges come from the often very complicated interplay between the application, the application mapping, and the underlying hardware architecture. With MPSoC, we have the technology to design and fabricate dynamically reconfigurable hardware platforms. However, such platforms will pose new challenges to tools and methods to efficiently explore these platforms at run-time.

<http://www.mpsoc-forum.org/>

Invited talk: Industrial Embbed Systems**1st International Symposium on Applied Science in Biomedical and Communication Technologies (ISABEL)***Aalborg, Denmark – 25-28 October, 2008*

Anders Tranberg-Hansen from DTU gave an invited talk on “A Service Based Component Model for Composing and Exploring MPSoC Platforms”, in the proceedings of the 1st International Symposium on Applied Science in Biomedical and Communication Technologies,

<http://isabel2008.es.aau.dk/>

3. Milestones, and Future Evolution

3.1 *Problem to be Tackled over the next 12 months (Jan 2009 – Dec 2009)*

The activities started in Y1 will continue in Y2. A summary of the problems to be tackled and of the integration opportunities is summarized as follows.

Optimization-centric MPSoC Design (University Bologna together with ETHZ)

ETHZ and Bologna will continue on combining their MPSOC design frameworks MPARM and DOL. In particular, the focus will be on designing predictable communication fabrics in order to improve the matching between performance estimation results on the one hand and cycle-true simulations on the other.

Design of fault tolerant distributed embedded systems

During the second year Braunschweig will address the issue of design and optimisation of fault tolerant distributed and MPSoC systems considering various hardening degrees of the underlying hardware platform. This will be based on the analysis techniques developed as part of the "Platform and MPSoC Analysis" activity. The approach will allow for a fine-grained trade-off between cost (hardening degree), performance, and reliability of embedded systems implemented on distributed or MPSoC platforms.

Energy efficient embedded system design

Linkoeping will continue our research concerning temperature aware and energy efficient design of real-time embedded systems. Concerning the temperature awareness we will investigate in particular two aspects:

1. Exploiting the relation between temperature and frequency in order to further improve the efficiency of dynamic voltage/frequency selection.
2. Application of fast and sufficiently accurate analytical temperature models for the system level, which allow for a more efficient design space exploration.

Photovoltaic scavenging systems from the model to the optimized desing (UoB, ETHZ)

University of Bologna and ETHZ will continue on the design and optimization of energy harvesting devices for distributed embedded systems. In particular we intend to provide an accurate study of the long-term behavior of the proposed scavenging platforms, and an analysis on how the behaviour and the characteristic will change using different end-devices with different profiles of power consumption.

System-level design framework with cycle-accurate simulator

The issue of design and optimisation of on-chip communication semantic will be addressed during the second year by UNIBO. We will develop a new software communication support for MPSoC systems considering several configuration options, from FIFO buffer location, to synchronization semantic, or notification mechanism. These options span across a large set of hardware platforms, ranging from multi-core architectures with shared memory based communication to architectures with scratch pads associated to each core tile, as well as hybrids of the previous ones.

We will investigate exact algorithms for the mapping, scheduling and power control (based on shutdown and variable and frequency scaling) for application task graphs onto multi-processor platforms. Deterministic and conditional task graphs will be considered.

Task distribution and migration

In the next year, the collaboration between IMEC and NTNU on task migration will focus on the customization of the existing methodologies for biomedical applications. Additionally, the collaboration between IMEC and DUTH and UCM will focus on the customization of the existing methodologies for shared/distributed memory hierarchies for MPSoC. Finally, the collaboration between IMEC and TU/e and KTH will focus on integration of the TU/e SDF³ (SDFG transformation tool) and KTH Nostrum (NoC simulator) academic tools within a toolflow that includes the IMEC MPA tool (Multiprocessor Parallelization Assistant).

MPSoC design and programming

DTU will continue to work on multi-core architectures. In particular, collaboration with IMEC on memory performance models will be initiated. Collaboration with B&O ICEpower will be extended to experiment with a larger industrial case. Work on dynamically reconfigurable architectures will be extended to support adaptivity and self-maintenance. Moreover, DTU will continue to work on programming models for multi-core architectures. In particular, developing a task-based shared memory programming model where inter-task communication is made explicit. Potential programming models for dynamically reconfigurable architectures will also be studied.

Synthesis for Biochips.

DTU and Duke will continue to work on biochip design. In particular, aiming at a more realistic biochip and biochemical application model, that can take into account the variability in the current biochip implementations.

3.2 Current and Future Milestones

System-level design framework and Optimization-centric MPSoC design

In the first year a system-level design framework for application specification, functional validation, debugging, and performance estimation with cycle-accurate simulation support was to be implemented by UNIBO. Moreover The DOL and MPARM tools of ETHZ and Bologna have been coupled in the first year.

The above milestone has been fulfilled.

During the second year the research will be continued with the following two milestones:

1. Developing a new software communication support for MPSoCs.
2. Investigate algorithms for the mapping, scheduling and power control for application task graphs onto MPSoCs.

The DOL-MPARM integration is still at its infancy, as many desirable features for an integrated mapping/simulation framework still need to be developed. It is the goal to have a demonstrable prototype within the time frame of the ARTISTDesign NoE.

Design of fault tolerant distributed embedded systems

In the first year, Linköping University will develop an approach to the design of safety critical, fault tolerant embedded applications with soft and hard real-time constraints (for the analysis aspects see “Platform and MPSoC Analysis” activity report). A quasi-static scheduling strategy will be used, where a set of schedules is synthesized off-line and, at run time, the scheduler will select the right schedule based on the occurrence of faults and the actual execution times of processes. An optimisation technique for the generation of schedule tables supporting such a quasi-static scheduling approach will be developed and implemented. A preemption technique will be elaborated as a method to generate flexible schedules that maximize the overall utility for the average case while guarantee timing constraints in the worst case.

The above milestone has been fulfilled.

During the second year we will address the issue of design and optimisation of fault tolerant distributed and MPSoC systems considering various hardening degrees of the underlying hardware platform. This will be based on the analysis techniques developed as part of the “Platform and MPSoC Analysis” activity.

Energy efficient embedded system design

In the first year a temperature-aware dynamic voltage selection technique for energy minimization will be elaborated. A temperature-aware task mapping technique will be developed for energy optimization in systems with dynamic voltage selection capability.

The above milestone has been fulfilled.

During the second year the research concerning temperature aware and energy efficient design of real-time embedded systems will be continued with the following two milestones:

1. Exploiting the relation between temperature and frequency in order to further improve the efficiency of dynamic voltage/frequency selection.
2. Application of fast and sufficiently accurate analytical temperature models for the system level, which allow for a more efficient design space exploration.

Modelling of and evaluation of fault-tolerance mechanisms with respect to real-time

TU Braunschweig will investigate the performance implications of fault-tolerance mechanisms in real-time systems. For this, event and error models will be introduced to model the occurrence of transient errors. We will propose and evaluate different methods to capture the run-time behaviour of unreliable components.

This milestone has been fully achieved. Initial timing models have been developed to reflect the performance of such systems in the error-free case as well as in case of errors. These models enable an exact specification of the timing effects different fault-tolerance mechanisms may have. We have proposed two methods for reliability evaluation: One is Monte-Carlo simulation, in which errors are randomly introduced into a simulation, another one is formal analysis, which delivers faster results.

Extension of reliability analysis to more general systems with extended event and error models To improve the applicability and precision of the initial reliability analysis, TU Braunschweig will work on extending this concept to more complex models, such as release jitter and burst errors. This will remove the current constraints of reliability analysis methods, which are restricted to simplified system and component models. Constraints to be addressed are the

exclusive consideration of strictly period activations as well as the analysis of single bit errors without any correlation amongst each.

Synthesis of digital microfluidic biochips

In year 1 DTU and Duke will work on digital microfluidic biochips. The goal is to model a biochemical application executing on a two-dimensional array of cells, where each cell can hold a droplet. A synthesis methodology that, starting from a biochemical application and a given biochip, determines the allocation, placement, resource binding, and scheduling of the operations in the application will be developed. The placement step should take into account potentially faulty cells, reconfiguring the biochip to provide fault-tolerance.

The above milestone has been fulfilled

During the second year, DTU and Duke will propose a more realistic biochip and biochemical application model, that can take into account the variability in the current biochip implementations, and the potential for contamination during operations. The addressed design tasks will be revisited considering the new stochastic model and contamination constraints.

MPSoC architectures and programming models

In year 1 DTU worked on architectures and programming models for MPSoC platforms. The goal was to focus on two areas i) exploring high-level programming models focusing on programmer productivity and ii) investigating the hardware/software interface between the processing elements and the interconnect network.

The above milestone has been fulfilled

During the second year, DTU will continue this work and start a collaboration with IMEC. No concrete collaboration action points have been defined. The primary purpose is to discuss memory performance models. However, IMECs work on nomadic embedded systems will also be discussed and possible collaboration areas will be identified.

Run-time resource management

In year 1 DTU extended work on run-time reconfigurable systems started in ARTIST2. The goal is to extend the COSMOS model to be able to experiment with different run-time resource management policies.

The above milestone has been fulfilled

During the second year, DTU will continue the work on run-time reconfigurable systems and extend the focus on the hardware architecture to support run-time reconfiguration and elf-maintenance.

Component-based service model

In year 1 DTU extended its service-based model initiated during ARTIST2, to be applied in an industrial setting together with B&O ICEpower. The goal is to extend the model to capture MPSoC systems and to show the feasibility of the model by applying it to a simple industrial case.

The above milestone has been fulfilled

During the second year, DTU and B&O ICEpower will extend the work on the service-based model with focus on performance evaluation of MPSoC platforms. Focus will be on modeling the software executing on the platform and on experimenting with a larger case study.

3.3 Main Funding

ETHZ:

- ICT-Project COMBEST
- ICT-Project SHAPES
- ICT-Project PREDATOR
- National funding on Sensor Networks (MICS, SwissExperiment), and corresponding industry-funded projects.

Linköping University:

- Swedish Foundation for Strategic Research (SSF)
- Swedish research Council

University of Bologna:

- ICT-Project PREDATOR
- Industrial funding on Sensor Networks from Telecom Italia spa

DTU

- DaNES (Danish Network for Embedded Systems, funded by the Danish Advanced Technology Foundation), Denmark. Period 2007-2010.
- MoDES (project on Model Driven Development of Intelligent Embedded Systems funded by the Danish Strategic Research Council), Denmark. Period 2006-2009.
- ProCell (project on programmable cell chip: culturing and manipulation of living cells with real-time reaction monitoring funded by the Danish Strategic Research Council),

TU Braunschweig

- **Autonomous Integrated Systems (AIS) Project**
Within the German research project “Autonomous Integrated Systems” (AIS) new design methodologies are explored to tackle the challenges resulting from unreliable components. The project is funded half by the German “Federal Ministry of Education and Research” and half by an industry consortium arranged within the “edaCentrum”.
<http://www.edacentrum.de/ais>
- **MOSART IST-215244 Project:**
Mapping Optimization for Scalable multi-core ARchiTecture. ArtistDesign partners involved: Interuniversitair Micro-Elektronica Centrum (IMEC) vzw., Democritus Uni. Thrace (DUTH) and Kungliga Tekniska Hagskolan (KTH)
<http://www.mosart-project.org/>
- **MNEMEE IST-216224 Project:**
Memory maNagEMEnt technology for adaptive and efficient design of Embedded systems. ArtistDesign partners involved: Interuniversitair Micro-Elektronica Centrum (IMEC) vzw., Democritus Uni. Thrace (DUTH) and Technische Universiteit Eindhoven (TU/e)
<http://www.mnemee.org/>

- **IMEC Apollo research program:**

Disruptive technologies needed to realize nomadic embedded systems for 2012 and beyond. These are technology aware architectures, multiprocessor system-on-chip technology, and reliable design methodologies for sub-45nm unreliable components. For the Apollo research, IMEC cooperates with industrial partners, such as integrated device manufacturers, fabless and fablite IC solution providers, and system integrators. http://www2.imec.be/imec_sites/objects/80acd42f851591023f893a7d96fd96bf/annualreport.pdf (page 36)

4. Internal Reviewers for this Deliverable

Lothar Thiele, ETHZ

Petru Eles, Linkoeping