IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Activity - Progress Report for Year 1

Platform and MPSoC Analysis

Clusters:

Hardware Platforms and MPSoC

Activity Leader:

Prof. Jan Madsen (DTU)

http://www.imm.dtu.dk/

Policy Objective (abstract)

The main objective of the activity is to build a common research environment, which integrates performance analysis algorithms and tools for hardware platforms and Multi-Processor System-on-Chip (MPSoC). The main challenge is the introduction of new aspects such as robustness, adaptivity and power consumption, which need to be addressed at run-time. The teams involved in the activity aim at developing and integrating modelling and analysis techniques for scalable performance analysis of applications executing on embedded hardware platforms.

Versions

number	comment	date
1.0	First version delivered to the reviewers	December 19th 2008

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1. Overview of the Activity

1.1 ArtistDesign Participants and Roles

Activity leader: Prof. Jan Madsen – Technical University of Denmark, DTU (Denmark)
System-level modelling and analysis of MPSoC and networked embedded systems. Architectures and programming models for multi-core embedded systems. Analysis and optimization of real-time and fault-tolerant applications implemented on distributed platforms and MPSoC. Reconfigurable platforms and run-time resource management.

Team leader: Prof. Petru Eles – Linköping University, LiU (Sweden)
(i) Timing Analysis.
(ii) Analysis and optimization of real-time and fault-tolerant applications implemented on distributed platforms and MPSoC.
(iii) Analysis and optimization of energy efficient, time constrained embedded systems.

Team leader: Prof. Lothar Thiele – TIK, ETH Zürich, ETHZ (Switzerland)
Developing a calculus to describe the performance of communication-centric systems, unifying the models for computation, combining tools for component-based performance analysis of MPSoC. Our role in this activity will be on component-based analytic methods to analyze the performance properties and memory requirements of distributed embedded systems.

Team leader: Prof. Rolf Ernst – TU Braunschweig, TUBS (Germany)
TU Braunschweig contributes formal performance analysis methods for MPSoC, with a focus on the timing implications of inter-task synchronization.

Team leader: Dr. Stylianos Mamagkakis – Interuniversity Microelectronics Centre, IMEC vzw. (Belgium)
This team will introduce novel software metadata extraction and analysis methodologies for design-time and run-time resource management optimizations of MPSoC platforms.

Team leader: Prof. Luca Benini – University of Bologna, UNIBO (Italy)
(i) Development of power modelling and estimation framework for systems-on-chip.
(ii) Development of optimal allocation and scheduling techniques for energy-efficient mapping of multi-task applications onto MPSoC.
(iii) Development of energy-scavenging techniques for ultra-low power sensor network platforms.

Professor, Prof. Hannu Tenhunen, Royal Institute of Technology, KTH (Sweden)
The contribution from KTH focuses on various design aspects, architectures, and agent based run-time reconfigurability and adaptivity.

1.2 Affiliated Participants and Roles

Dr. Daniel Karlsson, Volvo Technology Corporation

Architecture and Design of Automotive Embedded Systems

Dr. Kai Richter – Symtavision (Germany)
Symtavision contributes industrial methodologies.

Dr. Arne Hamann – Robert Bosch GmbH (Germany)
Contributes on important embedded systems related research problems in the automotive industry.

Prof. Dimitrios Soudris – Democritus Uni. of Thrace, DUTH (Greece)
This team will introduce software metadata for novel dynamic data type and data allocation optimizations for MPSoC platforms.

Prof. David Atienza – Uni. Complutense de Madrid, UCM (Spain)

This team will introduce software metadata for novel run-time memory management optimizations for MPSoC platforms.

Prof. Per Gunnar Kjeldsberg - Norges Teknisk-Naturvitenskapelige Uni., NTNU (Norway)

This team will introduce software and hardware metadata for novel task migration methodologies for MPSoC platforms utilizing hardware accelerators.

Bjørn Sand Jensen – Bang & Olufsen ICEpower (Denmark)
Areas of his team's expertise: chip design for audio signal processing

CTO Rune Domsteen – Prevas (Denmark)
Areas of his team's expertise: platform design for embedded systems

Dr. Patrick Schaumont – Virginia Tech (USA)

Design methods and architectures for secure embedded systems. Hardware/software codesign tools.

1.3 Starting Date, and Expected Ending Date

Starting date: January 1st, 2008

Ending date: Modelling and analysis is a long term effort and is expected to continue after the end of the project due to the lasting integration achieved by the NoE.

1.4 Policy Objective

With growing maturity of scalable performance analysis algorithms and tools, new aspects, such as the platform robustness, can be included in analysis. Robustness to changes is particularly important for systems-on-chip since the cost of a redesign is high. At the same time robustness to faults is becoming a concern with shrinking feature sizes. In most practical cases, power consumption must be considered. There is currently no team in Europe that addresses all aspects and their interdependencies. So integration of methods and tools will be needed to be able to (1) define meaningful robustness metrics that reflect design tradeoffs (2) assess the robustness of a design based on such metrics. This integration will extend the world leading position of Europe in the field of scalable formal performance analysis to the domain of hardware platform and MPSoC design.

1.5 Background

The activity will be based on the complementary expertise of the participating partners in terms of Hardware Platform and MPSoC Analysis. In particular, the following areas are covered: Power modelling and analysis, power robustness assessment (University Bologna), platform performance modelling (University Braunschweig), analytical methods for reliability, performance and adaptability analysis of execution platforms (University of Denmark), reliability modelling, analysis and optimization (University Linköping), interfaces that communicate at run-time, aspects that are relevant for the efficiency of the run-time mapping components (IMEC, Belgium), simulation techniques and tools for NoC performance estimation and validation, interconnect and communication centric performance estimation techniques (KTH Sweden).

In addition, there have been already joint work and publications by some of the members of this activity, which will be used as a valuable starting point.

In more details, the above mentioned groups has been working intensively on Power Modelling for SoC Platforms. In particular, they developed a virtual platform for power modelling of complex multi-core systems on chip. This platform can facilitate further integration among partners and associates, thanks to is flexibility and generality. In terms of “scheduling based energy optimization for energy-scavenging wireless sensor networks”, a novel scheduling strategy (referred to as *lazy scheduling*) that is well suited to energy-scavenging systems operating under real-time constraints has been developed by ETHZ and University Bologna. It is the first result of this kind in this quickly growing research area and received a lot of attention in the scientific community.

At ETHZ, an open tool set is available that allows the performance analysis of distributed embedded systems and MPSoC. It is based on the concept of Modular Performance Analysis (MPA). In addition, there are first results available that connect this system to the MPARM simulation framework from University Bologna and the SymTA/S analysis system from University Braunschweig/Symtavision.

1.6 Technical Description: Joint Research

The major focus of the activity on Platform Analysis is to establish a set of models and analysis methods that (a) scales to massively parallel and heterogeneous multiprocessor architectures, (b) is applicable to distributed embedded systems, (b) allows for the analysis of global predictability and the efficiency of system properties and (c) takes the available shared hardware resources and the corresponding management policies into account. Promising approaches are based on composable frameworks and on the treatment of resources as first class citizens in the analysis. Both, simulation-based and analytic methods will be combined. In addition, methods that focus on worst-case/best-case results, as well as those based on stochastic models, will be combined.

As a central ingredient of any analysis model, synchronization & communication abstractions are required for successfully deploying MPSoC hardware in embedded application domains. Efficiency is inherently related to both power and performance; hence it can be assessed as an energy metric. In embedded systems, abstractions are acceptable only if they do not compromise efficiency. It also extremely important to take into account variability of both hardware fabrics and application workloads, which are deemed to rapidly increase. In particular, the above abstractions need to be embedded into a framework that allows to analyze the performance properties and memory requirements of distributed systems. In particular, we will focus on methods that satisfy composability properties and use existing component-based methods, as known from software design, in the context of interfaces that communicate resource interactions. In addition, we are interested in adding run-time adaptivity to systems while using efficient run-time estimation methods combined with distributed finite horizon control methods. Again, the focus is on predictability AND efficiency. Here, we will use the expertise of members that will be involved in this activity are available at ETH Zurich (Lothar Thiele), University of Bologna (Luca Benini), KTH (Hannu Tenhunen), IMEC (Stylianos Mamagkakis), DTU (Jan Madsen) and TU Braunschweig (Rolf Ernst).

Another major challenge is to provide analysis tools and techniques to support the transitions between different abstraction levels in the design flow. Constraints should be communicated at design-time from one step to the next, taking into account the global effect that they will introduce in the system. Also, in order to ensure adaptivity of the system an interface should communicate at run-time the changes in the resource requests and the changes in the actual resource availability.

1.7 Problem Tackled in Year 1

A number of problems were tackled in Year 1, through several cooperations involving two or more partners. In the following paragraphs, we briefly summarize the problems tackled and the partners involved.

The Linköping group has addressed two major issues: (i)*Timing analysis of distributed real-time systems*. In this context, the emphasis was on heterogeneous systems using various task scheduling policies and heterogeneous communication protocols with static and dynamic phases. Both formal and simulation based approaches were developed. (ii) *Analysis of fault tolerant real time systems considering various reliability requirements and fault tolerance mechanisms*. In particular, the issue of transient faults has been considered. The basic effort was toward development of adequate scheduling algorithms. This work has been performed in cooperation with the DTU group.

In the past year, ETHZ followed the following research directions: Together with University Bologna, ETHZ worked on combining the MPARM simulation framework with the performance analysis framework MPA (Modular Performance Analysis). In particular, we attempted to set up the simulation environment in a way, that it follows the semantics of the analytic models and a comparison is possible. Together with University Braunschweig, ETHZ worked on the combination of the Symta/S symbolic analysis tool with the MPA framework. In particular, a tool coupling has bee established that allows a seamless integration of both analysis methodologies. In addition, both research groups worked on a proper modelling of hierarchical event stream concepts.

To provide a formal performance analysis that captures the timing implications of MPSoC, the applicability of concepts from the analysis distributed systems is limited. A major difference lies in the use of common resources by the multiple Processing Elements, either physically, such as a shared coprocessor or memory, or logically, such as a semaphore or a shared data structure in the memory. In ARTIST2 already first steps were taken towards addressing implications of a shared memory, which need to be extended in order to achieve the goals of this activity in the ArtistDesign context. Therefore, University of Braunschweig have taken steps towards generalization of the concepts from shared memory modelling to cover arbitrary shared resources. The approach chosen promises a higher accuracy than traditional approaches, due to more sophisticated modelling of the shared resource load, and a better composability of designs, as the analysis of the shared resource delay is decoupled from the response time analysis of the requesting tasks.

The main problem tackled by IMEC and its affiliated partners (i.e., DUTH, NTNU and UCM) was the definition of a specific software metadata format, which can be linked to each embedded software application or downloadable software service. This software metadata information can be used to configure and self-adapt the run time resource management software for dynamic data transfer and storage on MPSoC platforms. Additionally, IMEC has developed profiling and analysis tools that extract and post-process these software metadata, in order to be used for both memory hierarchy assignment (i.e., Memory Hierarchy - MH tool) and source code parallelization tools (i.e., MPSoC Parallelization Assistant - MPA tool, not to be confused with MPA by ETHZ).

DTU have continued and extended their development of a framework for analytical performance evaluation based on timed automata models of MPSoC platforms. Other models for model checking of non-functional properties, such as interval logic (e.g. Duration Calculus), has also been investigated, as well as models which brings the modelling closer to hardware. The work on defining a suitable model-of-computation for describing hardware at the architectural level has been done in collaboration with Virginia Tech in the US.

University of Bologna has addressed, in cooperation with DTU, the issue of prolonging the system's life-time. Even though systems that harvest energy from the environment are adopted

today, such an environmental energy is not distributed uniformly and there is a lot of parameters that influence the efficiency and the schedulability of tasks. In particular we tackled the problem of routing messages in a sensor network with energy awareness and real-time responsiveness together with scheduling policies, which guarantee the execution of tasks under the unpredictable profile of the harvested energy.

KTH has focused on three main topics during year 1: contract based architecture dimensioning; Integration of the communication architecture with the memory architecture; modeling and analysis of adaptive systems.

Contract based architecture dimensioning attempts to formulate the performance aspect of interfaces between IPs, applications and the SoC infrastructure in terms of traffic flows, that specify the traffic characteristics with respect to throughput, burstiness, and delay. Based on traffic contracts, performance analysis and infrastructure dimensioning can be done in a modular way. Also, KTH is developing a MPSoC platform that integrates memory services into the communication infrastructure with the aim of providing an appropriate memory abstraction to embedded software programmers. Furthermore, the MPSoC platform shall support a release consistency memory model and dynamically allocated abstract data types such as linked lists, arrays and container classes. Finally, KTH has developed concepts for modelling adaptivity in an abstract way to make relevant and interesting properties of adaptive systems explicit. The type and level of adaptivity is an important design consideration in many systems and it should be possible for the designer to systematically explore the design space with adaptivity being one more design parameter just like performance, cost and power consumption.

KTH has systematically studied resource allocation for delivering high performance and QoS in a variety of applications and systems. This work has resulted in a survey paper [JL2008] and several case studies and architecture specific techniques. For on-chip communication networks a TDM based technique has been developed for guaranteeing minimum bandwidth and maximum latency services [LJ2008].

Standard communication interfaces facilitate the integration of hardware IP modules. Examples of (de facto) standard interfaces that are in use today are AMBA-AXI or OCP-IP. Although such interfaces enable seamless interfacing of IP modules with interconnects, they provide no explicit support for obtaining the required performance for the functions executing on the IP modules.

2. Summary of Activity Progress

2.1 Technical Achievements

Simulation-based and analytical methods for performance estimation of distributed real-time systems (Linköping, DTU)

University of Linköping and DTU have conducted work regarding analysis and optimization of distributed embedded real-time systems, with application in automotive electronics. The main goal is to develop models and tools for the analysis and optimization of such communication-intensive systems. Emphasis is placed on the analysis of timing properties, considering the heterogeneous nature of such systems and the particularities of the various communication protocols.

In the most recent research the Technical University of Denmark (DTU) and Linköping University (LiU) have proposed an approach to the timing analysis of applications using heterogeneous task scheduling policies (time and event triggered approaches) and mixed static and dynamic communication protocols.

We have finalized and improved our simulation-based and analytical platforms for the validation of distributed embedded systems. One of the main directions was the evaluation of the simulation-based platform with regard to its capacity to be used for validation of time critical systems. Based on experimental results with the simulation-based platforms we were also able to draw interesting conclusions regarding the potential pessimism of formal approaches to the validation of distributed real-time systems. The experiments were performed considering FlexRay and CAN-based distributed systems which are of great interest to the automotive industry.

Modelling and analysis of fault tolerant distributed embedded systems (Linköping, DTU)

As part of the collaboration between Linköping University and DTU and as a continuation of the work in the previous years, an approach to the analysis and scheduling of safety critical, fault tolerant embedded applications with soft and hard real-time constraints has been developed. The goal is to guarantee the deadlines for the hard processes even in the case of faults, while maximizing the overall utility. Time/utility functions are used to capture the utility of soft processes. Process re-execution is employed to recover from multiple faults. A single static schedule computed off-line is not fault tolerant and is pessimistic in terms of utility, while a purely online approach, which computes a new schedule every time a process fails or completes, incurs an unacceptable overhead. Thus, a quasi-static scheduling strategy is used, where a set of schedules is synthesized off-line and, at run time, the scheduler will select the right schedule based on the occurrence of faults and the actual execution times of processes

Integration of MPARM simulation and MPA performance analysis frameworks (ETHZ, University of Bologna)

There have been numerous physical meetings and phone conferences between the research groups at ETHZ and University Bologna in order to establish a close link between the MPSOC simulation framework MPARM and the Modular Performance Analysis (MPA) framework. The simulation environment has been transferred to ETHZ and has been integrated into the Distributed Operation Layer (DOL) analysis and design framework. Applications can be specified and a functional simulation can be performed in DOL. After the mapping optimization, it can be simulated in MPARM. This way, functional simulation, instruction- and cycle-accurate simulations and analytic methods can be compared with respect to their accuracy.

Integration of SymTA/S - MPA and unifying approaches for hierarchical scheduling (ETHZ, University of Braunschweig)

In a recently published paper J. Rox and R. Ernst from University Braunschweig introduced the hierarchical event model that is going to be implemented in the SymTA/S framework. Alternative approaches to deal with merged event streams should be found for the MPA framework used at the ETHZ. In a first step, ETHZ analyzed the formalism by Braunschweig and are now considering various solutions how to embed the hierarchical event model into MPA. The major issue here is to also allow an extraction of single event streams from previously merged – and transformed event streams. The transformation is hereby due to the fact that incoming streams can be combined via OR-operation and may pass different system components, which may buffer these streams due to scheduling policies. In a next step, analysis and comparisons of the different approaches will be done. To this end, a PhD student from ETHZ visited University Braunschweig for a week (6th of Oct until 10th of Oct. 2008). A technical report has been written that will be submitted for publication.

Energy Harvesting in Sensor Nodes (University of Bologna, ETHZ)

In the area of distributed low-power systems, wireless sensor networks are the key technology drivers, given their tightly power constrained nature. One important trend in this area is toward "battery free" operation. This can be achieved through energy storage devices (e.g. super-capacitors) coupled with additional devices capable of harvesting energy from environmental sources (e.g. solar energy, vibrational energy). Battery-free operation requires carefully balancing harvested energy and stored energy against the energy consumed by the system, in a compromise between quality of service and sustainable lifetime. The main developments achieved in this activity can be summarized as follows:

(a) We presented feedback controllers, which adapt task rates so that maximal utility is obtained, while respecting the time-varying amount of harvested energy. Instead of solving the optimization problem online which may be prohibitively complex in terms of execution time and power consumption, we propose the use of multiparametric, optimal online controllers.

(b) We presented a hierarchical control design which overcomes several drawbacks of previously proposed designs: First, the computation overhead and storage demand of the online controller is reduced significantly. In a case study, the achieved reductions compared to a single controller amount 91% and 83%, respectively. Second, by designing the controller for worst-case situations, depletion of the energy storage is avoided and robustness of the overall system is increased.

(c) For some applications of practical concern, the optimal multiparametric solutions may grow to complex for constraint systems like sensor nodes. For those applications, we proposed a novel algorithm for approximate multiparametric linear programming. We demonstrate, that the online complexity of the generated control laws is highly reduced compared to an optimal solution in terms of computation overhead and storage demand. For an example investigated, we found improvements of 98% and 92%, respectively. Furthermore, simulations show that the performance of the found control laws is comparable with the one achieved by complex, optimal control laws.

(d) We proposed a practical technique for the efficient implementation of the controller and demonstrate the practical relevance of our approach by measurements of the controller running on a real sensor node.

(e) Beside this theoretical framework, a novel analogue circuit for solar energy harvesting has been developed and presented. Here, a key design challenge is how to optimize the efficiency of the solar energy collection under non stationary light conditions. The proposed scavenger exploits miniaturized photovoltaic modules to perform automatic maximum power point tracking.

Modelling of Shared Resources in Multiprocessor Systems (TU Braunschweig)
State-of-the-art schedulability tests for multiprocessor systems lack general applicability: Common constraints are a periodic or sporadic task activation pattern, with deadlines no larger than the period. Where these constraints are overcome, shared resources, typical elements in every real-time system, are not covered anymore. But state-of-the-art real-time operating systems have none such constraints, which has previously hindered the general application of the proposed methods. Building on results from a collaboration with Bosch (affiliate member), we addressed these constraints and presented a general analysis which allows calculating the response time for tasks in a partitioned MPSoC with arbitrary task activation and deadlines, while also considering the use and timing implications of shared resources protected with the Multiprocessor Priority Ceiling Protocol (MPCP). We have derived an improved bound on the blocking time in this setup. Results will be published in [NSE08].

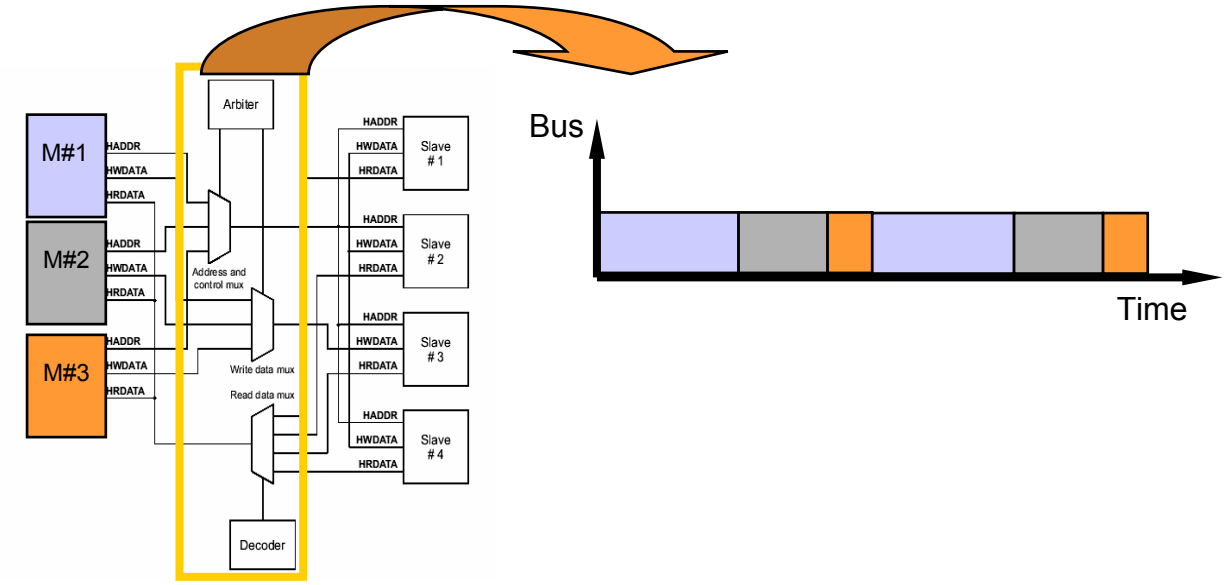
Robustness Optimization of a MPSoC (TU Braunschweig)
We have applied optimization techniques known from distributed multiprocessor systems with the analysis methodologies for MPSoC. Previous approaches (i.e., the evolutionary algorithms from ETHZ and the exploration framework from TU Braunschweig) turned out to be flexible enough to be easily adapted to explore parameters of memory controllers and traffic shapers. With this, an optimal configuration for a media processing application could be found, in which a feasible balance between worst case latency and guaranteed throughput is achieved for the memory subsystem. Background and results of this case study have been presented in [SHR+08].

Vertically Hybrid performance analysis for a MPSoC (TU Braunschweig, ST Microelectronics, Symtavision)
In a collaboration with École Polytechnique de Montréal and STMicroelectronics that has started during the ARTIST2 project, we have investigated a realistic media processing application mapped to a model of industrial hardware. The results of this case study were presented in [SNN+08]. For this, we could adopt a performance investigation methodology known from automotive network analysis, and apply it to the given MPSoC. The experience from the automotive domain was provided by Symtavision GmbH (affiliated partner). The performance analysis is “vertically hybrid”, in the sense that the bottom layers of the timing hierarchy (task timing) are investigated with simulation, and formal methods are only used on the integration level (system timing), where the problems otherwise would become intractable due to state space explosion.

Software Metadata Profiling and Analysis (IMEC, DUTH, UCM, NTNU)

This work focuses on a methodology and tools that extract and process information from embedded software applications that will be mapped on MPSoC platforms. This information is used by source code parallelization optimization tools and for static and dynamic memory management tools. http://www2.imec.be/imec_com/mpsoc_runtime.php

TDMA arbitration policy on AMBA AHB protocol for MPSoC’s system bus (University of Bologna, Linköping)
Deep submicron technologies are making the integration of a large number of IP blocks on the same silicon die technically feasible. The communication architecture is becoming the bottleneck for these MPSoC, and efficient contention resolution schemes for managing simultaneous access requests to the shared communication resources are required to prevent system performance degradation.



UoB and Linköping have analyzed the impact on MPSpC performance of TDMA arbitration policy and the strong correlation of its effectiveness with the communication requirements of the applications. Since the most widely adopted interconnect architecture for the SoC IP blocks is AMBA AHB, a TDMA arbitration policy has been developed on top of AMBA AHB protocol.

Energy Harvesting Aware Routing with Scheduling optimization (DTU, University of Bologna)

One way to prolong the system life time is to harvest energy. Unfortunately environmental energy is not distributed uniformly and there is a lot of parameters that influence the efficiency and the schedulability of tasks. Currently energy-driven scheduling scenario for a system, whose energy storage is recharged by an environmental energy, should be able to execute tasks defined by an arrival time, an energy demand and a deadline in an optimal way. So far, such scheduling policies have been tackled only for nodes locally. On the other hand, energy optimal routing protocols focus on finding the most energy optimal route and use it for all communications. If nodes are equipped with an energy harvesting unit, this may not be the best strategy to achieve a long network lifetime; nodes on this route may not harvest the same amount of energy as nodes on alternative suboptimal paths. Therefore, it remains unclear how the designer can address and merge these two issues as a global view; and how routing messages in a sensor network, with real-time responsiveness of these inherently energy constrained devices can be guaranteed within the deadline.

As technical achievement we start to develop a simulation framework able to address routing policies in the wireless sensor network domain and scheduling algorithms on nodes. The framework is able to apply for all kind of energy harvesting systems, which must schedule processes under deadline constraints.

The main developments obtained in this activity are related to establish a mutual understanding of the model to implement in the simulation framework .

Modelling and Verification of Embedded Systems (DTU, AAU)

DTU has continued the work from ARTIST2 on formalizing the ARTS simulation model and to make it usable for designers early in the design process. In order to support designers of industrial applications, the timed-automata model is hidden for the user, allowing the designer to work directly with the abstract system-level model of embedded systems. The designer

provides an application consisting of a set of task graphs, an execution platform consisting of processing elements interconnected by a network and a mapping of tasks to processing elements. The system model is then translated into a timed-automata model which enables schedulability analysis as well as being able to verify that memory usage and power consumption are within certain limits. In the case where a system is not schedulable, the tool provides useful information about what caused the missed deadline. DTU does not propose any particular methodology for design space exploration, but provides an analysis framework, MoVES, where embedded systems can be modeled and verified in the early stages of the design process. Thus, the MoVES Analysis Framework provides tool support for system designers to explore alternatives in an easy and efficient manner.
An important aspect in the design of MoVES is to provide an experimental framework, supporting easy adaptability of the ”core-model” to capture energy and memory considerations, for example, or to experiment with, say new principles for task scheduling and allocation. Furthermore, the MoVES Analysis Framework is equipped with different underlying UPPAAL models (some of which have been developed together with AAU), aiming at efficient verification in various situations. For the moment DTU is operating with the following underlying models for

- schedulability analysis in connection with worst-cases execution times only,
- schedulability analysis for the full core model (including best- and worst-case executing times),
- schedulability analysis addressing memory and energy issues as well, and
- schedulability analysis for the full core model on the basis of stop-watch automata. This analysis approach is based on over approximations, but it has provided exact results in the experiments carried out so far and it appears to be the most efficient Uppaal implementation.

Formal verification of design properties of hardware architectures (DTU, Virginia Tech)

DTU has worked on a formal language for hardware models based on the Gezel hardware description language developed and maintained by Virginia Tech, USA. The language depends on reasonably few, simple and clean concepts, and it strikes a balance between software and hardware concerns that suits the needs for a modern top-down approach to hardware design. The semantical domain of the language has been related to timed-automata using the UPPAAL system. They have demonstrated a formal verification of design properties of a few simple example circuits including the Simplified Data Encryption Standard (SDES) Algorithm and different algorithmic implementations of the Greatest Common Divisor. Verification guarantees properties of the underlying algorithm, e.g. correct output for any given input, as well as other properties such as upper limits on the number of clock cycles for the algorithm to stabilize with a given input and upper limits on the number of register updates, to serve as an indicator of energy consumption.

Analysis tools for embedded systems (DTU, Oldenburg)

This activity addresses the problem of establishing decidability and model-checking results for fragments of interval logics. The aim is, in particular, to establish efficient tools for the analysis of real-time properties of embedded systems, and, in general, tool support for the analysis of more general resource constraints of embedded systems. The activity is a co-operation with Prof. Martin Fränzle, Oldenburg University.

Contract based architecture dimensioning (KTH)

KTH, together with partners from NXP, ARM and ST, has developed extensions to (the use of) IP communication interfaces that enable the correct integration of IP modules so that performance requirements are met and the required Quality of Service (QoS) is obtained. The extensions to the interfaces enable a SoC integrator to explicitly define the services that need to be provided by a communication infrastructure to an IP module so that it can provide the desired QoS. Specifically we have introduced the notion of QoS contract to specify the services required for correct operation of an IP. We have defined different types of QoS contracts for Device-Level Interfaces (like AMBA-AXI) and we have studied how they can be configured and how monitoring and traffic regulation can be included. We have used the theory for modelling complex memory controllers and analyzing performance of memory transactions. Work in progress develops a contract based system dimensioning and analysis method where contracts are formulated as Network Calculus arrival curves.

Integration of the communication architecture with the memory architecture (KTH, IMEC)

Efficient MPSoC platforms have to efficiently integrate the communication infrastructure with the memory architecture and they have to provide proper memory abstractions to application designers and programmers. The required memory abstractions should offer an intuitive memory consistency model and it has to be efficiently implemented. Moreover, it should offer an intuition of the delay of different memory accesses since that will differ significantly depending on the physical location of the addressed memory.

KTH, together with partners from ICCS in Greece, Thales Communication, IMEC, VTT in Finland, and Inracom in Greece, started developing a MPSoC platform in the context of the MOSART project, which integrates memory services into the communication infrastructure with the aim of providing an appropriate memory abstraction to programmers. Furthermore, the MPSoC platform shall support a release consistency memory model and basic support for dynamically allocated abstract data types such as lists, arrays and container classes.

Modeling and analysis of adaptive systems (KTH)

Adaptivity is a common concept used in embedded system and custom hardware design for many years. Reconfigurable FPGAs, embedded software, configurable datapaths and parameterisable analog components are all familiar examples of adaptivity. We use the term to denote the general, abstract concept of changing the behaviour of a system at run-time which encompasses software, configurable or parameterisable digital and analog hardware.

KTH, together with partners from OFFIS, TU Vienna, University of Cantabria, THALES and DS2, has developed concepts for modelling adaptivity in an abstract way to make relevant and interesting properties of adaptive systems explicit. The type and level of adaptivity is an important design consideration in many systems and it should be possible for the designer to systematically explore the design space with adaptivity being one more design parameter just like performance, cost and power consumption. In order to provide a sound basis that captures adaptivity in a broad and general sense we have introduced adaptivity as an extension to a formal modelling framework. This allows us to formally and systematically study adaptivity and its interesting properties and it establishes a clean and consistent conceptual basis for development of design analysis and exploration methods and tools.

Together with our partners, KTH has developed general concepts for formally modelling adaptive objects and applied them to dynamically reconfigurable systems [SJ2008]. Based on these concepts, a performance analysis method and accompanying tools for reconfigurable systems [ZSJ2008a] has been developed. Moreover, we have developed a method to minimize

power consumption for streaming applications on MPSoC platforms while meeting all real-time constraints [ZSJ2008b]

Design Space Exploration for Real-time Bio-Medical Monitoring (KTH, University of Bologna)
As a minor activity in 2008 we have continued an earlier project in the medical application domain, where an ECG analysis has been studied thoroughly and which has resulted in a design methodology and performance analysis and design space exploration method [KPB+2008].

2.2 Individual Publications Resulting from these Achievements

Linköping University

1. Soheil Samii, Sergiu Rafiliu, Petru Eles, Zebo Peng, “A Simulation Methodology for Worst-Case Response Time Estimation of Distributed Real-Time Systems”, Design Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, pp. 556-561.

ETHZ

2. Clemens Moser, Jian-Jia Chen, Lothar Thiele: Reward Maximization for Embedded Systems with Renewable Energies. IEEE Computer Society, Los Alamitos, CA, USA, August, 2008.
3. Clemens Moser, Jian-Jia Chen, Lothar Thiele: Approximate Control Design for Solar Driven Sensor Nodes. Hybrid Systems: Computation and Control, Lecture Notes in Computer Science, Springer , Berlin / Heidelberg, Vol. 4981, pages 634-637, April, 2008.

TU Braunschweig

4. [SHR+08] Simon Schliecker and Arne Hamann and Razvan Racu and Rolf Ernst. "Formal Methods for System Level Performance Analysis and Optimization." In *Proc. of the Design Verification Conference (DVCon)*, San José, CA, February 2008.
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2.3 Interaction and Building Excellence between Partners

Simulation-based and analytical methods for performance estimation of distributed real-time systems (Linköping, DTU)

The interaction in this activity has been between Linköping and DTU.

- -Meeting/discussion at the conference "Design, Automation and Test in Europe (DATE08)", Munich, Germany, March 10-14, 2008.
- Paul Pop from DTU has visited Linköping several times during 2008.

Modeling and analysis of fault tolerant distributed embedded systems systems (Linköping, DTU)

The interaction in this activity has been between Linköping and DTU.

- -Meeting/discussion at the conference "Design, Automation and Test in Europe (DATE08)", Munich, Germany, March 10-14, 2008.
- Paul Pop from from DTU has visited Linköping several times during 2008.

TDMA arbitration policy on AMBA AHB protocol for MPSoC's system bus

The interaction in this activity has been between Linköping and UNIBO.

- Several phone meetings/discussions between UNIBOB and Linköping during 2008.
- Paolo Burgio from UNIBO has visited Linköping during 2008.
- The MPARM platform from Bologna has been extensively used by Linköping. This has led to frequent interactions between the groups.

Energy Harvesting Aware Routing with Scheduling optimization (DTU, UNIBO)

DTU and University of Bologna have tackled the problem of scheduling messages in a multi-hop energy-harvesting sensor network. The close cooperation has been performed during several research exchanges:

- Meeting/discussion at the conference "Design, Automation and Test in Europe (DATE08)", Munich, Germany, March 11-14, 2008
- Mikkel Koefoed Jakobsen from the DTU visits the research group at University of Bologna from 15th until 21th of June 2008 for scientific collaboration.

Integration of simulation and performance analysis frameworks (ETHZ, University of Bologna, University of Braunsweigh, Uppsala)

Between ETHZ and partners at University Bologna, University Braunschweig and Uppsala University there have been numerous technical meetings as well as PhD student exchanges. The integration happened in the area of methods as well as tools. For example, there was a unification of the application models between University of Bologna and ETHZ in order to enable a comparison of the different analysis methods used. In addition, the hierarchical event models developed at Braunschweig and ETHZ have been compared. Finally, tools have been coupled such as MPARM-DOL and Symta/S-MPA. This way, not only the unification of methods has been verified but also a detailed comparison on the efficiency of the various methods has been possible.

- Meeting on Application Model in Bologna, June 5, 2008; attendees: UNIBO, ETHZ: Discussion about the application model for the common research interest of mapping optimization. Agreement on further corporation to integrate ETHs heuristic polynomial time and UNIBOs complete but exponential time analysis approach.
- Meeting on 20th of May 2008, Zurich: The main goal of this meeting was to set up the basis of the cooperation between ETHZ and University of Bologna, addressing the topic of using the MPARM cycle-accurate simulation as calibration platform for the system-level Distributed Operation Layer (DOL) framework which is based on the MPA model.

Analysis tools for embedded systems (DTU, Oldenburg)

The interaction in this activity has been between DTU and Oldenburg.

- Prof. Martin Franzle is a guest professor at DTU. Martin Franzle has visited DTU several times for one or two weeks. He participated and lectured in the PhD course on

Automated Formal Verification for Embedded Systems organized by DTU at DTU, June 4-12, 2007.

- Michael R. Hansen from DTU has visited Oldenburg.

Modeling and Verification of Embedded Systems (DTU, AAU)

The interaction in this activity has been between DTU and AAU.

- Joint work on modelling the ARTS framework using the timed automata semantics of UPPAAL and extension to handle detailed hardware aspects. Several visits between DTU and AAU have taken place. Results have been published by DTU in 4 papers.

Formal verification of design properties of hardware architectures (DTU, Virginia Tech)

The interaction in this activity has been between DTU and Virginia Tech.

- PhD student Aske W. Brekling from DTU has visited Virgina Tech for 1 month with the aim to expand on the joint research.
- Joint plans on Embedded Systems education based on the Gezel hardware description language from Virginia Tech has been initiated.

TU Braunschweig and Symtavision have discussed the different data acquisition, modelling, and analysis flows in industrial automotive projects, and hardware design projects.

Two PhD candidates, namely Miguel Peon from UCM and Alexandros Bartzas from DUTH, visited IMEC for 2 months in the beginning of 2008 to work on definition of a software metadata format for DMA and Memory assignment optimizations for MPSoC.

KTH has been closely collaborating with Turku University in Finland with regular visits and one joint workshop April 7-10, 2008.

KTH, ISSC and IMEC cooperate closely in developing a memory architecture for MPSoC platforms. IMEC has organized a workshop Nov 3-5, 2008, to introduce thei MPA tools.

KTH has cooperated with Bologna University on developing an ECG analysing system on an MPSoC platform.

KTH is cooperating with NXP Research and ARM in developing a contract based MPSoC infrastructure dimensioning method.

KTH cooperates with OFFIS and TU Vienna in developing methods for modelling, design and analysis of adaptive systems.

2.4 Joint Publications Resulting from these Achievements

1. Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng, “Scheduling of Fault-Tolerant Embedded Systems with Soft and Hard Timing Constraints”, Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, 915-920.
2. Traian Pop, Paul Pop, Petru Eles, Zebo Peng, Alexandru Andrei, “Timing Analysis of the FlexRay Communication Protocol”, Real-Time Systems Journal, Volume 39, Numbers 1-3, August, 2008, pp 205-235.

3. Traian Pop, Paul Pop, Petru Eles, Zebo Peng, Alexandru Andrei, “Analysis and Optimisation of Hierarchically Scheduled Multiprocessor Embedded Systems”, Intl. Journal of Parallel Programming, Volume 36, Number 1, February, 2008, pp. 37-67.
4. Bengt Jonsson, Simon Perathoner, Lothar Thiele, Wang Yi: Cyclic Dependencies in Modular Performance Analysis. ACM & IEEE International Conference on Embedded Software (EMSOFT), ACM Press, Atlanta, Georgia, USA, pages 179-188, October, 2008.
5. Simon Perathoner, Ernesto Wandeler, Lothar Thiele, Arne Hamann, Simon Schliecker, Rafik Henia, Razvan Racu, Rolf Ernst, Michael González Harbour: Influence of Different Abstractions on the Performance Analysis of Distributed Hard Real-Time Systems Design Automation for Embedded Systems, Springer Science+Business Media, LLC, 2008.
6. Davide Brunelli, Clemens Moser, Luca Benini, Lothar Thiele: An Efficient Solar Energy Harvester for Wireless Sensor Nodes. Design, Automation and Test in Europe (DATE 08), Munich, Germany, March, 2008.
7. Clemens Moser, Lothar Thiele, Davide Brunelli, Luca Benini: Robust and Low Complexity Rate Control for Solar Powered Sensors Design, Automation and Test in Europe (DATE 08), Munich, Germany, March, 2008.
8. Tolga Ovatman, Aske Brekling, and Michael R. Hansen. Cost analysis for embedded systems: Experiments with Priced Timed Automata. In proceedings of FESCA 2008.
9. Bartzas, A.; Peon-Quiros, M.; Mamagkakis, S.; Catthoor, F.; Soudris, D. and Mendias, J., ‘Enabling run-time memory data transfer optimizations at the system level with automated extraction of embedded software metadata information’, Asia and South Pacific Design Automation Conference - ASP-DAC, 2008
10. Balasa, F.; Kjeldsberg, P.; Vandecappelle, A.; Palkovic, M.; Hu, Q.; Zhu, H. and Catthoor, ‘Storage estimation and design space exploration methodologies for the memory management of signal processing applications’, F. Journal, Journal of VLSI Signal Processing Systems, 2008
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2.5 Keynotes, Workshops, Tutorials

Invited Talk L. Thiele (ETHZ): MPSOC Conference. Aachen, Germany, June 23-27, 2008: Lothar Thiele described a new approach for mapping algorithms onto MPSoC architectures. It is a result of cooperation between ArtistDesign partners from Aachen, TIMA and LETI. The design methodology is named DOL (Distributed Operation Layer) and targets real-time and efficient multiprocessor systems and applications.

Summer School: Course on Embedded Systems (ETHZ, L. Thiele), Florianopolis, Brasil, August 25-2, 2008. The summer school was dedicated to promote the interaction between the embedded system communities in Europe and South America. Lothar Thiele was presenting a wide range of subjects, starting from basic methods to design embedded software for

embedded systems. In addition, he presented methods for real-time scheduling and performance analysis of distributed embedded systems.

ARTIST Summer School: Invited talk on design space exploration and performance analysis (ETHZ, L. Thiele), Grenoble, France, Sept 8-12, 2008. During the ARTIST Summer School in Grenoble, Lothar Thiele presented interface-based design techniques for stream-based embedded systems. Real-time behavior is obtained by extending the usual component interfaces by resource-aware guarantee-assume predicates. This way, constraints and properties of single components propagate through the whole system and define the relation between the component-based and system-based properties.

ArtistDesign meeting, location: Düsseldorf, Germany; date: 27th and 28th of November 2008: Within the frame of this ArtistDesign meeting which addresses the mapping of applications to MPSoCs, ETHZ presents an overview and a SW demonstration of the Distributed Operation Layer framework.

Castness 2008 Workshop; location: Rome, Italy; date: 15th-18th of January 2008: The objectives of CASTNESS workshops and schools are, first, to provide training about the future of multi-processor/adaptable embedded systems (system SW, HW architectures, applications) and second, the cross-dissemination among European projects. ETHZ presented an overview and a SW demonstration of the Distributed Operation Layer framework, included in a complete MPSoC design flow, as well as detailed information about the design space exploration and mapping optimization steps within this framework.

Tutorial : Formal methods in system and MpSoC performance analysis and optimization (Organizer: R. Ernst; speakers: R. Ernst (TU Braunschweig), S. Charkaborty (NU Singapore), Hans Sarnowsky (BMW), Marco Bekooj (NXP), M Jersak (Symtavision))

DATE 2008
Munich, Germany – March 10, 2008

The tutorial provided an introduction to formal platform performance analysis covering the main communication and resource modelling techniques and their application to embedded systems and MPSoC. It included industrial applications and experiences, use cases from automotive design which demonstrated how to acquire the necessary model data, an overview on predictable MPSoC platform sharing using service shaping concepts, as well as an introduction on how to combine state-based and functional models for MpSoC in a single analysis to improve modelling precision.

Invited talk:
17th International Federation of Automatic Control (IFAC) World Congress
Seoul, Korea – 6-11 July, 2008

Jan Madsen from DTU gave an invited talk on “System-level Verification of Multi-core Embedded Systems using Timed-Automata”. The talk presented the MoVES modelling framework, which allows for cross-layer modelling and verification, covering the application layer, middleware layer (RTOS), and hardware layer. The modelling framework allows the designer to verify the impact of execution platform and application mapping on the schedulability (meeting hard real-time requirements), power consumption and memory utilization, while taking communication into account. The modelling framework is implemented using timed-automata in UPPAAL.

Conference: Industrial Embedded Systems
3rd International Symposium on Industrial Embedded Systems (SIES)
Montpellier, France – 11-13 June, 2008

Anders Tranberg-Hansen from DTU gave a talk on "A Service Based Estimation Method for MPSoC Performance Modelling". The talk presented an abstract service based estimation method for MPSoC performance modeling, which allows fast, cycle accurate design space exploration of complex architectures including multi processor configurations at a very early stage in the design phase. To illustrate the method, a small MPSoC system, developed at Bang & Olufsen ICEpower was modelled and performance estimates were produced for various configurations of the system implementation.

PhD-course: Automated Formal Methods for Embedded Systems
Lyngby, Denmark – 16-24 June, 2008

DTU has organized a second version of the PhD course on "Advanced Topics in Embedded Systems", that took place at IMM, DTU, Lyngby, Denmark, June 16-24, 2008. Lectures were given by ARTIST memebers from Oldenburg. The course was again a success and will be repeated in 2009. The course was mainly funded by Artist2, but was also announced to the ArtistDesign. From 2009 it will be a ArtistDesign sponsored event.

http://www.artist-embedded.org/artist/Automated-Formal-Methods.html

Mini-keynote: Codesign
8th International Forum on Application-Specific Multi-Processor SoC (MPSoC)
St. Gerlach, The Netherlands, June 23-27, 2008.

Jan Madsen from DTU gave a talk on "*Adaptive Embedded Systems Challenges of Run-Time Resource Management".* The mini-keynote addressed some of the challenges of run-time resource management in adaptive embedded systems. The challenges come from the often very complicated interplay between the application, the application mapping, and the underlying hardware architecture. With MPSoC, we have the technology to design and fabricate dynamically reconfigurable hardware platforms. However, such platforms will pose new challenges to tools and methods to efficiently explore these platforms at run-time. http://www.mpsoc-forum.org/

Invited talk Martino Ruggiero (UNIBO): MPARM simulation platform
ArtistDesign meeting,
Pisa, Italy – Oct 2-3, 2008
With this occasion several results obtained in the ARTIST context have been made accessible to an international audience.

Invited Talk: Luca Benini (University of Bologna) - Ambient-Assisted Living for an Aging Society: From Passive Monitoring to Prevention and Therapy
1st International Workshop on Sensor Networks and Ambient Intelligence
Dunedin, New Zealand, December 1-4, 2008 (upcoming)
The presentation will looks into hardware-software architectures and design issues for Ambient-Assisted Living systems. The focus will be on systems that not only perform basic sensor processing, storage and transmission, but also react autonomously to the incoming sensor information with bounded response time. Critical event detection and bio-feedback fall within the classes of applications targeted by these systems. We will look in details at the technical challenges and emerging trends in this area, with particular emphasis on how to guarantee safe and robust operation under tight form-factor, energy and cost constraints.

http://www.aut.ac.nz/schools/engineering/senami_2008/

Invited Talk: Luca Benini (University of Bologna) – Ambient Intelligent Systems: from enablignntechnologies to applications
Padova, Italy, May 13, 2008

Workshop : ArtistDesign Workshop on Design for Adaptivity
Ingo Sander gave a talk on Modeling of Adaptivity in ForSyDe, at the ArtistDesign Workshop on Design for Adaptivity, May 13-14, 2008, Lund, Sweden

Invited talk : Nostrum network on chip
Axel Jantsch (KTH) gave an invited talk at the Turku center of Computer Science, April 2008.

Invited talk : Quality of service in networks on chip
Axel Jantsch and Zhonghai Lu gave an invited talk at the Research Center Telecommunciation Vienna (FTW), April 2008.

Tutorial: A formal framework for heterogeneous models of computation
Axel Jantsch gave a tutorial at Design Automation and Test Conference (DATE), March 2008.

Tutorial: Network layer communication performance in networks on chip
Axel Jantsch gave a tutorial at the Asian Pacitific Design Automation Conference, January 2008.

3. Milestones, and Future Evolution

3.1 Problem to be Tackled over the next 12 months (Jan 2009 – Dec 2009)

The activities started in Y1 will continue in Y2. A summary of the problems to be tackled and of the integration opportunities is summarized as follows.

Modelling and analysis of fault tolerant distributed embedded systems

During the second year we will address the issue of reliability analysis of distributed and MPSoC systems considering various hardening degrees of the underlying hardware platform. This will allow for taking into consideration further particularities of the multiprocessor platform during performance and reliability analysis which increase the spectrum of possible tradeoffs during the design process.

Simulation-based and analytical methods for performance estimation of distributed real-time systems

During the second year we will try to extend our analysis approach and make a step forward towards the actual application area. Instead of only looking after worst case execution and response times we would like to analytically derive quality of service figures that can be expected from an application running on a certain hardware platform. Firstly, we will look at control applications implemented on distributed embedded systems.

ETHZ and Braunschweig wil continue to work on combining the Symta/S and MPA framework. In particular, the domain of hierarchical event stream representations will be investigated further.

Run-time resource management

Over the next 12 months, IMEC with the collaboration of DUTH and UCM will extend the Software Metadata extraction and analysis methodology to enable collection of information at run-time. Therefore, a number of monitors will be developed that will be able to update the software metadata information that was extracted at design-time and feed the run-time resource management mechanisms with more up-to-date data for their optimizations.

TDMA arbitration policy on AMBA AHB protocol for MPSoC's system bus

Results show that the performance of TDMA arbitration policy on AMBA AHB protocol is not good, mostly because supporting TDMA on top of the AMBA protocol makes everything quite inefficient. During next year, Bologna will look into re-defining completely the bus access protocol and make it TDMA friendly.

Energy Harvesting Aware Routing with Scheduling optimization

DTU and University of Bologna will continue to address the problem of scheduling messages in a multi-hop energy-harvesting sensor networks by implementing and assessing a simulation framework which permits to compare routing algorithms and energy aware scheduling policies on sensor nodes.

We plan to test the theoretical energy harvesting framework and demonstrate sustainable operation using scavenged energy with and effective routing management over the network. Finally, we plan to demonstrate the usefulness of our simulation results in a practical application by a deployed sensor network.

ETHZ and Bologna will continue to work on low power sensor network design. In particular, the results so far will be extended towards application-level decisions.

Modelling and Verification of Embedded Systems

DTU will continue the work on analytical performance models based on timed automata. In particular, the formalisation of the ARTS model will be extended to capture more aspects of both the application and the platform. Another important issue to be addressed is the scalability of the model such that larger and more complex systems can be modelled. The work will be done in collaboration with AAU.

Formal verification of design properties of hardware architectures

DTU will extend its collaboration with Virginia Tech to support model based design and analysis of hardware platforms and MPSoC. During next year, DTU will investigate how this platform level modeling can be linked with the system-level models. Further, studies towards using the model for education in Embedded Systems Design will be conducted.

Analysis tools for embedded systems

The goal is to establish efficient methods for verification of resource constraints, where one activity will focus on the real-time logic durations calculus. DTU will develop a prototype model-checking tool and experiment with verifying strong timing constraints.

Contract based architecture dimensioning:

While much of the basic concepts have been built, a concrete methodology has to be formulated and demonstrated. During the next year, a methodology for dimensioning interconnect capacity, memory access bandwidth and buffer sizes in heterogeneous MPSoCs will be formulated based on traffic contracts on individual traffic flows. Experiments and case studies will be conducted to study the efficacy of the method.

Integration of the communication architecture with the memory architecture:

During the second year the memory and data management services for a MPSoC platform will be formulated and partially implemented. The services will include a cache coherence, memory consistency and support for abstract data type management. The platform shall integrate various cores, such as processors, DSPs, customized logic like ASIC, reconfigurable logic like FPGA, and memories via a packet-switched network. A distinguishing feature of the architecture is that the memories are distributed. However, they can be shared, thus the conventional shared variable programming model is supported. In addition, the platform provides transparent support for cache coherency and memory consistency. Furthermore, it provides a set of services for memory access, data movement, power management and architectural configurations. These services, which are built on the basis of the underlying architectural services for global memory access, cache coherency and memory consistency, are to be used by applications. Finally, to enable applications to access the defined services and hide the implementation details, the platform will define Application Programming Interfaces (APIs).

Modeling and analysis of adaptive systems:

During the second year an extensive industrial case study will be conducted to validate the modelling and performance analysis methods. Also, the method and tool will be improved and adapted based on the results from the case study.

3.2 Current and Future Milestones

Modelling and analysis of fault tolerant distributed embedded systems

In year 1, Linköping University and DTU will work on fault tolerant embedded applications with soft and hard real-time constraints. The goal is to guarantee the deadlines for the hard processes even in the case of faults, while maximizing the overall utility. Time/utility functions will be defined to capture the utility of soft processes. Process re-execution will be employed to recover from multiple faults. A quasi-static scheduling strategy will be developed, where a set of schedules is synthesized off-line and, at run time, the scheduler will select the right schedule based on the occurrence of faults and the actual execution times of processes.

The above milestone has been fulfilled.

During the second year we will develop a reliability analysis approach for distributed and MPSoC systems considering various hardening degrees of the underlying hardware platform.

Simulation-based and analytical methods for performance estimation of distributed real-time systems

In year 1, Linköping and DTU will develop an approach to the timing analysis of applications using heterogeneous task scheduling policies (time and event triggered approaches) and mixed static and dynamic communication protocols. A simulation-based and analytical platform for validation of distributed embedded systems will be finalized. The simulation platform will be evaluated with regard to its capacity to be used for validation of time critical systems.

The above milestone has been fulfilled.

During the second year we will extend the analysis approach and make a step forward towards the actual application area. Instead of only looking after worst case execution and response times we will analytically derive quality of service figures that can be expected from an application running on a certain hardware platform. For the first time, we will look at control applications implemented on distributed embedded systems.

Integration Milestone

In year 1, we will investigate possible integrations between various analysis tools developed by the partners.

Various tool and method integrations have been achieved during the first year of ArtistDesign. In particular, MPARM (University Bologna), MPA (ETHZ) and Symta/S (University Braunschweig) have been mutually combined.

This integration of methods and tools will be brought to a next level where the integrated tools result in a prototype that can be demonstrated.

Performance analysis of inter-task synchronization in multiprocessor systems

Driven by an industrially provided multicore system, TU Braunschweig and Symtavision will evaluate the timing implications of a multiprocessor synchronization protocol.

This milestone has been achieved. The investigated synchronization protocol was MPCP (Multiprocessor Priority Ceiling Protocol), which has been chosen because of its applicability to first-generation automotive multicore components, which will be based on partitioned scheduling. Building on previous work that considered the timing implications of shared memories [e.g. SNN+08], an analysis was developed to address resource locking with MPCP (to be published in [NSE08]). A key improvement over previous analysis is the permission of arbitrary task sets, where previously it was constrained to periodic task activations, as well as an increase in analysis precision.

In the next year, the concept of shared resources in multiprocessor systems shall be systematically formalized to capture resource sharing in MPSoC. For this, the previous results that apply to shared memory and MPCP shall be generalized into a framework that allows capturing the timing implication of shared resources, while keeping the composability of the analysis of each component.

TDMA arbitration policy for MPSoC's system bus

In the first year, a TDMA arbitration policy on top of AMBA AHB protocol will be implemented and integrated it into a cycle-accurate simulation platform.

The above milestone has been fulfilled.

During the second year, a new bus interconnection model will be specified and a more TDMA-friendly bus access protocol will be defined.

Energy Harvesting Aware Routing with Scheduling optimization

In year 1 DTU and UNIBO will start cooperating on energy harvesting, with the aim of integrating the energy aware node scheduling from UNIBO with the energy harvesting aware network routing from DTU.

The above milestone has been fulfilled.

The cooperation will be continued. Main goal for the coming period is to consolidate the results regarding the scheduling optimization over a multi-hop sensor network where nodes are equipped with energy harvesting unit. The main directions are to improve and refine the energy prediction model in an environment, adding factors which may hamper the harvested power (i.e. natural shadow for a photovoltaic harvester sensor node). And to improve the model of communication in the sensor network, adding timing and power requirements for the communication stack;

Modelling and Verification of Embedded Systems

In year 1, DTU will continue to formalize the ARTS system-level simulation model using timed automata based on UPPAAL. This work was started in ARTIST2. The aim is to make it usable for designers early in the design process. In order to support designers of industrial applications, the timed-automata model will be hidden for the user, allowing the designer to work directly with the abstract system-level model of embedded systems. The work will be carried out in cooperation with AAU.

The above milestone has been fulfilled, resulting in a prototype framework called MoVES, which allows to experiment with different models-of-computation.

During the second year, this work will be continued with the aim to capture more aspects of both the application and the platform. A goal is to make a stronger link between the system-level model and a more detailed hardware platform model.

DTU will refine its formal model to address modelling and verification issues closer to the hardware layer of the execution platform.

Formal verification of design properties of hardware architectures

In year 1, DTU will work on a formal language for hardware models based on the Gezel hardware description language developed and maintained by Virginia Tech, USA. The aim is to define a clear semantics of the language which allows to formulate the model-of-computation using timed automata, and hence, being able to formally reason about the hardware architecture.

The above milestone has been fulfilled.

In year 2, this work will be continued with the aim to reason about non-functional properties such as power consumption and memory usage. A number of larger design cases will be carried out.

Analysis tools for embedded systems

In year 1, DTU will establish efficient methods for verification of resource constraints. One activity will focus on the real-time logic durations calculus.

The above milestone has been fulfilled. A model-checking result was established which has the potential of verifying strong timing constraints as well as other kinds of resource constraints. The work has been done in collaboration with University of Oldenburg.

Based on the encouraging results from a first prototype implementation, the plan for next year it to extend the theory and to advance the development of the tool.

3.3 Main Funding

Linköping University:

- Swedish Foundation for Strategic Research (SSF)
- Swedish research Council

ETHZ:

- ICT-Project COMBEST (FP7)
- ICT-Project SHAPES
- ICT-Project PREDATOR
- National funding on Sensor Networks (MICS), and corresponding industry-funded projects.

DTU

- DaNES (Danish Network for Embedded Systems, funded by the Danish Advanced Technology Foundation), Denmark. Period 2007-2010. http://danes.aau.dk/
- MoDES (project on Model Driven Development of Intelligent Embedded Systems funded by the Danish Strategic Research Council), Denmark. Period 2006-2009. http://modes.cs.aau.dk/index.html
- ProCell (project on programmable cell chip: culturing and manipulation of living cells with real-time reaction monitoring funded by the Danish Strategic Research Council). http://www.nanotech.dtu.dk/research/theory/tmf/research_topics/procell.aspx

IMEC vzw.:

- **MOSART IST-215244 Project:**
  Mapping Optimization for Scalable multi-core ARchiTecture. ArtistDesign partners involved: Interuniversitair Micro-Elektronica Centrum (IMEC) vzw., Democritus Uni. Thrace (DUTH) and Kungliga Tekniska Hagskolan (KTH) http://www.mosart-project.org/
- **MNEMEE IST-216224 Project:**
  Memory maNagEMEnt technology for adaptive and efficient design of Embedded systems. ArtistDesign partners involved: Interuniversitair Micro-Elektronica Centrum (IMEC) vzw., Democritus Uni. Thrace (DUTH) and Technische Universiteit Eindhoven (TU/e)
  http://www.mnemee.org/
- **IMEC Apollo research program:**
  Disruptive technologies needed to realize nomadic embedded systems for 2012 and beyond. These are technology aware architectures, multiprocessor system-on-chip technology, and reliable design methodologies for sub-45nm unreliable components. For the Apollo research, IMEC cooperates with industrial partners, such as integrated device manufacturers, fabless and fablite IC solution providers, and system integrators. http://www2.imec.be/imec_sites/objects/80acd42f851591023f893a7d96fd96bf/annualreport.pdf (page 36)

UNIBO

- ICT-Project PREDATOR
- Industrial funding on Sensor Networks from Telecom Italia spa

KTH:

- **ANDRES (**Analysis and Design of run-time Reconfigurable, heterogeneous Systems) Project) – EU FP6 **(**http://andres.offis.de/)
- **SPRINT (**Open SoC Design Platform for Reuse and Integration of IPs): EU FP6 (http://www.ecsi-association.org/sprint*)*
- **MOSART (**Mapping Optimization for Scalable multi-core ARchiTecture) – EU FP7 (http://www.mosart-project.org/)

4. Internal Reviewers for this Deliverable

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