IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Progress Report for Year 1

Transversal Activity:
Design for Predictability and Performance

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Policy Objective (abstract)

Embedded systems are required to satisfy requirements on predictability of timing, memory, processing power, power consumption, etc. They also have increasing demands on (average) performance. The objective of this activity is to develop technology and design techniques for achieving predictability of systems built on modern platforms, and to investigate the trade-offs between performance and predictability. This work will need to be carried out in a synergistic manner, involving all levels of abstraction in embedded systems design, spanning from high-level requirements to detailed implementation details on specific platforms.

Versions

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Table of Contents

1. Overview

1.1 High-Level Objectives

Embedded systems in many application domains are required to satisfy strict requirements on timing, while respecting limited supply of resources in terms of memory, processing power, power consumption, etc. All systems also have increasing demands on (average) performance, which has motivated the introduction of efficiencyincreasing features which drastically increase variability and decrease predictability and analyzability. Since the introduction of new architectural features is inevitable, it is important to

- develop technology and design techniques for achieving predictability of systems built on modern platforms, and
- investigate the trade-offs between performance and predictability.

This work will need to be carried out in a synergistic manner, involving all levels of abstraction in embedded systems design, spanning from high-level requirements to detailed implementation details on specific platforms, and is therefore the subject of a transversal activity involving all clusters of the NoE.

1.2 Industrial Sectors

Predictability is an important system requirement in all sectors of embedded systems, whose operation should not fail for different reasons. An obvious sector is that of safety-critical systems, which arise in transportation, power automation, medical systems, and related areas. The market for safety-critical embedded systems is large and steadily increasing. According to a study by the international ARC Advisory Group with headquarters based in Dedham, Massachusetts, the safety systems and critical control system market, which was around $650 million in 2003, will grow at an average annual rate of over 7 percent per year to over $900 million in 2008. ARC's Safety and Critical Control System Worldwide Outlook Market Analysis and Forecast Through 2008 predicts a healthy growth of the safety system market for process industries over the next five years.

The industry developing safety-critical embedded systems is severely suffering from design practices leading to unpredictable system behaviour. The determination of guarantees for non-functional requirements is postponed to a late design stage, and then often fails because of design decisions taken earlier. Establishing a methodology reconciling predictability and efficiency will have a very strong impact on systems-design and implementation practice in industry.

Predictability is important also in other sectors, where systems failure may lead to economic consequences, as in consumer electronics, telecom, etc.

1.3 Main Research Trends

Predictability can be regarded as an effect of choosing suitable hardware and software architectures (in a wide sense) that lead to systems whose worst-case behaviour is easy to predict, and of utilizing analysis techniques that are able to provide these guarantees for the chosen system architecture. Important architectural considerations occur on many levels in a system hierarchy. As a general rule, static allocation of resources leads to predictable systems, whereas dynamic allocation makes predictability difficult. Challenges addressed by this activity appear at all levels of abstraction in the design process

- **Modeling and Validation of systems and of components**: Principles and structures for system and component modeling that are conducive to achieving predictability, by allowing *a priori* predictability analysis and by allowing mappings to platform architectures that preserve predictability. Investigations of how modeling and analysis techniques extend to non-traditional system structures, including distributed and networked architectures, for which predictability is more difficult to achieve. Exploring trade-offs between predictability, resource consumption and performance.
- **Timing Analysis**: Foundations for timing predictability and system-design concepts that increase predictability. Timing analysis, i.e., predicting the worst-case execution time (WCET) of a piece of code, is a hard problem, but significant breakthroughs have been obtained in recent years for many types of processors. Commercial tools, all from Europe, are available. The issues stretch from the processor architecture across all layers to the application and is caused by the variability of execution times. This activity should increase the predictability of system behaviour. Timing analysis for compilation, especially in the light of multiple processors and other architectural features. An important goal is to marry timing analysis with compilation, in order to make timing properties immediately visible to the embedded systems developer.
- **OS/MW/Networks**: On the operating system level, scheduling and reservation of resources is a widely researched topic, with a vast literature. Operating system mechanisms, such as scheduling, mutual exclusion, interrupt handling and communication, can heavily affect task execution behaviour and hence the timing predictability of a system. For example, preemptive scheduling reduces program locality in the cache, increasing the worst-case execution time of tasks compared with non-preemptive execution. The object-oriented programming style, although attractive as a software development methodology, introduces dynamics into the execution time by the dynamic binding of methods to calls. Techniques that improve predictability include schemes that a priori reserve resources in a wide sense. This can be in the form of reserving time slots for execution of tasks, reserving time slots for communication between tasks (e.g., in the time-triggered architecture and in the synchronous programming paradigm). In future research, it is important to explore the tradeoff between performance and predictability in scheduling. Also important is to investigate of software architectures for time-predictable real-time operating systems, with the goal to avoid that the execution of OS code adversely affects the time-predictability of application tasks and vice versa, thus making the computation-time needs of both operating system activities and application tasks easily predictable.
- **System and Processor Architecture:** Simple processor architectures lead to more predictable systems than complicated ones. Current architectures include many features that decrease predictability, such as implicit concurrency, e.g., pipelining, super-scalarity, out-of-order execution, and dynamically scheduled multi-threading. The restricted processor-memory channel-bandwidth and the growing speed gap between processor and memory has led to the introduction of deep memory hierarchies and several types of speculation. Dynamic power management technology, which is critical for reducing the power consumption of hardware, also has a significant impact on predictability. Research on predictability has considered, e.g., to replace dynamic memory management by static and predictable ones, such as scratchpads, to characterize and develop more predictable replacement policies in dynamic caches,

  The current introduction of multicore processors provides new challenges to predictability, since they introduce new concurrency and communication needs to system development. It is not yet clear how to build predictable and performant systems on multicore platforms.

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2. State of the Integration in Europe

2.1 Brief State of the Art

The problem of WCET determination has been solved for single tasks and several types of processors and some replacement strategies, including least-recently-used (LRU). Higher degrees of predictability in the cache system can be achieved by taking decisions statically instead of dynamically. Compiler-directed memory management using scratchpad memory, originally developed to decrease energy consumption, also increases time predictability. Reactive processors are also promising because they allow the direct predictable execution of synchronous languages (Esterel), thanks to the direct support of the multi-threading and of the synchronization between threads. Analysis of scheduling policies has been well-researched for single processor systems, but is still not a resolve task for multicore platforms. From the hardware point of view, system interconnects present a significant challenge to predictability, in that they are shared among multiple communication actors (cores, IOs, accelerators, etc.). Time-triggered communication protocols have been proposed, among others, to enhance interconnect robustness and predictability. Techniques for general analysis of timing and researches in predictable, often distributed, embedded systems model messages and communication resources in a similar way as tasks and computation resources. They start from a restricted event model, e.g. periodic, sporadic or periodic with jitter, and have been able to provide analysis results where the interference between event triggered and time triggered computation and/or communication paradigms can be bounded. A unifying approach to performance analysis has beeen proposed based on real-time calculus.

2.2 Main Aims for Integration and Building Excellence through ArtistDesign

Predictability is a concern which cuts vertically across levels of abstraction in embedded systems design, spanning from high-level requirements to detailed implementation details on specific platforms. It therefore needs to be carried out in a synergistic manner, and is therefore the subject of a transversal activity involving all clusters of the NoE. Previous activities in ARTIST2 have primarily focussed on integration for different layers of abstraction: hardware platforms, compiler technology, timing analysis, modelling, etc. The main purpose of this activity is to integrate research teams working on differen levels of abstraction in embedded systems design.

2.3 Other Research Teams

Much of the cutting-edge research is performed in Europe, to a large extent by Artist Design Partners.

The group at Univ. of Saarland with its spin-off company AbsInt is world-wide leading in the area of timing analysis of hard real-time systems. The development of aiT, the timing-analysis tool of AbsInt, is based on many years of research on static analysis. Static analysis of an embedded program is used to derive invariants about execution states for all inputs to the program. These invariants allow the derivation of reliable upper and lower bounds on the execution times of programs on a given hardware architecture. The ETHZ group has been developing analytic methods based on max+ algebra to analyze combined computation and communication systems, alloiwing a modular approach to analysis of performance and predictability of distributed hardware-software systems. TU Dortmund is a leader on the combination of compiler and architectural techniques for predictable embedded systems. The Uppsala team has developed UPPAAL, a leading model checker for analyzing timed systems.

The Univ. of Bologna has produced several significant contributions in the area of low power design, power management and energy-predictable system design. The group has also pioneered the concept of network-on-chip, a new paradigm for building scalable and efficient on-chip communication fabrics for next-generation multi-core platforms. The Vienna team has developed leading architectures and protocols for predictable networked systems. York is one of the leading groups concerning techniques for designing real-time predictable systems.

The two teams worldwide that are leader in the design of reactive processors are the University of Kiel (Germany) and the University of Auckland (New Zealand).

2.4 Interaction and Building Excellence between Partners

During the operation of the Artist2 Network of Excellence links have been developed between groups working on compiler techniques for achieving predictability of code. Examples include the cooperation between ETH Zurich (Lothar Thiele) and Saarland University (Reinhard Wilhelm), working on timing analysis, and the TU Dortmund (Peter Marwedel), working on compiler techniques. An interesting outcome of future work would be the integration of analysis techniques with compiler techniques, resulting in “predictability-aware compilers”. Links have also been established with groups working on general techniques for guaranteeing predictability in component-based design. For instance, EPFL (Tom Henzinger) and ETHZ (Lothar Thiele) are part of a large national project in the area of mobile information and communication systems. EPFL, University of Salzburg and PARADES are collaborating on compositional languages and approach to embedded system that can be considered the extension of the Giotto approach and are reminiscent of the Metropolis and Ptolemy work carried out at Berkeley. Finally, work in the Operating Systems and Networks areas have established many links both to other activities, e.g., by the development of technology for contract-based scheduling, which provides a nice interface to systems modelling activities.

2.5 Interaction of the Transversal Activity with Other Communities

The predictability activity interacts with several ongoing European projects. These include Predator, which aims at developing a research and design discipline that looks at predictability and efficiency in a synergistic maner, involving all levels of abstraction and implementation in embedded system design. Several ArtistDesign Partners are active in Predator.

Bologna and Dortmund participate in the HIPEAC NoE: this will help establishing links between ArtistDesign and the computer architecture and compiler community, through presentation in HIPEAC-organized events.

Dortmund is member of the European STREP project MORE dealing with resource-constrained embedded systems. This link will be valuable since resource management is a central aspect of both ArtistDesign and MORE.

The German nationally funded project, Automatic Verification and Analysis of Complex Systems (AVACS), is among others concerned with validating timing-analysis methods and tools as well as timing properties of embedded systems, and are well connected with ArtistDesign.

The COSTA (Compiler-Support for Timing Analysis) project at TU Vienna, funded by the Austrian Science Fund, focuses on techniques for compilers to support WCET analysis. One of the main goals within the project is to make code more predictable, where the elimination of timing anomalies by appropriate code generation strategies is a central aim within the project.

3. Summary of Activity Progress

3.1 Technical Achievements

The technical work involves all levels of abstraction in embedded systems design, spanning from high-level requirements to detailed implementation details on specific platforms. Let us consider them in some order

Modeling and Validation of systems and of components

The challenge of building predictable systems, and the challenge to build robust systems have been considered from a conceptual viewpoint in work by EPFL [Hen08]. This work considers two major challenges in embedded systems design:

- the challenge to build, on top of nondeterministic system implementations, system abstractions that are deterministic with regard to non-functional properties such as time and resource consumption; and
- the challenge to build, on top of noncontinuous system implementations, system abstractions that are continuous with regard to physical quantities.

Both challenges require a rethinking of the conventional, purely discrete, purely functional (i.e., nonphysical) foundation of computing. Embedded systems design, therefore, offers a prime opportunity to reinvigorate Computer Science. A main technical contribution of the work is to suggest how predictability can be formalized as a form of determinism, and robustness as a form of continuity.

Predictability analysis of complex distributed systems (ETHZ, Uppsala)
The Modular Performance Analysis based on Real-Time Calculus (MPA-RTC), developed by Thiele et al. At ETHZ, is an abstraction for the analysis of component-based real-time systems. The formalism uses an abstract stream model to characterize both workload and availability of computation and communication resources. Components can then be viewed as stream transformers. The Real-Time Calculus has been used successfully on systems where dependencies between components, via either workload or resource streams, are acyclic. For systems with cyclic dependencies the foundations and performance of the formalism are less well understood. In the joint work between ETHZ and Uppsala (Bengt Jonsson, Wang Yi), we developed a general operational semantics underlying the Real-Time Calculus, and use this to show that the behavior of systems with cyclic dependencies can be analyzed by fixpoint iterations. We characterized conditions under which such iterations give safe results. The results are a fundamental step towards a more general predictability analysis of distributed real-time systems.

Integration of contract-based scheduling framework with a Component-based technology (Cantabria, Thales)
Work has been performed in cooperation between Cantabria and Thales Communications France (TCF) to Integrate the contract-based scheduling framework developed in the FRESCOR EU project with a component-based framework, in order to provide the required level of time predictability in the use of resources to install independently developed real-time components. The component based technology is the microCCM framework, that implements the component-container model with an infrastructure that is idependent of CORBA. The integration with the contracts is provided by adding two kind of services: one managing task creation (called ThreadActivationService), and another one managing scheduling attributes (called SchedulingAttributeService). The contracts are declared in the deployment and configuration plan, and therefore the corresponding tool has been modeified to read this

information and automatically generate the code to create the contracts and manage the interceptors that bind threads to the corresponding contracts.

Timing analysis and Compiler Techniques

Timing Analysis and Timing Predictability (USaar and AbsInt)
The notion of predictability of cache architectures has been clarified. A definition of predictability of caches has been given, and the relative competitiveness of four different cache replacement strategies (LRU, PLRU, FIFO, MRU) has been analysed. In particular, by relating the hit and miss rates for different cache analyses, it was shown that sound analyses for FIFOand MRU can be built from analyses for FIFO. This was the first such work to formally define cache predictability and to rigorously compare different replacement policies. Similarly, sensitivity of cache replacement policies to the initial state have been investigated.

Within rhe PREDATOR, work has identified the PROMPT (PRedictability Of Multi-processor Timing) design rules for predictable multi-processor design. The first principles are to avoid interference on shared resources in the architecture and to allow the application designer the mapping of applications to target architecture without the introduction of new interferences that were not present in the application.

WCET Analysis for Cooperative Task Scheduling (USaar)
USaar hasj investigated timing-analysis aspects of cooperative scheduling/deferred preemption. Deferring preemption enables a tradeoff between the flexibility of a preemptive schedule and the predictability of a non-preemptive one. A method guiding developers of an embedded system to select optimal preemption points (with respect to minimizing the maximal blocking time and/or preemption costs) is under development. To bound the context switch costs, we can use known approaches, but also incorporate the extra knowledge given by the set of preemption points. A technique to derive the maximum blocking time is already available.

Parametric Timing Analysis (USaar, AbsInt and Mälardalen)
Timing analyses require that information such as bounds on the maximum numbers of loop iterations are known statically, i.e., during design time. Parametric timing analysis softens these requirements: it yields symbolic formulas instead of single numeric values representing the upper bound on the task's execution time. So, some input parameters to the program can remain unknown until the final use of the task. The developed analysis determines the parameters of the program, constructs parametric loop bounds, takes processor behaviour into account and attains a formula automatically.

Integration of timing analysis and compilation (TU Dortmund, AbsInt)
The integration of the aiT timing analysis tool from AbsInt and the experimental worst-case excution time (WCET) aware compiler has been continued. The resulting wcc compiler can be considered the leading WCET aware compiler. The integrated tool set allowed studying the impact of optimizations for WCET minimization. This achievement concerns item 2 of sections 1.5 to 1.7.

OS/MW/Networks

Integrating Scheduling Analysis and Model Checking (Uppsala, York)
In real-time systems two common approach to validate timing properties are scheduling analysis and model checking (typically using a timed automata). Scheduling analysis involves the construction of a tractable model for predicting the worst-case behaviour of a system. Model checking explores the state space of possible behaviour. The advantage of scheduling is that the tractable analysis is scalable, but for many situations the resulting tests are sufficient but not necessary. Proof that the analysis model is valid is usually undertaken as a paper exercise. Model checking has the potential to be exact, but typically does not scale. This work involves the use of model checking in the verification of the scheduling model itself, so that scalable predictability based on proven analysis is possible.

Influence of different abstractions on the schedulability analysis of distributed hard real-time systems (ETHZ, TU Braunschweig, Cantabria)
The Computer Engineering and Networks Laboratory at ETH Zurich, Switzerland , the Institute of Computer and Communication Network Engineering at TU Braunschweig, Germany, and the University of Cantabria have collaborated in a study of different real-time analysis methods for distributed systems evaluating their influence on the results of the analysis [PWT+08].

Time-Predictable Operating System (TU Vienna)
In the core of this activity is the investigation of software architectures for time-predictable real-time operating systems, with the goal to avoid that the execution of the operating system code adversely affects the time-predictability of applications. To get a better understanding of the problems involved and to assess the feasibility of a completely time-predictable OS, a very simple and rudimentary OS prototype was realized. In this OS all decisions about the control flow are resolved before runtime and communication (I/O) is planned offline. In an experiment, an application implemented in single-path code was run on this operating systems. This experiment showed that a cycle-accurate prediction of the operating system and application timing can indeed be achieved. This work has been published at the SEUS2008 workshop.

Architecture and System Design

Predictable, Fault-tolerant Embedded Systems Design (Linköping, DTU)
Linköping University and DTU have an ongoing collaboration concerning the design of embedded systems which have to behave in a predictable way even in the presence of transient faults. During the last year the emphasis of the work has been on generating predictable (fault-tolerant) and efficient schedules for embedded applications with soft and hard real-time constraints. The goal is to guarantee the deadlines for the hard processes even in the presence of faults, while maximizing the overall utility. Time/utility functions are used to capture the utility of soft processes. Process re-execution is employed to recover from multiple faults. A single static schedule computed off-line is not fault tolerant and is pessimistic in terms of utility, while a purely online approach, which computes a new schedule every time a process fails or completes, incurs an unacceptable overhead. Thus, a quasi-static scheduling strategy is used, where a set of schedules is synthesized off-line and, at run time, the scheduler will select the right schedule based on the occurrence of faults and the actual execution times of processes.

Prof. Paul Pop from DTU has visited Linköping with several occasions during this period.

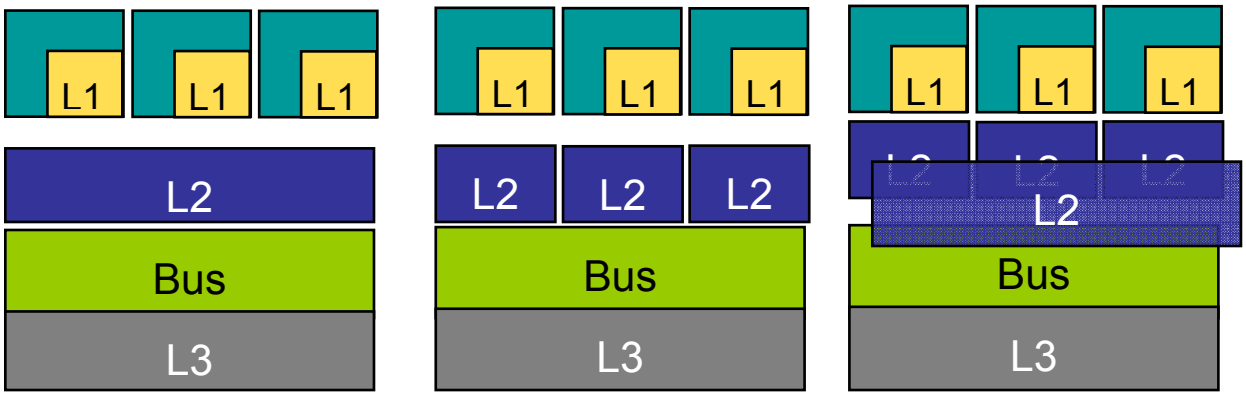
Predictability for Multiprocessor SoC Architectures (Linköping, Bologna, Braunschweig)
One of the major issues in the context of predictability for multiprocessor systems is the shared communication infrastructure. The traffic on the bus does not solely originate from data transfers due to data dependencies between tasks, but is also affected by memory transfers as result of cache misses. A bus access policy and bus access schedule has to be developed which (1) guarantees predictability and (2) provides efficiency in terms of system performance. We have developed an overall strategy and framework for predictable multiprocessor applications. We have addressed the issues of bus access optimization and bus controller design. Bus access optimization is crucial in achieving predictability while, at the same time, maintaining efficiency in terms of performance. In order to demonstrate the practicality of the approach, we have designed and synthesised adequate bus controllers fro the proposed protocols.

A master student from Bologna, Paolo Burgio, has spent the period June 2007 – April 2008 at Linköping working, in particular, on controller design. The Symta/P tool for WCET analysis, from Braunschweig, has been used in this project.

Trade-offs analysis of L2 on-chip cache architectures for embedded MPSoCs (UoB)

On-chip memory organization is one of the most important aspects that can influence the overall system behaviour in MPSoCs. While there is general consensus on L1 private cache organization, for L2 there is still not a dominant paradigm unlike for the high-performance general-purpose processors.

UoB developed a set of parameterizable models for L2 caches and integrated them in an accurate virtual platform environment specifically designed for Embedded MPSoC design space explorations. A detailed analysis of how micro-architectural differences in L2 cache architectures can impact at macro-level the overall system behaviour, as well as power consumption and area occupancy has been conducted. We modeled several L2 cache templates, namely private, shared, or hybrid configuration, and tested their behaviours with various applications.



Our experimental results show that the selection of the optimal cache architectural template is not trivial. The private L2 cache schema performs better than the shared one. However, the hybrid L2 cache achieves better execution time and energy consumption in presence of private and shared data, but at the cost of a larger area. From the predictability perspective, the separate L2 cache performs better than the shared caches. This behaviour is due by the presence of shared resources which introduce variable access time to cache facilities.

A PRET architecture and programming language (INRIA)
In collaboration with de University of Auckland, INRIA is designing a PRET architecture based on a reactive processor coupled with a MicroBlaze general purpose processor. This architecture will be multi-threaded, will offer native support for the reactive constructs of Esterel-like programming languages, and above all will be predictable w.r.t. timing. We are also extending the C programming language with reactive constructs and with specific constructs to specify timing requirements; we call it PRET-C. Finally, we are working on a compiler from PRET-C to our new architecture that will also compute the exact-case execution time of the program.

3.2 Individual Publications Resulting from these Achievements

Cantabria

[Ma1-08] Patricia López Martínez, Julio Medina, & José María Drake. "Real-Time extensions to "Deployment and Configuration of Component-based Distributed Applications". OMG Workshop on Distributed Object Computing for Real-Time Embedded Systems, Washington, DC, USA, July, 2008.

[Ma2-08] Patricia López Martínez, Julio L. Medina, Pablo Pacheco and José M. Drake. "Ada-CCM: Component-based Technology for Distributed Real-Time Systems" 11th International Symposium on Component Based Software Engineering (CBSE-2008) Karlsruhe, Germany October 2008.

[Gi-08] J.L. Gilbert, O. Hachet, J. Chauvin, P. López, J.M. Drake, M. González Harbour, "Integration of Flexible Real-Time Scheduling Services in a Lightweight CCM-Based Framework". OMG Workshop on Distributed Object Computing for Real- Time Embedded Systems, Washington, DC, USA, July, 2008.

EPFL

[Hen08] T. A. Henzinger. Two challenges in embedded systems design: Predictability and robustness. Philosophical Transactions of the Royal Society A 366:3727-3736, 2008.

Linköping

[AEP08] A. Andrei, P. Eles, Z. Peng, J. Rosén, Predictable Implementation of Real-Time Applications on Multiprocessor Systems on Chip, Proceedings of 21st Intl. Conference on VLSI Design, IEEE 2008, pp. 103-110.

TU Vienna

[KPD08] Guenter Khyo, Peter Puschner, and Martin Delvai. An Operating System for a Time-Predictable Computing Node . In Software Technologies for Embedded and Ubiquitous Systems, 6th IFIP WG 10.2 International Workshop, Springer, LNCS, p. 150-161, 2008.

USAAR

[HRW08] J. Herter, J. Reineke, and R. Wilhelm. *CAMA: Cache-Aware Memory Allocation for WCET Analysis*. In Marco Caccamo, editor, Proceedings Work-In-Progress Session of the 20th Euromicro Conference on Real-Time Systems, pages 24–27, July 2008.

[GR08] D. Grund and J. Reineke. *Estimating the Performance of Cache Replacement Policies*. In MEMOCODE '08: Proceedings of the 6th IEEE/ACM International Conference on Formal Methods and Models for Codesign, pages 101–111, June 2008.

[RG08a] J. Reineke and D. Grund. *Relative Competitiveness of Cache Replacement Policies.* In SIGMETRICS '08: Proceedings of the 2008 ACM SIGMETRICS international conference on Measurement and modeling of computer systems, pages 431–432, June 2008.

[RG08b] J. Reineke and D. Grund. *Relative Competitive Analysis of Cache Replacement Policies.* In LCTES '08: Proceedings of the 2008 ACM SIGPLAN-SIGBED conference on Languages, compilers, and tools for embedded systems, pages 51–60, June 2008.

[WW08] R. Wilhelm and B. Wachter. *Abstract Interpretation with Applications to Timing Validation*. In Aarti Gupta and Sharad Malik, editors, CAV, volume 5123 of Lecture Notes in Computer Science, pages 22–36. Springer Verlag, 2008. Princeton, NJ, USA.

[R08]. J. Reineke: *Caches in WCET Analysis: Predictability, Competitivenes, Sensitivity.* Dissertation, Saarland University, November 2008.

3.3 Joint Publications Resulting from these Achievements

[AHLW08] S. Altmeyer, Chr. Hümbert, B. Lisper, and R. Wilhelm: Parametric timing analysis for complex architectures. Proc. 14th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 08), Kaohsiung, Taiwan, Aug. 2008

[AG08] S. Altmeyer and G. Gebhard. WCET Analysis for Preemptive Systems. In Raimund Kirner, editor, *Proceedings of the 8th International Workshop on Worst-Case Execution Time (WCET) Analysis*, pages 105–112, Prague, Czech Republic, July 2008. OCG.

[EIP08] P. Eles, V. Izosimov, P. Pop, Z: Peng, Synthesis of Fault-Tolerant Embedded Systems, Proceedings of DATE: Design, Automation, and Test in Europe, IEEE 2008, pp. 1117-1122.

[IPE08] V. Izosimov, P. Pop, P. Eles, Z. Peng, Scheduling of Fault-Tolerant Embedded Systems with Soft and Hard Timing Constraints, Proceedings of DATE: Design, Automation, and Test in Europe, IEEE 2008, pp. 915-920.

[JPTY08] B. Jonsson, S. Perathoner, L. Thiele, W. Yi: Cyclic Dependencies in Modular Performance Analysis. ACM & IEEE International Conference on Embedded Software (EMSOFT), ACM Press, Atlanta, Georgia, USA, October, 2008.

[KHW+08] D. Kästner, R. Wilhelm, R. Heckmann, M. Schlickling, M. Pister, M. Jersak, K. Richter, Chr. Ferdinand: Timing Validation of Automotive Software. 3rd International Symposium on Leveraging Applications of Formal Methods, Verification and Validation (ISOLA), Kassandra, Greece, 2008.

[LFMT08] P. Lokuciejewski, H. Falk, P. Marwedel, H. Theiling: *WCET-Driven, Code-Size Critical Procedure Cloning*, Proceedings of the 11th International Workshop on Software & Compilers for Embedded Systems (SCOPES), Munich, Germany, March, 2008.

[PWT+08] S. Perathoner, E. Wandeler, L.Thiele, A.Hamann, S.Schliecker, R.Henia, R.Racu, R.Ernst, M. G. Harbour, "Influence of different abstractions on the performance analysis of distributed hard real-time systems". Journal on Design Automation for Embedded Systems, Springer, April, 2008, ISSN: 0929-5585

[WEE+08] R. Wilhelm, J. Engblom, A. Ermedahl, N. Holsti, S. Thesing, D. Whalley, G. Bernat, Chr. Ferdinand, R. Heckmann, F. Mueller, I. Puaut, P. Puschner, J. Staschulat, and P. Stenström. *The Determination of Worst-Case Execution Times—Overview of the Methods and Survey of Tools.* ACM Transactions on Embedded Computing Systems (TECS), 7(3), 2008.

3.4 Keynotes, Workshops, Tutorials

Invited talk: Petru Eles - Synthesis of Fault-Tolerant Embedded Systems DATE 2008 Conference, Munich, Germany - March 10, 2008 As part of the special day on Dependable Embedded Systems: With this occasion several results obtained in the Artist context have been made accessible to an international audience. They are related, in particular, to fault tolerance aspects of distributed real-time systems like those used in automotive applications.

Invited Lecture: Challenges in Embedded Systems Design: Predictability and Robustness
Thomas Ad. Henzinger - Royal Society Meeting: From Computers to Ubiquitous Computing, London, United Kingdom, March 2008.
We discuss two main challenges in embedded systems design: the challenge to build predictable systems, and the challenge to build robust systems. We suggest how predictability can be formalized as a form of determinism, and robustness, as a form of continuity.

Invited talk: Peter Marwedel: Mapping of Applications to MPSoCs
4th Compiler Assisted SoC Assembly Workshop (CASA08)
Atlanta, USA – Oct. 19th, 2008
The talk summarized the presentations of the "1st workshop on the mapping of applications to MPSoCs" for a wider audience.
http://www.esweek.org/

Invited Talk L. Thiele (ETHZ): MPSOC Conference. Aachen, Germany, June 23-27, 2008: Lothar Thiele described a new approach for mapping algorithms onto MPSoC architectures. It is a result of a cooperation between ArtistDesign partners from Aachen, TIMA and LETI. The design methodology is named DOL (distributed operation layer) and targets predictable and efficient multiprocessor systems and applications.

Invited Talk L. Thiele (ETHZ): Workshop Mapping Algorithms onto MPSOC.
Germany, June 16-17. 2008.
Lothar Thiele presented the current state-of-the art in mapping algorithms onto multi-processor platforms. Different approaches have been compared and a classification based on the application domain and estimation methods has been provided.

Summer School: Course on Embedded Systems (ETHZ, L. Thiele),
Florianopolis, Brasil, August 25-2, 2008.
The summer school was dedicated to promote the interaction between the embedded system communities in Europe and South America. Lothar Thiele was presenting a wide range of subjects, starting from basic methods to design predictable software of embedded systems. In addition, he presented methods for real-time scheduling and performance analysis of distributed embedded systems.

Artist Summer School
Grenoble, France, Sept 8-12, 2008.
During the Artist Summer School in Grenoble,
Lothar Thiele presented a tutorial on design space exploration and performance analysis, presenting interface-based design techniques for stream-based embedded systems. Predictability is obtained by extending the usual component interfaces by resource-aware guarantee-assume predictates. This way, constraints and properties of single components propagate through the whole system and define the relation between the component-based and system-based properties.

Reinhard Wilhelm gave a tutorial on timing analysis and timing predictability.

Peter Marwedel gave a tutorial on Memory architecture aware compilation for Embedded Systems
http://www.artist-embedded.org/artist/ARTIST2-Summer-School-2008.html

Artist Summer School
Shanghai, China, July 12-18, 2008.

Michael González Harbour presented a lecture focused on the methods used to schedule event-driven real-time systems and to guarantee the predictability of their response times. The lecture started with simple single processor systems scheduled with fixed priorities, and then progressed through dynamic scheduling and distributed systems. The MAST modelling and analysis tools for schedulability analysis was introduced and discussed. Advanced flexible scheduling techniques were reviewed that allow protection among different components of a complex application and provide the designer with services that facilitate building real-time applications at a higher level of abstraction.

http://www.artist-embedded.org/artist/Programme,1352.html

Workshop: Casteness 2008 Workshop;
Rome, Italy;15th-18th of January 2008:
The objectives of CASTNESS workshops and schools are, first, to provide training about the future of multi-processor/adaptable embedded systems (system SW, HW architectures, applications) and second, the cross-dissemination among European projects. ETHZ presented

an overview and a SW demonstration of the Distributed Operation Layer framework, included in a complete MPSoC design flow, as well as detailed information about the design space exploration and mapping optimization steps within this framework.
http://www.artist-embedded.org/artist/CASTNESS-08.html

Tutorial: Timing Analysis and Timing Predictability
Embedded Networked Systems: Theory and Applications
Heraklion, Crete – July 21–25, 2008
The 2008 Lectures in Computer Science of the Onassis Foundation were dedicated to theory and applications of Embedded Systems. Among the talks by leading researchers was a two-part tutorial by Reinhard Wilhelm on Timing Analysis and Timing Predictability.
http://www.forth.gr/onassis/lectures/2008-07-21/lecturers.html

Tutorial: Abstract Interpretation with Applications to Timing Validation
Princeton, USA – July 7–14, 2008
This invited tutorial was given by Reinhard Wilhelm (Saarland University). It explained the technique of abstract interpretation and its application to static timing analysis.
http://www.princeton.edu/cav2008/

Tutorial: Artist South American Summer School
Florianopolis, Brazil, Aug. 25.-29., 2008
The tutorial focused on compilation techniques exploiting descriptions of the memory architecture. Lothar Thiele (ETHZ) and Peter Marwedel (TU. Dortmund) gave lectures on Several topics in embedded systems design.
http://www.artist-embedded.org/artist/Objectives,1365.html

Tutorial, Martino Ruggiero (UoB): MPARM tutorial
Pisa, Italy – Nov 5-6, 2008
It was a two-day tutorial about the MPARM tool. Both the SW and HW environments have been discussed and described.

4. Overall Assessment and Vision

4.1 Assessment for Year 1

Overall, the collaborations planned in the activity have started very well, with a lot of interesting results. A conducive factor for this is the launch of the PREDATOR project, which involves several partners of the activity. Examples of successful collaborations include the integration of timing analysis techniques (Absint, Mälardalen, and USAAR) and compiler techniques (by Dortmund) to create a timing-aware compiler, and the collaboration on predictability for multicore processor platforms (Linköping, Bologna, and Braunschweig). Several more collaborations of this form are being launched, and publications and results will be produced in the next year.

The work on time-Predictable Operating System, driven by TU Vienna, has this year containe work on a case study to check the feasibility of building a very simple operating system with static and predictable timing behaviour. As the result of this experiment was positive, it is planned to interact with the groups from the operating systems and networks cluster to investigate if and how the used concepts can be used and adapted for operating systems that provide a wider functionality. Conceptual and experimental studies are planned in this direction.

Technically, the activity has laid good foundations to address the important longer term goal of providing techniques for timing predictability on multicore platforms. On the level of individual cores, USAAR and others gave for the first time ever a precise and useful definition of predictability of cache replacement policies, competitiveness and sensitivity. This work can pave the ground for the analysis of cache predictability in the presence of multiple core and of sensitivity to disturbances from outside influences. Together with the present expertise and with the additional work on quantifying the influence of preemptive scheduling on cache contents and on guiding developers to select preemption points which minimise the costs of preemption, this provides a foundation for integration into a coherent timing analysis for multi-core systems.

There have been many smaller collaborations and partner meetings. So far, there was no global event organized by the activity, such as, e.g., a one-day workshop at a major event. This issue should be considered in the planning for the second year.

4.2 Indicators for Integration

There were no explicit indicators stated for this activity for the first year in the Description of Work, but we can provide some observations below.

- 9 joint publications
- A large number of research collaborations and visits involving more than one partner, including several European projects
- Educational events (summer schools) organized or co-organized by the partners. (Two ARTIST summer schools, and a strong presence at the summer school in Florianopolis

4.3 Long-Term Vision

Further work needs to be done to derive sound design principles for performance and predictability in system design. This work will ultimately culminate in the definition of a multi-core architecture, including low-level hardware specification and scheduling, which can be subjected to timing analysis with a high degree of precision while still giving all the benefits of hardware parallelism. Within this work, all areas of system architecture, operating system design, compilation and timing analysis will be integrated.

Similar development should be aimed for operating systems, on which applications can be run so that the timing of the whole software system is well-predictable. To this end the software structures of both, the applications taks and the operating systems will have to be predictable, and unwanted timing interactions (OS-task and task-task interactions) have to be avoided, or at least minimized.

The activities within ArtistDesign and connected activities should provide the conceptual tools for these developments, as well as provide reference implementations to push their realization in industry Having a prototypical implementation of, e.g., a timing aware compiler, a predictable multicore architecture, and an operating system would be considered a successful result.

4.4 Tools and Platforms

4.4.1 Tool or Platform: aiT

Objectives

aiT is the leading tool for computing worst case execution times (WCETs).

Main Results

In a previous project, aiT was integrated with an experimental worst-case execution time aware compiler called wcc. During the last year, this integrated tool set was used for exploring the optimization potential for compiler optimizations using WCETs as the objective function.

Current work

The current work explores the optimization potential of wcc.

Participating partners:

- AbsInt, Saarbrücken
  AbsInt provides aiT.
- TU Dortmund
  TU Dortmund integrates aiT into wcc and explores the optimization potential.

Web
http://ls12-www.cs.tu-dortmund.de/research/activities/wcc/

4.4.2 Tool or Platform : MPA (Modular Performance Analysis)

Objectives

The MPA toolbox allows the analysis of distributed embedded real-time systems. It is based on the real-time calculus which allows a component-based investigation of essential system properties like throughput, end-to-end constraints and buffer space.

Main Results

During the first year of ArtistDesign, the tool box have been extended towards the modelling of hierarchical event streams (together with University Braunschweig) and coupled to the Symta/S tool from SymtaVision. In addition, it has been integrated into the MPSOC design environment DOL. As a result of activities in ArtistDesign, a design flow has been established that includes the MPARM simulation envrionement from University Bologna (Luca Benini). In the context of this activity, the semantics of DOL will be modelled in BIP (Verimag, Joseph Sifakis) in order to verify additional important system properties.

Current work

The integration of MPA and DOL with other tools of partners just started.

Participating partners:

- VERIMAG
  Link to BIP from Verimag.
- Braunschweig
  Link to Symta/S and the modelling of hierarchical event streams
- University Bologna
  Combining MPARM simulation and the DOL specification and mapping environment.
- Uppsala
  Providing insights into the analysis of cyclic systems which lead to an extension of the toolbox.

4.4.3 Tool or Platform : MPARM

Objectives
MPARM is a virtual SoC platform almost written in SystemC, which could be used to model both HW and SW of a system. The MPARM virtual platform is highly modular and capable of simulating at cycle-accurate level an entire MPSoC, including cores, L1 and L2 caches, L3 memories and system buses.

Current work
We are working on defining and implementing new ways to enhance the predictability of MPSoC systems. We will consider both SW and HW techniques, applied to the CPU, bus and memory sub-systems.

5. Transversal Activity Participants

5.1 Core Partners

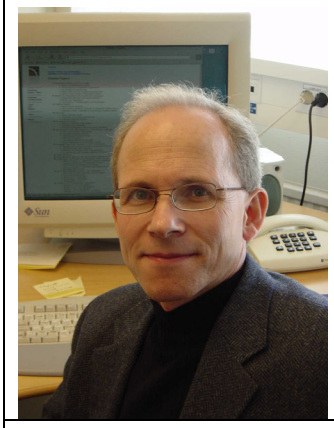
Team Leader **Leader for transversal activity "Design for predictability and Performance"**	
	Bengt Jonsson http://user.it.uu.se/~bengt/
Technical role(s) within ARTIST2	Participant in discussions, contributions regarding compositionality, modelling, analysis of timing properties, tool building (TIMES)
Research interests	Research interests include: embedded systems, semantics, verification, modelling, specification, testing of distributed and embedded systems
Role in leading conferences/journals/etc in the area	Have been PC member of most conferences in the area.
Notable past projects	ASTEC, Competence Center for Software Technology, 1995-2005. http://www.astec.uu.se/ WOODDES (IST project) A UML profile for Automotive industry http://wooddes.intranet.gr/ Advance http://www.liafa.jussieu.fr/~haberm/ADVANCE/ Regular model checking (www.regularmodelchecking.com)

Team Leader	
	Prof. Luca Benini, University of Bologna http://www-micrel.deis.unibo.it/%7Ebenini/

Technical role(s) within ArtistDesign	Member of the Strategic Management Board Co-leads Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Participates in Intercluster activity: Design for Predictability and Performance Leader of the JPRA Activity: “Platform and MPSoC Design”
Research interests	(i) Development of power modeling and estimation framework for systems-on-chip. (ii) Development of optimal allocation and scheduling techniques for energy-efficient mapping of multi-task applications onto multi-processor systems-on-chips. (iii) Development of energy-scavenging techniques for ultra-low power sensor network platforms.
Role in leading conferences/journals/etc in the area	▪ Program chair and vice-chair of Design Automation and Test in Europe Conference. ▪ Member of the 2003 MEDEA+ EDA roadmap committee 2003. ▪ Member of the IST Embedded System Technology Platform Initiative (ARTEMIS): working group on Design Methodologies ▪ Member of the Strategic Management Board of the ARTIST2 Network of excellence on Embedded Systems ▪ Member of the Advisory group on Computing Systems of the IST Embedded Systems Unit. ▪ Member of the technical program committee and organizing committee of several technical conferences, including the Design Automation Conference, International Symposium on Low Power Design, the Symposium on Hardware-Software Codesign. He is Associate Editor of the IEEE Transactions on Computer-Aided Design of Circuits and Systems and of the ACM Journal on Emerging Technologies in Computing Systems. ▪ Fellow of the IEEE.
Notable past projects	ICT-Project **REALITY - *Reliable and variability tolerant system-on-a-chip design in more-moore technologies.*** Funded under 7th FWP (Seventh Framework Programme). ICT-2007.3.1 Next-Generation Nanoelectronics Components and Electronics Integration. Start date: 01/01/2008; Duration: 30 months; Contract Type: Collaborative project; Project Reference: 216537; Project Cost: 4.45 million euro; Project Funding: 2.9 million euro. ICT-Project **PREDATOR - *Design for predictability and efficiency.*** Funded under 7th FWP (Seventh Framework Programme). ICT-2007.3.3 Embedded Systems Design. Start date: 01/02/2008; Duration: 36 months; Contract Type: Collaborative project; Project Reference: 216008; Project Cost: 3.93 million euro; Project Funding: 2.8 million euro. ICT-Project **GALAXY - *interface for complex digital system integration.*** Funded under 7th FWP (Seventh Framework Programme). ICT-2007.3.3 Embedded Systems Design. Start date: 01/12/2007; Duration: 36 months; Contract Type: Collaborative project; Project Reference: 214364; Project Cost: 4.08 million euro; Project Funding: 2.9 million euro.

	ICT-Project **DINAMICS - *Diagnostic Nanotech and Microtech Sensors.*** Funded under 6th FWP (Sixth Framework Programme). FP6-NMP 'Nanotechnologies and nanosciences, knowledge-based multifunctional materials and new production processes and devices'. Contract Type: Integrated project; Project Reference:IP 026804-2. Start date: 01/04/2007. Duration: 18 + 30 months. Project Cost:7276856 Euro. Project Funding: 4499542 Euro. http://www.dinamics-project.eu/ ICT-Project **SHARE - *Sharing open source software middleware to improve industry competitiveness in the embedded systems domain.*** Funded under 7th FWP (Seventh Framework Programme). ICT-2007.3.7 Network embedded and control systems. Start date: 01/05/2008; Duration: 24 months; Contract Type: Coordination and support actions; Project Reference: 224170; Project Cost: 1.1 million euro; Project Funding: 590000.00 euro.

Team Leader	
	Professor Alan Burns University of York, UK URL: www.cs.york.ac.uk/~burns
Technical role(s) within ArtistDesign	Undertakes research in real-time systems scheduling, particularly for flexible systems. Also concerned with the development of programming languages for this domain.
Research interests	Scheduling, languages, modeling and formal logics.
Role in leading conferences/journals/etc in the area	Previous Chair of the IEEE Technical Committee on Real-Time Systems. Edited special issue of ACM Transactions on Embedded Systems (on education).
Notable past projects	DIRC – Dependability Interdisciplinary Research Collaborations – A large, UK, 6-year, multisite project looking at dependability of computer-based systems. Burns was a PI and managed the work on temporal aspects of dependability. FIRST – EU funded project concerning flexible scheduling FRESCOR – EU follow on project to FIRST

	Petru Eles (Linköping University)
Technical role(s) within ArtistDesign	Main areas of research: Embedded Systems ArtistDesign activities and role: Communication centric systems, system analysis, optimisation, low power embedded systems, power management, modelling, analysis, and simulation of distributed embedded systems, predictable real-time systems, fault tolerance.
Research interests	Research interests include real-time systems, design of embedded systems, electronic design automation, hardware/software co-design,.
Role in leading conferences/journals/etc in the area	- Associate Editor, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems; - Associate Editor, IEE Proceedings - Computers and Digital Techniques; - TPC Chair and General Chair, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS). - Topic chair, Design Automation and Test in Europe (DATE). - Topic Chair, Int. Conference on Computer Aided Design (ICCAD). - Program chair of the Hw/Sw Codesign track, IEEE Real-Time Systems Symposium (RTSS). - TPC Chair IEEE Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia). - Steering Committee Chair, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS).
Awards / Decorations	- Best paper award, European Design Automation Conference (EURO-DAC), 1992. - Best paper award, European Design Automation Conference (EURO-DAC), 1994. - Best paper award, Design Automation and Test in Europe (DATE), 2005. - Best presentation award, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS), 2003.

	- IEEE Circuits and Systems Society Distinguished Lecturer, for 2004 - 2005.

Partner in Activitiy on Predictability	
	Alain Girault (INRIA Grenoble Rhône-Alpes)
Technical role(s) within ArtistDesign	Main areas of research: Embedded Systems ArtistDesign activities and role: formal methods for the design of embedded systems, predictable real-time systems, dependability analysis and design, fault tolerance.
Research interests	Research interests include embedded and real-time systems, formal methods, dependability, fault tolerance.
Role in leading conferences/journals/etc in the area	- Associate Editor, Eurasip Journal on Embedded Systems; - TCP co-chair of the Workshop on Model-driven High-level Programming of Embedded Systems (SLA++P'08).

Partner in Activitiy on Predictability	
	Michael González Harbour (Universidad de Cantabria)
Technical role(s) within ARTISTDesign	ArtistDesign activities and role: Participates in Operating Systems and Networks cluster, and also in the Intercluster activity: Design for Predictability and Performance
Research interests	Research interests include schedulability analysis for distributed real-time systems, real-time operating systems, real-time languages

Role in leading conferences/journals/etc in the area	Has been program committee chair in the ECRTS and Ada-Europe conferences, and in the International Real-Time Ada Workshop. Has participated in the past five years in the program committes of the following international conferences: ECRTS, Ada-Europe, RTSS, RTAS, ACM Symposium on Applied Computing, WPDRTS, CORDIE, DATE, ETFA, EUC, EMSOFT, IRTAW, EDF. Has been invited editor in the Real-Time Systems Journal and the Eurasip Journal on Embedded Systems. Has participated actively in the development of the POSIX standards, in the extensions of operating systems services for real-time applications.
Notable past projects	FRESCOR: Framework for Real-time Embedded Systems based on COntRacts (EU project) FIRST: Flexible Integrated Real-Time Systems Technology (EU project)
Further Information	Group home page: http://www.ctr.unican.es MAST toolset: http://mast.unican.es MaRTE OS: http://marte.unican.es

Cluster Leader **Activity Leader for "Software Synthesis and Code Generation"**	
	Prof. Dr. Peter Marwedel (TU Dortmund) http://ls12-www.cs.tu-dortmund.de/~marwedel/
Technical role(s) within ArtistDesign	Cluster leader, activity leader SW Synthesis and Code Generation Improved code quality for embedded applications is the main goal of the work at Dortmund University. Due to the widening gap between processor and memory speeds, emphasis has been on improving the efficiency of memory accesses, in terms of average and worst case execution time and in terms of the energy consumption.
Research interests	Peter Marwedel's Embedded Systems Group focuses on embedded software. Particular emphasis is on compilers for embedded processors. One of the very first publications in this area, the book "Compilers for Embedded Processors", edited by Peter Marwedel and Gert Goossens, was the result of the CHIPS project, funded by the European Commission. The group's current focus is on advanced optimizations for embedded processors (e.g. by using bit-level data flow analysis) and energy-aware compilation techniques. Current research also includes high-level transformations of algorithms as well as WCET-aware code generation.

Role in leading conferences/journals/etc in the area	Member of the EDAA (European Design and Automation Association) Main Board. Editorial Board Member of the Journal of Embedded Computing. Editorial Board Member of the Microelectronics Journal. Co-Founder and Steering Board Chair of the SCOPES Workshop (Software and Compilers for Embedded Systems) Series. >14 years of service for the DATE conference and its predecessors (program chair: 3 times, chairman of the steering committee, European representative to ASPDAC) DAC: Topic chair and reviewer Various other conferences
Notable past projects	MAMS: Multi-Access modular-services framework, national project funded by the German Federal Ministry of Education and Research (BMBF) MORE: Network-centric Middleware for group communications and resource sharing across heterogeneous embedded systems, supported by the European Commission http://www.ist-more.org HiPEAC: European NoE on High-Performance Embedded Architecture and Compilation; http://www.hipeac.net Others: Various earlier projects supported by the EC, DFG etc.
Awards / Decorations	Teaching award, TU Dortmund, 2003 DATE fellow, 2008
Further Information	CEO of the Informatik Centrum Dortmund (ICD), a technology transfer centre founded in 1989.

	Dr. Stylianos Mamagkakis (IMEC vzw.) http://www.imec.be
Technical role(s) within ArtistDesign	SW Synthesis and Code Generation; collaboration with TU Dortmund on high-level transformations for source code optimizations.

Research interests	Stylianos Mamagkakis received his Master and Ph.D. degree in Electrical and Computer Engineering from the Democritus Uni. Thrace (Greece) in 2004 and 2007, respectively. Since 2006, he coordinates a team of PhD students within the NES division at IMEC, Leuven, Belgium. His research activities mainly belong to the field of system-level exploration, with emphasis on dynamic resource management and system integration.
Role in leading conferences/journals/etc in the area	Stylianos Mamagkakis has published more than 25 papers in International Journals and Conferences. He was investigator in 6 research projects in the embedded systems domain funded from the EC as well as national governments and industry.
Notable past projects	EASY IST project Energy-Aware System-on-chip design of the HIPERLAN/2 standard, http://easy.intranet.gr/ AMDREL IST project Architectures and Methodologies for Dynamic Reconfigurable Logic, http://vlsi.ee.duth.gr/amdrel/

Transversal Activity Leader Activity Leader for "NoE Integration: Low Power"	
	Prof. Dr. Peter Puschner (TU Vienna) Real-Time Systems Group Institute of Computer Engineering Vienna University of Technology http://www.vmars.tuwien.ac.at/people/puschner.html
Technical role(s) within ArtistDesign	Peter Puschner and his group are participating in the timing analysis and design for predictability activities of ArtistDesign. They will provide technical contributions in compiler support for timing analysis, software/hardware architectures that make real-time systems more time-predictable and composable, and operating systems with predictable timing.
Research interests	Peter Puschner's main research interst is on real-time systems. Within this area he focuses on Worst-Case Execution Time Analysis and Time-Predictable Architectures.
Role in leading conferences/journals/etc	Member of the Euromicro Technical Committee on Real-Time Systems, the steering committee of the Euromicro

in the area	Conference on Real-Time Systems (ECRTS) Member of the advisory board and organizers committee of the IEEE International Symposium on Object- and Component-Oriented Distributed Computing (ISORC) conference series Chair of the Steering Committee of the Euromicro Workshop on Worst-Case Execution-Time Analysis (WCET) series
Notable past projects	DECOS - Dependable Embedded Components and Systems Develop the basic enabling technology to move from a federated distributed architecture to an integrated distributed architecture. http://www.decos.at MoDECS - Model-Based Development of Distributed Embedded Control Systems Model-based construction of distributed embedded control systems: shift from a platform-oriented towards a domain-oriented, platform-independent development of composable, distributed embedded control systems. http://www.modecs.cc/ NEXT TTA Enhance the structure, functionality and dependability of the time-triggered architecture (TTA) to meet the cost structure of the automotive industry, while satisfying the rigorous safety requirements of the aerospace industry. http://www.vmars.tuwien.ac.at/projects/nexttta/
Awards / Decorations	
Further Information	

Team Leader	
	Alberto Sangiovanni Vincentelli (PARADES) http://www.parades.rm.cnr.it/
Technical role(s) within ARTIST2	Bring in Expertise in embedded system modelling, validation, tools and methodologies and IC design. Deep involvement in cooperation with the industry: tools (co-founder Cadence and Synopsys), telecommunications

	(Telecom Italia), automotive (member of the GM STAB)
Research interests	Embedded system design methodologies and tools including modelling, validation, synthesis and formal verification, semantic foundations.
Role in leading conferences/journals/etc in the area	Program Committee Member CODES and EMSOFT. Member of the Editorial Boards Member of the ARTEMIS High-level Group and Steering Committee
Notable projects	SPEEDS - Speculative and Exploratory Design in Systems Engineering Provide a semantics based modelling methods with analysing techniques to support the construction of complex embedded systems by composing heterogeneous subsystems together with a speculative tool-supported design process. HYCON NoE: Taming Hybrid Systems Center for Hybrid and Embedded Software Systems (CHESS) co-director Gigascale System Research Center, Core theme leader RIMACS: Industrial Automation
Awards/Decorations	IEEE Fellow, Member National Academy of Engineering, Kaufmann Award for pioneering contributions to EDA, IEEE Graduate Teaching Award, Gulliemin-Cauer Award, Darlington Award, Aristotle Award, University of California Distinguished Teaching Award

Participant in Activitiy on Adaptivity	
	Lothar Thiele (ETH Zurich)
Technical role(s) within	Main areas of research: Embedded Systems and Software

ARTISTDesign	Artist2 activities and role: Communication Centric Systems: Formal Performance Analysis, Linking Simulation and Verification, Design Space Exploration of Embedded Systems
Research interests	Research interests include models, methods and software tools for the design of embedded systems, embedded software and bioinspired optimization techniques.
Awards / Decorations	In 1986 he received the "Dissertation Award" of the Technical University of Munich, in 1987, the "Outstanding Young Author Award" of the IEEE Circuits and Systems Society, in 1988, the Browder J. Thompson Memorial Award of the IEEE, and in 2000-2001, the "IBM Faculty Partnership Award". In 2004, he joined the German Academy of Natural Scientists Leopoldina. In 2005-2006, he was the recipient of the Honorary Blaise Pascal Chair of University Leiden, The Netherlands. Chair of ACM SIGBED.

	Prof. Dr. Dr. h. c. Reinhard Wilhelm (Saarland University) http://rw4.cs.uni-sb.de/people/wilhelm
Technical role(s) within ArtistDesign	Timing Analysis
Research interests	Compilers, Static Analysis, Timing Analysis
Role in leading conferences/journals/etc in the area	PC member of SCOPES, LCTES, MEMOCODE, RTSS etc. Steering committee member of EMSOFT, member at large of the steering committee of LCTES Member of the ACM SIGBED Executive Committee
Notable past projects	DAEDALUS
Awards / Decorations	Prix Gay-Lussac-Humboldt in 2007 Honorary doctorates of RWTH Aachen and Tartu University in 2008
Further Information	Co-founder of AbsInt Angewandte Informatik GmbH Scientific Director of the Leibniz Center for Informatics Schloss Dagstuhl

5.2 Affiliated Academic Partners

Team Leader	
	Rolf Ernst (TU Braunschweig)
Technical role(s) within ArtistDesign	Main areas of research: Embedded Systems Participates in Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Participates in Intercluster activity: Design for Predictability and Performance Participates in Intercluster activity: Integration Driven by Industrial Applications
Research interests	Research interests include embedded architectures, hardware-/software co-design, real-time systems, and embedded systems engineering.
Role in leading conferences/journals/etc in the area	He chaired major international events, such as the International Conference on Computer Aided Design of VLSI (ICCAD), or the Design Automation and Test in Europe (DATE) Conference and Exhibition, and was Chair of the European Design Automation Association (EDAA), which is the main sponsor of DATE. He is a founding member of the ACM Special Interest Group on Embedded System Design (SIGBED), and was a member of the first board of directors. He is an elected member (Fachkollegiat) and Deputy Spokesperson of the "Computer Science" review board of the German DFG (corresponds to NSF). He is an advisor to the German Ministry of Economics and Technology for the high-tech entrepreneurship program EXIST (www.exist.org).

6. Internal Reviewers for this Deliverable

Jan Madsen, DTU