214373 ArtistDesign
Network of Excellence
on Embedded Systems Design

Periodic Activity Report for Year 1

Executive Summary

Joseph Sifakis – ArtistDesign Scientific Coordinator
Bruno Bouyssounouse – ArtistDesign Technical Coordinator

ArtistDesign Consortium

1. Project Objectives

The ArtistDesign NoE is the visible result of the ongoing integration of a community.

The central objective for ArtistDesign is to build on existing structures and links forged in the ARTIST2 NoE, to become a virtual Centre of Excellence in Embedded Systems Design. This is achieved through tight integration between the central players of the European research community. Also, the consortium is smaller, and integrates several new partners. These teams have already established a long-term vision for embedded systems in Europe, which advances the emergence of Embedded Systems as a mature discipline.

ArtistDesign is becoming the main focal point for dissemination in Embedded Systems Design, leveraging on well-established infrastructure and links. It will extend its dissemination activities, including Education and Training, Industrial Applications, as well as International Collaboration. ArtistDesign will establish durable relationships with industry and SMEs in the area.

ArtistDesign builds on existing international visibility and recognition, to play a leading role in structuring the area.

The research effort aims to integrate topics, teams, and competencies, grouped into 4 Thematic Clusters: “Modelling and Validation”, “Software Synthesis, Code Generation, and Timing Analysis”, “Operating Systems and Networks”, “Platforms and MPSoC”. “Transversal Integration” covering both industrial applications and design issues aims for integration between clusters.

2. Contact Details and Contractors Involved

2.1 Core Partners

For a complete description including web links, see:
http://www.artist-embedded.org/artist/-ArtistDesign-Participants-.html

Scientific Coordinator:
Joseph Sifakis
Tel: +33 4 56 52 03 51
Joseph.Sifakis@imag.fr

Technical Coordinator:
Bruno Bouyssounouse
Tel: +33 4 56 52 03 68
Bruno.Bouyssounouse@imag.fr

N°	Beneficiary name	Beneficiary short name	Country
1	UJF FILIALE	FLORALIS	France
2	UNIVERSITE JOSEPH FOURIER GRENOBLE 1	UJF/VERIMAG	France
3	RHEINISCH-WESTFAELISCHE TECHNISCHE HOCHSCHULE AACHEN	AACHEN	Germany
4	AALBORG UNIVERSITET	AALBORG	Denmark
5	UNIVERSIDADE DE AVEIRO	AVEIRO	Portugal
6	ALMA MATER STUDORIUM - UNIVERSITA DI BOLOGNA	BOLOGNA	Italy
7	TECHNISCHE UNIVERSITAET BRAUNSCHWEIG	TUBS	Germany
8	UNIVERSIDAD DE CANTABRIA	CANTABRIA	Spain
9	COMMISSARIAT À L'ENERGIE ATOMIQUE	CEA	France
10	DANMARKS TEKNISKE UNIVERSITET	DTU	Denmark
11	UNIVERSITAET DORTMUND	DORTMUND	Germany
12	ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE	EPFL	Switzerland
13	EMBEDDED SYSTEMS INSTITUTE	ESI	Netherlands
14	EIDGENOESSISCHE TECHNISCHE HOCHSCHULE ZUERICH	ETH Zurich	Switzerland
15	INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM VZW	IMEC	Belgium
16	INSTITUT NATIONAL DE RECHERCHE EN INFORMATIQUE ET AUTOMATIQUE	INRIA	France
17	TECHNISCHE UNIVERSITAET KAISERSLAUTERN	TUKL	Germany
18	KUNGLIGA TEKNIKA HOGSKOLAN	KTH	Sweden
19	LINKÖPINGS UNIVERSITET	LINKOPING	Sweden
20	LUNDS UNIVERSITET	ULUND	Sweden
21	MAELARDALENS HOEGSKOLA	MDH	Sweden
22	OFFIS E.V.	OFFIS	Germany
23	PROJECT FOR ADVANCED RESEARCH OF ARCHITECTURE AND DESIGN OF ELECTRONIC SYSTEMS	PARADES	Italy
24	UNIVERSITAET PASSAU	PASSAU	Germany
25	SCUOLA SUPERIORE DI STUDI UNIVERSITARI E DI PERFEZIONAMENTO SANT'ANNA	SSSA-PISA	Italy
26	INSTITUTO SUPERIOR DE ENGENHARIA DO PORTO	PORTO	Portugal
27	UNIVERSITAET DES SAARLANDES	SAARLAND	Germany
28	UNIVERSITAET SALZBURG	PLU-SALZBURG	Austria
29	UPPSALA UNIVERSITET	UPPSALA	Sweden
30	TECHNISCHE UNIVERSITAET WIEN	VIENNA	Austria
31	UNIVERSITY OF YORK	YORK	UK

2.2 Affiliated Partners

Affiliated partners play a very strong role in the Spreading Excellence from the core partners to the research and industrial communities at large.

Affiliated partners generally play an active role in the research activities, either participating directly in research, or transferring the results directly to industry.

Each of the JPRA and JPIA activities' deliverables provides the list of the corresponding affiliated partners and roles.

Affiliated Industrial Partners

The complete set of Affiliated Industrial partners, including web links, is available online, here: http://www.artist-embedded.org/artist/-Affiliated-Industrial-Partners-.html

Christer Norström Göran Arinder	ABB	Peter Mårtensson	NOKIA Connecting People
David Lesens	EADS Astrium Space (EADS)	Dirk Ziegenbein	BOSCH Robert Bosch AG
Thomas Thurner Matthias Grochtmann	DaimlerChrysler	Sven Holme Sørensen	SIEMENS
Dr Joachim Stroop	dSPACE	Roberto Zafalon	ST
Alain Ourghanlian	EDF Electricité de France	Dr. Kai Richter	SYMTA VISION
Jan Lindblad	ENEA	Thomas Hune	TERMA
Johan Eker	ERICSSON	Dominique Potier, Philippe Kajfasz	THALES

Philippe Baufreton	Hispano-Suiza Groupe SAFRAN
Vladimir Havlena	Honeywell
Dr. Michael Winokur	IAI Israel Aircraft Industries
Dr. Matthias Gries	intel Intel Gmbh
Peter Mårtensson	MAQUET Maquet Critical Care
Fabian Wolf	VW
Magnus Hellring	VOLVO
Magnus Hellring	VOLVO
Jakob Axelsson	VOLVO for life

Affiliated SME Partners

Alan Moore	ARTiSAN SOFTWARE
Dr. Monica Donno	BullDAST Design Automation Services and Tools
Joachim Stroop	dSPACE
Jan Lindblad	ENEA
Bernard Dion	ESTEREL Technologies
Paolo Gai	Evidence
Carl von Platen	IAR SYSTEMS
António Garrido	LIFTECH LIFT TECHNOLOGIES
Fernando Santos	Micro I/O www.microio.pt
	VALIOSYS

Affiliated Academic Partners

Prof. Ahmed Bouajjani

LIAFA - Université Paris 7 & CNRS UMR 7089

Tel: +33 (0) 1 4427 7819

Dr. Frédéric Boulanger

Ecole supérieure d'électricité (Supélec), Computer Science Department
Component-Based Design of Heterogeneous Systems

Tel: +33 1 69 85 14 84

Prof. Lubos Brim

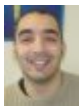
Masaryk University Brno

Tel: +420 549 493 647

Prof. Dr. Dr. h.c. Manfred Broy

TU München

Tel: +49 89 289-17304



Ass. Prof. Salvatore Carta

Università degli Studi di Cagliari

Tel: +39 070-675-8780

Dr. Francky Catthoor

IMEC

Tel: +32 16 281202

Prof. Lucia Lo Bello

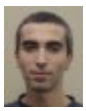
University of Catania

Tel: +39 095 7382386

Prof. Dr. Miroslaw Malek

Humboldt University Berlin

Tel: +49 30 2093 3027



Dr. Pau Martí Colom

Universitat Politècnica de Catalunya

Tel: +34 93 401 1679

Dr. Fabio Martinelli

Istituto di Informatica e Telematica

National Research Council C.N.R.

Tel: +39.050.315.3425

Dr. Marius Minea

Timisoara - Institute e-Austria Timisoara

Tel: +40-256-403284

Associate Prof. Laurent Pautet

ENST

Tel: +33 1-45-81-73-22

Prof. Geert Deconinck

Katholieke Universiteit Leuven

Tel: +32 16 32.11.26

Prof. Giovanni DeMicheli

EPFL Lausanne

Tel: (+41 21) 693-0911

Prof. Ivo De Lotto

Università degli studi di Pavia
Team leader

Tel: +39 0382 98 53 57

Prof. Dr. Ed Deprettere

Leiden University

Tel: +31 (0)71 5275776

Prof. Luca Fanucci

University of Pisa

Prof. Dr. Marisol Garcia-Valls

Universidad Carlos III de Madrid

Tel: +34 91-624-8783

Julián Proenza

University of the Balearic Islands

Tel: (+34) 971 17 29 92

Dr. Isabelle Puaut

IRISA

Tel: +33 02 99 84 73 10

Michael Rusinowitch

INRIA
Formal methods on embedded systems – in particular on verification of security properties.

Tel: +33 03 83 59 30 20

Prof. Pablo Pedro Sanchez

Universidad de Cantabria
Design and Implementation of Embedded H/S Systems

Tel: +34 942 201548

Dr. Markus Schordan

TU Vienna

Prof. Donatella Sciuto

Politecnico di Milano

Tel: +39-02-2399 3662


Prof. José Maria Giron-Sierra
University Complutense of Madrid
Tel: +34913944387


Prof. Axel Jantsch
Royal Institute of Technology (KTH)
Tel: +46 8 790 4124; +46 70 713 7428


Prof. Christoph Kirsch
University of Salzburg
Tel: +43 (0) 662 8044-6328


Prof. Stefan Kowalewski
RWTH Aachen
Tel: +49 241 80 21150


Prof. Andreas Krall
TU Vienna


Prof. Luciano Lavagno
Politecnico di Torino
Tel: +39-011-5644150


Prof. Johan Lilius
Åbo Akademi University


Ass. Prof. Dimitrios Soudris
Democritus University of Thrace
Tel: +30 25410 79557


Prof. Neeraj Suri
TU Darmstadt
Tel: +49 6151 16 3513


Prof. Dr.-Ing. Jürgen Teich
University of Erlangen-Nuremberg
Design Methodology for Embedded Systems
Tel: +49 9131 85 25150


Dr. ir. Jan Tretmans
University of Nijmegen
Tel: +31 24 365 2069


Prof. Pierre Verbaeten
Katholieke Universiteit Leuven
Tel: +32 (0)16 32 75 66


Prof. Eugenio Villar
Universidad de Cantabria
Design and Implementation of Embedded H/S Systems
Tel: +34 942 201398

Tel: +358-40-544 0741	

Affiliated International Collaboration Partners

Prof. Tarek Abdelzaher

University of Illinos at Urbana-Champaign
Technical expert

Tel: +1 217 265-6793

Prof. Zhou Chaochen

Chinese Academy of Sciences

Prof. Giovanni De Micheli

EPF Lausanne

Tel: +41 21 693-0911

Assoc. Prof. Stephen A. Edwards

Columbia University

Tel: +1 212 939 7019

Prof. Sharon Hu

University of Notre Dame - Indiana USA
Design for Low Power

Tel: +1 574 631-6015

Shankar Sastry

Berkeley University

Tel: +1 (510) 643-2200

Prof. Heinz Schmidt

Monash University (Australia)

Tel: +61 3 9905-2479

Prof. Lui Sha

University of Illinos at Urbana-Champaign
Technical expert.

Tel: +1 244-1887

Assoc. Prof. Mircea R. Stan

University of Virginia
Power and thermal modeling at the device, circuit and system level.
Self-consistent power modeling by taking into account thermal effects.
Temperature-aware circuit design.
Automotive computing applications.
Participates in the activity on Design for Low Power.

Tel: +1 434 924 3503

Prof. Mathai Joseph

Tata Research Development & Design Centre (TRDDC)

Prof. Edward A. Lee

UC Berkeley

Tel: +1-510-642-0253

Prof. Xiaojian Liu

Zhiming Liu

UNU-IIST Macau
Co-organiser of the Artist2 / UNU-IIST School in China - 2007

Tel: +853 712930

Prof. Kang Shin

University of Michigan

Tel: +1 (734) 763-0391

Prof. John Stankovic

University of Virginia

Tel: +1 (434) 982-2275

Prof. Janos Sztipanovits

Vanderbilt University USA

Tel: +1 615-343-7572

Prof. P.S. Thiagarajan

National University of Singapore

Tel: (65) 6516 7998

3. Vision and Assessment of the Work Performed

ArtistDesign finances durable integration between teams and not the concrete elements of the JPA which most often belong to other projects. These specific technical objectives may or may not be attained (this is the essence of research as opposed to development), but we feel that the main product of ArtistDesign is the emergence of a lasting European research community, that has a significantly enhanced capacity for preparing Europe's future.

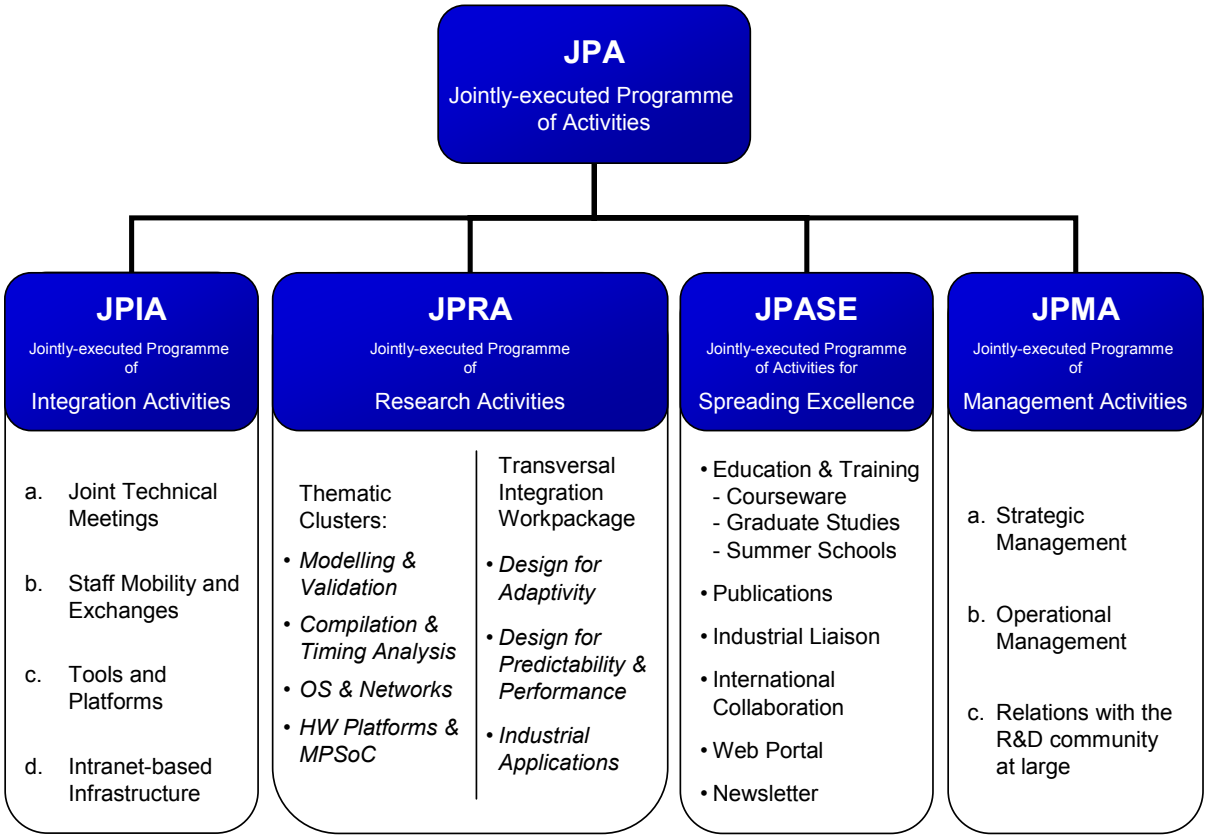
The research is completed by work in the JPIA (Jointly Executed Programme of Integration Activities) workpackage, which aim to transform research results in tangible tools and components, and bring teams closer together on a day to day basis.

We believe that the topics chosen provide a good coverage of the area, for embedded software and systems.

The ArtistDesign NoE is a complex construction assembled from world-leading communities, teams, and individuals. This is certainly an asset, but also a source of complexity in management. Each team has two essential characteristics: world-class excellence and strong interaction with top industrial players. ArtistDesign partners play a leading role in the different communities in embedded systems design, and they advance the state of the art in each of these.

It is difficult to abstract out a global synthesis of the overall technical achievements. This is due to the diversity and the low granularity of the actions to be covered (meetings, publications, attendance at workshops, visits, and platforms).

The following is a certainly non-exhaustive assessment of the work in the Joint Programme of Activities' 4 main branches.



3.1 Joint Programme of Research Activities (JPRA)

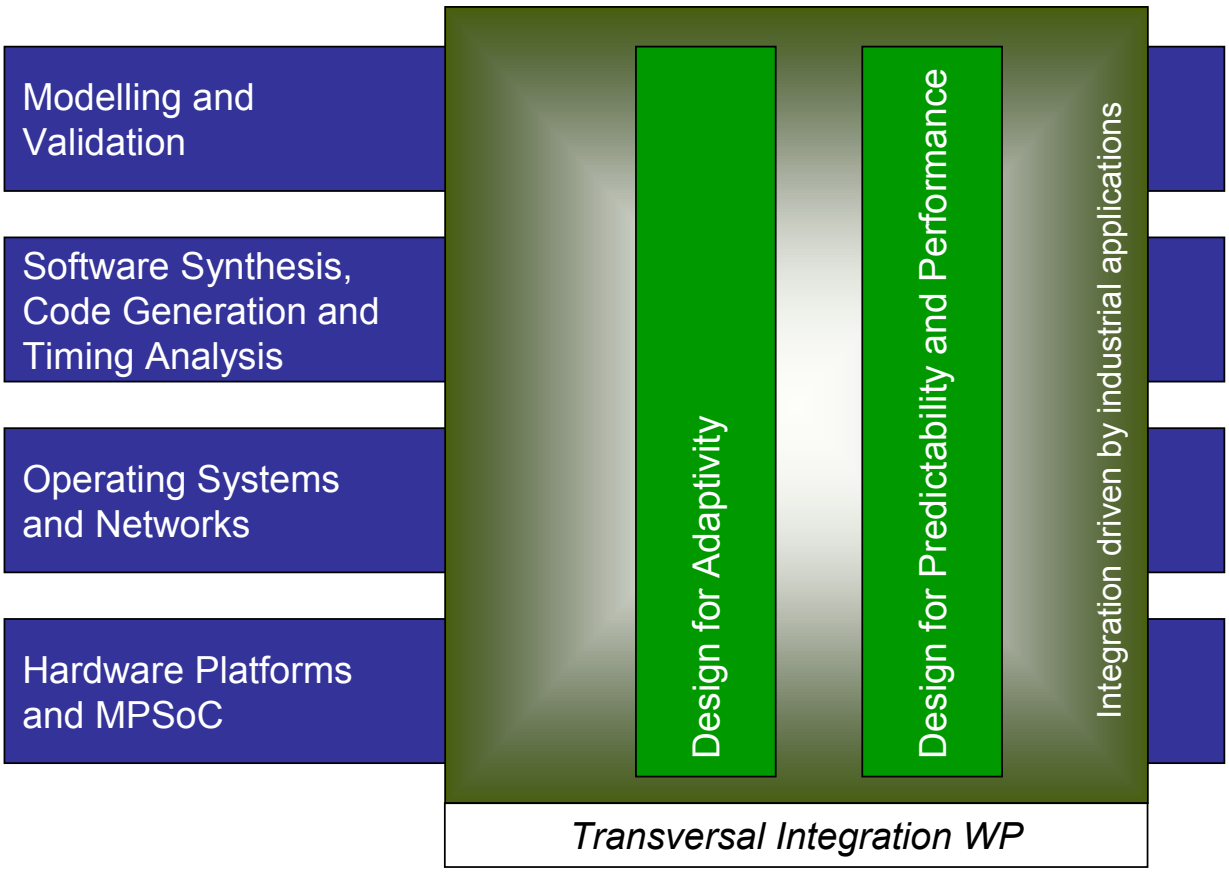
3.1.1 Structure of the Research Effort

The JPRA is composed of intra and inter-cluster research activities on cutting-edge topics in embedded systems design. While the main bulk of financing for these activities is taken up by outside programmes (Integrated Projects, National Programmes, Industrial Contracts, etc), the ArtistDesign NoE finances the extra burden due derived from integrating these into a single coherent research programme.

Thus, the essential ingredient within ArtistDesign is the JPRA, which motivates the participating research teams far more than the actual financing, which is tiny in comparison with the overall research aims. It is completed by the Joint Programme of Integrating Activities (JPIA), and the Joint Programme of Activities for Spreading Excellence (JPASE), and overseen by the Joint Programme of Management Activities (JPMA).

The structure of the research activities reflects the following decomposition of the embedded systems design flow.

This design flow is composed of the following cooperating activities, starting with component-based modelling and leading to implementation. These activities must be well coordinated, and supported by tools and methods to ensure satisfactory levels of productivity and quality. Accordingly, we have structured the area of embedded systems design into the following topics.



Modelling and Validation. Unlike other computer systems, embedded systems are strongly connected with a physical environment. A scientific foundation for embedded systems must therefore deal simultaneously with software, hardware resources, and the physical environment, in a quantitative manner. In order to gain independence from a particular target platform, embedded system design must be model-based. In order to scale to complex applications, embedded system design must be component-based. The overall objective of this activity is develop model and component based theories, methods, and tools that establish a coherent family of design flows spanning the areas of computer science, control, and hardware. The activity brings together the most important teams in the area of model and component based design in Europe.

SW Synthesis, Code Generation and Timing Analysis. There is a continuing demand for higher performance of information processing, which stimulates using a growing amount of parallelism (including using multiple processors). This trend affects the design of embedded systems. We address issues related to multiple heterogeneous processors on a chip, also containing memory hierarchies and communication interfaces. Such processors can only be exploited if (sets of) applications can be efficiently mapped to heterogeneous processors. Timing analysis is also affected by the trend toward the new platforms. Timing analysis has to cope with the kind of memory hierarchies found in MPSoCs. Also, timing analysis beyond the single processor is required. Hence, timing analysis will also consider the timing of communication. The overall objective is to provide safe timing guarantees for systems consisting of local memories hierarchies and multiple processors.

Operating Systems and Networks. We investigate how current real-time operating systems have to be extended or modified to support emerging real-time embedded systems characterized by a high degree of complexity, highly variable resource requirements and parallel processing such as multicores. Most embedded systems are often characterized by scarce resources in terms of processing power, memory, space, weight, energy, and cost. Hence, another objective is to investigate kernel mechanisms that can efficiently manage the available resources, taking multiple constraints into account, whilst guaranteeing isolation properties. Also, to support dynamic applications with variable resource requirements or to cope with unpredictable resource availability, feedback control techniques for resource management at the operating system and application level are also investigated.

Hardware Platforms and MPSoC Design. While hardware platforms for embedded applications will continue to be multi-core, with increasing degrees of parallelism, the evolution trajectory on programming models, design-time and run-time application environments is much less clear. The consequence is fragmentation: while many research teams are working on one or more of these domains, there is little communication and integration, this leads to duplication of results and overall slow progress. The teams involved in this activity have a wide-ranging research experience which covers all the key areas in MPSoC application specification mapping. The integration activity supported by ArtistDesign will help the participants to the cluster in strengthening the coherency of their approaches and focus on addressing complementary issues in a synergistic fashion.

Design for Adaptivity. An embedded hardware-software system is adaptive, if it can modify its behaviour and/or architecture to changing requirements. Adaptivity is increasingly important as the complexity and autonomy of embedded systems increases. Adaptivity is a cross-cutting system characteristic that affects both hardware and software. At the software-level adaptivity is mainly concerned with flexible and adaptive resource scheduling, e.g., CPU time scheduling. At the hardware-level adaptivity includes both adaptation of operation modes, e.g., supply voltage and clock frequency, processor instruction sets, and dynamic management of hardware resources, e.g., processing elements and memory.

Design for Predictability and Performance. Many applications have strict requirements on timing, and limited resources (memory, processing power, power consumption, etc.). All systems also have increasing demands on (average) performance, which has motivated the introduction of features such as caching, pipelining, and (now becoming very prominent) multiprocessor platforms. Almost all such efficiency-increasing features drastically increase variability and decrease analyzability of response-times, etc. and thus have a detrimental effect on predictability. Since the introduction of new architectural features is inevitable, it is important to: a) develop technology and design techniques for achieving predictability of systems built on modern platforms, and b) investigate the trade-offs between performance and predictability.

Integration Driven by Industrial Applications. To have a strong impact on industry and society at large, the results of the Thematic Clusters need to be harmonized in an overall design flow that can sustain the embedded design chain from conception of the product to its implementation. The design chains vary in length and players according to the industrial segment addressed: for example, the design chain in automotive electronics starts with the car maker (e.g., BMW, Daimler Chrysler, Peugeot, Fiat), goes through the Tier 1 suppliers (e.g., Contiteves, Bosch, Magneti Marelli) and connects to the Tier 2 suppliers (e.g., FreeScale, ST, Infineon, Hitachi). It often includes IP providers such as programmable cores, RTOS and software development tool providers and design service companies. In the mobile communication domain, the chain starts with the application developers (e.g., gaming and video content), includes the telecommunication operators (e.g., Telecom Italia and Telefonica), the device makers (e.g., Nokia and Ericsson), the silicon makers (e.g., TI, Qualcomm and ST) and outsourcing manufacturing companies (e.g., Flextronics). Today, there is stress in the chain as the technology advances may create opportunities to redefine the roles of the various players. In addition, the system integrators are often faced with an almost impossible task of composing their design out of parts supplied by companies whose design methods and standards are widely different and about which they have limited or no information. There is a need for an all-encompassing approach to system design that can make an entire industrial segment work as a virtual vertically integrated company.

3.1.2 *Overview of the Year1 Research Results*

We present an overall vision integrating aspects from both the Artist2 European Network of Excellence (ended Sept 30th 2008) and ArtistDesign. This more complete vision is not necessarily followed in the Cluster and Activity deliverables, to avoid “double reporting”.

3.1.2.1 Modeling and Validation

Modeling

On modelling heterogeneous systems, we have obtained some very significant results:

- Work by INRIA, PARADES, and VERIMAG, on the theory of tagged systems provides conditions for correct implementation of synchronous systems on “less synchronous” architectures. Work by INRIA on new models of computation, the Kahn-extended Event Graph (KEG), which adds “static control” in the Model of Computation of Marked Graphs.
- Work on the BIP component framework, introduces a notion of expressiveness for component-based formalisms, which provides a basis for their comparison. This notion

drastically differs from the usual one, as it takes into account the expressive power of composition operators (glue operators).

- Significant progress has been achieved in methods for distributed implementation of non-distributed specifications. VERIMAG studied a method for the automatic generation of distributed implementations of BIP models. INRIA, PARADES and VERIMAG studied the concept of loosely time-triggered architectures, implementing time-triggered architectures. Finally, fully asynchronous implementations of synchronous systems have been studied.
- Other results on distributed implementations include reliability, new heuristics in scheduling for reliability, design of communication architectures and time-triggered system-on-chip architectures.

Validation

At the crossroads between Modeling and Validation, we have obtained significant results on Interfaces and Composability, including:

- The development of interface theories supporting component reuse (EPFL). We have shown that existing interface theories provide no formal support for component reuse. We enriched interface theories with a new operation allowing the same component to implement several different interfaces in a design.
- The development of contract-based verification techniques for the heterogeneous rich component (HRC) model (INRIA, PARADES, VERIMAG), in the framework of the SPEEDS project. The techniques allow handling multiparty interaction, as well as many different languages for describing notions of refinement under contexts. These results found application in the verification and analysis of HRC models.
- In joint work, ETHZ and Uppsala propose modular performance analysis techniques, based on the real-time calculus and timed automata. A prototype tool name CATS for compositional timing and performance analysis has been developed.
- VERIMAG has continued the work on compositional deadlock verification of BIP programs, and its implementation in the DeadlockFinder tool. Other results include the enhancement of existing component models, such as the synthesis of controllers from specifications and the generation of component models from their observed behaviour.
-

On qualitative validation, work has been carried out in the following directions:

- Significant contributions to game-theoretic approaches to real-time system testing. By modelling the systems as timed game automata and specifying the test purposes as formulas, we developed a timed game solver Tiga to synthesize testing strategies.

  We studied games for different extensions of timed automata such as weighted timed automata, priced timed automata, multi-priced timed automata. The results relate to the complexity of decision problems for these automata, as well as model checking and synthesis algorithms. The notion of timed parity games has been studied, with a focus on robustness and complexity. We have also studied reachability in timed games.

- Continuing on work from previous years, we have extended and improved the functionality of the UPPAAL tool, including the use of slicing techniques for model optimization as well as features supporting interface theory for real-time systems.

- We have studied quantitative testing techniques. In particular, we have developed a theory allowing testing of systems in the presence of measurement imprecisions. We also studied testing methods for probabilistic processes.

- We have studied quantitative model checking techniques for timed models, including timed automata, linear hybrid automata and general non-linear hybrid systems. The work on verification has been applied to non-trivial case studies and systems, in particular in collaboration with industry.

Finally, we have studied compositional synthesis and verification techniques. These include modular supervisory control, as well as the verification of component-based systems.

3.1.2.2 Software Synthesis, Code Generation and Timing Analysis

Software Synthesis and Code Generation

We developed research in the following directions:

- We studied the influence of scratchpad memory allocation techniques on worst case execution times (WCET). We developed integer linear programming models to decide which parts of a program's code or data can be moved onto the highly predictable scratchpad. First experiments show WCET reductions of more than 50% for several benchmarks.
  We also investigated WCET-aware register allocation techniques, by extending existing techniques based on graph colouring.

- We continued work on scalable source-level analysis and annotation-based timing analysis methods. The SATIrE infrastructure allows building analysers that take source code annotations as additional input, and generate output as annotations. This allows a significant increase in productivity, by requiring the user to annotate the relevant timing information that cannot be automatically computed. The integration of PAG was instrumental in investigating the scalability of analyses.

- We studied polyhedral loop parallelisation techniques for multi-core systems.

Regarding tools and platforms, we developed work in the following directions:

- We designed a Static Loop Analyzer, allowing to estimate loop iteration bounds. This information is essential for a large number program analyses. Our analyser improves analysis techniques based on conventional abstract interpretation by integrating a new static polytope-based loop evaluation method.
  We have demonstrated the applicability of the analyser on benchmarks taken from the benchmark suites MRTC, DSPStone, MiBench, UTDSP and MediaBench. Our loop analyser was the only tool able to answer all questions related to flow fact during the WCET tool challenge 2008.

- In continuation of work performed in Year 3, we developed a new WCET-aware procedure positioning and cloning technique. The compiler optimisations obtained were exploited for WCET reduction. Results on real-world benchmarks show WCET reductions of 10% on average, while ACET is reduced by 2 on average.

The cooperation between ACE and Aachen on the retargetable code optimizations has been continued. The conditional execution engines have been extended by a strong retargeting formalism.

Timing Analysis

In addition to experimental work, we developed important results on Timing Analysis.

We have studied a notion of time predictability of cache architectures, which is the first precise notion found in the literature. Four different cache replacement strategies were compared and the LRU strategy was found to be optimal. This research is related to work within the PREDATOR FP7 project, which attempts to reconcile performance and predictability.

The study of Timing anomalies, where local worst-case choices may not lead to the global worst-case scenario, is essential for time predictability. We have studied techniques for handling timing anomalies for efficient WCET analysis, as well as for measuring the impact of timing anomalies on WCET analysis.

Other work on Timing Analysis includes parametric Timing Analysis, where some parameters of the program can remain unknown until execution. We also developed Timing Analysis techniques, in collaboration with BOSCH, taking into account operating modes of programs, computed semi-automatically. Finally, we developed WCET analysis for systems with preemptive scheduling.

Work on the AIR format has continued. The format was extended and adapted to the needs of the partners. The attribute database was extended with new attributes.

We also worked on the development and improvement of formats for ensuring the interoperability of the tools. The work on formats includes ALF for computation semantics representation, conversion of the ABSINT AIR format to SWEET format, and the definition of common flow description attributes.

As was the case last year, the WCET Challenge 2008 consisted of a set of benchmark programs and analysis tasks to be performed by the contestants.
http://www.artist-embedded.org/artist/-WCET-08-.html

3.1.2.3 Operating Systems and Networks

Resource-aware Operating Systems

In addition to work done in Artist2, we developed work in the following directions:

- Modeling and analysis of control-driven tasks. The standard design of control is based on the periodic sampling. We studied a model which saves a considerable amount of computational resources which samples the inputs when needed.
- Implementation of a flexible scheduling framework called FRSH that is capable of handling multiple concurrent activites with different criticality and timing in the same system. The framework has been designed to be implemented on different platforms.
- ERIKA support for the EasyBee radio transceiver has been developed.
- We studied issues relating to the operating system support needed by advanced users of a real-time specification for Java. In particular, two issues have been addresses: how to handle systems that contain a large number of events; and how to measure blocking time.

Scheduling and Resource Management

We have had a large volume of activity on this topic:

- All the partners, under the leadership of York, have worked for establishing a taxonomy of resource usage. The taxonomy distinguishes between different classes of resources - each class being subdivided into a number of resource types.
- The architectural model of a Flexible Scheduling Framework developed in the FRESCOR and FIRST EU-IST projects has been extended to include a contract model. Contracts represent complex requirements of the applications which can be managed by the underlying system to provide the required level of service.
- Several activities on scheduling, in particular multi-resource scheduling for multi-core platforms, schedulability for CAN-based control applications, sensitivity analysis, flexible scheduling on low-cost microcontrollers.
- Other work related to the Transversal Activity: “Design for Adaptivity” has been carried out, including dynamic runtime adaptability, optimal period selection and scheduling for embedded controllers.

Real-Time Networks

We have carried out work on:

- Analysis techniques, including Worst Case analysis and dimensioning of cluster-tree Wireless Sensor Networks, as well as analysis for specific networks.
- We studied techniques for supporting real-time communication and QoS for Wireless Sensor Networks. These include work around the use of IEEE 802.15.4 and ZigBee as federating communication protocols for Wireless Sensor Network applications, as well as supporting real-time communication of the Erika real-time operating system.
- We have also furthered work, started in Artist2, on student design competitions in the scope of the IEEE Real Time Systems symposium.

3.1.2.4 Hardware Platform and MPSoC Design

Platform and MPSoC Design

The work has included:

- Study of system design methodologies handling the dynamic nature of embedded systems and allowing predictability and optimal use of resources.
  Bologna, with ETHZ, has studied optimalisation-centric MPSoC design techniques. The main goal of this work was to establish a common understanding of the MPARM framework developed in Bologna, and the DOL framework developed at ETHZ.
  Bologna and Linkoping have studied a temperature power-optimization system. A temperature-aware dynamic voltage selection technique has been developed for energy minimisation.
  Other work on design optimization for fault-tolerant distributed embedded systems is developed by Linkoping and DTU.

- Bologna and ETHZ have improved the design of a scavenger prototype, to perform automatic maximum power point tracking. They developed a compact model for small solar modules that accurately describes their behaviour over a wide range of irradiance conditions. Furthermore, they improved the efficiency of the DC-CD converter at the solar harvester.
- We (DTU) have studied programming models for MPSoC architectures as well as investigated the hardware/software interface between the processing elements and the interconnect network. We also have studied a component-based service model for early design space exploration and performance estimation.

Platform and MPSoC Analysis

Work on analysis complete the design techniques above, with simulation, and performance analysis techniques:

- We studied techniques for performance estimation of distributed real-time systems, based on simulation, in particular for applications using heterogeneous task scheduling policies. We also studied performance analysis techniques for a MPSoC in collaboration with ST Microelectronics.
- An important work direction is modelling and performance analysis for multi-processor and/or networked systems.

  We studied relations between simulation-based and analytical methods for performance evaluation of distributed real-time systems. Based on experimental simulation results, we were able to draw interesting conclusions regarding the pessimism of formal approaches. The experiments were performed on FlexRay and CAN-based distributed systems.

  We also studied interesting relations between MPA (Modular Performance Analysis) and Timed Automata.
- We have extended the fault-tolerant process model, to consider a combination of hardware and software fault-tolerant techniques. We have proposed a method for computing the reliability of a system, taking into account: a) hardening levels in hardware; b) the re-execution levels in software; c) scheduling for sharing recovery slacks.
- We have worked on modelling and optimisation of a miniaturized solar energy harvester. We focused on the optimisation of two important metrics: a) maximisation of the energy harvesting efficiency and b) the minimisation of the energy used for ineffective operations. A hierarchical control solution has been designed which overcomes several drawbacks of previously proposed approaches. A novel algorithm for approximate multi-parametric linear programming has also been proposed.
- We studied scheduling-based energy optimisation techniques for energy-scavenging wireless sensor networks.

3.1.2.5 Design for Adaptivitty (Transversal Integration activity)

We have worked mainly in two complementary directions: a) Study of architectures and algorithms for ensuring adaptivity; b) Study of modelling and analysis techniques for adaptive systems:

- We studied a symbolic quality control technique for multi-media applications. Adaptivity is ensured by using a controller, which moniotors system execution and adapts quality parameters of its functions so as to meet hard real-time contraints.
- We studied adaptive energy management techniques in clusters of wireless sensor nodes. They allow tuning the application parameters according to the time-varying amount of harvested energy.
- We studied a reference architecture for self-configuring embedded systems in collaboration with Volvo. Algorithms suitable for runtime configuration management, load balancing, and quality of service have been developed and adapted to automotive applications.
- We designed adaptive techniques to enhance real-time support of IEEE 802.11.e networks. For such networks, we developed protocols to enhance the resilience to interference, and to provide an estimation of a relative localisation based on the radio frequency signal.
- We studied techniques allowing the design and performance analysis for multi-mode systems. We also studied online performance analysis techniques for distributed systems. A novel distributed algorithm for control of the global analysis flow has been proposed.
- Several partners have collaborated in the STREP projects FRESCOR and ACTORS to develop an infrastructure for adaptive scheduling of real-time applications.

3.1.2.6 Design for Predictability (Transversal Integration activity)

The technical work on Predictability has intersected work in all the Thematic Clusters.

Modeling and Validation of component –based systems

- We studied the concept of predictability in relation with robustness, and identified two major challenges in embedded systems design. These challenges require a rethinking of the conventional, purely discrete and purely functional foundation of computing.
- We worked on modular performance analysis techniques, based on real-time calculus for systems with cyclic dependencies. We integrated a contract-based scheduling framework with a component-based technology.

Timing Analysis and Compiler Techniques

- The main contribution is work on relations between Timing Analysis and Timing Predictability. A definition of predictability for cache architectures has been proposed, and the relative competitiveness of 4 different cache replacement strategies has been analysed.
- We also investigated WCET analysis techniques for cooperative task scheduling. A method guiding developers of an embedded system to select optimal pre-emption points is under development.
- We also studied parameteric timing analysis techniques that overcome usual limitations of analysis techniques requiring the maximum number of loop iterations to be known statically.

OS/MW/Networks

Our work addressed various issues, including: Integrating scheduling analysis and model checking; influence of abstractions on the schedulability analysis of distributed real-time systems, time-predictable operating systems.

Architecture and System Design

- We studied techniques allowed predictability for fault-tolerant embedded systems and predictability for multi-processor MPSoC architectures.
- We also developed a set of parametyerisable models of L2 Caches and integrated them in an accurate virtual platform environment.
- Finally, we are designing a Precision Timed (PRET) architecture based on a reactive processor, coupled with a MicroBlaze general purpose processor.

3.1.2.7 Industrial Integration (Transversal Integration activity)

This activity groups a set of industrial interactions and collaborations with ArtistDesign teams. The long-term goal is to understand industrial design methodologies and identify the research results that could be applied in these methodologies.

The work this year has consisted in organising a few high-profile meetings with industry (eg: Embedded Systems: Industrial Applications ’08) as well as joint workshops and technical meetings.

At this point, these constitute a rich set of events and interactions, which need to be structured and which need a more specific focus.

3.2 Joint Programme of Integration Activities (JPIA)

3.2.1 Structure of the Integration Effort

The JPIA activities promote integration of geographically dispersed teamsand have long-lasting effects:

Joint Technical Meetings. Joint Technical meetings aim to present, discuss and integrate the ongoing work, and exchange points of view with other teams. They also serve to identify future work directions.

Staff Mobility and Exchanges. This is essential for integration within the NoE, including mobility of students and/or researchers, between core teams, or between core teams and affiliated teams. Mobility is justified by and refers to involvement in an activity from the JPRA or JPIA, or one of the following: co-funded scholarships with industry; exchange of students and personnel within the consortium.

Tools and Platforms. A research platform is composed of competencies, resources, and tools targeting specific technical and scientific objectives around a chosen topic. These are at the state-of-the-art, and are made available to the R&D community for experimentation, demonstration, evaluation, and teaching.

The research platforms, tools and facilities are an essential tool for implementing the JPIA. They will lay the groundwork for the JPRA, allowing common research to occur and capitalisation on research results. Platforms are used as the basis for transfer of research results to industry. They allow teaching practical knowledge of the concepts and techniques.

ArtistDesign platforms are not defined from scratch – they integrate the results of long-term efforts, and are meant to be durable, evolving with the state of the art. The partners are committed to durability, and have invested significant resources into their development. The construction of ArtistDesign has provided the opportunity to assemble existing pieces into a rationally-structured set of platforms, covering the area of embedded systems design.

Some of the ArtistDesign platforms have international visibility, and the ambition is for these to serve as world-wide references in their respective topics.

The detailed information regarding the JPIA activities is available in the JPIA deliverable.

3.2.2 Assessment

The ArtistDesign Network of Excellence is a significant evolutionary step for integrating the leading embedded systems design research teams in Europe. The clusters are more tightly woven together, and each represents a significantly greater critical mass than did the clusters in the Artist2 Network of Excellence, which ended Sept 30th 2008, and has nearly the same consortium.

Despite this strong overlap with the Artist2 NoE, the overall assessment for the WP at the end of ArtistDesign Y1 (Jan–Dec 2008) is positive - both in terms of impact on the overall structuring and lasting integration within the consortium and more generally within the area in Europe.

- The ArtistDesign clusters have been actively pursuing operational integration through joint meetings, staff mobility, and shared platforms and tools.
- The level of activity shows that the Cluster / Activity structure and research topics defined for ArtistDesign make sense, and are viable vehicles for integrating the area. In operational terms, they generate sufficient interest for the partners and individual researchers to participate actively in the joint meetings, to exchange personnel, and to orient the tools and platforms developed to make sense within this structure.
- There is clearly a greater level of maturity for tools and platforms than had been the case at the start of the Artist2 NoE – and the partner teams are actively pursuing a policy of implementing tools, demontrators, and in many cases their accompanying methodologies.
- Nonetheless, it is important to remember that these are tools and platforms for research. The aim is not necessarily always for these to lead to commercially viable tools and start-up companies. In general, they are the concrete realisation of the state-of-the-research, allowing to explore possibilities for future research and later tools (some of which may in turn lead to commercially viable products).
- The level of activity varies according to individual clusters / activities, which is normal. We believe this is partly due to the remaining overlap with Artist2 – which should no longer be the case in Y2.

3.3 Jointly-executed Programme of Activities for Spreading Excellence *(JPASE)*

ArtistDesign leverages on the worldwide visibility of the ARTIST2 NoE. It is progressively creating a European embedded systems design community and spreading the "Artist culture" in all major research institutions.

To ensure that the next generation of researchers will continue in this direction we, as a consortium, devote a great deal of effort to Spreading Excellence, in both academic and industrial circles. Furthermore, through our links with both core and affiliated partners, we actively set up permanent links between industry and public research, based on existing partner collaborations with major industrial players in the area.

The JPASE activities are intended to spread excellence and structure the community at large. They are planned by the Strategic Management Board, and are implemented by ArtistDesign core and affiliated partners.

The NoE will leverage on its members and teams, who play a main role in the organisation of world-class scientific events, to disseminate results in the area. We expect that the NoE's structured and authoritative dissemination will have a strong effect on the community as a whole, for orienting and creating synergy for research.

3.3.1 Education and Training

- Courseware – The NoE has the ambition to serve as a resource and point of reference for the area, including by collecting and disseminating course materials for teaching embedded systems design.
- Graduate Studies – The NoE will provide support for selected graduate studies programmes, as the means for training engineers and researchers in embedded systems design.
- Summer Schools – The NoE will actively support and participate in summer schools and seminars in embedded systems design.
- International Workshop on Embedded Systems Education – We will continue this series of international workshops, started in ARTIST2. York has accepted to lead this activity.
- Implement a high-visibility International Summer School. The ArtistDesign NoE will organise each year a high-visibility international Summer School, drawing top European lecturers in Embedded Systems Design. The audience is researchers, PhD students, and engineers. The following group of core partners will lead this activity: Luca Benini (Bologna), Giorgio Buttazzo (SSSA-Pisa), Petru Eles (Linkoping), Kim Larsen (Aalborg), Peter Marwedel (Dortmund).
- Training Engineers – Many partners are already active in this area, such as IMEC, EPFL, ESI, and Aalborg's CSI. The ArtistDesign NoE will provide logistical, financial dissemination through the Web Portal and newsletter.

3.3.2 Publications in Conferences and Journals

The ArtistDesign consortium is very active in publishing in scientific journals and conferences, as attested by the list of significant publications by the partners' teams.

The NoE leverages on its members and teams, who are strongly implicated in collaboration with industry, to organize and structure industrial relations, and develop mutually beneficial

interactions. Furthermore, through Industrial Liaison, ArtistDesign receives useful feedback about the relevance of work directions and priorities.

3.3.3 Links to Artemisia

ArtistDesign seeks a tight interaction with the Artemis community, through the **Artemisia Liaison Task Force**. This is composed of the following prominent ArtistDesign members, also active in ARTEMIS/ARTEMISIA: Luca Benini, Ed Brinksma, Werner Damm, Jean-Luc Dormoy, Rudy Lauwereins, and Joseph Sifakis. Amongst these, 3 are elected members of the ARTEMIS Steering Board. Joseph Sifakis is the chair of ARTEMISIA's Chamber B.

ArtistDesign partners will be encouraged to join ARTEMISIA.

3.3.4 International Collaboration

The ArtistDesign "*International Collaboration*" activities allow ArtistDesign to be visible internationally, and to monitor the evolution of the state of the art in the area worldwide.

International Collaboration fits into a global win-win strategy for achieving the participants' long-range aims. Examples of activities include:

- **High-level meetings** gathering top representatives from industry, funding agencies, and research, to discuss avenues for International Collaboration, including on R&D and standards e.g. IST/NSF Workshop on Component-based Engineering (Paris, June 05).
- International Collaboration **Working Groups** for exploring possible avenues for research and education in a chosen topic and producing white papers and reports e.g. joint EU/US Working Groups: on Timing Validation, Adaptive Real-Time Systems for Dynamic Applications, Semantic Platform for Hard Real Time (2002 – 2003).
- Organization and sponsoring of international conferences and schools, to disseminate recent research results, and promote the emergence of embedded systems as a discipline e.g. Embedded Systems Week, New Jersey, October 2005.
- International Collaboration **Publications**.
- **Joint international projects**. Set up joint collaborative projects e.g. Columbus project or extend existing projects, by allotting them an extra budget.

International Collaborations is implemented mainly in collaboration with the USA, building on existing links between IST and the US funding agencies (mainly NSF).

ArtistDesign leverages on and extend the successful International Collaboration activities initiated in the ARTIST2 NoE.

3.3.5 Web Portal

The ArtistDesign Web Portal is a major tool for Spreading Excellence within the Embedded Systems Community. It aims to be the focal point of reference for events and announcements of interest to the embedded systems community.

This will play a key supporting role for collaboration and Integration, such as interaction between clusters, management information, such as scholarships, internal events, and progress of the work. The web portal will also be used to disseminate any relevant information to the community at large. We believe the web portal will be an essential mechanism for achieving integration.

It acts as a repository of knowledge in the area, including courseware, information about standards, methods and tools, research publications and results. This web portal will be made available within the NoE core and affiliated partners, and to other parties.

This repository is to be the reference for the embedded systems design community. It builds on the existing ARTIST2 Portal, which includes several features that help keep it coherent and up to date:

- Authorised users (principally, the ARTIST2 partners) can access the back end of the site to modify and update information directly. The changes are immediately visible on the site, which greatly streamlines the updating process.
- It's possible to track changes and go back to previous versions of individual web pages.
- Events are automatically sorted by date, and transferred to 'Past Events'. When appropriate.
- Structural information (hierarchy of pages) is maintained automatically.
- Ergonomics are set for the entire site. The "look and feel" of the site is always homogeneous throughout the site. It's possible to change these ergonomics, and these changes are applied homogeneously throughout the site, via automated mechanisms.

The ArtistDesign Web Portal offers information about:

- **Workshops, Conferences, Schools and Seminars**
  Provide information about the main scientific events in the area, and in particular those organised by ArtistDesign.
- **International Collaboration**
  Advertise the ArtistDesign International Collaboration events, and provide pointers to the most visible International Projects (either about significant projects outside Europe, or joint International Collaboration projects.
- **Publications**
  Publications from core partners, with emphasis on Position Papers, White Papers, etc. that may have a particularly deep impact.
- **Course Materials Available Online**
  The web portal will centralize course materials from as many sources as possible, to make them available to the general public.

3.4 Managing the Network of Excellence (JPMA)

We believe that the current two-tiered Management structure - dividing the management amongst cluster leaders and the Strategic Management Board composed of both cluster leaders and a limited number of other selected prominent core partners – has been the right one for managing such a large research entity. It has provided the right combination of flexibility and accountability, while leaving room for innovation and evolution.

This management structure is reproduced with adaptations in the ArtistDesign NoE. The adaptations reflect the greater cohesion between partners, and move to capitalize on and strengthen the integration achieved in Artist2.

4. End Results

We are achieving a significantly more integrated scientific community. Initially, there was a strong fragmentation by topics and communities, with little interaction between them. Over the course of the NoE, the clusters have evolved and merged. A gradually cohesion has taken

place, through transversal “NoE Integration” activities, and more importantly through strategic alliances.

We are seeing a convergence of interests, and the gradual emergence of recognized leaders.

214373 ArtistDesign
Network of Excellence
on Embedded Systems Design

Periodic Activity Report for Year 1

Joseph Sifakis – ArtistDesign Scientific Coordinator
Bruno Bouyssounouse – ArtistDesign Technical Coordinator

ArtistDesign Consortium

Table of Contents

1. Overview

1.1 Project Objectives and Major Achievements

A detailed description of objectives, and particularly the main aims for integration, is provided for each cluster in the sections labelled « State of Integration in Europe ».

1.1.1 Historical Perspective: Artist FP5, then Artist2 in FP6

Within IST FP5, a subset of the current consortium implemented an Accompanying Measure, whose objectives were to:

- Coordinate the R&D effort in the area of Advanced Real-time Systems
- Improve awareness of academics and industry in the area
- Define innovative and relevant work directions

This was achieved through work along 3 axes:

- Roadmaps for selected actions: (Hard Real Time, Component-based Design, Adaptive Real Time, Execution Platforms)
- International Collaboration
- Education

Information about these results is publicly available:

http://www.artist-embedded.org/Roadmaps/

Within IST FP6, a consortium very similar to the current one implemented the highly successful ARTIST2 NoE. The main changes between Artist2 and ArtistDesign are :

- An evolution of the clusters to reflect the ongoing integration.
  There are now 4 clusters instead of 6, and they are significantly larger.
- Reinforced role of the Transversal Activities (called NoE Integration activities in Artist2). In ArtistDesign these now have nearly the same role and autonmy as did the clusters in Artist2.
- Tighter consortium. The number of partners in the consortium has been reduced by approximately 25%. The “departing” partners continue interaction with the NoE, as Affiliated Partners. This allows them to participate in the technical meetings and occasionally claim some costs for travel, but none for manpower.
- Tools and procedures continue to evolve. The tools (eg web) and procedures developed within Artist2 contionue to evolve within ArtistDesign.
- Change of Coordinator. The Financial and Legal Issues handled by the CDC in Artist2 are now handled by Floralis in ArtistDesign.

1.2 Workpackage progress of the period

Given the size of this NoE, and the structuring by clusters, this information is provided in detail in separate physical sections of this document (chapters 2-5 of the Project Activity Report).

1.3 Deliverables for the Reporting Period

WP0: Joint Programme of Management Activities (JPMA)

Floralis	D1-(0.1)-Y1	**Project Management Report**
	D2-(0.2)-Y1	Project Activity Report
UJF/Verimag	D2-(0.2a)-Y1	*ch. 1* - **Executive Summary and Overview**
Aalborg	D2-(0.2b)-Y1	*ch. 2* - **Modelling and Validation**
Dortmund	D2-(0.2c)-Y1	*ch. 3* - **SW Synthesis, Code Generation and Timing Analysis**
Pisa	D2-(0.2d)-Y1	*ch. 4* - **Operating Systems and Networks**
DTU	D2-(0.2e)-Y1	*ch. 5* - **Hardware Platforms and MPSoC Design**

WP1: Joint Programme of Integration Activities (JPIA)

UJF/Verimag	D3-(1.0)-Y1	**Integration Activities Report**

WP2: Joint Programme of Activities for Spreading Excellence (JPASE)

UJF/Verimag	D4-(2.0)-Y1	**Spreading Excellence Report**

WP3: Modeling and Validation (JPRA)

EPFL	D5-(3.1)-Y1	**Modelling**
Aalborg	D6-(3.2)-Y1	**Validation**

WP4: Software Synthesis, Code Generation and Timing Analysis (JPRA)

Dortmund	D7-(4.1)-Y1	**Software Synthesis, Code Generation**
Saarland	D8-(4.2)-Y1	**Timing Analysis**

WP5: Operating Systems and Networks (JPRA)

Pisa	D9-(5.1)-Y1	**Resource-aware Operating Systems**
York	D10-(5.2)-Y1	**Scheduling and Resource Management**
Aveiro	D11-(5.3)-Y1	**Embedded Real-Time Networking**

WP6: Hardware Platforms and MPSoC (JPRA)

Bologna	D12-(6.1)-Y1	**Platform and MPSoC Design**
DTU	D13-(6.2)-Y1	**Platform and MPSoC Analysis**

WP7: Transversal Integration (JPRA)

Lund	D14-(7.1)-Y1	**Design for Adaptivity**
Uppsala	D15-(7.2)-Y1	**Design for Predictability**
PARADES	D16-(7.3)-Y1	**Integration Driven by Industrial Applications**

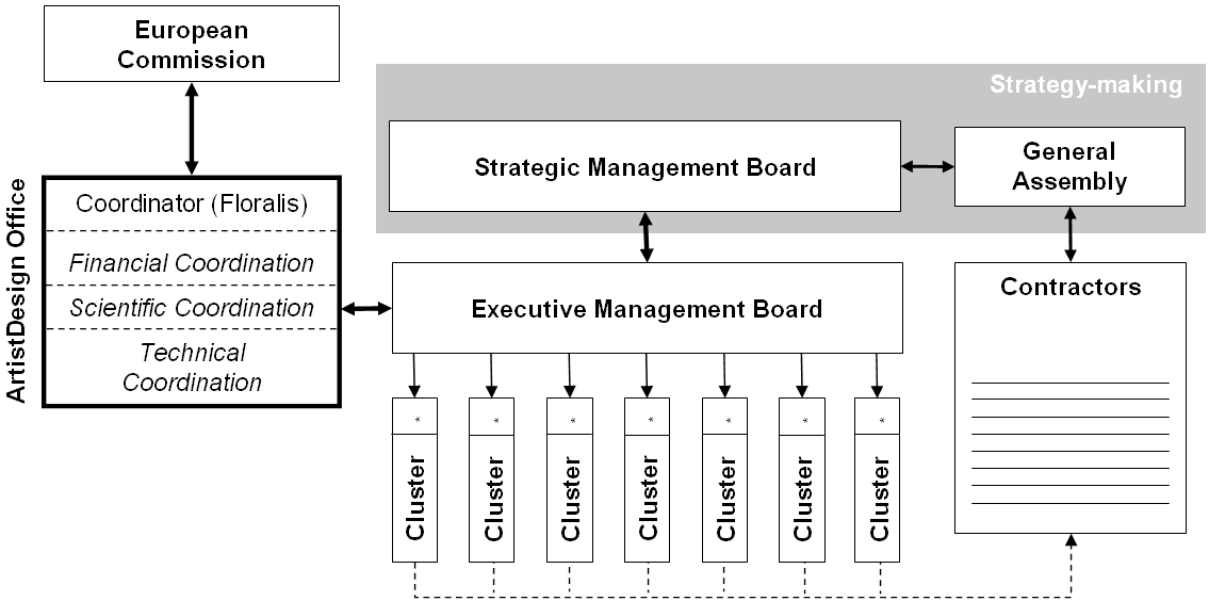
1.4 Consortium Management

This is unchanged from Artist2.

1.4.1 Governance Structure

Scientific Coordinator: Joseph Sifakis Tel: +33 4 56 52 03 51 Joseph.Sifakis@imag.fr	Technical Coordinator: Bruno Bouyssounouse Tel: +33 4 56 52 03 68 Bruno.Bouyssounouse@imag.fr
Mailing address: Verimag Laboratory - Centre Equation - 2, ave de Vignate - 38610 Gières - France	

The methodology adopted for achieving the JPA objectives follows the same lines as for managing a laboratory. The activities, their objectives, their technical description, the partners involved, their roles, and the resources available have been clearly defined in the initial Description of Work, and updated in the deliverables. This will be monitored and guided by a tight and rigorous management, as defined in the diagram below:



The main governance bodies are:

The **General Assembly** is composed of one representative per core partner. It is convened at the beginning of the project and meets once per year. It is chaired by the Scientific Manager.

The **Strategic Management Board** is initially composed of the NoE cluster leaders, and a representative of the Coordinator – who attends, with no voting rights. It is chaired by the Scientific Manager, assisted by the Technical Manager. It meets at least once per year – close to the General Assembly meeting. Its members are elected by the General Assembly every two years, according to modalities to be determined in the Consortium Agreement.

The **Cluster Leaders** (who compose the Executive Management Board) are responsible for the overall coordination of the activities led by their cluster. A cluster functions as a virtual team – with a degree of autonomy for defining its internal meetings and day to day management.

1.4.2 Partners Involved

This is provided in the publishable Executive Summary, in the first part of this document.

1.4.3 Contractors

There are no changes to the consortium at the end of Year 1.

1.4.4 Project Timetable

The JPA is organized into activities. The activities should not be considered as tasks of a workprogramme, with begin/end and synchronisation dependencies. Of course, the detailed description of an activity could be decomposed into sub-tasks and intermediate milestones, but this would imply a granularity that is too fine for research activities.

1.4.5 Other Issues

None

1.4.6 Plan for using and disseminating the knowledge

The main instruments for using and disseminating knowledge are:

- Workshops and Schools organised.
  The list is quite impressive, and is provided in the deliverable on “Spreading Excellence”.
- ArtistDesign Web Portal.
  Here also, the quantity of information made available to the greater embedded systems community is quite impressive, and continuously growing. This is possible through the efforts of the entire consortium, who now have direct access for updating the contents.
- Course Materials.
  There is a growing body of course materials made available via the Artist2 web portal.
- Publications.
  The ArtistDesign consortium is very prolific in publishing research articles, surveys, textbooks, roadmaps, and position papers.

1.5 Metrics

It should be noted that these metrics are imperfectly measured, relying on voluntary feedback from partners.

1.5.1 Excellence Indicators

Indicator	number	*Method used*
Number of publications (journals, proceedings, etc) by ARTIST Partners in Embedded System Design over Year 1	668	*from partners, (web form)*
Number of course books published by ArtistDesign Partners in the area in Year 1.	20	*from partners, (web form)*
Number of public keynotes, conferences, seminars and workshop in the area by ArtistDesign partners in Year 1. *NB: Due to differing definitions and data collection methods from one partner to the next, it should be noted that this figure is probably not very reliable.*	178	*From JPASE deliverable, section 5*
Number of white papers published in the area by ArtistDesign Partners in Year 1.	31	*from partners, (web form)*

1.5.2 Integration indicators

Indicator	number	*Method used*
Number of EC-funded projects in embedded systems, involving two or more ArtistDesign partners over Year 1 *NB: Due to differing definitions and data collection methods from one partner to the next, it should be noted that this figure is probably not very reliable.*	32	*from partners, (web form)*
[ICT-2007.1.2] IRMOS; [IST FP6] ACTORS (2008-2011), [ST] WASP (2008-2011), [FP6] HYCON NoE, [FP6] PREDATOR, [FP6] RIMACS, [FP7] COMBEST (2007-2010), [FP7] Speeds (2006/2009), [FP6] WASP (2006-2010), [FP6]FRESCOR (May 2006 May 2009), [FP7] MNENEE (2007-2010), [IST] ASSERT (2004-2007), [IST] MORE (2006-2009), [ITEA]ES_PASS (2007-2009), [ITEA2] TECOM (2007/2010), [NABIIT] MoDES (2006-2009), [VTU] D-ARTEMIS (2007-2009), ALL-TIMES 2008-2009, EU FP7 CONET (2008/2011), EU MORE 6/2006-5/2009, FP6 HiPEAC (2004-2008), FP7 HiPEAC (2008 – 2011), FP6 SHAPES (2006-2009), FRESCOR (2007-2010), [IST-FP7] Genesys FP7 18 months, [IST] ATESST, 04/01/2006 => 03/31/2008, KKS WCET 2006-2008, Quasimodo (Jan 2008-Dec2010), SPEEDS, Verisoft (03-10), VINNOVA FISS2 May 2007 - Dec 2009;; [FP7] FEEEDNETBACK; FP7 INTERESTED		

Number of other source funded projects in embedded system design, implying two or more ArtistDesign partners in year 1. *NB: Due to differing definitions and data collection methods from one partner to the next, it should be noted that this figure is probably not very reliable.*	18	*from partners, (web form)*
[CH] FIRE, [CH] MICS, [CH] PerformanceEvaluation, [ESA] Prototype Execution Time Analyzer for SPARC (Sept 2006/Feb 2007), [HTF] DaNES (2007-2010), [NABIIT] MoDES (2006-2009), [Spain PN] THREAD (2005-2008), [Spanish Government]THREAD (05/08), [Spanish project]THREAD (Jan 2005, Dec 2008) [Swedish Foundation for Strategic Research] SAVE(2003-2008), [US DARPA and Industry]: GSRC, [US NSF] CHESS, [VTU] D-ARTEMIS (2007-2009), ALL-TIMES 2008-2009, KKS WCET 2006-2008, SuReal (German BMBF, 2006-2008), Verisoft (03-10), VINNOVA FISS2 May 2007 - Dec 2009; EUROSYSLIB (Summer2007 - Dec2009)		
Number of PhD visiting other partners in the network in year 1	68	*from partners, (web form)*
Number of joint PhDs over year 1	34	*from partners, (web form)*
Number of visits between teams over year 1	48	*from partners, (web form)*
Number of public conferences, special sessions and workshop organised by ARTIST in year 1.	26	*from website*
Number of jointly published papers from two or more partners from ArtistDesign in year 1. *NB: Due to differing definitions and data collection methods from one partner to the next, it should be noted that this figure is probably not very reliable.*	156	*From JPASE deliverable section 9*
Number of research platforms or facilities shared for research	27	*JPIA*

1.5.3 Indicators about Spreading Excellence

Indicator	**number**	***Method used***
Large Summer Schools organised and funded by ARTIST in year 1.	3	*from website,*
Smaller Summer Schools organised and funded by ARTIST in year 1.	3	*from website,*

Other Summer Schools with ArtistDesign funding or participation in Year 1.	1	*from website*
Education: International seminars / training sessions organised specifically on Education WESE'08: WS on Embedded Systems Education *October 23rd, 2008 Atlanta, Georgia - USA (within ESWEEK)*	1	
Other international seminars / training sessions organised:	180	*from JPASE deliverable, section 5*
Number of papers published in top international journals and conferences	*Very large. This is very difficult to measure with any meaningful degree of accuracy.*	
Number of hits on the ARTIST2 web portal	2759886	*from JPASE deliverable, section 6*
International collaboration : nb of projects defined at the events	*This is impossible to measure.*	
Number of external links referring to ARTIST2 web portal	161	
Obtained from google, by searching for: `link:www.artist-embedded.org`		

1.5.4 Indicators on the financial independence from EC funding and from other sources

Indicator	**number**	***Method used***
Number of affiliated industrial partners	22	*from website*
Number of spinoff companies created	12	*from partners, (web form)*
Percentage of the ARTIST2 funding, respective to the partners' overall operating budget	*This is absolutely impossible to measure any meaningful way.*	
Number of affiliated partners willing to pay for membership in ARTIST2 *This would depend on the cost of membership, and the benefits they would get. Part of the benefits is the "seal of approval" involved in obtaining EC funding.*		
Overall revenue from membership dues from affiliated partners. *See previous question.*		

1.5.5 Indicators for Integrating the Gender Dimension

Indicator	**number**
Number of women currently active in the NoE	4
Number of women initially active in the NoE	1
Promotion of women in the area	No statistics

IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Cluster - Progress Report for Year 1

Cluster:
Modeling and Validation

Cluster Leader:

Professor Kim G. Larsen (CISS, Aalborg University)

http://www.cs.aau.dk/~kgl

Policy Objective (abstract)
The sheer complexity of future embedded devices seriously challenges current development practice; new, integrated and scalable methods are urgently needed. The use of *modeldriven* and *component-based* approaches are seen as a way of obtaining dependable embedded implementations with high performance and with reduced time and cost. Embedded systems involve monitoring and control of complex physical objects or phenomena using a number of dedicated hardware and software components often within a networked solution.

Therefore, an objective of the cluster is to advance the utilizagion of *models, analysis techniques* and *supporting tools* spanning the areas of control theory, computer science, hardware, networks and even mechatronic all well established research areas which however – by and large – have been developed independently.

Versions

number	comment	date
1.0	First version delivered to the reviewers erroneous version	December 19th 2008
1.1	Second (correct) version delivered	January 20th 2009

Table of Contents

1. Overview

In this section we give an overview of the current situation for the cluster's research area in terms of overall objectives and trends.

1.1 High-Level Objectives

The sheer complexity of future embedded devices seriously challenges current development practice; new, integrated and scalable methods are urgently needed. The use of *modeldriven* and *component-based* approaches are seen as a way of obtaining dependable embedded implementations with high performance and with reduced time and cost. Embedded systems involve monitoring and control of complex physical objects or phenomena using a number of dedicated hardware and software components often within a networked solution. Therefore, the use of models, analysis techniques and supporting tools span the areas of control theory, computer science, hardware, networks and even mechatronic all well established research areas which however – by and large – have been developed independently. This has the unfortunate consequence that it often becomes impossible to state, not to mention validate, overall properties of an embedded system.

Overall objectives of the cluster are:

1. Establish a coherent family of modelling formalisms spanning the areas of computer science, control, hardware and networks covering all aspects of embedded systems.
2. Development and combination of efficient means for analysis of models including simulation, testing, static analysis, model-checking, run-time verification, monitoring, diagnosability, controller synthesis.
3. Emphasis on support for compositional methodologies in terms of allowing new complex systems to be assembled from already constructed and validated components.
4. Realization of coherent tool chain obtained by adjusting and combining the models and tools from the different research areas. This will provide the basis for a cost-efficiency development process allowing for early design-space exploration and verification as well as reduce the sizeable amount of final testing-time and –cost.
5. Interaction with the thematic activities in the Transversal Integration workpackage on validating the formalisms and tools through real industrial development projects and case studies.

1.2 Industrial Sectors

The modeling and validation techniques and supporting tools developed and disseminated within the cluster have relevance and potential impact on literally *all* industrial sectors developing or using embedded systems solutions. Within the Strategic Research Agenda of the ARTEMIS research platform[1] *Design Methods and Tools* is one of the three research priorities put forward. Here model- and component-based approaches are proposed as necessary for coping with the growing complexity of systems while meeting "time-to-market" requirements. Methods and tools for testing and verification are to play a central role in the ARTEMIS research strategy, as can be seen from the following citations:

[1] http://www.artemis-office.org/

- ".. methods and tools for simulation, automatic validation and proving, and virtual Verification and Validation (V&V). Methods and tools for developing product lines of embedded systems."
- ".. reduce the cost of the system design by 50%. Matured product family technologies will enable a much higher degree of strategic reuse of all artifacts, while component technology will permit predictable assembly of Embedded Systems."
- ".. achieve 50% reduction in development cycles. Design excellence will aim to reach a goal of "right first time, every time" by 2016, including Validation, Verification and certification (to the same and higher standards as today)."
- "..manage a complexity increase of 100% with 20% effort reduction. The capability to manage uncertainty in the design process and to maintain independent hardware and software upgradeability all along the life cycle will be crucial."
- ".. reduce by 50% the effort and time required for re-validation and recertification after change, so that they are linearly related to the changes in functionality."

The industrial needs for improved tools and methods for system validation have also been witnessed by a number of industrial and industry inspired case-studies and projects using model-based testing and verification carried out by the individual partners. Detailed information of these (and others) is to be found in the ARTIST2 Open Repository for Test and Verification Case Studies (https://bugsy.grid.aau.dk/artist2). Based on the above case-studies, it seems that the actual financial benefits of using a model-driven approach are likely to be even greater than those of the ARTEMIS goals, due to the capabilities of capturing functional as well as non-functional problems early on in the development process.

1.3 Main Research Trends

With respect to modeling and validation of embedded systems the overall trends include the need for dealing with increasingly complex systems with and increasing number of (functional and non-functional) features.

The need for a scientific foundation for embedded systems dealing simulataneously with software, hardware resources and physical environments have received substantial attention during the last year with significant contributions from the partners of the ARTIST Design Modeling and Validation Cluster. Emphasis is on quantitative modeling as well as component-based design methodologiy with the ambition of establishing a coherent family of design flows spanning computer science, control and hardware.

The quantitative and component-based modeling formalism are accompanied with advances in analysis techniques allowing for early exploration and assessment of alternative design solutions as well as validation of final implementations. Efforts in combining techniques ranging from simulation, testing, model-checking, run-time verification, artificial intelligence, compositionality, refinement as well as abstact interpretation are currently pursued.

Also, a number of newly started STREP, IP and ARTEMIS projects are actively pursuing the accessibility of state-of-the art research result on quantitative modeling and validation from industrial too-chains.

2. State of the Integration in Europe

The objective of the Modeling and Validation cluster is to combine the efforts and skills of the individual leading researchers and research groups in Europe into a world-class virtual team, for advancing the state-of-the-art. The partners span the leading research teams in European level and are well connected with leading research teams outside Europe.

2.1 Brief State of the Art

An important class of industrially applied model-based methodologies is those based on a synchronous execution model (e.g. Lustre, Esterel, and Signal). Other model-based approaches are built around a class of popular languages exemplified by Matlab Simulink. Originating from the design automation community, SystemC also chooses synchronous hardware semantics, but allows for the introduction of asynchronous execution and interaction mechanisms from software (C++). More recent modeling languages, such as UML and AADL, attempt to be more generic in their choice of semantics and thus bring extensions in two directions: independence from a particular programming language; and emphasis on system architecture as a means to organize computation, communication, and constraints.

Design often involves the use of multiple models that represent different views of a system at different levels of granularity. Some transformations between models can be automated; at other times, the designer must guide the model construction. While the compilation and code generation for functional requirements is often routine, for non-functional requirements, such as timing, the separation of human-guided design decisions from automatic model transformations is not well understood

By far the most common validation technique applied in embedded industrial today is based on rather ad-hoc and manual (hence quite error-prone) testing. Given that some 30-50% of the overall development time and cost are related to testing activities it is clear that the impact of improved validation technologies is substantial.

Whereas validation techniques for assessing functional correctness have reached a certain level of maturity and industrial acceptance, there is a need for mature validation techniques addressing quantitative being accessible from within industrial tool-chains.

2.2 Main Aims for Integration and Building Excellence through ArtistDesign

The integration of the research groups within the cluster is well established and with significant impact on the larger research community on modeling and validation through strong impact on a number of important international conferences within the area. Also, partners of the cluster – often in collaboration with other clusters – have made significant effort in spreading of excellence beyond the ARTIST2 NoE through PhD schools and industrial seminars. More systematic knowledge transfer to industry through long-term collaboration on industrial development projects has been performed by individual partners. Here the national centers ESI (Embedded Systems Institute, Eindhoven, The Netherlands) and CISS (Center for Embedded Software Systems, Aalborg, Denmark) have specific resources reserved for such activities.

Also at the national level of the various partners in the Testing and Verification cluster involvement in ARTEMIS are planned with the ambition of having an impact on the long-term take-up of testing and verification technology in industrial practice.

2.3 Other Research Teams

During the first year the number of affiliated partners contributing actively to the cluster has been growing significantly as can be seen from the detailed activity reports on Modeling (D5-(3.1)-Y1) and Validation (D6-(3.2)-Y1) in comparison with the original DoW.

Other prominent research groups not being partner of the cluster include a number of teams from United Kingdom, in particular School of Computer Science, Birminghan (probabilistic model checking), Oxford University Computing Laboratory (real-time verification), Microsoft Research Laboratory at Cambridge and Royal Holloway, University of London. From Italy important contributions come from the Automated Verification and Synthesis Group, Trento University (symbolic model-checking, SAT-solving, applications to planning) with support of the nuSMV tool. In all of the above cases individual partnersof the cluster are collaborating with the particular research group.

The partners of the cluster are collaborating extensively with leading research teams outside Europe both on the level of concrete research problems and topics and in terms of organising the testing and verification research community. The cluster has strong links to the work on software verification and testing taking place at Microsoft Research, Redmond, (Ball), NASA Ames and Kestrel Technologies (Holzman, Visser and Havelund) and Kansas (Hatcliff). Extraordinary strong links exist to Cadence (Sangiovanni Vincentelli, director of Cadence and core-partner of ARTIST Design), Rice University, Texas (Vardi, longstanding collaboration with Wolper on the highly appreciated and influential automata theoretic approach). Also ARTIST Design has collaborated with leading research groups and researchers from Israel including Weizmann Institute (Pnueli, Harel), Haifa (Grumberg) and Hebrew University (Kupfermann).

2.4 Interaction of the Cluster with Other Communities

During the first year the methods of the cluster has been successfully applied to the automatic generation of test suites (with guaranteed coverage), and is also increasingly applied successfully within and by other communities including hardware/software co-design, control theory, discrete event systems, fault-tolerance, planning and scheduling and performance evaluation.

Members of the cluster has published and given invited talks at main conferences and in journals of these neighbouring communities.

Similarly leading research groups within AI are finding applications of existing search heuristics from planning to the improved model-checking (e.g. Friburg University, Germany within the AVACS project and Trento University, Italy).

At the *organization* level, members of the cluster have been active in the European ARTEMIS initiative, and are involved in several of the to-be-funded projects from the first ARTEMIS call.

3. Overall Assessment and Vision for the Cluster

3.1 Assessment for Year 1

Both research activities with the cluster – the *Modeling Activity* and the *Validation Activity* – have progressed substantially within the first year, and with significant synergy between modeling formalisms proposed and enabled validation techniques:

With the sub-activities on *Component Modeling* and *Compositional Validation* substantial efforts have been made towards frameworks for modelling composite systems with heterogeneous systems permitting a variety of non-functional aspects. The work includes generic frameworks allowing for contract-based circular reasoning as well as industrial application of component-based methods allowing for compositional safety, robustness and failure analysis. Also, in several cases the work has been motivated and validated by industrial needs.

Within the sub-activity *Resource Modeling (*of the *Modeling Acitivity)* – studied the design of resource-constrained systems, where resource can be quantitative (e.g energy) or not (e.g. shared memory access) and with a number of applications considered. Within the sub-activity *Quantitative Modeling (*of the *Modeling Acitivity)* focus has been on design frameworks for quantitative modeling, mainly timing and resources.

Within the sub-activity *Quantitatvie Validation (*of the *Validation Acitivity)* an array of validation techniques dealing with timing, hybrid behaviour, stochastic aspects as well as recource including energy and memory consumption have been put forward. Still, techniques for simultaneous analysis of multiple quantitative aspects are less developed.

Within the sub-activity *Cross-layer Validation (*of the *Validation Acitivity)* progress on testing real-time and data-intensive systems have been made. Also substantial effort has been made by several partners on controller synthesis of controllers taking partial observability, quantitative aspects (time and probabilites) as well as resource constraints into account. Predicable realisation of synthesized strategies on specific platforms is still to be dealt with.

3.2 Overall Assesment since the start of the ArtistDesign NoE

During the period of ARTIST Design the partners of the Modeling and Validaiton cluster have demonstrated true research excellence as witnessed by the extensive list of publications at leading conferences and journals, numerous invited keynote presentation by members of the cluster as well as the co-hosting of several PhD schools and workshops.

The industrial impact of the cluster has been significant during the period, witnessed by a large number of dissemination activities carried out by the partners. In particular, in several collaborative projects with companies the adaptation of model-driven development has resulted in notable reduced time-to-market.

Within the first year of ARTIST Design the partners have continued their involvement in building the European Embedded Systems community as clearly demonstrated by the high number of joint projects (FP7, ESF as well as national) that have been initiated by members of the cluster.

3.3 Indicators for Integration

Interactions planned between partners include:

- Tool Connection
    - Connections to SPEEDS;
      The HRC component format has been stabalised enabling explotatation in the next years.
    - UPPAAL & RAPTURE & MODEST;
      Partially obtained with the introduction of a branch of UPPAAL supporting Probabilistic Timed Automata. The goal is extended to link to the probabilistic model checkers MRMC and PRISS
    - Metropolis and HDL (Giotto);
      Partially obtained.
    - UPPAAL & IF;
      Not pursued during the first year.
    - ARTS & UPPAAL (from simulation to verification);
      Has been achieved allowing for simulation as well as verification of schedulability propeties of MPSoC to be made. Future effort includes simulation and verification of performance properties (energy and memory consumption).
    - TrueTime.
      Has not been achieved during the first year.
- 10 Joint publications between partners/year
    - *Achieved*
- 2 open workshops / year
    - *Achieved*
- Connections between tools of partners; joint meetings.
    - *Achieved*

3.4 Long-Term Vision

The long-term vision of the cluster is to enable future development of embedded devices to cope with the growing complexity.

In particular, the cluster wants to develop model-driven and component approaches based on riogours modeling formalisms and supporting validation techniques spanning allowing all relevant aspects of embedded systems (hardware, software and physical environment) to be taken into account. Here, a special challenge is to overcome the current weakness of model-driven development methodologies in dealing with physical constraints and quantitative aspects.

This calls for development of efficient means for analysing and validating such designs, as well as realization of coherent tool chains integrating academic efficient tool components into existing industrial tool chains.

4. Work Related to the Joint Programme of Integration Activities (JPIA)

4.1 Joint Technical Meetings

Organization of the workshop, **Veronique Bruyere and Jean-Francois Raskin.** "Automata and Verification", University of Mons-Hainaut, Belgium, August 25-26, 2008.

Summer school: Movep 08: Co-organization of the Movep school (http://www.univ-orleans.fr/movep2008/) about modeling and verifying parallel processes in June 2008, partially funded by Artist 2.

RTSS08 track on Design and Verification of Embedded Real-Time Systems, the 29th IEEE Real-Time Systems Symposium. Barcelona, Spain. November 30 - December 3, 2008. This is one of the four tracks of RTSS 2008.

The objective is to promote research on design and analysis, and verification of embedded real-time systems. It intends to cover the whole spectrum from theoretical results to concrete applications with an emphasis on practical and scalable techniques and tools providing the designers with automated support for obtaining high-quality software and hardware systems. A particular goal is to provide a forum for interaction between different research communities, such as scheduling, hardware/software co-design, and formal techniques. http://www.rtss.org

Workshop : SafeCert 2008, International Workshop on the Certification of Safety-Critical Software Controlled Systems, ETAPS 2008 Budapest, Hungary, 29 March, 2008, organized by TU Braunschweig and OFFIS.

The need for certification, like for instance in the rail sector, imposes the burden of not only validating a system, but also proving in a juridical sense, that the validation can be trusted. The major question addressed in the workshop was how to embed formal methods and tools in a seamless design process which covers several development phases and which includes an efficient construction of a safety case for the product.
http://safecert08.offis.de/

Workshop FIT 2008: Foudnation of Interface Theories ETAPS 2008 Budapest, Hungary, 29 March, 2008, organized by CISS, Aalborg University and ITU, Copenhagen. Invited presentations from INRIA, Rennes, and Twente U.

Component-based design is widely considered as a major approach to developing systems in a time and cost effective way. Central in this approach is the notion of an interface. Interfaces summarize the externally visible properties of a component and are seen as a key to achieving component interoperability and to predict global system behavior based on the component behavior. To capture the intricacy of complex software products, rich interfaces have been proposed. These interfaces do not only specify syntactic properties, such as the signatures of methods and operations, but also take into account behavioral and extra-functional properties, such as quality of service, security and dependability. Rich interfaces have been proposed for describing, e.g., the legal sequences of messages or method calls accepted by components, or the resource and timing constraints in embedded software. The development of a rigorous framework for the specification and analysis of rich interfaces is challenging. The aim of this

workshop is to bring together researchers who are interested in the formal underpinnings of interface technologies.

Workshop: 1st International Workshop on Model Based Architecting and Construction of Embedded Systems
Toulouse -- September 29th, 2008

This ARTIST workshop is held in conjunction with MODELS 2008 as a follow-up workshop of the SVERTS and MARTE workshops organised in previous years, the objective of this workshop is to bring together researchers and practitioners interested in model-based software engineering for real-time embedded systems. We are seeking contributions relating to this subject at different levels, from modelling languages and semantics to concrete application experiments, from model analysis techniques to model-based implementation and deployment. Given the criticality of the application domain, we particularly focus on model-based approaches yielding efficient and provably correct designs. Concerning models and languages, we welcome contributions presenting novel modelling approaches as well as contributions evaluating existing ones. The organisers of this workshop are partners from the ASSERT and SPICES project; the ARTIST partners are CEA and Verimag.
http://www.artist-embedded.org/artist/ACES-MB-08.html

Workshop SLA++P 2008: Model-driven High-level Programming of Embedded Systems European Joint Conference on Theory and Practice of Software ETAPS 2008
Budapest, Hungary – April 5th, 2008

SLA++P is a workshop dedicated to synchronous languages and the model-driven high-level programming of reactive and embedded systems. Firmly grounded in clean mathematical semantics, synchronous languages are receiving increasing attention in industry ever since they emerged in the 80s. Lustre, Esterel, Signal are now widely and successfully used to program real-time and safety critical applications, from nuclear power plant management layer to Airbus air flight control systems. At the same time, model-based programming is making its way in other fields of software engineering, too, often involving cycle-based synchronous paradigms. The purpose of the SLA++P workshop is to bring together researchers and practitioners who work in the field of languages and tools for the model-driven development of embedded applications both in hardware and software. The workshop is not limited to synchronous approaches but open to other engineering design approaches with strong semantical foundations providing a way to go from a high-level description to provable executable code.
http://www.artist-embedded.org/artist/SLA-P-2008,1231.html

Workshop : ACESMB 2008, 1st Int. Workshop on Model Based Architecting and Construction of Embedded Systems
ACM/IEEE 11th Int. Conf. on Model Driven Engineering Languages and Systems
Toulouse, France - September 29th, 2008

New real-time systems have increasingly complex architectures because of the intricacy of the multiple interdependent features they have to manage. They must meet new requirements of reusability, interoperability, flexibility and portability. These new dimensions favour the use of an architecture description language that offers a global vision of the system, and which is particularly suitable for handling real-time characteristics. Due to the even more increased complexity of distributed, real-time and embedded systems (DRE), the need for a model-driven approach is more obvious in this domain than in monolithic RT systems. The purpose of this

workshop is to provide an opportunity to gather researchers and industrial practitioners to survey existing efforts related to behaviour modelling and model-based analysis of DRE systems. This workshop seeked contribution from researchers and practitioners interested in all aspects of the representation, analysis, and implementation of DRE system behaviour and/or architecture models.
http://www.artist-embedded.org/artist/ACES-MB-08.html

Workshop : UML & AADL 2008
13th IEEE International Conference on Engineering of Complex Computer Systems
Belfast, Northern Ireland - April 2nd, 2008

New real-time systems have increasingly complex architectures because of the intricacy of the multiple interdependent features they have to manage. They must meet new requirements of reusability, interoperability, flexibility and portability. These new dimensions favour the use of an architecture description language that offers a global vision of the system, and which is particularly suitable for handling real-time characteristics. Due to the even more increased complexity of distributed, real-time and embedded systems (DRE), the need for a model-driven approach is more obvious in this domain than in monolithic RT systems. The purpose of this workshop is to provide an opportunity to gather researchers and industrial practitioners to survey existing efforts related to behaviour modelling and model-based analysis of DRE systems. This workshop seeked contribution from researchers and practitioners interested in all aspects of the representation, analysis, and implementation of DRE system behaviour and/or architecture models.
http://www.artist-embedded.org/artist/Topics,1199.html

4.2 Staff Mobility and Exchanges

Alberto Sangiovanni Vincentelli has visited VERIMAG. INRIA and VERIMAG researchers spent significant amount of time visiting Rome to carry out research work in the area of methodologies and tools for embedded system design. Alberto Ferrari has visited Grenoble and other locations to maintain connectivity with the rest of the research community.

Dr. Pierre America participated and provided a presentation during the ArtistDesign workshop Intercluster activity: Integration Driven by Industrial Applications. Title of his presentation was Embedded Systems in Healthcare.

Dr. Ir. Twan Basten participated in the ArtistDesign WFCD 2008 workshop, held on 19th of October during the Embedded Systems Week.

Dr. Michael Borth participated and provided a presentation during the ArtistDesign Workshop Intercluster activity: Integration Driven by Industrial Applications, 13-14 November, Rome. His presentation was titled: Future Car Platform Development.

Kim Larsen was awarded Doctor Honoris Causa at ENS Cachan acknowledging his regular collaboration with LSV. Kim Larsen also spent a month as an invited professor at LSV.

From Aalbrog to CFV (Brussels): one week visit of Prof. Kim Larsen to the team of Prof. JF Raskin.

From ENS Cachan to Aalborg: one week visit of Patricia Bouyer and Nicolas Markey.

From Aalborg to ENS Cachan: one week visit of Ulrich Fahrenberg.

Ghassan Oreiby wil after his position as PhD student at LSV go to Aalborg University for a post doc position starting November 1, 2008.

EPFL + CFV collaborated on efficient algorithms for classical decision problems in automata theory (emptiness, language inclusion, universality), with application to the model-checking of linear time properties.

EPFL + LSV collaborated on games with imperfect information. We work on building a tool to solve such games, with parity objectives.

From INRIA to LSV and CVF (Mons): one week visit of Nathalie Bertrand in each place on probabilistic semantics for timed automata.

From CFV (Brussels) to Inria Rennes: two month visit of Gabriel Kalyon and one month visit of Thierry Massart.

From INRIA to CFV (Brussels) one week visit of T. Legall to ULB followed by post-doc started in September 2008.

From ESI to Inria Rennes: one week visit of Jan Tretmans to Inria for participation to the summer school EJCP.

Uppsala has collaborated with ETH in Zurich on modular performance analysis. Jointly, we have established a fixed point theorem on the existence of fixed points for component networks containing feedback cycles. Uppsala has also initiated collaboration with North Eastern University in China, on multiprocessor scheduling.

The SPEEDS project lead to an important collaboration between INRIA, OFFIS, PARADES and VERIMAG on the definition of the SPEEDS metamodel HRC [BCSM07] which is the basis of an important analysis platform (platform 1). This collaboration continues for the definition of a verification methodology. From the collaboration in SPEEDS has started a broader collaboration on a general framework for the semantics of communication in distributed

systems with INRIA, PARADES and VERIMAG with external collaboration of University of Columbia and Cadence Design Systems [BCC+].

In the Combest project several joint activities are being carried out. In particular, Verimag and ETHZ collaborate on the combination of analytical performance analysis via performance analysis of a corresponding more precise operational model in order to obtain more precise results.

Interaction between RWTH and Saarland University on design notations and model checking

Iinteraction between CISS and RWTHon quantitative versions of priced timed automata

From Aalbrog to CFV (Brussels): one week visit of Prof. Kim Larsen to the team of Prof. JF Raskin.

From CFV (Brussels) to EPFL (Henzinger): Dr. Laurent Doyen formerly in CFV is post-doct at EPFL.

From CFV (Brussels) to EPFL (Henzinger): several visits during 2007-2008 by Prof. JF Raskin.

From EPFL (Henzinger) to CFV (Brussels): several visits during 2007-2008 by Dr. L Doyen.

4.3 Tools and Platforms

Here we list some of the stable, downloadable tools and platforms of the cluster. The cluster are working on several other tools and platforms. For more and detailed information we refer to the reports of the activities *Modeling* and *Validation*.

- **AMT**
  - AMT (Analog Monitoring Tool) is a tool for checking the correctness of analog and mixed-signal simulation traces with respect to a formal specification expressed as an assertion. The specification language supported by the tool is STL/PSL, an extension of the temporal logic inspired by the PSL language, which allows to express properties of real-valued continuous-time behaviors.
    http://www-verimag.imag.fr/~nickovic/index.php?id=nickovic&page=amt

- **IF TOOLBOX**
  - IF is a language for the structured representation of concurrent real-time systems and a set of tools allowing the analysis and verification of requirements on such systems. The tool evolved from the CADP toolset. Its development was motivated by the need for a structured representation of systems, allowing the application of simplifications for avoiding state explosion before its translation into a global (symbolic) transition relation.
    In particular, IF has frontends allowing the verification and analysis of models of real-time systems represented in SDL and UML.
    http://www-if.imag.fr./

- **MARTE**
  - MARTE consists in defining foundations for model-based description of real time and embedded systems. These core concepts are then refined for both modeling and analyzing concerns. Modeling parts provides support required from specification to detailed design of real-time and embedded characteristics of systems. MARTE concerns also model-based analysis. In this sense, the intent is not to define new techniques for analyzing real-time and embedded systems, but to support them. Hence, it provides facilities to annotate models with information required to perform specific analysis. Especially, MARTE focuses on performance and schedulability analysis. But, it defines also a general framework for quantitative analysis which intends to refine/specialize any other kind of analysis.
    http://www.omgmarte.org/

- **METROPOLIS**
  - Establishing formal design methodologies is imperative to effectively manage complex design tasks required in modern-date system designs. It involves defining levels of abstraction to formally represent systems being designed, as well as formulating problems to be addressed at and across the abstraction levels. This calls for a design environment in which systems can be unambiguously represented throughout the abstraction levels, the design problems can be mathematically formulated, and tools can be incorporated to solve some of the problems automatically. Developing such an environment is precisely the goal of Metropolis.

    Metropolis consists of an infrastructure, a tool set, and design methodologies for various application domains. The infrastructure provides a mechanism such that heterogeneous components of a system can be represented uniformly and tools for formal methods can be applied naturally.
    http://embedded.eecs.berkeley.edu/metropolis/index.html

- **PHAVER**
  - PHAVer is a tool for verifying safety properies of hybrid systems. It stands out from other tools with the following features:
    - exact and robust arithmetic with unlimited precision,
    - on-the-fly over-approximation of piecewise affine dynamics
    - improved algorithms and termination heuristics
    - support for compositional and assume-guarantee reasoning.
  - http://www-verimag.imag.fr/~frehse/phaver_web/index.html

- **UPPAAL**
  - Uppaal is an integrated tool environment for modeling, validation and verification of real-time systems modeled as networks of timed automata, extended with data types (bounded integers, arrays, etc.).

    The tool is developed in collaboration between the Department of Information Technology at Uppsala University, Sweden and the Department of Computer Science at Aalborg University in Denmark.
    www.uppaal.com

- **UPPAAL TIGA**
  - UPPAAL TIGA (Fig. 1) is an extension of UPPAAL [BDL04] and it implements the first efficient on-the-fly algorithm for solving games based on timed game automata with respect to reachability and safety properties. Though timed games for long have been known to be decidable there has until now been a lack of efficient and truly on-the-fly algorithms for their analysis.
    http://www.cs.aau.dk/~adavid/tiga/

- **UPPAAL TRON**
  - Uppaal TRON is a testing tool, based on Uppaal engine, suited for black-box conformance testing of timed systems, mainly targeted for embedded software commonly found in various controllers. By online we mean that tests are derived, executed and checked simultaneously while maintaining the connection to the system in real-time.
    http://www.cs.aau.dk/~marius/tron/

- **SARTS**
  - SARTS is a model based schedulability analysis tool used for hard real-time systems. SARTS is used to translate hard real-time systems, implemented in Java, to a finite state machine in the modeling tool Uppaal.

    The system being analyzed must be implemented in SCJ2, a safety critical profile for Java developed in this project, based on SCJ. The target hardware is the time predictable Java processor JOP, developed specifically for hard real-time systems.

    Several experiments have been conducted to illustrate the accuracy of SARTS compared to existing tools. It is shown how the model based approach can result in a more accurate analysis, than possible with traditional analyses.
    http://sarts.boegholm.dk/

- **STG**
  - STG (Symbolic Test Generator) generates conformance tests, based on this framework:
    - Implementation: black-box, only input/output behavior is observable.
    - Specification: IOSTS(input/output behavior + internal structure)
    - Test Purpose: IOSTS, tells which part of the specification is to be tested
    - Test Case: IOSTS generated by STG from a specification and a test purpose
      - Test Cases are symbolic, and possibly parameterized by constants
      - They take into account possible non-determinism of the Spec;
      - They include a verdict (no manual interpretation needed)
  - http://www.irisa.fr/prive/ployette/stg-doc/stg-web.html

- **TIMES**
  - TIMES is a **T**ool for **M**odeling and **I**mplementation of **E**mbedded **S**ystems. It is a tool set for modelling, schedulability analysis, synthesis of (optimal) schedules and executable code. It is appropriate for systems that can be described as a set of tasks which are triggered periodically or sporadically by time or external events.
    http://www.timestool.com/

5. Cluster Participants

5.1 Core Partners

Cluster Leader	
	Professor Kim G Larsen (Aalborg) http://www.cs.aau.dk/~kgl/
Technical role(s) within ArtistDesign	Leads and coordinates the overall activities in the cluster together with Tom Henzinger; Team Leader for Aalborg. Contributes with expertise on timed automata based models with particular emphasis on extensions with cost, probabilities and multiplayer extensions. Verification, synthesis, performance evaluation and model-based testing.

Cluster Leader	
	Professor Tom Henzinger (EPFL) http://mtc.epfl.ch/~tah/
Technical role(s) within ArtistDesign	Leads and coordinates the overall activities in the cluster together with Kim Larsen; Team Leader for EPFL. Contributes with expertise on Rich interface theory for component-based design. Quantitative properties for the design of reactive systems with resource constraints. Languages and algorithms for specifying, checking and comparing resource-dependent specifications.

Team Leader	
	Professor, Director Ed Brinksma (University of Twente/Embedded Systems Institute) http://wwwhome.cs.utwente.nl/~brinksma/
Technical role(s) within ArtistDesign	Team Leader for ESI; Contributes with expertise on quantitative and resorce modelling as well as model based testing.

Team Leader	
	Professor Wang Yi (Uppsala) http://user.it.uu.se/~yi/
Technical role(s) within ArtistDesign	Contributes with expertise on Resource modelling and Timing Analysis.

Team Leader	
	Scientific Leader Thierry Jeron (INRIA) http://www.irisa.fr/prive/jeron/
Technical role(s) within ArtistDesign	Team Leader for INRIA. Contributes with his expertise on models with data and time for model-based test selection and coverage criteria, as well as for quantitative verification, control and diagnosis.

Team Leader	
	Susanne Graf (VERIMAG) http://www-verimag.imag.fr/~graf/
Technical role(s) within ArtistDesign	Team Leader for Verimag. Contributes with expertise on component-based design, the BIP framework, platform-aware implementation of embedded systems, structural verification. Modelling taking into account extra-functional properties.

Team Leader	
	Prof. Dr. Werner Damm (OFFIS) http://www.offis.de/
Technical role(s) within ArtistDesign	Team Leader for OFFIS. Contributes with expertise on component-based design and semantic foundation, in particular non-functional aspects as real-time and safety.

Team Leader	
	Dr. Sébastien Gérard, CEA.
Technical role(s) within ArtistDesign	Team Leader for CEA. Contributes with expertise on model-based engineering, specific focus on standard modelling (specially OMG UML, SYSML and MARTE standards) and RT/E (Real-Time/Embedded) domains.

Team Leader	
	Professor Bengt Jonsson (Uppsala) http://user.it.uu.se/~bengt/
Technical role(s) within ArtistDesign	Team Leader for Uppsala. Contributes with expertise on Component Modeling and Verification.

Team Leader	
	Professor Martin Törngren (KTH) http://www.md.kth.se/~martin/
Technical role(s) within ArtistDesign	Team Leader for KTH. Contributes with expertise on Integrated models supporting cross-layer validation. Methods for validation of self-configuring systems.Compositional validation of integrated models/components.

Team Leader	
	Professor Christoph Kirsch (Salzburg) http://cs.uni-salzburg.at/~ck/
Technical role(s) within ArtistDesign	Team Leader for Salzburg. Contributes with expertise on Compositional timing and reliability modeling in the Giotto family of languages.

Team Leader	
	Professor Alberto L. Sangiovanni-Vincentelli (Parades) http://www.eecs.berkeley.edu/Faculty/Homepages/sangiovanni-vicentelli.html
Technical role(s) within ArtistDesign	Team leader for Parades. Contributes with expertise on Platform-Based Design, the Metropolis and COSI frameworks, industrial applications and international activities.

Team Leader	
	Joseph Sifakis (Director of VERIMAG) http://www-verimag.imag.fr/~sifakis/
Technical role(s) within ArtistDesign	Team Leader for Verimag. Contributes with expertise on component-based design, the BIP framework, platform-aware implementation of embedded systems, structural verification. Context-based analysis.

5.2 Affiliated Partners

	Dr Henrik Lönn, Volvo Technology
Technical role(s) within ArtistDesign	*System engineering and modelling at Volvo. Leading the effort in developing the EAST-ADL modelling language for automotive embedded systems, through the series of projects EAST-EAA, ATESST and ATESST2.*

	Jacques Pulou (France Telecom R&D, France)
Technical role(s) within ArtistDesign	*Component behaviour modeling, Component Based OS construction.*

	Prof. Albert Benveniste (INRIA Rennes, France)

Technical role(s) within ArtistDesign	*Interfaces and modal automata*

	Prof. Roderick Bloem (TU Graz, Austria)
Technical role(s) within ArtistDesign	*Game models for the synthesis problem.*

	Prof. Roberto Passerone (Uni. Trento, Italy)
Technical role(s) within ArtistDesign	*Formal analysis of heterogeneous composition, abstract algebra, and metamodeling*.

	Dr. Koos Rooda, (TU Eindhoven, The Netherlands)
Technical role(s) within ArtistDesign	*Systems engineering*.

	Prof. Dr. Paul van den Hof, (TU Delft, The Netherlands)
Technical role(s) within ArtistDesign	*Performance modelling*

	Prof. Tiziano Villa (Uni. Verona, Italy)
Technical role(s) within ArtistDesign	*Formal verification methods for hybrid systems. Competence in reachability for Hybrid Systems.*

	Prof. Pierre Wolper (CFV, Belgium)
Technical role(s) within ArtistDesign	*Computer-aided verification*
	Prof. Yiannis Papadopolis, Univ. Of Hull (UK)
Technical role(s) within ArtistDesign	*Compositional safety analysis and design optimization w.r.t. safety.*

	Ahmed Bouajjani - LIAFA (France)
Technical role(s) within ArtistDesign	*Real-time and hybrid model checking*

	Stavros Tripakis – Cadence Research lab (USA)

Technical role(s) within ArtistDesign	*Monitoring and test of real-time properties*

	Jean-Francois Raskin (CVF – Belgium);
Technical role(s) within ArtistDesign	*Efficient Model-checking of linear-time properties.* *Verification and synthesis for reactive systems. Timed and hybrid automata.*

	Joost-Pieter Katoen (Aachen – Germany)
Technical role(s) within ArtistDesign	*Model checking of quantitative system properties. Verification of (continuous-time) probabilistic and stochastic systems.*

	Holger Hermanns (Saarlandes U – Germany);
Technical role(s) within ArtistDesign	*Probabilistic and stochastic model checking.*

	Christel Baier (Dresden – Germany);
Technical role(s) within ArtistDesign	*Probabilistic and stochastic model checking*

	Patricia Bouyer, Nicola Markey and Phillippe Schnoebelen (LSV Cachan – France),
Technical role(s) within ArtistDesign	*Decidability and algorithms for priced timed automata and games. Algorithms for solving games of imperfect information*

	Prof. dr. ir. Wil van der Aalst, professor at Eindhoven University of Technology, The Netherlands
Technical role(s) within ArtistDesign	*Information System. Affiliated participant in the ESI Octopus project.*

	Prof. dr. Mehmet Aksit, professor at Twente University, The Netherlands.
Technical role(s) within ArtistDesign	*Software Engineering. Affiliated participant in the ESI Darwin project.*

	Prof. dr. Sandro Etalle, professor at Eindhoven University of Technology, The Netherlands.
Technical role(s) within ArtistDesign	*Security. Affiliated participant in the ESI Darwin project.*

	Prof. dr. Arjen van Gemund, professor at Delft University of

	Technology, The Netherlands. Embedded Software Laboratory.
Technical role(s) within ArtistDesign	*Affiliated participant in the ESI projects Trader and Octopus.*

	Prof. dr. Frits Vaandrager, professor at Radboud University, The Netherlands.
Technical role(s) within ArtistDesign	*Formal methods. Affiliated participant in the ESI Octopus project.*

6. Internal Reviewers for this Deliverable

Bruno Bouyssounouse (Verimag)

IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Cluster - Progress Report for Year 1

Cluster:
Software Synthesis, Code Generation and Timing Analysis

Cluster Leader:

Prof. Dr. Peter Marwedel (TU Dortmund)
http://ls12-www.cs.tu-dortmund.de/~marwedel

Policy Objective (abstract)

The objective of this activity is to provide software synthesis, code generation and timing analysis tools which are required for modern embedded architectures. A particular focus is on multi-processor systems. The parallelism and communication structures found in such architectures pose a particular challenge.

Versions

number	comment	date
1.0	First version delivered to the reviewers	December 19th 2008

Table of Contents

1. Overview

1.1 High-Level Objectives

There is a continuing demand for higher performance of information processing. This growing demand stimulates using a growing amount of parallelism (including using multiple processors), due to limitations of increasing clock speeds any further. This trend also affects the design of embedded systems. Hardware platforms, containing connected processors, are becoming increasingly parallel. Actually, there are various kinds of connectivity. In multi-processors in a system on a chip (MPSoC), processors are tightly connected and communication is fast. In other cases, networked processors may be less tightly connected and communication may be slower. In this project, we would like to address the issues resulting from the use of multiple processors, in particular in the form of multiple heterogeneous processors on a chip, also containing memory hierarchies and communication interfaces.

These processors can only be exploited if (sets of) applications can be efficiently mapped to heterogeneous processors. Mapping techniques can be either based on task graphs or on sequential applications. The latter require the use of automatic parallelization techniques. In this cluster, we want to provide at least partial solutions to the problem of mapping specifications of embedded systems to networks of embedded processors. These networks will be characterized by different speed parameters reflecting the communication and memory architectures. These parameters will be considered during the mapping. We will focus on mappings from simple sequential code from C or C-like languages. However, we will also look at the generation of code from other specifications, being based, for example, on MATLAB or UML. Such languages could simplify the mapping since such specifications might be inherently parallel (and also more appropriate for embedded systems). In general, mapping techniques will be indispensable for using future architectures.

Timing analysis is also affected by the trend toward the new platforms. Also, timing analysis beyond single processors is required. Timing analysis has to cope with the kind of memory hierarchies found in MPSoCs. Hence, timing analysis will also consider the timing of communication. The overall objective is to provide safe timing guarantees for systems consisting of local memories hierarchies and multiple processors. In addition, overcoming the traditional separation between compilers and timing analysis continues being on the agenda.

The design of efficient embedded systems also requires additional work. In particular, minimizing the energy consumption, addressing the memory wall problem and customizing instruction sets are hot topics, for which integrated approaches from various partners are being extended and exploited.

Partners in this cluster also participate in the activities of the thematic activities of the Transversal Integration workpackage, where they address adaptivity and predictability of complex systems comprising MPSoCs. Predictability is also to be addressed in the cooperation between partners of the two activities of this cluster.

It is understood that the current project can only help integrating work that provides potential solutions. The actual work on those solutions is mostly paid through other projects.

1.2 Industrial Sectors

Software Synthesis and Code Generation: The work performed in the cluster is relevant for all industrial sectors using embedded software. This includes semiconductor houses, system houses, companies working on audio processing, video processing, data streaming

applications in the TV, Set Top boxes, DVD players and recorders, mobile phones, base stations, printers and disk drives. Efficiency of embedded software, in particular the efficiency of memories, is relevant for high-speed embedded systems. It is expected that most mobile devices will provide some kind of multimedia processing.

Timing Analysis: WCET estimations are relevant for all industrial sectors using hard real-time systems. Therefore, industrial sectors in this case include avionics, automotive, defence and some areas where control systems are applied. Especially in the automotive and the aeronautical domains, there is a need to have precise knowledge on the worst-case timing behaviour of safety critical software. Therefore, timing-analysis tools entered industrial practice and are in routine use in the aeronautics and automotive industry. This need is underlined by the fact that the worst-case timing of large parts of the software used within the new Airbus A380 has been analyzed using AbsInt's aiT. AbsInt's timing analysis tool, aiT, has been used in the certification of time-critical subsystems of the Airbus A380 and has thus acquired the status of a *validated* tool.

Link between timing analysis and compilers: The availability of precise timing analyses does not fulfil all industrial needs. Since the code of safety critical applications is typically generated by a compiler, the compiler should also be aware of worst-case timings. This work is relevant in all areas for which a physical environment is integrated with software. The focus is on sectors having safety critical applications.

1.3 Main Research Trends

Mapping of applications to MPSoCs can be considered as an extension of scheduling. Traditionally, scheduling mostly focused on independent tasks. This assumption is not valid for most applications of embedded systems. Additional research is performed in the multi-core context. Multi-core processors are usually considered to be homogeneous. For embedded systems, this assumption is also not valid. Therefore, new mapping techniques are required. Some papers have been published in this area (for example, there will be a session on this topic at the forthcoming DATE 2009 conference). It is a trend to combine the mapping problem with non-traditional objectives. For example, minimization of the operating temperatures, maximization of the life-time of processors, and dependability in the presence of failing processors etc are considered. However, these approaches mostly consider tasks as black boxes with little information, for example, on the memory access characteristics. This can lead to sub-optimum mappings. This trend is important in all industrial areas in which high performance embedded computing is required.

Taking the well-known (frequently negative) results on automatic parallelization in high-performance computing into account, automatic parallelization is being experimented with in a way which is appropriate for embedded systems. Results obtained (for example at the University of Edinburgh and the University of Passau) indicate that this parallelization is feasible within a restricted scope of applications and architectures. This trend is also important in all industrial areas in which high performance embedded computing is required.

Energy efficiency, initially mostly a topic considered for embedded systems, is now becoming mainstream. Energy availability is continuing to be the most challenging constraint for embedded system design, but performance constraints also exist. Therefore, the design of efficient embedded systems continues being important. Constraints are most dominating for small, mobile products.

The importance of timing is slowly being recognized by larger groups of people. For example, there is increasing interest in the automotive domain. At the same time, researchers are also giving timing issues more attention. In-line with this, the first compiler including a fully

integrated WCET estimator was designed in the Artist2 project. This research direction is finding more attention recently.

WCET analysis has so far almost exclusively dealt with sequential code running on uni-processors. The main trend has been towards managing more complex sequential hardware architectures. Increasing the level of automation, e.g., by more advanced analyses constraining the possible program flows, is also a topic of active research. As multi-core and MPSoC architectures arise, the research focus will have to shift towards analysis of parallel systems.

2. State of the Integration in Europe

2.1 Brief State of the Art

Software Synthesis and Code Generation: Mapping applications to MPSoCs is an important topic in various places in the world, due to its extreme relevance for industry. In Europe, Ed Deprettere (U. Leiden) performed significant work, working together with adjacent universities on the DEADALUS tool. Also, the group of Jürgen Teich from the University of Erlangen Nürnberg is proposing the SystemCoDesigner tool. In the automotive context, additional work has been performed at TU Braunschweig. METROPOLIS by Sangiovanni-Vincentelli et al. is a tool working on a global level. CHARMED by Bhattacharyya places an emphasis on signal processing applications. Recent tools try to combine task allocation with non-standard cost functions such as energy (e.g. Chang at DAC 2008), temperature (e.g. Ciskun at DATE 2007), lifetime or dependability.

The design of efficient embedded systems is the target of numerous optimization tools. There are clearly too many tools to make any attempt to present a survey in limited space useful. Even within the more restricted area of optimization the memory structure, many approaches have been proposed by computer architects. Due to the increasing speed gap between processors and memories, efforts for improving the performance of systems have been predicted to hit the “memory wall”. Work was done in the context of caches (loop caches, filter caches etc.). However, these approaches have mostly focussed on hardware approaches for reaching the goals. For these approaches, compilers were considered to be black boxes and untouchable. Only few authors (e.g. Barua, Catthoor, Dutt, Kandemir, Egger) have taken a holistic approach, looking at hardware and software issues.

Timing Analysis: Several commercial WCET tools are available. They have experienced positive feedback from extensive industrial use in the automotive and aeronautics industry. The existing tools serve some particular and highly relevant points in this space. AbsInt’s tool for example has been used in the development and the certification of safety-critical systems in the Airbus A380. However, they currently do not serve distributed architectures well.

2.2 Main Aims for Integration and Building Excellence through ArtistDesign

The Compiler and Timing Analysis Cluster and the Execution Platforms Cluster aim at developing a common methodology to enable resource aware design and compilation and to increase predictability while retaining a performant system. The main aim of using the ArtistDesign network is to get access to competences, knowledge and tools which are not available locally at each of the institutions. The cooperation provides the required size of research teams, necessary to handle the complexity of today’s technology. Furthermore, a major goal is the combination of areas of excellence of the different partners by defining and implementing interfaces between their design flows and tools in order to achieve compilation platforms applicable to a wider problem scope.

WCET analysis of parallel systems, including MPSoC, is a more or less novel research area. However, it is becoming rapidly important as MPSoC's become increasingly used. Therefore, it is urgently needed to initiate more research in this area, and the ArtistDesign network will be used for this. The network will also be used for research initiation activities within the WCET analysis area. Contacts with other clusters, such as the HW Platform and MPSoC design cluster, will also be of importance since the success of the cluster’s activities depends critically on the properties of the underlying hardware design.

2.3 Other Research Teams

For mapping applications to MPSoCs, section 2.1 contains a brief description of the work of other research teams in this area. Ed Deprettere (U. Leiden), Jürgen Teich and two of their students participated in the working meeting at Düsseldorf in November 2008. They are clearly candidates for being added as affiliates.

Essentially three more research teams have competed with Europe in the area of Timing Analysis, one at Seoul National University (SNU), one at Florida State University, now with some branches in North Carolina etc., and Singapore National University. Seoul has turned to power-aware computing, and flash memory based components research. Singapore and Florida have cooperated with the ArtistDesign partners in writing a survey paper. Singapore has participated in the WCET Tool Challenge, arranged within ArtistDesign, with their academic prototype. There is a continuous exchange of PhD students and PostDocs with the team of Prof. Sang Lyul Min at SNU.

Only few groups have been working on the integration of worst-case execution times and compilers. Smaller, apparently volatile efforts have been reported from Sweden and South Korea. Some work was performed in the group of David Whalley at the Computer Science Department of the Florida State University. However, only very simplified timing models and highly predictable processor architectures are considered at Florida.

Additional work has been performed at INRIA by Isabelle Puaut et al. More information about the work of other teams is available in section 1.5 of the two related activity reports.

2.4 Interaction of the Cluster with Other Communities

For mapping application to MPSoCs, links have been established with the execution platform cluster of ArtistDesign, where some related work is being performed, for example, at Zürich, Bologna and TU Denmark. For timing analysis, the same applies for the modelling and validation cluster. The three clusters were represented by Lothar Thiele, Nicolas Halbwachs and Peter Marwedel at the South American Summer School on Embedded System Design at Florianopolis in 2008. Cluster members Peter Marwedel and Rainer Leupers performed further teaching activities at ALARI, Lugano, together with ArtistDesign members like Luca Benini (Bologna), Rudy Lauwereins (IMEC) and Lothar Thiele (Zürich). Further links of ArtistDesign members existed to the SHAPES project and to the HiPEAC Network of Excellence.

TU Dortmund:

The interaction with the local technology transfer centre ICD (see http://www.icd.de/index_eng.html) is key for interacting with industry. ICD is headed by Peter Marwedel. ICD is used for transferring research results to industry. The group promoted education in embedded systems through a published text book and through courses at ALARI (Lugano) and at spring or summer schools in Brazil, Portugal, Korea, and France. TU Dortmund organizes the SCOPES series of workshops on compilation for embedded systems.

IMEC:

IMEC is integrated in European research networks, including HiPEAC. Moreover, IMEC is the central partner of a Marie Curie Host Fellowship project that involves more than 10 universities across Europe. IMEC also has many industry co-operations including most large European multi-media and communication systems oriented companies. Additionally, several news sites featured the launch of the CleanC tools for source code parallelization assistance. Articles talking about the launch of the tools could be found on sites like EETimes, EDN, Electronics Weekly, Azonano, EDACafé.com, EDA DesignLine, Electronic Design, Topix, SOCCentral, Ugens Erhverv, or Global-Electronics.net.

U. Passau:

The group at the University of Passau is internationally well connected in parallelism and programming methodology. This is most visibly documented by Christian Lengauer's chairmanship of the steering committee of the yearly international conference series Euro-Par (Parallel Computing in Europe) and the IFIP Working Group 2.11 on Program Generation. Here, the paradigm of feature orientation is receiving special interest.

Passau is also a member of the CoreGRID network of excellence which terminated in August 2008 bur will continue as an informal interest group. Some of the software engineering and parallelization issue of CoreGRID are also relevant to ArtistDesign.

In the past year, Lengauer has spear-headed the submission of a proposal for a national research activity ("*Schwerpunktprogramm*") to the German Research Foundation ("*Deutsche Forschungsgemeinschaft*") with the title "Manycore: Parallelism for everybody. One of several application areas is the use of multi-cores and many-cores in embedded systems. The national research activity programme is highly competitive, and an acceptance of the proposal is not certain. If granted, funding of €10+ million can be expected for a period of 6 years, funding up to 25 research projects. A decision will have been made by May 2009.

RWTH Aachen:

A close cooperation existed with the ArtistDesign Execution Platforms cluster, in particular between Dortmund, Aachen, and Bologna University. RWTH Aachen participated in the HiPEAC network of excellence and worked on cooperations related to code optimization, e.g. with Edinburgh University. Furthermore, Aachen maintained tight industry cooperations, e.g. with CoWare, ACE, and Infineon. Since Oct 2006, RWTH Aachen is running the UMIC research cluster (http://www.umic.rwth-aachen.de) of the German excellence initiative.

Mälardalen:

The WCET analysis group maintains close contacts with several industrial partners, and has conducted a number of case studies using their production codes. The group also interacts heavily with the Component-based Software Engineering community through the national centre PROGRESS for research on component-based software design for embedded systems.

Saarland University:

Timing-Analysis activities in the cluster interacted closely with the Execution-Platform cluster in the area of increasing the timing-predictability of real-time systems. Airbus and Bosch participated in the Predator FP7 proposal aimed at reconciling performance with predictability. The PREDATOR project started in 2008. Saarland University worked on modularizations of the Sagiv/Reps/Wilhelm shape analysis together with Mooly Sagiv, Tel Aviv University, and Arnd Poetzsch-Heffter, University of Kaiserslautern.

ACE:

ACE worked closely with ST and with Philips having both a commercial relationship with them as well as being co-members of EU project consortia – in one case along with Verimag. ACE has been working closely with Aachen in this domain for some time. One of the results of this cooperation has been the integration of compiler technology in a start-up company that span out of the university. Cooperation with Imperial College and Edinburgh has also started.

AbsInt:

Within the EmBounded Project (IST-510255), AbsInt was also involved in the development of the Hume compiler. Hume is a domain-specific high-level programming language for real-time embedded systems.

TU Berlin:

TU Berlin is generally involved in methods and tools for software engineering for embedded systems. TU Berlin has cooperated with Edinburgh University (Björn Franke) concerning the optimization of compilers based on machine learning techniques. Furthermore, TU Berlin has done research on the verification of embedded operating systems, also by cooperating with the Fraunhofer institute FIRST. Finally, TU Berlin visited and was visited by other cluster members, e.g. ACE, RWTH Aachen and TU Vienna.

Tidorum, York:

Tidorum (and partially York through Rapita Systems) were engaged in a project for the European Space Agency to study the timing and verification aspects of cache memories in space systems. The PEAL project ended in February 2007. An extension was started in late 2007. The main partner from the aerospace domain was Thales Alenia Space, France.

TU Vienna:

TU Vienna worked on measurement-based timing analysis together with TU Munich. It also maintained a close interaction with the Lawrence Livermore National Laboratory, CA, USA, in optimizing high-level abstractions.

3. Overall Assessment and Vision for the Cluster

3.1 Assessment for Year 1

The partners promised starting with a joint workshop, at which the directions of the work on the mapping of applications should be set. This workshop (held at Rheinfels castle) found a wider interest than initially conceived: both activities decided to be present at the workshop. The announcement of the workshop also found the interest of people outside ArtistDesign. At the workshop, attendees agreed to cooperate. Slides from the workshop are available at the ArtistDesign website (http://www.artist-embedded.org/artist/Mapping-of-Applications-to-MPSoCs.html). A summary of the workshop was presented at the CASA workshop (see http://www.esweek.org). An invitation to turn this summary into a survey in some journal was received. A follow-up meeting, more details about the cooperation were fixed. In this sense, the partners are working on the problems, but no tool integration could be expected in this new area in the very first year.

The integration of timing analysis and compilers is building on top of worked performed during the lifetime of the Artist2 network. Hence, tool integration is essentially complete and can now be exploited. A major number of papers reflect the fact that the current work was built on top of earlier work. Also, separate funding through the PREDATOR project allowed increasing the man power in this area.

Within Timing Analysis, work has been initiated in the area of timing predictability. Results for cache replacement policies have been obtained for individual cores: the plan is to extend these to multiple core systems. The influence of scheduling on cache contents has also been studied. For measurement-based timing analysis methods, joint work is carried out regarding test-case generation and learning techniques to identify timing model features.

An important part of the timing analysis work will be the formulation of design principles for architectures with predicable behaviour. This work is now being initiated. The immediate plan is to have a joint workshop with the HW Platforms and MPSoC Design cluster, and to write a white paper explaining the timing predictability problem for MPSoC from a timing analysis perspective.

The generation of efficient embedded systems is a second area where we could build on top of tools integrated during the lifetime of Artist2. Work in this area continues. Additional funding is available, for example through the MNEMEE project, in which IMEC and TU Dortmund's spin-off ICD are involved. The work on scratchpads is now widely recognized. For example, a previously published paper of TU Dortmund has been found to be the second most frequently cited paper at the CODES and ISSS symposia between 1996 and 2006 [F. Vahid, T. Givargis: Highly-cited ideas in system codesign and synthesis, *Proceedings of the 6th IEEE/ACM/IFIP international Conference on Hardware/Software Codesign and System Synthesis, p.* 191-196].

Software synthesis was represented at the Rheinfels workshop. It will be included in our considerations in the future. However, software synthesis is a wide area and the cluster has only few members. Therefore, the full breadth of this area could not and will not be covered.

3.2 Overall Assessment since the start of the ArtistDesign NoE

Support for various multi-processor systems has been selected as the key new topic for ArtistDesign. The importance of this topic has increased since the description of the work was written. It is now even more clear that clock speeds can hardly be increased and that performance increases have to rely on using parallel processors. There is still the **risk that missing tools will stop further increases of the performance of embedded systems** and

that huge investments into parallel architectures will be partially lost. Hence, **this topic is of outmost importance**. It turns out that the two activities of this cluster have joint interests in this area. Code generation tools are clearly needed and timing analysis is also mandatory. An early warning by timing analysis specialists is needed. Otherwise, architects might select architectures having absolutely non-acceptable WCET bounds. Therefore, code generation and timing analysis specialists decided to have a joint workshop.

The importance of timing for embedded system design is being recognized more widely. Ed Lee formulated this importance in a very well memorizable way. He wrote "The lack of timing in the core abstraction (of computer science) is a flaw" [Edward A. Lee: *Building Unreliable Systems out of Reliable Components: The Real Time Story*, University of California at Berkeley, Technical Report No. UCB/EECS-2005-5, 2005]. In the US, the term "cyber-physical systems" has been introduced. This term is intended to denote embedded systems and the introduction was mainly a marketing issue. Nevertheless, the explicit link to physics demonstrates the importance of timing. Accordingly, the keynote by F. Vahid and T. Givargis at the Workshop on Embedded system Education (WESE), supported by ArtistDesign, was called "Timing Is Everything – Embedded Systems Demand Early Teaching of Structured Time-Oriented Programming". It is now more widely recognized that the inclusion of timing is the key differentiator between embedded and non-embedded software. This insight demonstrates the importance of the work on timing analysis and WCET-aware compilation.

Efficiency of embedded systems continues being a key concern. The trend for higher resolution images in many industrial sectors continues. As a result, tight performance constraints exist for many advanced applications. The importance of energy efficient computing (initially just considered for embedded computing) has reached the attention of the general public. The carbon (-dioxide) footprint left by various technologies, including embedded systems, is now considered in most countries. Research on energy-efficient computing is counter-acting against increasing footprints.

3.3 Indicators for Integration

Partners promised the following Interactions:

- Partners announced an integration of techniques developed by the high-performance computing community and the compiler for embedded systems community. They predicted having at least one tool flow demonstrating the advantages of combining these approaches and having examples demonstrating the power of the integrated techniques for MPSoCs. According to the "description of the work", compilation techniques will be made available to the MPSoCs community. Along these lines, a common workshop and a meeting were held and plans for a cooperation conceived. The actual integration will require more time.
- The partners promised integrating at least one timing analysis tool with an experimental compiler, to design optimizations within this compiler considering multiple objectives (including worst-case execution times) and to generate a detailed set of results demonstrating the advantages and limitations of such an integration. This promise was kept: the integration of aiT and WCC has been completed. The results are being demonstrated in an increasing list of papers (see references). Tradeoffs between multiple objectives have not yet been studied.

  http://ls12-www.cs.tu-dortmund.de/research/activities/wcc/
- The partners promised organizing at least one open, internationally visible workshop on software generation, compilers and timing analysis per year. This promise was kept: the SCOPES workshop was held in March 2008. In addition, the WCET Workshop was held in July 2008.

- The partners promised publishing at least four joint papers per year. This promise was kept even in the very first year, despite the latency of the whole process from research to publications. There are six joint papers for the software synthesis and code generation activity (including submitted papers) and four joint papers for the timing analysis activity
- The Timing Analysis partners conducted the second WCET Challenge, WCET 2008. This is an effort in tool evaluation, where WCET anaysis tools are evaluated with respect to a number of criteria on a common set of benchmarks. The WCET Challenge has now been established as an ongoing activity.

3.4 Long-Term Vision

The long term vision of the project is to have an impact on the tool landscape supporting embedded computing. We intend to contribute to programming tools for MPSoCs, to timing predictability for all kinds of platforms (including MPSoCs) and to resource-aware platform mapping techniques. We predict that an increasing amount of industrial areas will require a guaranteed timing. However, the trend toward higher performances and the use of multi-processor systems with shared resources is working in the opposite direction. It will be required to raise the awareness of timing issues.

4. Cluster Participants

4.1 Core Partners

Cluster Leader **Activity Leader for "Software Synthesis and Code Generation"**	
	Prof. Dr. Peter Marwedel (TU Dortmund) http://ls12-www.cs.tu-dortmund.de/~marwedel/
Technical role(s) within ArtistDesign	Cluster leader, activity leader SW Synthesis and Code Generation Improved code quality for embedded applications is the main goal of the work at Dortmund University. Due to the widening gap between processor and memory speeds, emphasis has been on improving the efficiency of memory accesses, in terms of average and worst case execution time and in terms of the energy consumption.
Research interests	Peter Marwedel's Embedded Systems Group focuses on embedded software. Particular emphasis is on compilers for embedded processors. One of the very first publications in this area, the book "Compilers for Embedded Processors", edited by Peter Marwedel and Gert Goossens, was the result of the CHIPS project, funded by the European Commission. The group's current focus is on advanced optimizations for embedded processors (e.g. by using bit-level data flow analysis) and energy-aware compilation techniques. Current research also includes high-level transformations of algorithms as well as WCET-aware code generation.
Role in leading conferences/journals/etc in the area	Member of the EDAA (European Design and Automation Association) Main Board. Editorial Board Member of the Journal of Embedded Computing. Editorial Board Member of the Microelectronics Journal. Co-Founder and Steering Board Chair of the SCOPES Workshop (Software and Compilers for Embedded Systems) Series. >14 years of service for the DATE conference and its predecessors (program chair: 3 times, chairman of the steering committee, European representative to ASPDAC) DAC: Topic chair and reviewer Various other conferences
Notable past projects	MAMS: Multi-Access modular-services framework, national project

	funded by the German Federal Ministry of Education and Research (BMBF) MORE: Network-centric Middleware for group communications and resource sharing across heterogeneous embedded systems, supported by the European Commission http://www.ist-more.org HiPEAC: European NoE on High-Performance Embedded Architecture and Compilation; http://www.hipeac.net Others: Various earlier projects supported by the EC, DFG etc.
Awards / Decorations	Teaching award, TU Dortmund, 2003 DATE fellow, 2008
Further Information	CEO of the Informatik Centrum Dortmund (ICD), a technology transfer centre founded in 1989.

Activity Leader for "Timing Analysis"	
	Prof. Björn Lisper (Mälardalen University) http://www.idt.mdh.se/personal/blr/
Technical role(s) within ArtistDesign	Activity for "Timing Analysis" Timing analysis, program analysis.
Research interests	Timing analysis, static program analysis, language design for embedded and real-time systems, program transformations, parallelism
Notable past projects	FP7 STREP ALL-TIMES, Integrating European Timing Analysis Technology (coordinator). http://www.all-times.org Several national projects, funded by Swedish Research Council, VINNOVA, KKS, SSF, Ericsson

	Dr. Stylianos Mamagkakis IMEC vzw. http://www.imec.be

Technical role(s) within ArtistDesign	Representing IMEC Nomadic Embedded Systems (NES) division in: -Cluster: SW Synthesis, Code Generation and Timing Analysis -Cluster: Operating Systems and Networks -Cluster: Hardware Platforms and MPSoC Design -Intercluster activity: Design for Adaptivity -Intercluster activity: Design for Predictability and Performance -Intercluster activity: Integration Driven by Industrial Applications
Research interests	Stylianos Mamagkakis received his Master and Ph.D. degree in Electrical and Computer Engineering from the Democritus Uni. Thrace (Greece) in 2004 and 2007, respectively. Since 2006, he coordinates a team of PhD students within the NES division at IMEC, Leuven, Belgium. His research activities mainly belong to the field of system-level exploration, with emphasis on MPSoC run-time resource management and system integration.
Role in leading conferences/journals/etc in the area	Stylianos Mamagkakis has published more than 35 papers in International Journals and Conferences. He was investigator in 9 research projects in the embedded systems domain funded from the EC as well as national governments and industry.
Notable past projects	Project leader of MNEMEE IST project ωωω.μνεμεε.οργ Project leader of OptiMMA IWT project ωωω.ιμεχ.βε/ΟπτιΜΜΑ Participation in: 1 international IMEC project (M4), 3 European IST projects (AMDREL, EASY, ARTIST2), 2 Greek projects (PRENED, DIAS)
Awards	1st prize in 'Technogenesis' Competition for Business Innovation, Greece, June'06 3rd prize in 'Otenet Innovation 2006' Competition for Business Innovation, Greece, November'06
Further Information	http://www2.imec.be/imec_com/nomadic-embedded-systems.php

	Prof. Dr. Christian Lengauer http://www.infosun.fim.uni-passau.de/cl/staff/lengauer
Technical role(s) within ArtistDesign	Strengthen link between high-performance computing and parallel programming and embedded systems
Research interests	Parallel systems, program analysis, programming methods
Role in leading conferences/journals/etc in the area	Journal editor for: *Parallel Processing Letters*, World Scientific Publ. Co. ; *Science of Computer Programming*, Elsevier Science B.V. ; *Scientific Programming*, IOS Press; *Int. J. of Parallel, Emergent and*

	Distributed Systems, Taylor & Francis; Chair of the Euro-Par steering committee, Chair of the IFIP WG 2.11 on Program Generation, programme committee member of various conferences
Notable present and past projects	LooPo: a loop parallelizer based on the polytope model (past and present DFG funding); FeatureFoundation: Feature-Oriented Program Synthesis (DFG: 2008-2010, renewable); Meta-Programming (DAAD: 2004-2005, EC FP6: from 2004) PolyAPM: abstract parallel machines for the polytope model (DFG: 2000-2002); HDC: a language for parallel higher-order divide&conquer (DFG: 1996-2000) ; SAT: performance-directed parallel programming (1994-98) ; PLR: parallel linear recursion (1994-98) ; OSIDRIS: object-oriented specification of distributed systems (DFG: 1993-97)

	Prof. Dr. Rainer Leupers http://www.iss.rwth-aachen.de
Technical role(s) within ArtistDesign	SW Synthesis and Code Generation, code optimization
Research interests	Compilers, ASIP design tools, MPSoC design tools
Role in leading conferences/journals/etc in the area	TPC member of DAC, DATE, ICCAD etc. Co-founder of SCOPES workshop General Co-Chair of MPSoC Forum 2008 (www.mpsoc-forum.org)
Notable past projects	HiPEAC NoE, SHAPES IP, several DFG-funded projects Industry-funded projects with Infineon, Philips, Microsoft, CoWare, ACE, Tokyo Electron etc.
Awards / Decorations	Several IEEE/ACM best paper awards
Further Information	Co-founder of LISATek Inc. (acquired by CoWare Inc.) European Commission expert in FP7 Editor of “Customizable Embedded Processors”, Morgan Kaufmann, 2006 Vice Coordinator of UMIC (Ultra High-Speed Mobile Information and Communication) research cluster (www.umic.rwth-aachen.de)

	Prof. Dr. Reinhard Wilhelm (Saarland University) http://rw4.cs.uni-sb.de/users/wilhelm/wilhelm.html
Technical role(s) within ArtistDesign	Timing Analysis
Research interests	Compilers, Static Analysis, Timing Analysis
Role in leading conferences/journals/etc in the area	EMSOFT 2007 program co chair.
Notable past projects	DAEDALUS
Awards / Decorations	Prix Gay-Lussac-Humboldt

	Prof. Dr. Peter Puschner (TU Vienna) Real-Time Systems Group Institute of Computer Engineering Vienna University of Technology http://www.vmars.tuwien.ac.at/people/puschner.html
Technical role(s) within ArtistDesign	Peter Puschner and his group are participating in the Timing-Analysis activities of the Compilation and Timing Analysis cluster. Within ArtistDesign the contributions are in the area of path-description languages for static WCET analysis, compilation support for WCET analysis, methods and problems of measurement-based execution-time analysis, and on software and hardware architectures that support time predictability.
Research interests	Peter Puschner's main research interest is on real-time systems. Within this area he focuses on Worst-Case Execution-Time Analysis and Time-Predictable Architectures.
Role in leading conferences/journals/et	Member of the Euromicro Technical Committee on Real-Time Systems, the steering committee of the Euromicro Conference

c in the area	on Real-Time Systems (ECRTS) Member of the advisory board and organizers committee of the IEEE International Symposium on Object- and Component-Oriented Distributed Computing (ISORC) conference series Chair of the Steering Committee of the Euromicro Workshop on Worst-Case Execution-Time Analysis (WCET) series
Notable past projects	DECOS - Dependable Embedded Components and Systems Develop the basic enabling technology to move from a federated distributed architecture to an integrated distributed architecture. http://www.decos.at MoDECS - Model-Based Development of Distributed Embedded Control Systems Model-based construction of distributed embedded control systems: shift from a platform-oriented towards a domain-oriented, *platform-independent* development of composable, distributed embedded control systems. http://www.modecs.cc NEXT TTA Enhance the structure, functionality and dependability of the time-triggered architecture (TTA) to meet the cost structure of the automotive industry, while satisfying the rigorous safety requirements of the aerospace industry. http://www.vmars.tuwien.ac.at/projects/nexttta/

	Dr. Iain Bate (University of York) http://www-users.cs.york.ac.uk/~ijb/
Technical role(s) within ArtistDesign	Responsible for the WCET cluster at University of York. Also involved in the Design for Adaptivity cluster.
Research interests	Worst-case execution time analysis. Design and certification of critical real-time systems. Design for flexibility. Search-based systems engineering. Use of novel computation techniques, e.g. Artificial Immune Systems.
Further Information	Also director of Origin Consulting (York) Ltd. a spin-off company providing consultancy on the design and certification of critical systems.

4.2 Affiliated Industrial Partners

	Joseph van Vlijmen (ACE, Netherlands)
Technical role(s) within ArtistDesign	The design and construction of extensions to CoSy required for ArtistDesign projects.
Research interests	The development and exploitation of compilation techniques and development systems in the wider contexts of SoC and EDA supported by descriptions of the system including application and target architectures. Particular interests include MPSoC and highly parallel system.
Role in leading conferences/journals/etc in the area	Programme Committees of SCOPES and DATE.
Notable past projects	COMPARE/PREPARE ESPRIT projects: These projects, particularly COMPARE, were precursors for CoSy. PREPARE focused on retargetable compilation for Fortran 90 and High Performance Fortran using massively parallel MIMD machines. MESA/NEVA (ongoing): Framework IPs addressing the challenges of designing and constructing multi-processor systems.
Further Information	Principal architect of the CoSy. Previously, architect of ACE's shared memory heterogeneous multiprocessor UNIX OS.

	Dr. Marco Bekooj (NXP)
Technical role(s) within ArtistDesign	Strengthen link to work on code synthesis and industry
Research interests	Design of predictable systems

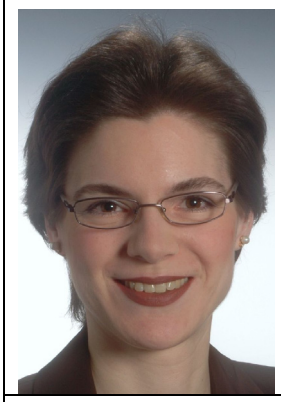
	Dr.ir. Bart Kienhuis (Compaan Design B.V., Leiden) http://www.liacs.nl/~kienhuis/
Technical role(s) within ArtistDesign	Strengthen link to work on code synthesis and industry
Research interests	Design of predictable systems

	Dr. Niklas Holsti (Tidorum Ltd) http://www.tidorum.fi
Technical role(s) within ArtistDesign	Participate in the definition of the common WCET tool-set architecture, the analysis modules and the interchange representations (languages, file formats). Adapt Tidorum's WCET tool, Bound-T, to integrate with the architecture and interchange formats defined in ArtistDesign
Research interests	Static analysis of the worst-case execution time of embedded programs.

	Dr. Christian Ferdinand (AbsInt Angewandte Informatik GmbH) http://www.absint.com/
Technical role(s) within ArtistDesign	Christian Ferdinand coordinates the activities of AbsInt within Artist Design.
Research interests	Timing analysis, program optimization, compiler construction.
Notable past projects	Transferbereich 14 "Run-time Guarantees for modern Processor Architectures" of the German DFG. DAEDALUS RTD project IST-1999-20527 of the European FP5 program on the validation of software components embedded in future generation critical concurrent systems by exhaustive semantic-based static analysis and abstract testing methods based on abstract interpretation. http://www.di.ens.fr/~cousot/projects/DAEDALUS/index.shtml INTEREST EU Framework VI Specific Targeted Research Project IST-033661 aiming at overcoming the lack of integration and interoperability of tools for developing Embedded Systems software.

	http://www.interest-strep.eu/
Awards / Decorations	Dr. Ferdinand received the Dr. Eduard Martin Preis in 1999 (award for best Ph.D Thesis in computer science at Saarland University). AbsInt has been awarded a 2004 European Information Society Technology (IST) Prize for its timing analyzer aiT.

4.3 Affiliated Academic Partners

	Prof. Dr. Sabine Glesner (Technical University of Berlin) www.pes.cs.tu-berlin.de
Technical role(s) within ArtistDesign	Activity Leader for Compiler Platform Compiler Verification
Research interests	Compilers, Verification, Embedded Systems and Software, Formal Semantics
Role in leading conferences/journals/etc in the area	PC Member of Compiler Construction 2007 Date'06, Design, Automation and Test in Europe, TPC Member of Topic B9 on Formal Verification Workshop Compiler Optimization meets Compiler Verification COCV, ETAPS Conferences, PC Member in 2005 and 2006, Program Co-Chair in 2007 Workshop Formal Foundations of Embedded Software and Component-Based Software Architectures (FESCA), ETAPS Conferences, PC Member 2005 and 2006 Editorial Board Member of “Informatik – Forschung und Entwicklung” by Springer, starting with Vol. 21, No. 1
Notable past projects	VATES (Verification and Transformation of Embedded Systems), funded by DFG Aktionsplan Informatik (Emmy Noether-Program), funded by DFG, support for young researchers to build a research group, with a focus on optimization and verification in the compilation of higher programming languages, from 2004 to 2009 Correct and Optimizing Compilers for Modern Processor Architectures, funded by a postdoc excellence program of Baden-Württemberg, Germany, 2003-2005

	Grant in the Wrangell-Habilitation Program of Baden-Württemberg, Germany, 2001-2005
Awards / Decorations	Award of the “Forschungszentrum Informatik” for one of the two best PhD theses of the Faculty for Computer Science, University of Karlsruhe, 1998/99 Member of the “Studienstiftung des deutschen Volkes”, the German national scholarship organization, 1991-1996 Fulbright grant to study at the University of California, Berkeley, 1993-1994 Member of the Siemens Internationaler Studenten / Doktorandenkreis, 1993-1999

	Dr. Björn Franke (Lecturer, University of Edinburgh) http://homepages.inf.ed.ac.uk/bfranke/Welcome.html
Technical role(s) within ArtistDesign	Provide a link to work on program analysis and parallelization
Research interests	Compilers, embedded systems

	Prof. Paul Kelly (Imperial College, London) http://www.doc.ic.ac.uk/~phjk/
Technical role(s) within ArtistDesign	Provide a link to work on program analysis and parallelization
Research interests	Software performance optimization

	Dr. Alain Darte Scientific leader of Inria Project Compsys (Compilation and Embedded Computing Systems) Laboratoire de l'Informatique du Parallélisme CNRS, Inria, UCBL, ENS-Lyon http://perso.ens-lyon.fr/alain.darte
Technical role(s) within ArtistDesign	Activity in automatic parallelization, source to source transformations for high-level synthesis of hardware accelerators, possibly WCET.
Research interests	Code optimizations for embedded computing systems: back-end code optimizations (SSA form, register allocation, static/JIT compilation), source-to-source code transformations for HLS tools (code rewriting, memory and communication optimizations).
Role in leading conferences/journals/etc in the area	Editorial board of ACM Transactions on Embedded Computing Systems (ACM TECS). Program committees in 2008-09: SCOPES 2009, PLDI 2008, CC 2008. Before 2008: many DATE, CASES, ASAP, ICS, CGO, etc.
Notable past projects	Minalogic project SCEPTRE Collaboration with STMicroelectronics, funded by French Ministry of Research and Région Rhône-Alpes
Awards / Decorations	Best paper awards: IPDPS 2002, CGO 2007

4.4 Affiliated International Partners

None.

5. Internal Reviewers for this Deliverable

Prof. Dr. Olaf Spinczyk (TU Dortmund)

Prof. Dr. Christian Lengauer (U. Passau)

IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Cluster Progress Report for Year 1

Cluster:
Operating Systems and Networks

Cluster Leader:

Prof. Giorgio Buttazzo (Scuola Superiore S. Anna)
http://feanor.sssup.it/~giorgio/

Policy Objective (abstract)
The objective of this cluster is to build the fundamental basis of a new real-time software technology that can provide a more efficient and predictable support to the development of future embedded systems, characterized by high complexity dynamic behaviour and distributed organisation. In particular, the new software technology should:

- simplify the management of resources to control the growing complexity and distribution of embedded systems;
- take advantage of parallel processing platforms, such as multicores, in order to satisfy timing and adaptivity requirements;
- support distributed computing to deal with the dynamics and ubiquitous nature of the computing infrastructure;
- increase system adaptivity to react to environmental changes, still providing a sufficient level of performance;

To cover these issues, the cluster is organized into 3 activities:

1. JPRA Cluster: Resource-Aware Operating Systems
2. JPRA Cluster: Scheduling and Resource Management
3. JPRA Cluster: Real-Time Networks

Versions

number	comment	date
1.0	First version delivered to the reviewers	December 19th 2008

Table of Contents

1. Overview

1.1 High-Level Objectives

The high level objective of this cluster is to build the fundamental basis of a new real-time software technology that can provide a more efficient and predictable support to the development of future embedded systems, characterized by high complexity dynamic behaviour and distributed organisation. In particular, the new software technology should:

- support scalability to facilitate the porting of control applications to different platforms;
- simplify the management of resources to control the growing complexity and distribution of embedded systems;
- take advantage of parallel processing platforms, such as multicores, in order to satify timing and adaptity requirements;
- be light-weight to opimize the usage of scarce resuources in tiny embedded computing devices;
- increase programming flexibility, for specifying functional and performance requirements to simplify test and verification;
- enable run-time reconfigurability and functionality updates to deal with the dynamics and ubiquitous nature of the supporting computing infrastructure;
- increase programming productivity, by raising the level of abstraction of the resource management services;
- increase system adaptivity to react to environmental changes, still providing a sufficient level of performance;
- be robust to tolerate transient and permanent overload conditions due to wrong design assumptions or unpredictable changes.

Such features would have a concrete impact on European industry to reduce time to market, and improve software reliability and testability. To support industry in such a transition phase, new tools, algorithms and kernel mechanisms must be also provided. In this respect, this cluster is playing an active role, acting as a bridge between the academic and the industrial world, especially in the domain of consumer electronics, robotics, industrial automation, telecommunications, and the so called cyber-physical systems.

A means to achieve such a goal is to develop a research platform for real-time systems to share competencies, resources, and tools targeting at the development of applications, such as control systems, with performance and timing requirements. The use of a shared platform is essential for experimenting new real-time software technology, including novel scheduling algorithms, resource management techniques, communication paradigms, energy-aware policies and overload handling approaches to increase robustness and predictability. A shared platform also facilitates the transfer of research results to industry, as it allows teaching practical knowledge of concepts and techniques. In addition, several solutions can be developed and tested in parallel in different partner sites, allowing the evaluation of the most appropriate approach for specific applications.

Specific research topics addressed in this cluster are related to operating systems and networks, with particular emphasis on scheduling and resource management, including energy-aware strategies and exploitation of parallelism in multicores.

1.2 Industrial Sectors

The industrial sectors that can benefit from adaptive real-time technology include Consumer Electronics, Industrial Automation, and Telecommunications.

Consumer Electronics (CE) products range from miniature cameras and MP3 players to advanced media servers and large displays. Mainly driven by Moore's law, the evolution in the CE industry is very fast [Bou05]. Utilizing available hardware and software resources in an optimal fashion is crucial both to save costs and to keep the competitive edge. Moreover, multimedia systems exhibit a highly dynamic behavior, since task execution times are often dependent on input data that are difficult to predict [Riz06]. As a consequence, these systems are prone to intermittent overload conditions that could degrade the performance in an unpredictable fashion [Wus05, Loo03]. To address these problems, the cluster aimed at integrating the most recent research results achieved in the real-time community to build flexible as well as predictable real-time systems that can react to load changes and perform QoS adaptation in a controlled fashion.

In the area of Industrial Automation there is a trend to use distributed solutions for connecting the general plant actuators, sensors and the controllers. At the same time, there is an increase of demands for new options and improvements in the automation results, fetching more control of plant secondary data. This imposes a continuous increment in processing power and memory capacity that requires adaptivity at different levels of system operation. The contribution of the cluster in this domain was to investigate how to achieve predictability and adaptivity in distributed systems.

Embedded systems for telecommunications applications are mainly targeted to the interfaces between communication technologies and to coding/decoding operations. They may be considered real-time as they have timeliness requirements for some of the critical operations they must perform. The referred systems are microprocessor based platforms, often integrating a second processor (e.g., a DSP) devoted to specific functions, like MPEG coding. From the software point of view, a modern mobile phone typically consists of several million lines of code with use-cases involving large number of concurrent activities. A system supporting ``memory and temporal protection'' would allow safely mixing real-time and non real-time applications with the benefit of achieving a more scalable platform. The work on resource reservation carried out in the cluster was of crucial importance to manage the increased complexity of the applications in this domain.

1.3 Main Research Trends

Today's embedded systems are required to work in dynamic environments, where the characteristics of the computational load cannot always be predicted in advance. The combination of real-time features in dynamic environments, together with cost and resource constraints, creates new problems to be addressed in the design of such systems, at different architecture levels.

To efficiently operate in dynamic environments, a system must be adaptive; that is, it must be able to adjust its internal strategies in response to a change in the environment, to keep the system performance at a desired level [Loo03, Eke05]. Implementing adaptive embedded systems requires specific support at different levels of the software architecture. The most important component affecting adaptiveness is the kernel, hence specific research efforts are being devoted to flexible, as well as predictable real-time scheduling and resource management policies [But06]. However, flexibility can also be introduced above the operating system, in a software layer denoted as a middleware. To investigate such a possibility, other research groups are working on this level to introduce adaptivity and QoS management [Sch03, Wan05, Sch06, Gar02].

Some embedded systems are large and distributed among several computing nodes. In these cases, special network methodologies are investigated to achieve adaptive behavior and predictable response [Alm03] [Ped05]. Several research efforts have also been placed in addressing wireless sensor networks (WSN) [Sta03], mobile ad-hoc networks MANET [Joh96, Wu04, Fac05] and other networked systems for which, albeit the dynamic nature and resource scarcity of the infrastructure, timeliness is still a requirement.

Finally, as the complexity of real-time systems increases, high demand will be placed on the programming abstractions provided by languages. Unfortunately, current programming languages are not expressive enough to prescribe certain timing behavior and hence are not suited for realizing predictable real-time applications. As a consenquence, most of the work on programming languages for real-time applications is aimed at providing real-time functionality via language constructs rather than operating system calls.

2. State of the Integration in Europe

2.1 Brief State of the Art

The main reason for investigating adaptive real-time systems is to provide predictability and flexibility for systems and environments where requirements on resources are inherently unstable and difficult to predict in advance. Such a difficulty is due to different causes. First of all, modern computer architectures include several low-level mechanisms that are designed to enhance the average performance of applications, but unfortunately introduce high variations on tasks' execution times. In other situations, as in multimedia systems, processes can have highly variable execution times that also depend on input data [Riz06]. As a consequence, the overall workload of a computing system is subject to significant variations, which can produce an overload and degrade the performance of the entire system in an unpredictable fashion [Loo03, Eke05]. This situation is particularly critical for small embedded devices used in consumer electronics, telecommunication systems, industrial automation, and automotive systems. In fact, in order to satisfy a set of constraints related to weight, space, and energy consumption, these systems are typically built using small microprocessors with low processing power and limited resources.

For most of these systems, the classical real-time approach based on a rigid off-line design, worst-case assumptions and a priori guarantee would keep resources unused for most of the time, therefore it is not acceptable for efficiency reasons. When resources are scarce, they cannot be wasted. On the other hand, an off-line design based on average-case behavior is also critical, because it would be difficult to guarantee timing constraints when resources are overloaded.

To prevent unpredictable performance degradations due to overloads, a real-time system must react to load variations, degrading its performance in a controlled fashion acting on system, as well as application parameters. The process of controlling the performance of a system as a function of workload variations is referred to as Quality of Service (QoS) Management. Performing efficient QoS management requires specific support at different levels of the system architecture. Hence, new software methodologies are emerging in Embedded Systems, which strictly relate to Real-Time Operating Systems (RTOS), Middleware, and Networks.

Real-time scheduling is the kernel mechanism having the most impact on RTOS performance. Most scheduling algorithms have been developed around one of three basic schemes: table driven [Foh95], fixed priority [Aud95], or dynamic priority [Spu96]. Depending on whether scheduling decisions are resolved before or during runtime, they are classified as offline or online.

Adapting to changing environmental situations may involve changes to task parameters at runtime. System wide changes, e.g., for changing operational modes in the system, have been addressed by mode change algorithms [Foh93].

Feedback scheduling changes task parameters, in particular periods [But02], to respond to online variations in the environment and current load conditions of the system. As both conditions can vary frequently, too frequent responses, which in turn influence the conditions, can introduce instability in the system. Feedback control scheduling applies control theory to estimate effects of changes and to choose parameters to provide for smooth responses and avoid instability [Cas06].

Each of the basic scheduling paradigms has specific advantages. When advantages of different schemes are demanded in the same system, more than one scheme could be used for different tasks. For example, in a complex system including hard periodic and soft aperiodic tasks, two scheduling schemes need to be integrated for satisfying the different requirements of each task class.

In hierarchical scheduling [Reg01] a meta algorithm arbitrates between a set of diverse scheduling algorithms. Thus, it can appear to the individual scheduling algorithms and their applications that they execute alone in the system. Furthermore, the amount of the CPU portion can be set individually for each scheduler and application. Special attention has to be given to shared resources.

In those systems subject to higly varialble workload, an overload condition could degrade the system performance in an unpredictable fashion. Novel scheduling methodologies have been recently proposed to cope with transient and permanent overload conditions. Transient overloads due to execution overruns can be effectively handled using resource reservation techniques [Mer94], according to which each activity consumes a fraction of the processing resource, independently of the actual execution demand. Permanent overload conditions, typically occurring in a periodic environment, can be efficiently handled by sporadic job skipping [Kor95] or by rate adaptation techniques (like elastic scheduling) [But02], which keep the load below a given threshold by acting on task periods.

Major needs for flexible scheduling techniques are typical of industries working in consumer electronics, industrial automation, and telecommunications, as resulted from a study carried out within the ARTIST 5FP project [Bou05].

For example, mobile terminals today are getting more and more advanced and their source code consists of several million lines of code involving a large number of parallel activities. For these applications, the use of flexible real-time scheduling techniologies would allow to safely mix real-time and non real-time processes. The benefit of such a solution would be a much more scalable platform. Adding and removing features would become predictable and less hazardous, allowing configuring the system without worrying about unpleasant surprises.

In the area of Industrial Automation, the continuous increment in processing power and memory capacity in local processors gives the opportunity to add new tasks into them, increasing system complexity in terms of supervision, diagnostics, presentation, communication, etc. Adaptive tasks scheduling that preserves the real-time constraints is a possible way to handle such situation and manage the complexity of the application.

In telecommunication companies, the main current interest seems to be in exploring the use of real-time extensions for the Linux OS. It also seems that QoS mechanisms are starting to be recognized as important for these embedded applications to increase the efficiency of subsystems and to support the possibility to serve more clients with similar levels of resources.

2.2 Main Aims for Integration and Building Excellence through ArtistDesign

Achieving adaptivity in embedded real-time systems is a complex task that requires expertize from several disciplines, including operating systems and kernels, scheduling theory, distributed systems, network communication, control theory, quality of service management, and programming languages. Combining the results achieved in such different domains and orchestrating the various groups active in these fields is only possible by a tight interaction among the cluster participants. Hence, the aim of the integration through ArtistDesign is to facilitate communication among cluster members in order to:

- Improve the understanding of the key features to be added at different architecture levels (operating system, network, middleware, and language) to support adaptive real-time systems;
- Clarify the terminology to provide a common language for exchanging information between different cluster and research communities;
- Build a common operating system platform to perform experiments and develop tools that can be shared by the different research teams;
- Identify new research directions aimed at overcoming the problems encountered during the integration phase;
- Interact with industries to understand their problems and identify possible solutions;
- Form new consortia and make concrete project proposals to address specific research problems or develop critical applications of industrial interest.

2.3 Other Research Teams

The cluster had several interactions with the following research teams:

- University of Illinois at Urbana Champagne (reference persons: Prof. Lui Sha, Prof. Tarek Abdelzaher, and Prof. Marco Caccamo) on wireless communication protocols for real-time distributed emebedded systems.
- University of Virginia (reference persons: Prof. John Stankovic and Prof. Sang Son) on adaptive real-time systems for sensor networks.
- University of Lund (reference persons: Karl-Erik Arzen and Anton Cervin) on feedback control tecniques for adaptive real-time systems.
- University of California at Berkeley (reference person: Alberto Sangiovanni Vincentelli) on the design of component-based operating systems.
- Philips Research Eindhoven (reference persons: Dr. Sjir van Loo) on resource management for consumer electronics.
- NXP (reference persons: Dr. Liesbeth Steffens) on resource management for consumer electronics.
- Ericsson Mobile Platforms (reference person: Dr. Johan Eker) on resource reservation and adaptive QoS management.
- Microchip Technology (reference person: Dr. Antonio Bersani) on real-time embedded platforms for monitoring and control.
- Carnagie-Mellon University (reference person: Prof. Raj Rajkumar) on wireless sensor networks, cooperative computing, andQoS adaptation.
- Seoul National University (reference persons: Dr. Jungkeun Park, Dr. Kanghee Kim) on distributed embedded systems and stochastic analysis of periodic task sets.
- Malardalen University, Sweden (reference person: Dr. Thomas Nolte) on integration of networked subsystems in resource constrained environments and on stochastic analysis of hybrid task sets.

2.4 Interaction of the Cluster with Other Communities

Interaction with the control community

There are at least two reasons that motivate a tight collaboration of the cluster with the control community. From the operating system prespective, the use of feedback control techniques allow making real-time embedded systems more reactive to environmental changes, hence system adaptivity can be improved by integrating control theory and real-time scheduling [Sta99]. From the control perspective, using flexible scheduling technologies allows making control systems more robust and predicatable: integrating feasibility analysis in the design of complex control systems allows the system designer to better analyze/control/compensate for delays and jitter caused by concurrency and intertask interference [Arz00].

A joint work involving people from Pavia, Pisa and Lund has been carried out on feedback control schemes to investigate the effects of different scheduling policies on delays and jitter in control loops.

Another strong collaboration has been established with the hybrid systems community. As a result of this connection, Giorgio Buttazzo has been invited as a co-Program Chair to organize the International Conference on Hybrid Systems: Computation and Control (HSCC 2007).

A joint work involving people from UPC (affiliated to TUKL) and Lund has been carried out to investigate feedback scheduling techniques. A PhD student from UPC spent 5 months in Lund working on the project.

Interaction with the cluster on compilers and timing analysis

A collaboration has been started with the cluster on compilers and timing analysis to investigate the problem of enhancing the predictability of real-time systems by reducing the variability of task execution times. In fact, internal kernel mechanisms, such as scheduling, mutual exclusion, interrupt handling and communication, can heavily affect task execution behaviour and hence the timing predictability of a system. For example, preemptive scheduling reduces program locality in the cache, increasing the worst-case execution time of tasks compared with non preemptive execution.

To address these issues, a new research was initiated that looks at predictability and efficiency in a synergistic manner and that involves all levels of abstraction and implementation in embedded-system design.

Thanks to the ArtistDesign NoE, the cluster got in contact with the cluster on Compilers and Timing Analysis. The two clusters started working together to develop a new approach consisting of a combination of several methods, including (a) design-space exploration on the hardware architecture level to identify good designs offering combinations of strong performance with good predictability, (b) appropriate kernel mechanisms for task and resource management that are predictable and analyzable, and (c) a synergistic development of models, design methods and matching analysis tools that extract precise system-behaviour properties.

Interaction with the consumer electronics industry

Thanks to the ArtistDesign NoE, the cluster got in contact with two major companies, Philips and Ericsson, acting in the domain of consumer electronics. After a tight interaction with the engineers responsible for the software development process, a number of industrial needs have been identified, that would make new generation products more robust and flexible.

To cope with a constantly increasing complexity of software applications (already consisting of several million lines of code and hundreds of concurrent activities), a system supporting memory and temporal protection would allow safely mixing real-time and non real-time applications with the benefit of achieving a more scalable platform. Therefore, the work on

resource reservation carried out within the cluster is of crucial importance to manage the increased complexity of the applications in this domain.

In addition, multimedia systems exhibit a highly dynamic behavior, since task execution times are often dependent on input data that are difficult to predict. As a consequence, these systems are prone to intermittent overload conditions that could degrade the performance in an unpredictable fashion. Again, the expertize existing in the cluster on overload management is of high interest for these companies, since it allows building flexible as well as predictable real-time systems that can react to load changes and perform QoS adaptation in a controlled fashion.

Interaction with the electronics industry

A new interaction of the cluster with Microchip Technology has been started on real-time embedded platforms for monitoring and control. In particular, the expertize existing in the cluster on real-time embedded control applications and real-time operating systems is extremely actractive for Microchip, who is interested in pushing the development of real-time embedded applications using 16-bit microcontrollers (as the dsPIC30 and the dsPIC33).

In this context, a big opportunity for the cluster is to find an agreament with Microchip to define the characteristics of a small real-time embedded platform for sensory acquisition and motor control that can be used (in conjunction with a wireless card) as a node of a mobile wirelss network. This unit would be more powerful and flexible than a mote and could be used to carry out experiments on sensor networks, embedded control, mobile robot teams and distributed control systems.

Interaction with the real-time components community

A collaboration between the clusters on components and adaptive real-time has been carried out along the ArtistDesign project. The main goal is to provide support for dealing QoS aspects in component-based systems. This technology is a relevant approach to complex system development and to allow a smooth integration of software from different vendors. QoS management is an adequate mean to provide a predictable quality to end-users. The collaboration between those clusters has brought competencies in component-based design for hard and adaptive real-time systems, to produce advances that would be difficult to achieve without all three.

This cooperation has facilitated the development of a number of technical achievents along four research lines: a) specification of QoS properties using UMNL profiles and aspect-based approachs, b) generation of analyzable models from the UML models, c) composition of QoS-aware components and adaptability, and d) QoS support in run-time components frameworks. The participants in this activity have actively participated in the development of a number of OMG standards

Dissemination

The cluster has been quite active in disseminating the research results achieved in the context of the ArtistDesign network of excellence, as an overall strategy for reaching other research/academic/industrial communities with related interests.

The platform developed in the context of the activity on Resource-Aware Operating System has been extensively used in graduate courses to teach how to develop embedded applications with real-time and performance requirements.

In addition, several scientific papers have been published and a number of workshops, and conferences have been organized by the cluster to spread the acquired knowledge in the

scientific community. The conferences and workshops in which the cluster has been involved include:

- OSPERT: Workshop on Operating Systems Platforms for Embedded Real-Time applications.
- ETFA: IEEE International Conference on Emerging Technologies and Factory Automation.
- RTSS: IEEE Real-Time Systems Symposium.
- ECRTS: Euromicro Conference on Real-Time Systems.
- RTAS: IEEE Real-Time and Embedded Technology and Applications Symposium.
- HSCC: ACM International Conference on Hybrid Systems: Computation and Control.
- RTCSA: IEEE International Conference on Embedded and Real-Time Computing Systems and Applications.
- IFAC World Congress.
- IECON: Annual Conference of the IEEE Industrial Electronics Society.
- WFCS: IEEE International Workshop on Factory Communication Systems.
- IECON: Annual Conference of the IEEE Industrial Electronics Society.
- RTN: International Workshop on Real Time Networks.
- OSERTS: Workshop towards Off-the-Shelf Embedded Real-Time Software.
- WPDRTS: International Workshop on Parallel and Distributed Real-Time Systems (In conjunction with IPDPS).
- Ada Europe: International Conference on Reliable Software Technologies.
- ISORC: IEEE International Symposium on Object and component-oriented Real-time distributed Computing.
- DIPES: IFIP Working Conference on Distributed and Parallel Embedded Systems.
- WTR: Brazilian Workshop on Real-Time Systems.
- RTNS: Int. Conf on Real-Time and Networked Embedded Systems.
- INCOM: IFAC Simposium on Information Control for Manufacturing.
- SAE World Congress.

Participation in Standards

Some cluster members are actively involved in the following standardization activities:

UML Profile QoS and Fault Tolerance

URL: http://www.artist-embedded.org/artist/UML-Profile-QoS-and-Fault.html

Member: Miguel A. de Miguel, UP Madrid.

Ada

URL: http://www.artist-embedded.org/artist/UML-Profile-QoS-and-Fault.html

Member: Alan Burns, Univ. of York.

POSIX 1003

URL: http://www.artist-embedded.org/artist/POSIX-IEEE-1003.html
Member: Michael Gonzalez Harbour, Univ. of Catabria.

MPEG Multimedia Middleware (M3W)

URL: http://www.artist-embedded.org/artist/MPEG-Multimedia-Middleware-M3W.html
Member: Alejandro Alonso, UP Madrid.

ETHERNET powerlink

URL: http://www.artist-embedded.org/artist/ETHERNET-Powerlink.html
Member: Lucia Lo Bello, Univ. of Catania (affiliated to Pisa).

References

[Alm03] L. Almeida. A Word for Operational Flexibility in Distributed Safety-Critical Systems. WORDS 2003, 8th IEEE Workshop on Object-oriented, Real-time and Dependable Systems, Guadalajara. Mexico, January 2003.

[Arz00] Karl-Erik Årzén, Anton Cervin, Johan Eker, Lui Sha, “An Introduction to Control and Scheduling Co-Design”, *39th IEEE Conference on Decision and Control,* Dec. 2000

[Aud95] N.C. Audsley and A. Burns and R.I Davis and K.W Tindell and A.J. Wellings, “Fixed Priority Preemptive Scheduling: An Historical Perspective”, Real-Time Systems, Vol. 8, pp. 173-198, 1995.

[But02] G. Buttazzo and L. Abeni, "Adaptive Workload Management through Elastic Scheduling", Real-Time Systems, Vol. 23, No. 1-2, pp. 7-24, July-September 2002.

[Bou05] Embedded Systems Design, The ARTIST Roadmap for Research and Development, Lecture Notes in Computer Science, Vol. 3436, Edited by Bruno Bouyssounouse and Joseph Sifakis, Springer, 2005.

[But06] G. Buttazzo, "Research trends in real-time computing for embedded systems", ACM SIGBED Review archive, special issue on major international initiatives on real-time and embedded systems, Vol. 3, No. 3, pp. 1-10, July 2006.

[Cas06] Rosa Castañé, Pau Martí, Manel Velasco, Anton Cervin and Dan Henriksson, “Resource Management for Control Tasks Based on the Transient Dynamics of Closed-Loop Systems”, 18th Euromicro Conference on Real-Time Systems 2006

[Eke05] “Embedded Software for Mobile Terminals”, Keynote Speech by Johan Eker; Ericsson Mobile Platforms AB. Euromicro Conference on Real-Time Systems (ECRTS 2005), Palma de Mallorca, Balearic Islands, Spain, July 6-8, 2005.

[Fac05] T Facchinetti, G. Buttazzo, L. Almeida. Dynamic Resource Reservation and Connectivity Tracking to Support Real-Time Communication among Mobile Units, EURASIP Journal on Wireless Communications and Networking, 2005(5): 712-730, December 2005.

[Foh93] G. Fohler. Changing operational modes in the context of pre run-time scheduling. IEIC transactions on information and systems, special issue on responsive computer systems, Nov 1993.

[Foh95] G. Fohler, "Joint Scheduling of Distributed Complex Periodic and Hard Aperiodic Tasks in Statically Scheduled Systems", in IEEE Real-Time Systems Symposium, December, 1995.

[Gar02] Marisol García-Valls, Alejandro Alonso, José F. Ruiz, Ángel Groba, “An Architecture for a Quality of Service Resource Manager Middelware for Flexible Multimedia

Embedded Systems", In Proceedings of the International Workshop on Software Engineering and Middleware - SEM 2002. Orlando, Florida (2002)

[Joh96] D. B. Johnson and D. A. Maltz, "Dynamic Source Routing in Ad Hoc Wireless Networks", In Mobile Computing, pp. 153-181, Kluwer Academic Publishers, 1996.

[Kor95] G. Koren and D. Shasha, "Skip-Over: Algorithms and Complexity for Overloaded Systems that Allow Skips", *Proceedings of IEEE Real-Time System Symposium*, December 1995.

[Loo03] "Living with uncertainty: A systems architect's view on real-time", Keynote Address by Sjir van Loo, Principal systems architect, responsible for the Philips Research long-term objectives for the Embedded Software Technology, Euromicro Conference on Real-Time Systems (ECRTS03), Porto, Portugal, 2-4 July 2003.

[Mer94] C. Mercer, S. Savage, and H. Tokuda, "Processor Capacity Reserves: Operating System Support for Multimedia Applications", IEEE International Conference on Multimedia Computing and Systems, 1994.

[Ped05] P. Pedreiras, P. Gai, L. Almeida, G. Buttazzo. FTT-Ethernet: A Flexible Real-Time Communication Protocol that Supports Dynamic QoS Management on Ethernet-based Systems. IEEE Transactions on Industrial Informatics, 1(3):162-172, August 2005.

[Reg01] John Regehr, John Stankovic, "HLS: a framework for composing soft real-time systems", Proc. RTSS 2001, London 2001.

[Riz06] L. Rizvanovic and G. Fohler, "Real-time Architecture for Networked Multimedia Streaming Systems", MiNEMA Workshop, 2006, Leuven, Belgium, February 2006.

[Sch03] Richard E. Schantz, Joseph P. Loyall, Craig Rodrigues, Douglas C. Schmidt, Yamuna Krishnamurthy, and Irfan Pyarali, "Flexible and Adaptive QoS Control for Distributed Real-time and Embedded Middleware", Middleware 2003, the ACM/IFIP/USENIX International Middleware Conference, Rio de Janeiro, Brazil, June 2003.

[Sch06] Richard E. Schantz, Joseph P. Loyall, Craig Rodrigues, Douglas C. Schmidt, "Controlling quality-of-service in distributed real-time and embedded systems via adaptive middleware", Software: Practice and Experience, Wiley, Vol. 36, No. 11-12, pp 1189-1208, 2006

[Spu96] M. Spuri and G. Buttazzo, "Scheduling Aperiodic Tasks in Dynamic Priority Systems", The Journal of Real-Time Systems, Vol. 10, No. 2, pp. 179-210, March 1996.

[Sta03] J. Stankovic et al. "Real-Time Communication and Coordination in Wireless Sensor Networks", In Proceedings of the IEEE, Vol. 91, N.7, July 2003.

[Sta99] J. Stankovic, C. Lu, S. Son, and G. Tao, "The Case for Feedback Control Real-Time Scheduling", *Euromicro Conference on Real-Time Systems*, June 1999.

[Wan05] X. Wang, D. Jia, C. Lu and X. Koutsoukos, Decentralized Utilization Control in Distributed Real-Time Systems, IEEE Real-Time Systems Symposium (RTSS'05), December 2005.

[Wu04] J. Wu and I. Stojmenovic, "Ad-Hoc Networks", IEEE Computer, vol. 37, no. 2, February 2004.

[Wus05] C. C. Wüst, L. Steffens, W. F. Verhaegh, R. J. Bril, and C. Hentschel, "QoS Control Strategies for High-Quality Video Processing", Real-Time Systems, Vol. 30, No. 1-2, pp. 7-29, May 2005.

3. Overall Assessment and Vision for the Cluster

3.1 Assessment for Year 1

The integration activities among the cluster participants is demonstrated by the number of joint publications, projects and events organized within the cluster. The main examples are our workshops, graduate courses, and the various research consortia that have led to new European projects, like FRESCOR, ACTORS, and PREDATOR.

3.2 Overall Assesment since the start of the ArtistDesign NoE

The overall assessment of the work carried out by the cluster within this first year is very good. The major benefit of the ArtistDesign NoE was to act as a large scientific arena, where different research groups had the possibility to discuss, interact, and collaborate for addressing challenging research problems in the complex domain of embedded systems. Such a collaborative work produced the following significant results:

- Education. A number of graduate courses, workshops and training laboratory activities have been organized to disseminate the knowledge of the cluster to graduate and PhD students.
- Challenging research issues. Different collaborations took place within the cluster that allowed exploiting complementary expertize available among the partners to address complex problems and propose interesting solutions. This can be assessed by the large number of joint papers produced by the cluster members.
- European projects. Several European projects started thanks to the integration activities triggered by ArtistDesign. Examples are ACTORS, PREDATOR, MORE, and INTERESTED.
- Bridge bewteen Industry and Academia. Several contacts with the industry have been established within ArtistDesign, which contributed to reduce the huge gap existing between the theoretical work carried out in the university and the applications developed by the companies. A significant effort has been made by the cluster to precisely define a common language between industry and academia.

3.3 Indicators for Integration

Interactions planned between partners include:

- 10 Joint publications / year in international journals and proceedings related to realtime and embedded computing systems;
- Organization of joint educational activities on real-time operating systems and networks, like training courses, summer schools, or student competitions;
- Organization of 3 workshops / year for discussing new trends and solutions on operating systems and networks;
- Creation of a repository for relevant publications, algorithms, and libraries related to real-time operating systems.

All these objectives has been achieved by the cluster in the first year, as reported in this deliverable.

3.4 Long-Term Vision

The long-term vision of the cluster is to build a significant amount of knowledge on problems, methodologies, techniques, and tools for embedded systems with highly dynamic behavior, so that it can be disseminated in the industry and in the academia to educate next generation engineers to make embedded systems more robust, more efficient, more flexible, and more predictable than what is possible today.

There are strong indications that adaptive real-time techniques will continue to be important for the embedded systems community. Scheduling and resource management must allow a higher flexibility to handle future applications, which are going to be more dynamic in terms of resource requirements.

The current industrial trend of developing multi-core platforms is introducing a higher degree of complexity that is pushing the research community towards new approaches and methodologies. In fact, the traditional programming model used so far in uniprocessor platforms is quite inadequate for systems consisting of multiple cores and needs to be completely revisited.

4. Cluster Participants

4.1 Core Partners

Cluster Leader **Activity Leader for "Resource-Aware Operating Systems"**	
	Prof. Giorgio Buttazzo Scuola Superiore Sant'Anna (SSSA), Pisa (Italy) URL: http://feanor.sssup.it/~giorgio/
Technical role(s) within ArtistDesign	Coordinating the cluster on Operating Systems and Network and the activity entitled "Resource-Aware Operating Systems". Providing support on real-time scheduling, operating systems, resource management, overload handling, energy aware algorithms, and quality-of-service strategies.
Research interests	Real-time operating systems, dynamic scheduling algorithms, quality of service control, multimedia systems, advanced robotics applications, and neural networks.
Role in leading conferences/journals/etc in the area	Editor-in-Chief of the Journal of Real-Time Systems (Springer). Associate Editor of the Journal of Embedded Computing (Cambridge International Science Publishing). Executive Board Member of the Euromicro Conference on Real-Time Systems. Program Chair of RTSS'01, ECRTS'03, EMSOFT'04, HSCC'07. General Chair of RTSS'02, EMSOFT'04, ECRTS'07. Reviewer for Real-Time Systems, IEEE Transactions on Computers, ACM Transactions on Embedded Computing. Program committee member of most real-time related conferences.
Notable past projects	"FIRST: Flexible Integrated Real-time Systems Technology", IST-2001-32467 (2002-2005) investigated advanced scheduling for handling applications with various real-time requirements. "OCERA: Open Components for Embedded Real-time Applications", IST-2001-35102 (2002-2005) integrated advanced real-time mechanisms in open-source kernels. "FABRIC: Federated Applications Based on Real_time Interacting Components", IST-2001-37167 (2002-2003) investigated QoS management methods for home networks.

	"ARTIST: Advanced Real-Time Systems", IST-2001-34820 (2002-2005) investigated adaptive real-time systems for QoS management. "TRACS - Flexible Real-Time Architecture for Traffic Control Systems", ESPRIT III project No. 6373 (1992-1995) investigated real-time techniques for vessel control systems.
Awards	Best paper Award at the 10th Int. Conference on Real-Time and Embedded Computing Systems and Applications (RTCSA 2004), Gothenburg, Sweden, August 2004. Paper: "The Jitter Margin and Its Application in the Design of Real-Time Control Systems". Award for the best paper and presentation at the ANIPLA Workshop on Operating Systems for Industrial Control Applications, Milan, November 18, 1999. HUSPI Award given by Honeywell for the best journal publication on robotic systems, November 1987.
Further Information	Senior Member of IEEE

Team Leader **Activity Leader for "Scheduling and Resource Management"**	
	Professor Alan Burns University of York, UK URL: www.cs.york.ac.uk/~burns
Technical role(s) within ArtistDesign	Undertakes research in real-time systems scheduling, particularly for flexible systems. Also concerned with the development of programming languages for this domain.
Research interests	Scheduling, languages, modelling and formal logics.
Role in leading conferences/journals/etc in the area	Previous Chair of the IEEE Technical Committee on Real-Time Systems. Edited special issue of ACM Transactions on Embedded Systems (on education).
Notable past projects	DIRC – Dependability Interdisciplinary Research Collabroations – A large, UK, 6-year, multisite project looking at dependability of computer-based systems. Burns was a PI and manged the work on temporal aspects of dependability. FIRST – EU funded project concerninf flexibile scheduling FRESCOR – EU follow on project to FIRST

Team Leader	
	Prof. Gerhard Fohler Technical Univeristy of Kaiserslautern (TUKL) URL: www.eit.uni-kl.de/fohler
Technical role(s) within ArtistDesign	The role of TUKL is to investigate resource management policies for controlling the quality of service in multimedia applications. The team is leading the activity on Adaptive Resource Management for Consumer Electronics and is involved in the development and analisys of algorithms for video streaming applications. A further focus is on flexible scheduling, with the aim of integrating offline and online approaches.
Research interests	Real-time scheduling, integration of offline and online scheduling, QoS management, video streaming and media processing.
Role in leading conferences/journals/etc in the area	Chairman, technical committee on real-time systems, Euromicro Member of executive board technical committees on, IEEE real-time systems, IE embedded systems Area editor real-time, Journal of System Architecture, Elsevier Program chair, IEEE Real-Time Systems Symposium, 2006 Program chair, subtrack real-time systems, DATE 2005-2007 Program committee member of most real-time related conferences
Notable past projects	FRESCOR - Framework for Real-time Embedded Systems based on COntRacts, EU IST STREP WASP - Wirelessly Accessible Sensor Populations, EU IST IP BETSY - BEing on Time Saves energY continuous multimedia experience with low battery power, EU IST STREP FIRST - Flexible Integrated Real-Time System Technology, EU IST STREP FABRIC: “Federated Applications Based on Real_time Interacting Components”, IST-2001-37167 (2002-2003) investigated QoS management methods for home networks.

Team Leader	
	Prof. Michael González Harbour Universidad de Cantabria http://www.ctr.unican.es/
Technical role(s) within ArtistDesign	The role of University of Cantabria is to provide support for schedulability analysis of embedded distributed systems with real-time requirements. The Group has also developed methodologies and tools for software engineering of real-time systems in which a mixture of soft and hard deadlines can be found and as such is leading the activity on Flexible Scheduling Technologies. The group is also actively participating in the development of the Real-time POSIX operating systems standards, and is active in real-time languages, (Ada) and therefore contributing to the platform being used in the Real-Time Languages activity. One important goal of the Group has always been to test the results of basic research in practical applications. As a consequence, the Group has contacts with industrial companies in the field of industrial automation.
Research interests	Real-Time Schedulability Analysis, Real-Time Operating Systems, Real-Time Languages, Real-Time networks
Role in leading conferences/journals/etc in the area	Program chair of ECRTS 07, Program Co-Chair of the International Conference on Reliable Software Technologies 2006, Program Committee Member of RTAS, RTSS, ECRTS, and various Workshops on real-time systems.
Notable past projects	FRESCOR, Framework for Real-time Embedded Systems based on COntRacts. The FRESCOR project is aimed at developing a framework that integrates advanced flexible scheduling techniques directly into an embedded systems design methodology, covering all the levels involved in the implementation, from the OS primitives, through the middleware, up to the application level (www.frescor.org)

Team Leader **Activity Leader for "Real-Time Networks"**	
	Prof. Luis Almeida University of Aveiro URL: http://www.ieeta.pt/lse
Technical role(s) within ArtistDesign	Leader of the team from the University of Aveiro.
Research interests	Real-time communication (traffic scheduling, protocols,…) Flexible architectures for distributed embedded systems
Role in leading conferences/journals/etc in the area	Usually participates in the Organizing and /or Program Committees of conferences in the fields of Real-Time Systems (e.g., RTSS, ECRTS, RTAS) and industrial communications (e.g., WFCS, ETFA, FET). Has chaired several workshops (e.g., RTN, WTR, WiP sessions). Reviewer for several related journals (e.g., IEEE TII, TIE, TC, ACM TECS, Kluwer JRTS)
Notable past projects	ARTIST (FP5 accompaning measure). CAMBADA – Cooperative Autonomous roBots with Advanced Distributed Architecture. Specification and development of a team of cooperating autonomous robots for the Robocup Middle-Size Soccer League. Particular focus has been devoted to the architecture of each robot and their communication for information sharing. http://www.ieeta.pt/atri/cambada/ DISCO, DIStributed embeddable systems for COntrol applications. The objectives of the project were to investigate techniques and to develop solutions to improve flexibility and adaptability in distributed embedded control systems in order to reduce operation and maintenance costs while maximising the utilisation of system resources. http://www.ieeta.pt/lse/DISCO_web.pdf CIDER, Communication Infrastructure for Dependable and Evolvable Real-time systems. The project pursued two objectives: to analyse the usability of Ethernet in dependable applications (static set-up) and to devise the necessary mechanisms to allow the set-up to change dynamically (dynamic set of services and hosts) while providing the required dependability. http://www.hurray.isep.ipp.pt/activities/cider/
Awards	Best Paper Award in WFCS 2004 Best Paper Award in SICICA 2000

Team Leader	
	Prof. Eduardo Tovar Polytechnic Institute of Porto (ISEP-IPP), Porto (Portugal) URL: http://www.hurray.isep.ipp.pt/asp/show_people.asp?id=1
Technical role(s) within ArtistDesign	The role of ISEP-IPP team is to investigate distributed embedded systems, with a particular focus on communication protocols for WSN and MANETs. The team is leading the activity on Real-Time Networks and involved in flexible scheduling technologies, resource management policies and QoS-aware collaborative computing. The team has also a strong commitment in Real-Time Languages.
Research interests	Real-time systems, wireless sensor networks, multiprocessor platforms, communication networks, factory automation and system integration.
Role in leading conferences/journals/etc in the area	Executive Board Member of the Euromicro Technical Committee on Real-Time Systems. Program Chair ECRTS'05, RTN'02, WDES'06. General Chair of WFCS'00, ECRTS'03. Program committee member in several editions of ERCTS, RTSS, RTAS, RTCSA, ICDCS, SRDS, WFCS, ETFA, EMSOFT and other IEEE, ACM and Euromicro events on real-time systems, embedded systems and factory communication systems. Reviewer for Real-Time Systems, IEEE Transactions on Computers, ACM Transactions on Embedded Computing, IEEE Transactions on Industrial Informatics.
Notable past projects	"REMPLI: Real-time Energy Management via Power-lines and Internet", NNE5-2001-00825 (2003-2006) investigated advanced scheduling and protocols for power-line communication systems (PLC). "R-Fieldbus: High Performance Wireless Fieldbus in Industrial Multimedia-Related Environment", IST-1999-11316 (2001-2003), integrated advanced real-time mechanisms in hybrid wired/wireless fieldbus neworks. Mobility protocols and end-to-end deadlines.. "CABERNET: Network of Excellence in Distributed Computing Systems Architectures", IST-2000-25088 (2001-2003). "CIDER: Communication Infrastructure for Dependable Evolvable Real-time systems", POSI/1999/CHS/33139 (2001-2003), Portuguese Science Foundation project on real-time communication networks.
Further Information	Senior Member of IEEE

Team Leader **Activity Leader for "Design for Adaptivity"**	
	Professor Karl-Erik Årzén Lund University URL: http://www.control.lth.se/user/karlerik/
Technical role(s) within ArtistDesign	Leader for the Transversal activity "Design for Adaptivity". Team leader for Lund University. Participates in the OS and Networks cluster
Research interests	Embedded control, real-time systems, adaptive resource management, veedback applied to computer systems
Role in leading conferences/journals/etc in the area	CoChair 4th Intl. Workshop on Feedback Control Implementation and Design in Computing Systems & Networks (FeBID 2009)
Notable past projects	RUNES, ARTIST2, ACTORS (ongoing)
Awards	The Dr Guido Carlo-Stella award in manufacturing automation from the World Batch Forum in 2006 for achievements in manufacturing automation and information structuring

Team Leader	
	Dr. Stylianos Mamagkakis IMEC vzw. http://www.imec.be
Technical role(s) within ArtistDesign	Representing IMEC Nomadic Embedded Systems (NES) division in: -Cluster: SW Synthesis, Code Generation and Timing Analysis -Cluster: Operating Systems and Networks -Cluster: Hardware Platforms and MPSoC Design -Intercluster activity: Design for Adaptivity -Intercluster activity: Design for Predictability and Performance -Intercluster activity: Integration Driven by Industrial Applications

Research interests	Stylianos Mamagkakis received his Master and Ph.D. degree in Electrical and Computer Engineering from the Democritus Uni. Thrace (Greece) in 2004 and 2007, respectively. Since 2006, he coordinates a team of PhD students within the NES division at IMEC, Leuven, Belgium. His research activities mainly belong to the field of system-level exploration, with emphasis on MPSoC run-time resource management and system integration.
Role in leading conferences/journals/etc in the area	Stylianos Mamagkakis has published more than 35 papers in International Journals and Conferences. He was investigator in 9 research projects in the embedded systems domain funded from the EC as well as national governments and industry.
Notable past projects	Project leader of MNEMEE IST project www.mnemee.org Project leader of OptiMMA IWT project www.imec.be/OptiMMA Participation in: 1 international IMEC project (M4), 3 European IST projects (AMDREL, EASY, ARTIST2), 2 Greek projects (PRENED, DIAS)
Awards	1st prize in 'Technogenesis' Competition for Business Innovation, Greece, June'06 3rd prize in 'Otenet Innovation 2006' Competition for Business Innovation, Greece, November'06
Further Information	http://www2.imec.be/imec_com/nomadic-embedded-systems.php

4.2 Affiliated Industrial Partners

Team Leader	
	Dr. Paolo Gai (Ph.D.) Evidence srl (Italy) URL: http://feanor.sssup.it/~pj/
Technical role(s) within ArtistDesign	Support for the SHaRK kernel maintenance, consulting on POSIX and OSEK standards, real-time kernels, design and analysis tools.
Research interests	Real-time scheduling, operating systems, design and analysis tools.
Notable past projects	FIRST: Flexible Integrated Real-time Systems Technology, IST-2001-32467 (2002-2005) investigated advanced scheduling for handling applications with various real-time requirements. OCERA: Open Components for Embedded Real-time Applications, IST-2001-35102 (2002-2005) integrated advanced real-time mechanisms in open-source kernels. ARTIST: Advanced Real-Time Systems. (http://www.artist-embedded.org)

4.3 Affiliated Academic Partners

Team Leader	
	Professor Juan A. de la Puente Universidad Politécnica de Madrid URL: http://www.dit.upm.es/jpuente
Technical role(s) within ArtistDesign	Team Leader of the Universidad Politécnica de Madrid, UPM leader on “Real-Time languages” and “Common infrastructure for Adaptive Real-Time Systems”
Research interests	Design of real-time systems, high-integrity systems, programming languages, scheduling, control systems and distributed systems

Role in leading conferences/journals/etc in the area	Associate editor of the Journal of Real-Time Systems. Participation in the Programme Committee of conferences such as Euromicro Real-Time Systems, International Conference on Reliable Software Technologies.
Notable past projects (optional – max 5)	ASSERT: Developmet of advance software techniques for high integrity systems for aerospace systems. TRECOM: Techniques for the development of advanced distributed real-time systems for safety and business critical systems. ORK (Open Ravenscar Real-TIme Kernel): Development of a kernel for safety-critical space systems.
Awards / Decorations	IFAC Fellow

Activity Leader for "Qos-aware components"	
	Prof. Alejandro Alonso Universidad Politécnica de Madrid. URL: http://www.dit.upm.es/aalonso
Technical role(s) within ArtistDesign	Activity Leader for "Qos-aware components" UPM leader on Adaptive resource management for CE"
Research interests	Design of real-time systems, programming languages, scheduling, distributed systems and quality of service
Role in leading conferences/journals/etc in the area	Participation in the Programme Committee of conferences such as Euromicro Real-Time Systems, International Conference on Reliable Software Technologies.
Notable past projects	MORE: Network-centric Middleware for GrOup communication and Resource Sharing across Heterogeneous Embedded Systems HIJA: High-Integrity Java Applications. The goal is to develop a new Java-based middleware platform fo the creation of Architecture-Neutral, high-integrity, distributed Real-Time Systems (ANRTS) ROBOCOP and Space4U. Development of component framework for embedded devices. It includes support for QoS and resource management. TRECOM: Techniques for the development of advanced distributed real-time systems for safety and business critical systems.

Team Leader	
	Prof. Hermann Härtig Dresden University of Technolgy URL: http://os.inf.tu-dresden.de/~haertig/
Technical role(s) within ArtistDesign	
Research interests	
Role in leading conferences/journals/etc in the area	
Notable past projects	

Team Leader	
	Name: Alfons Affiliation: Universidad Politécnica de Valencia, Spain URL: http://www.gii.upv.es/personal/alfons/
Technical role(s) within ArtistDesign	Real-time control on embedded platforms
Research interests	Virtualisation, hypervisor, real-time operating system, dynamic memory management
Role in leading conferences/journals/etc in the area	Program Committee member Reviewer
Notable past projects	ARTIST2: Network of Excellence on Embedded Systems Design. U.E. IST Programme - IST 004527. 2004-08 FRESCOR: Framework for Real-time Embedded Systems based on COntRacts FRESCOR. U.E. IST Programme - IST 034026. 2006-2009 THREAD: Integral support for embedded, distributed open real-time

	systems Spanish Ministry of Education, Science and Technology - TIC2005-08665-C03. 2005-2008 SENSE: Smart Embedded Network of Sensing Entities. U.E. IST Programme - IST 033279. 2006-2009 TECOM: Trusted Embedded Computing. Programme ITEA-2 and PROFIT (M. Industria, Spanish Governement). 2007-2010 OCERA: Open Components for Embedded Real-Time Applications. U.E. IST Programme (IST 35102). 2002-05

Team Leader	
	Prof. Jean-Dominique Decotignie Ecole Polytechnique Fédérale de Lausanne (Switzerland) URL: http://lamspeople.epfl.ch/decotignie/
Technical role(s) within ArtistDesign	
Research interests	
Role in leading conferences/journals/etc in the area	
Notable past projects	

Team Leader	
	Prof. Lucia Lo Bello University of Catania (Italy) – Affiliated to SSSA, Pisa URL: http://www.diit.unict.it/users/llobello/
Technical role(s) within ArtistDesign	Support for the SHaRK kernel maintenance. Implementation of industrial multimedia system using SHARK. Execution time measurement. Stochastic analysis of soft real-time tasks in the context of priority-driven soft real-time systems. Calculation of stochastic response time profiles of tasks that are hierarchically scheduled using server based techniques. Support for real-time communication in distributed embedded

	systems, with particular reference to networked embedded systems used in factory communication and in automotive environments. Real-time communication over wireless networks: modelling, timing analysis, and transmission scheduling to support soft real-time traffic over 802.11, 802.15.4 and Bluetooth networks. Design issues and protocols for wireless sensor networks and networked embedded systems.
Research interests	Real-time scheduling, overload handling, real-time communication protocols, factory communication, real-time communication over wireless networks, wireless sensor networks, automotive communications.
Role in leading conferences/journals/etc in the area	Program Chair of ETFA 05, ETFA 07. WIP Chair of ETFA 06. General Chair of ECRTS 04. PC member of many editions of ECRTS, RTSS;,RTAS,ETFA, WFCS, RTN , FET, RTNS ,WTR. Reviewer for the Real-Time Systems Journal, IEEE Transactions on Industrial Informatics, IEEE Transactions on Industrial Electronics, IEEE Transactions on Computers, Computer Standard and Interfaces, Journal of System Architectures. On the Editorial Board of the International Journal of Embedded Systems.
Notable past projects	Italian National project PRIN 04 entitled “Study and development of a realtime land control and monitoring system for fire prevention”, funded by the Italian Ministry of University and Research (http://www.prin.polito.it/) European project ESPRIT 26951 "NOAH - Network Oriented Application Harmonisation. Italian National COFIN 2001 inter-university project titled ‘’High-Performance Processing for Applications with High-Intensity Computational Requirements and Real-Time Constraints, funded by the Italian Ministry of University and Research (http://tsc.polito.it:7777/cofin2001/)
Further Information	Member of the International Electrotecnical Commission (IEC), Technical Committee SC65C, Working Group 11, Real-Time Industrial Ethernet (RTE), actively involved in standardization activities. Nominated expert member for the Italian Electrotechnical Committee (CEI-Comitato Elettrotecnico Italiano) in the Technical Committee SC65C “Digital Data Communications for Measurement and Control-Fieldbus for Use in Industrial Control Systems”, Maintenance Team 9, “High availability automation networks". Member of the Technical Committee on Factory Automation of the Industrial Electronics Society (IES). Co-chair of the Subcommittee 10 “Intelligent Sensors and Sensor Networks in Industrial & Factory Automation”.

Team Leader	
	Dr. Pau Martí Technical University of Catalonia, Barcelona, Spain URL: http://www.upcnet.es/~pmc16/
Technical role(s) within ArtistDesign	Real-time systems and control systems co-design
Research interests	Real-time and control systems, overload handling, jitter analsyis and compensation, control theory.
Role in leading conferences/journals/etc in the area	Program committee member of major real-time and control conferences. Reviewer for the Real-Time Systems Journal.

Team Leader	
	Prof. Ivo De Lotto Robotic Lab, University of Pavia, Italy http://www.unipv.it/ingegneria/servizi/scheda.php?mat=000300
Technical role(s) within ArtistDesign	Provide support for the development of real-time control applications in the domain of robotics and automation.
Research interests	Sensory systems, robotics applications, wireless communication, energy-aware computing.
Role in leading conferences/journals/etc in the area	Program committee member of major conferences on robotics. Reviewer of International journals on robotics. Member of the evaluation committee for national projects.
Awards / Decorations	Gold Medal of Italian Ministry of Education (1988)

Team Leader	
	Prof. Marisol García-Valls Universidad Carlos III de Madrid URL: http://www.it.uc3m.es/mvalls
Technical role(s) within ArtistDesign	UC3M leader on Adaptive resource management for CE”

Research interests	Distributed embedded systems, design and modelling of real-time systems, real-time programming languages, quality of service
Role in leading conferences/journals/etc in the area	Member of the Programme Committee of conferences such as ARCS 06, EstiMedia 04-06, JTRES 03-04, EUC 05, EMSOFT 03-04 Reviewer of the Real-Time Systems Journal
Notable past projects	ARTIST: Advanced Real-Time Systems. URL: http://www.artist-embedded.org MUSE: MUlti Service Access Everywhere Everyware: Personalized services in ubiquitous environments

Team Leader	
	Prof. Julian Proenza University of the Balearic Islands URL: http://dmi.uib.es/research/SRV/jpa_ppl_en.htm
Technical role(s) within ArtistDesign	Team leader of affiliated partner. Indirect participation in the Cluster, with the core team University of Aveiro
Research interests	Dependable and Real-Time Systems, in particular, on fault-tolerant distributed systems, clock synchronization and field-bus networks, like CAN (Controller Area Network).
Role in leading conferences/journals/etc in the area	Chair of several workshops in his fields of interest. Participation in several Organizing and Program Committees of related events.

4.4 Affiliated International Partners

	Professor Tarek Abdelzaher, University of Illinois at Urbana-Champaign http://www.cs.uiuc.edu/homes/zaher/

Technical role(s) within ArtistDesign	Technical expert
Research interests (optional)	Operating systems, networking, sensor networks, distributed systems, and embedded real-time systems.

	Professor Lui Sha, University of Illinois at Urbana-Champaign http://www.cs.uiuc.edu/directory/directory.php?name=sha
Technical role(s) within ArtistDesign	Technical expert.
Research interests	Distributed real-time computing systems, dynamic real-time architecture, QoS driven resource management and security and fault tolerance in networked embedded systems.

	Professor Sanjoy Baruah, University of North Carolina at Chapel Hill http://www.cs.unc.edu/~baruah/
Technical role(s) within ArtistDesign	Technical expert.
Research interests	Schedulability analysis and multiprocessor systems.

5. Internal Reviewers for this Deliverable

Karl-Erik Arzen (Univ. of Lund, Sweden)

Marco Caccamo (University of Illinois at Urbana Champaign, USA)

IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Transversal Activity - Progress Report for Year 1

Cluster:
Hardware Platform and MPSoC Design

Cluster Leader:

Prof. Jan Madsen (Technical University of Denmark)
http://www.imm.dtu.dk/

Policy Objective (abstract)

The purpose of this cluster is to integrate different view points and approaches to MPSoC design and programming. The cluster will consider the hardware architecture and software components in their interaction, investigate tools for accurate estimation of certain design parameters (power, performance), and provide the designer with adequate support for design space exploration and optimization.

Versions

number	comment	date
1.0	First version delivered to the reviewers	December 19th 2008

Table of Contents

1. Overview

In relation to the ArtistDesign network, it is the overall goal of the topic on hardware platforms and MPSoC design to extend the current state in composability towards issues like modelling of non-functional constraints, power and energy, end-to-end real-time behaviour, timing and performance analysis and heterogeneous models of computation.

Many application domains require adaptive real-time embedded systems that can change their functionality over time. In such systems it is not only necessary to guarantee timing constraints in every operating mode, but also during the transition between different modes. Therefore, it is one of the goals to develop new methods for the design and analysis of adaptive multi-mode systems.

One of the most critical issues to be faced in the research on execution platform is their rapidly growing complexity. Complexity increase is pushed by Moore's law, and by the ever-increasing demand for high performance computing. In addition, the boundaries between hardware and software domains are getting more blurred (dynamically re-configurable hardware, adaptable embedded systems, breakthrough in power consumption and performance) and challenging questions are at the border (trade-offs in mapping applications to hardware and software components, re-configurable hardware, WCET, performance of distributed computer and communication systems).

The cluster attempts to combine the diverse knowledge and to integrate different approaches in the area of execution platforms for embedded systems available in Europe and beyond.

1.1 High-Level Objectives

The purpose of this cluster is to integrate different view points and approaches to MPSoC design and programming. Therefore, the work is based on existing and future hardware platforms and their expected properties as well as anticipated application domains. The cluster will consider the hardware architecture and software components in their interaction, investigate tools for accurate estimation of certain design parameters (power, performance) based on appropriate models for hardware and software components, and provide the designer with adequate support for design space exploration and optimisation.
The importance of resource awareness in embedded systems is growing very rapidly. One major aspect is predictability, in particular concerning the timing behaviour. With the growing software content in embedded systems, and the diffusion of highly programmable and re configurable platform, software is given an unprecedented degree of control on resource utilization. Therefore, the major focus of the combined activities is to establish a design methodology that;

- scales to massively parallel and heterogeneous multiprocessor architectures,
- allows for predictable system properties
- uses the available hardware resources in an efficient manner.

Promising approaches are based on increasing the adaptivity on various levels and on composable frameworks.

1.2 Industrial Sectors

As hardware platforms are the backbone of embedded systems, the activities of this cluster spans all industrial sectors. A recent and accelerating trend is the move towards multicore platforms.

In the automotive domain, the increasing number of functions has led to automotive networks with a large number of distributed ECUs and increasing complexity with several busses and gateways that is difficult to handle. In next generation systems, large automotive OEMs are therefore proposing new structured hardware topologies, that focus on the application of powerful domain controllers connected over a high speed bus and several dedicated busses for the different functional domains. Multicore control units (MCUs) are perceived as a co-enabler for this technology, by allowing the integration of a large number of functions, at relatively low power and with various reliability and fail-safe options.

A similar trend can be observed in the aerospace domain, where multicore components need to be integrated into complex networks with commonly very high reliability requirements.

In the multimedia domain, the emerging trend for multimedia applications on mobile terminals, combined with a decreasing time-to-market and a multitude of standards have created the need for flexible and scalable computing platforms that are capable of providing considerable (application specific) computational performance at a low cost and a low energy budget. Platforms like TI OMAP, ST Nomadik, Philips Nexperia and IBM/Toshiba/Sonys CELL, contain multiple heterogeneous, flexible processing elements, a memory hierarchy and I/O components. All these components are linked to each other by a flexible on-chip interconnect structure. These architectures meet the performance needs of multimedia applications, while limiting the power consumption.

Also in the mechatronics domain, which traditionally was a rather sequential process, there is a trend towards multi-core platforms and the need to support the designer to make well-founded choices for an execution platform. Techniques from the multimedia domain are now being extended and adapted to deal with control-dominated high-tech applications as well.

Another clear trend is towards reconfigurable architectures, in general, and configurable processors, in particular. The generic goal is to achieve a high degree of flexibility (traditionally available only with software implementation) at an power consumption, which is much lower than achievable with a traditional software implementation using general purpose processors.

1.3 Main Research Trends

Many embedded system applications are implemented today using distributed architectures, consisting of several hardware nodes interconnected in a network. Each hardware node can consist of a processor, memory, interfaces to I/O and to the network. The networks are using specialized communication protocols, depending on the application area. For example, in the automotive electronics area communication protocols such as CAN, FlexRay and TTP are used. One important trend today is toward the integration of multiple cores on the same chip, hence embedded systems are not only distributed across multiple boards or chips, but also within the same chip.

As the complexity of the functionality increases, the way it is distributed has changed. If we take as an example the automotive applications, initially, each function was running on a dedicated hardware node, allowing the system integrators to purchase nodes implementing required functions from different vendors, and to integrate them into their system. Currently, number of such nodes has reached more than 100 in a high-end car, which can lead to large cost and performance penalties. Moreover, with the advent of poly-core (i.e. high cardinality multi-core) single-chip platforms, the effective number of processing nodes tends to grow in a “fractal” way, and future distributed systems with thousands of processing nodes are not a far away dream.

Not only the number of nodes has increased, but the resulting solutions based on dedicated hardware nodes do not use the available resources efficiently in order to reduce costs. For example, it should be possible to move functionality from one node to another node where

there are enough resources (e.g., memory) available. Moreover, emerging functionality, such as brake-by-wire, is inherently distributed, and achieving an efficient fault-tolerant implementation is very difficult in the current setting.

Moreover, as the communications become a critical component, new protocols are needed that can cope with the high bandwidth and predictability required. The trend is towards hybrid communication protocols, such as the FlexRay protocol, which allows the sharing of the bus by event-driven and time-driven messages. Time-triggered protocols have the advantage of simplicity and predictability, while event-triggered protocols are flexible and have low cost. A hybrid communication protocol like FlexRay offers some of the advantages of both worlds. The need for scalable and predictable communication is not only a characteristic of automotive designs, but even multimedia and signal processing systems are increasingly communication dominated.

While computation and communication are clear targets, common consensus has been growing on the criticality of memory architecture and related memory management software challenges. Even predictable and efficient processors and communication fabrics are not sufficient to provide a predictable and efficient application level view of the platform if not adequately supported by a memory system.

The trend towards distributed architectures introduces a new challenge. A lot, if not most of the traditional software is sequential in nature. Major reason for this is that most modern programming languages are sequential and do not have adequate language-level concurrency support. Traditionally the timing performance of software increased as a result of the increase in clock speed of the individual processing cores. However, this free lunch is over because clock speeds have hardly increased since 2003. Multi-core and hyperthreading techniques are now used to boost platform performance. Modern compilers based on sequential programming languages are not able to sufficiently utilize these additional computational resources. New languages, techniques and tools are required that seamlessly match modern execution platforms, for instance by adequate application-level concurrency support. Although a number potential techniques already exist, getting more momentum in these directions is crucial to deal with future complexity and performance requirements.

With growing embedded system complexity more and more parts of a system are reused or supplied, often from external sources. These parts range from single hardware components or software processes to hardware-software (HW-SW) subsystems. They must cooperate and share resources with newly developed parts such that the design constraints are met. There are many software interface standards such as CORBA, COM or DCOM, to name just a few examples that are specifically designed for that task. Nevertheless in practice, software integration is not a solved but a growing problem. This is especially true when performance and energy efficiency can be achieved only if a sufficient degree of parallelism in application execution is achieved.

New design optimization tools are needed to handle the increasing complexity of such systems, and their competing requirements in terms of performance, reliability, low power consumption, cost, time-to-market, etc. As the complexity of the systems continues to increase, the development time lengthens dramatically, and the manufacturing costs become prohibitively high. To cope with this complexity, it is necessary to reuse as much as possible at all levels of the design process, and to work at higher and higher abstraction levels, not only for specification of overall system functionality, but also for supporting communication among a number of parallel executing nodes.

One of the most significant achievements in the cultural landscape of low-power embedded systems design is the consensus on the strategic role of power management technology. It is now widely acknowledged that resource usage in embedded system platforms depends on application workload characteristics, desired quality of service and environmental conditions.

System workload is highly non-stationary due to the heterogeneous nature of information content. Quality of service depends on user requirements, which may change over time. In addition, both can be affected by environmental conditions such as network congestion and wireless link quality.

Power management is viewed as a strategic technology both for integrated and distributed embedded systems. In the first area, the trend is toward supporting power management in multi-core architectures, with a large number of power-manageable resources. Silicon technology is rapidly evolving to provide an increased level of control of-on chip power resources. Technologies such as multiple power distribution regions, multiple power-gating circuits for partial shutdown, multiple variable-voltage supply circuits are now commonplace. The challenge now is how to allocate and distribute workload in an energy efficient fashion over multiple cores executing in parallel. Also, one open issue is how to cope with the increasing amount of leakage in nanometer technologies, which tends to over-emphasize the cost of inactive logic, unless it can be set in a low-power idle state (which in many cases implies storage losses and high wakeup cost).

In the area of distributed low-power systems, wireless sensor networks are the key technology drivers, given their tightly power constrained nature. One important trend in this area is toward “battery free” operation. This can be achieved through energy storage devices (e.g. super-capacitors) coupled with additional devices capable of harvesting energy from environmental sources (e.g. solar energy, vibrational energy). Battery-free operation requires carefully balancing harvested energy and stored energy against the energy consumed by the system, in a compromise between quality of service and sustainable lifetime.

The concept of Multiprocessors-on-a-chip (MPSoC) has been discussed since some years but it appears that recently, the area has gained much more interest. In terms of industrial support, an increasing number of companies are active in the design of corresponding architectures as well as introducing the first products in the market. Whereas there are major breakthroughs in terms of new hardware architectures, corresponding programming environment are still at their infancy. In particular, ease of application specification, scalability, predictability of the overall system, parallelization, low power operation, efficiency and support of legacy code are just some of the main problems the community is facing.

A major industrial concern that comes with the integration of previously independent functions onto a single multicore or multiprocessor-system-on-chip is the resulting reliability of the individual functions. Depending on the criticality of a function, OEMs and indirectly their suppliers deliver guarantees to lawmakers on the overall failure rate of the system or component, with higher cost associated with the certification of higher level of reliability. Integration of functions with different reliability levels is then not cost efficient, if the resulting system needs to be verified for the highest level of reliability. A major research direction is therefore the investigation of methods that allow the co-integration of such functions. The researchers in ArtistDesign investigate countermeasures to this problem, for example by orthogonalization of the shared memory (e.g. Linköping University), or conservative bounds on the use of shared resources (e.g. TU Braunschweig).

2. State of the Integration in Europe

2.1 Brief State of the Art

Modern embedded systems for multimedia, imaging, and signal processing are characterized by high performance requirements on the one hand and stringent power requirements on the other hand. Often, these requirements can no longer be satisfied by embedded system architectures based on a single processor. Thus, emerging embedded system-on-chip platforms are increasingly becoming multiprocessor architectures. To compensate the high nonrecurring costs for designing and manufacturing multiprocessor chips, however, they need to be flexible such that they can be reused in different systems. This flexibility calls for programmability and sometimes reconfigurability. As a result, embedded systems platforms often have a heterogeneous architecture consisting of fully dedicated hardware components and different programmable processor cores.

A considerable number of multi-processor design frameworks have been proposed in the past, such as Artemis, Distributed Operation Layer (DOL), Embedded System-Level Platform Synthesis and Application Mapping (ESPAM), Koski, or StreamIt. While all frameworks provide an automated path from application specification to system implementation, they focus on different aspects of the design flow. In ArtistDesign, we attempt to unify the approaches developed by the various partners and extend them towards new methods for performance analysis, design space exploration and adaptivity.

The past several years have seen an increasing interest in wireless sensor nodes which are scavenging energy from their environment. In [5], several technologies have been discussed how, e.g., solar, thermal, kinetic or vibrational energy may be extracted from a node‘s physical environment. In particular, techniques to harvest energy via photovoltaic cells have attracted the interest of the sensor network community [6]. Solar energy is certainly one of the most promising energy sources and typical environmental monitoring applications have access to solar energy. If sensor nodes are equipped with photovoltaic cells as energy transducers, the autonomy of sensor nodes is increased substantially since frequent recharging and replacement of the batteries becomes unnecessary. Ideally, sensor nodes once deployed in a harsh environment benefit from a drastically increased operating time and become virtually immortal.

Clearly, the power generated by small solar cells is limited. Sensor nodes executing a given application may frequently run out of energy in times with insufficient illumination. If one strives for predictable, continuous operation of a sensor node, common power management techniques have to be reconceived. In addition to perform classical power saving techniques, the sensor node has to adapt to the stochastic nature of solar energy. Goal of this adaptation is to maximize the utility of the application in a long-term perspective. The resulting mode of operation is sometimes also called energy neutral operation: The performance of the application is not predetermined a priori, but adjusted in a best effort manner during runtime and ultimately dictated by the power source. Therefore, storage devices like batteries are solely used as energy buffers to compensate the variations of the underlying energy source. It is the goal of the interaction in ArtistDesign to improve the state-of-the-art in energy scavenging and the corresponding algorithms to adapt the running applications so as to optimize a long-term reward function.

2.2 Main Aims for Integration and Building Excellence through ArtistDesign

Following the activities presented in the previous section, the cluster on execution platforms follows the following strategy and uses the following mechanisms to spread the knowledge and integration achieved so far:

- Summer Schools and Training Activities to distribute the knowledge acquired in ArtistDesign to (a) other countries, (b) other communities and (c) young researchers.
- Tutorials at major conferences to reach new and larger research communities.
- Joint publications between partners, which not only show the integration within the cluster but are an excellent instrument to disseminate the integration results.
- New research projects with industrial partners, which allow us to apply the obtained results at an industrial scale. This way, we also receive feedback and ideas for new research directions.
- Cooperation with other research groups, especially outside the EU (mostly USA and Asia). In this case, spreading excellence is not the only objective. The cluster participants can be exposed to new research problems and new approaches that can be then explored and improved within the cluster.

2.3 Other Research Teams

It appears that main research groups in Europe dealing with execution platforms for embedded systems are in the ArtistDesign network, either as full or as affiliated partners. There are some exceptions though, caused by the fact that not all are accepting a European network of Excellence as a viable funding instrument. In the following, some of these groups are listed together with their relation to ArtistDesign.

The University of North Carolina at Chapel Hill, Sanjoy Baruah and Jim Anderson. Sanjoy Baruah and Jim Anderson are known in particular for their research in the domain of multiprocessor real-time scheduling.

University of Dresden, Hermann Härtig. Hermann Härtig is a leading researcher in the domain of micro-kernel based real-time operating systems.

Low power embedded systems design: In the area of low power embedded systems design, several new and relevant research themes are explored by other teams, not included in the ARTIST2 network. In particular research groups in the USA have a long tradition of excellence in low power research. We can mention the group lead by prof. Jan Rabaey in UC Berkeley, which is carrying out ground-breaking work on hardware platforms for wireless sensor networks. In the same area, several other groups are performing top-level research, e.g. Anantha Chandrakasan's group at MIT and David Blaauw's group at University of Michigan. Low power execution platforms are not relevant only for wireless sensor network, but also for mobile computing and even for servers and traditional computing infrastructure (e.g. servers). In these areas, the groups lead by Profs. Vijaykrishnan Narayanan, Mahmut Kandemir and Mary Jane Irwin at Penn State University, has produced a large number of interesting results in the last few years. We mention in particular their work on power issues for 3D integration and their analysis of power vs. reliability tradeoffs in high-performance computing. In this area, very interesting work is also performed by the group of prof. Kevin Skadron. The focus of this group is on thermal issues, which are very significant for high-performance system.

Universita degli Studi di Verona/Electronic Design Automation (EDA) group, Prof. Franco Fummi. Main research activities of the EDA group concern system verification, system synthesis and optimization, hardware description languages, power consumption, language

abstraction, and system testing. Interactions with members of the execution platforms cluster are, for example, by participation in European projects (e.g. the STRP "Vertigo") together with the Linköping group.

University of Southampton,/Electronic Systems Design Group, Prof. Bashir Al Hashimi. The Electronic Systems Design (ESD) Research Group is internationally recognized in two main areas - the development of novel algorithms and methodologies for Electronic Design Automation to support the design and test of large systems, and for intelligent sensor micro-systems. The group is working in the areas of system modelling, simulation, and synthesis, SoC design and testing, as well as smart sensors. Several cooperation projects have been undertaken, in particular with the Linköping group.

Carnegie Mellon University/System Level Design Group/Prof. Radu Marculescu. The System Level Design group performs research on formal methods for system-level design of embedded applications. They, in particular, focus on fast methods for power and performance analysis that can guide the design process of portable information systems. Important results have been obtained with regard to the communication-centric SOC design, providing formal support for analysis and optimization of novel on-chip communication architectures. In particular, this work addresses fundamental research problems for defining scalable and flexible communication schemes via the Network-on-Chip (NoC) approach. Interaction has been by, for example, PhD student exchanges with the Linköping group.

2.4 Interaction of the Cluster with Other Communities

Casteness 2008 Workshop; location: Rome, Italy; date: 15th-18th of January 2008: The objectives of CASTNESS workshops and schools are, first, to provide training about the future of multi-processor/adaptable embedded systems (system SW, HW architectures, applications) and second, the cross-dissemination among European projects. ETHZ presented an overview and a SW demonstration of the Distributed Operation Layer framework, included in a complete MPSoC design flow, as well as detailed information about the design space exploration and mapping optimization steps within this framework.

Invited Talk L. Thiele (ETHZ): MPSOC Conference. Aachen, Germany, June 23-27, 2008: Lothar Thiele described a new approach for mapping algorithms onto MPSoC architectures. It is a result of a cooperation between ArtistDesign partners from Aachen, TIMA and LETI. The design methodology is named DOL (distributed operation layer) and targets predictable and efficient multiprocessor systems and applications.

Summer School: Course on Embedded Systems (ETHZ, L. Thiele), Florianopolis, Brazil, August 25-2, 2008. The summer school was dedicated to promote the interaction between the embedded system communities in Europe and South America. Lothar Thiele was presenting a wide range of subjects, starting from basic methods to design predictable software of embedded systems. In addition, he presented methods for real-time scheduling and performance analysis of distributed embedded systems.

Tutorial L. Thiele (ETHZ): Analysis of Distributed Embedded Systems. CASTENESS WORKSHOP ROMA, Jan. 15-18, 2008. During the CASTNESS Workshop, ETHZ gave a tutorial on the different methods to estimate the performance of distributed embedded systems, including computation, communication and resource sharing.

TU Braunschweig and TU Eindhoven are guest editors of the ACM TECS special issue on Model-driven Embedded System Design (http://acmtecs.acm.org/mesd.htm).

Linköping has given an invited talk at the DATE 2008 Conference, as part of the special day on Dependable Embedded Systems. With this occasion several results obtained in the ARTIST

context have been made accessible to an international audience. They are related, in particular, to fault tolerance aspects of distributed real-time systems like those used in automotive applications.

Linköping has organised the 6th IEEE Workshop on Embedded Systems for Real-Time Multimedia, as part of the ARTIST sponsored Embedded Systems Week 2008.

UNIBO has been very active in the Multi-core Systems-on-Chip community and in the computer architecture community which is now aggressively targeting multi-core systems. UNIBO has become active member of the HIPEAC2 network of excellence and participated to several events in this area. Prof. Benini has been an HIPEAC instructor at the ACACES summer school, in L'Acquila. Members of the UNIBO team have participated to the main HIPEAC events in 2008.

DTU has become an active member of the HIPEC2 network of excellence and is participating in the chapter on programming models. Prof. Sven Karlsson from DTU has participated en several HIPEAC2 events.

DTU has been organizing the DaNES Mini-Case Workshop on industrial case-studies at DTU on May 22-23, 2008.

TU Braunschweig has been organizing the Embedded Software Track at the major European conference on design automation DATE (Design Automation and Test in Europe) that took place March 10-14, 2007. The track was devoted to modelling, analysis, design and deployment of embedded software, including formal methods, tools, methodologies and development environments. Thereby, the emphasis was on embedded software platforms, software integration and portability issues.

DTU has established collaboration with Duke University on design tools for biochips based on digital microfluidics. A PhD student from DTU has visited Duke for 6 months.

DTU has extended its long term relationship with Virginia Tech on hardware design using the Gezel hardware description language. A PhD student from DTU has visited Virginia Tech for 1 month.

DTU has been organizing the Special Sessions of the DATE 2008 conference. A total of 9 sessions were organized.

UNIBO, TU Braunschweig and DTU gave invited talks at the 8th International Forum on Application Specific Multi-Processor SoC, Aachen, Germany.

3. Overall Assessment and Vision for the Cluster

The research in embedded systems is still fragmented. This not only is true within a single subject but also between several sub-disciplines. It is one of the major goals of the cluster on 'Hardware Platforms and MPSoC Design' to establish closer links to the other communities and to take advantage of the scientific results and insights.

Cross-layer design is a key issue in embedded systems. The classical view of a strict layering according to chosen abstraction levels does not work any more because of the importance of non-functional constraints and limited resources. Therefore, completely new concepts are necessary that enable the integrated modelling and design under predictability and efficiency constraints. It is expected that this move towards a resource-aware design trajectory involves all current layers and a breakthrough can be obtained by integration only.

3.1 Assessment for Year 1

LINKÖPING-DTU: Interaction between Linköping and DTU has been in the area of fault tolerant embedded systems. Solutions have been developed in cooperation and publications have been written together. Prof. Paul Pop from DTU has visited Linköping.

LINKÖPING-BOLOGNA: Interaction between Linköping and Bologna has been in the area of predictable multiprocessor systems. Paolo Burgio has visited Linköping for 10 months and has worked on the elaboration of bus controllers. In this period he has also written his Master Thesis. Experiments at Linköping has been run using the MPARM tool from Bologna.

LINKÖPING-TUBS: Interaction between Linköping and Braunschweig has been in the area of performance analysis for distributed systems and predictable multiprocessors. The Symta/P worst case execution time analysis tool from Braunschweig has been further developed at Linköping and has been integrated in a predictable analysis and scheduling tool for multiprocessors.

ETHZ has been mainly involved in cooperations with University Bologna and University Dortmund. In particular, we looked at new approaches to map algorithms onto highly parallel MPSoC platforms. To this end, we linked the specification and mapping environment DOL (distributed operation layer) from ETHZ to the MPARM simulation platform from University Bologna. Major efforts have been invested into the corresponding alignment of the semantics, the generation of appropriate hardware-dependent software and the implementation of predictable communication fabrics. This work just started and will continue during the next phase of ArtistDesign. Together with University Dortmund, we are starting to investigate the influence of memory mapping on the whole MPSoC design process. A first visit of a PhD student from Dortmund to ETHZ took place which resulted in a first problem specification.

DTU-BOLOGNA: Interaction between DTU and Bologna has been in the area of networked embedded systems. Focus has been on power management in wireless sensor networks supported by energy harvesting. To this end, the sensor node scheduler based on Lazy-scheduling has been integrated in the wireless sensor network simulator from DTU, which provides a dynamic power-aware routing protocol. Two visits of a student from DTU to Bologna took place, resulting in a first integration and a definition of a case study.

DTU-KTH: Interaction between DTU and KTH has been in the area of system modelling suited for raising the level of abstraction for SMEs working with Embedded Systems, either as technology providers or as technology users. The result was a joint application to the ARTEMIS JU together with Tampare University of Technology and 8 SMEs. The project, called SYSMODEL, was accepted and will be started in the beginning of 2009.

DTU-AAU: Interaction between DTU and AAU (Modeling and Validation cluster) has been in the area of formalizing the ARTS system-level simulation model using timed automata based on UPPAAL. This work was started in ARTIST2. The result has been a prototype modelling framework (MoVES), which allows to experiment with different models-of-computation. In order to support designers of industrial applications, the timed-automata model is hidden for the user, allowing the designer to work directly with the abstract system-level model of embedded systems.

3.2 Overall Assessment since the start of the ArtistDesign NoE

Simulation platform for distributed embedded systems (Linköping, DTU)

A simulation environment is designed and implemented for distributed real-time systems such as those used in automotive applications. The ARTS environment, developed at DTU and targeting System-on-chip applications, has been used as a starting point by the Linköping team.

Modeling and response-time/buffer analysis for NoC (Linköping)

The Linköping group has developed a system model, based on which worst case response times and worst case buffer need for hard real-time applications implemented on NoCs can be calculated. On top of this analysis approach, an optimization tool for buffer space minimization has been implemented, for real-time NoC applications.

Predictability in Multiprocessor SoC architectures (Linköping, Bologna, Braunschweig)

The Linköping group has developed a framework for predictable WCET analysis, scheduling, and bus access optimisation for multiprocessors. With regard to the "classical" aspect of WCET analysis the group is building on the Symta/P tool from the Braunschweig group. The Linköping group is also interacting with the Bologna group with regard to the issues of bus control for predictable multiprocessors.

Power optimization via system-level resource allocation and scheduling (Linköping, Bologna)

The main objective here is to develop techniques for optimally mapping multi-task (parallel) applications onto System-on-chip (SoC) platforms with multiple processors (MP-SoCs). This is an industry-relevant problem, as most high-end embedded computing platforms in a number of target markets (automotive, multimedia, networking) are evolving toward multi-core architectures. The most critical challenge in this area is the complexity of the problem of optimally mapping tasks onto cores (and storage resources), while selecting frequency and voltage assignments for the various cores.

Optimization and analysis of distributed embedded systems (Linköping)

In the context of optimization and analysis of distributed embedded systems the following issues:

- Analysis of hierarchically scheduled systems
- Timing analysis of distributed task sets communicating through the FlexRay protocol
- Analysis and optimization mixed time and event triggered systems

Fault Tolerant Distributed Embedded Systems (Linköping, DTU)

Linköping and DTU have addressed the issue of fault tolerant distributed embedded systems, with special emphasis on handling transient faults. There are two main aspects of interest here:

- Analysis of timing properties in the presence of faults and possible guarantees regarding worst case behaviour
- System optimization, such that timing and fault tolerance requirements are satisfied given a certain, limited amount of resources.

An approach for scheduling and worst case analysis with fault tolerance has been developed. On top of this analysis approach, an optimization technique for task mapping and fault tolerance policy assignment has been elaborated and implemented.

Integration of Symta/S - MPA and unifying approaches for hierarchical scheduling (ETHZ together with University Braunschweig)

In a recently published paper J. Rox and R. Ernst from University Braunschweig introduced the hierarchical event model that is going to be implemented in the SymTA/S framework. Alternative approaches to deal with merged event streams should be found for the MPA framework used at the ETH Zurich. In a first step, ETHZ analyzed the formalism by Braunschweig and are now considering various solutions how to embed the hierarchical event model into MPA. The major issue here is to also allow an extraction of single event streams from previously merged – and transformed event streams. The transformation is hereby due to the fact that incoming streams can be combined via OR-operation and may pass different system components, which may buffer these streams due to scheduling policies. In a next step, analysis and comparisons of the different approaches will be done. To this end, a PhD student from ETHZ visited University Braunschweig for a week (6th of Oct until 10th of Oct. 2008). A technical report has been written that will be submitted for publication.

Optimization-centric MPSoC Design (University Bologna together with ETHZ)

The technical achievements are based on a set of joint meetings and visits. The primary goal of this activity was to establish a mutual understanding of the MPARM framework (developed at University of Bologna), on one hand, and the DOL framework (developed at ETHZ), on the other hand.

One main outcome of the meetings was to establish the design of the Modular Performance Analysis (MPA) analytic model for the MPARM platform. For this goal, the input specification and the API of the Distributed Operation Layer (DOL) framework, developed by ETHZ, was ported to the MPARM environment. This work is still under way. In particular, further phone conferences on the 22nd and 24th of October have been devoted to a refinement of the approach. These phone meetings had as main goal the identification of the basic design factors impacting on predictable communication fabrics.

Photovoltaic scavenging systems from the model to the optimized design (University Bologna, ETHZ)

University of Bologna and ETHZ have improved the design of a scavenger prototype which exploits miniaturized photovoltaic modules to perform automatic maximum power point tracking. We propose a detailed model of the solar cell that predicts the instantaneous power collected by the panel and improves the simulation of harvester systems. Furthermore, we focused on a methodology for optimizing the design of MPPT solar harvesters for self-powered

embedded systems and presented innovations in the circuit architecture with respect to our previous implementation. We verified that energy consumption and efficiency of the MPP tracker are very important design criteria in energy scavengers for sensor nodes, therefore we analyzed two important metrics: (i) maximization of the energy harvesting efficiency; (ii) minimization of the energy used for ineffective operations.

To this end the technical achievements can be summarized as follow:

(a) We presented a compact model for small solar modules that accurately describes the behaviour over a wide range of irradiance conditions, cell temperature variation and incident angle with out numerical approaches typically adopted;

(b) We improved the design process of the DC–DC converter at the solar harvester input stage boosting its efficiency

(c) We addressed the powering a sensor node with miniaturized photovoltaic modules of a few mm2 proposing a new inductor-less architecture for the harvesting process suitable for on-chip integration.

Energy Harvesting Aware Routing with Scheduling optimization (DTU, UoB)

DTU and Bologna have started a collaboration on energy-scavenging wireless sensor networks. Renewable energy sources can potentially lead to perpetual operation, but not without careful management of the energy both in the individual node and in the whole network. DTU has developed a simulator for wireless sensor networks, which is capable of capturing nodes with energy harvesting. Bologna and DTU have made the first attempts towards integrating lazy-scheduling with energy-aware routing within the simulator.

Modeling and Verification of Embedded Systems (DTU, AAU)

DTU has continued the work from ARTIST2 on formalizing the ARTS simulation model and to make it usable for designers early in the design process. In order to support designers of industrial applications, the timed-automata model is hidden for the user, allowing the designer to work directly with the abstract system-level model of embedded systems. The designer provides an application consisting of a set of task graphs, an execution platform consisting of processing elements interconnected by a network and a mapping of tasks to processing elements. The system model is then translated into a timed-automata model which enables schedulability analysis as well as being able to verify that memory usage and power consumption are within certain limits. In the case where a system is not schedulable, the tool provides useful information about what caused the missed deadline. DTU does not propose

3.2.1 List of Joint Publications

The following list contains publications, where authors are in different research sites which are participating in the ArtistDesign network and where at least one author is in the cluster on Execution Platforms. It clearly shows the degree of integration that has been achieved. The following list collects all joint publications since the start of ArtistDesign:

1. Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng, “Synthesis of Flexible Fault-Tolerant Schedules with Preemption for Mixed Soft and Hard Real-Time Systems”, 11th EUROMICRO CONFERENCE on DIGITAL SYSTEM DESIGN (DSD 2008), Parma, Italy, September 3-5, 2008, pp. 71-80.
2. Petru Eles, Viacheslav Izosimov, Paul Pop, Zebo Peng, “Synthesis of Fault-Tolerant Embedded Systems”, Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, pp. 1117-1122.

3. Wu, K., Madsen, J., Kanstein, A., Mladen, B., *MT-ADRES: Multithreading on Coarse-Grained Reconfigurable Architecture*, Intel. Journal of Electronics (IJE), Volume 95, Issue 7, July 2008. Page(s): 761-776.
4. Anders Tranberg-Hansen, Jan Madsen, Bjørn Sand Jensen, A Service Based Estimation Method for MPSoC Performance Modelling, to appear in the proceedings of the 3rd International Symposium on Industrial Embedded Systems, June 2008.
5. A Reactive and Cycle-True IP Emulator for MPSoC Exploration Mahadevan, S.; Angiolini, F.; SparsSparso, J.; Benini, L.; Madsen, J. Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Volume 27, Issue 1, Jan. 2008 Page(s):109 – 122
6. **'**Enabling run-time memory data transfer optimizations at the system level with automated extraction of embedded software metadata information', Bartzas, A.; Peon-Quiros, M.; Mamagkakis, S.; Catthoor, F.; Soudris, D. and Mendias, J., Asia and South Pacific Design Automation Conference - ASP-DAC, 2008
7. 'Optimization Methodology of Dynamic Data Structures based on Genetic Algorithms for Multimedia Embedded Systems', Baloukas, C.; Risco Martin, J.; Atienza, D.; Poucet, C.; Papadopoulos, L.; Mamagkakis, S.; Soudris, D.; Hidalgo, J.; Catthoor, F. and Lancares, J., Elsevier Journal of Systems and Software (JSS), 2008
8. 'MNEMEE: Memory management technology for adaptive and efficient design of embedded systems' S.Mamagkakis, P.Lemmens, D.Soudris, T.Basten, P.Marwedel, D.Kritharidis, G.Guilmin, 16th IFIP/IEEE International Conference on Very Large Scale Integration - VLSI-SOC, 2008.
9. 'MOSART: Mapping Optimisation for Scalable multi-core ARchiTecture', B. Candaele, A. Jantsch, T. Ashby, K. Tiensyrjä, F. Ieromnimon, B. Vanthournout, P. Di Crescenzo, D. Soudris, 16th IFIP/IEEE International Conference on Very Large Scale Integration - VLSI-SOC, 2008.
10. Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng, "Scheduling of Fault-Tolerant Embedded Systems with Soft and Hard Timing Constraints", Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, 915-920.
11. Traian Pop, Paul Pop, Petru Eles, Zebo Peng, Alexandru Andrei, "Timing Analysis of the FlexRay Communication Protocol", Real-Time Systems Journal, Volume 39, Numbers 1-3, August, 2008, pp 205-235.
12. Traian Pop, Paul Pop, Petru Eles, Zebo Peng, Alexandru Andrei, "Analysis and Optimisation of Hierarchically Scheduled Multiprocessor Embedded Systems", Intl. Journal of Parallel Programming, Volume 36, Number 1, February, 2008, pp. 37-67.
13. Bengt Jonsson, Simon Perathoner, Lothar Thiele, Wang Yi: Cyclic Dependencies in Modular Performance Analysis. ACM & IEEE International Conference on Embedded Software (EMSOFT), ACM Press, Atlanta, Georgia, USA, pages 179-188, October, 2008.
14. Simon Perathoner, Ernesto Wandeler, Lothar Thiele, Arne Hamann, Simon Schliecker, Rafik Henia, Razvan Racu, Rolf Ernst, Michael González Harbour: Influence of Different Abstractions on the Performance Analysis of Distributed Hard Real-Time Systems Design Automation for Embedded Systems, Springer Science+Business Media, LLC, 2008.
15. Davide Brunelli, Clemens Moser, Luca Benini, Lothar Thiele: An Efficient Solar Energy Harvester for Wireless Sensor Nodes. Design, Automation and Test in Europe (DATE 08), Munich, Germany, March, 2008.

16. Clemens Moser, Lothar Thiele, Davide Brunelli, Luca Benini: Robust and Low Complexity Rate Control for Solar Powered Sensors Design, Automation and Test in Europe (DATE 08), Munich, Germany, March, 2008.
17. Tolga Ovatman, Aske Brekling, and Michael R. Hansen. Cost analysis for embedded systems: Experiments with Priced Timed Automata. In proceedings of FESCA 2008.
18. 'Enabling run-time memory data transfer optimizations at the system level with automated extraction of embedded software metadata information', Bartzas, A.; Peon-Quiros, M.; Mamagkakis, S.; Catthoor, F.; Soudris, D. and Mendias, J., Asia and South Pacific Design Automation Conference - ASP-DAC, 2008
19. 'Storage estimation and design space exploration methodologies for the memory management of signal processing applications', Balasa, F.; Kjeldsberg, P.; Vandecappelle, A.; Palkovic, M.; Hu, Q.; Zhu, H. and Catthoor, F.Journal, Journal of VLSI Signal Processing Systems, 2008
20. Iyad Al Khatib, Francesco Poletti, Davide Bertozzi, Luca Benini, Mohamed Bech ara, Hasan Khalifeh, Axel Jantsch, and Rustam Nabiev, "A Multiprocessor System-on-Chip for Real-Time Biomedical Monitoring and Analysis: ECG Prototype Arc hitectural Design Space Exploration", ACM Transactions on Design Automation of Embedded Systems, vol. 13, no. 2, April 2008.
21. 'A System Scenario based Approach to Dynamic Embedded Systems', S.V. Gheorghita, M. Palkovic, J. Hamers, A. Vandecappelle, S. Mamagkakis, T. Basten, L. Eeckhout, H. Corporaal, F. Catthoor, F. Vandeputte, K. De Bosschere, ACM Transactions on Design Automation of Electronic Systems, ToDAES. To appear in 2009.
22. V. Izosimov, P. Pop, P. Eles, Z. Peng, "Design Optimization of Time- and Cost-Constrained Fault-Tolerant Embedded Systems with Checkpointing and Replication", IEEE Trans. on Very Large Scale Integrated (VLSI) Systems (accepted for publication).

3.3 Indicators for Integration

During year 1 we have done the following interactions between partners:

- *22 joint publications* have been produced. The plan was 10 Joint publications / year describing the results in terms of new methods and tools.
- Joint organization of workshops, tutorials, special sessions in international highly recognized conferences. In year 1 the following was accomplished:
  - Organized the 6th IEEE Workshop Embedded Systems for Real-Time Multimedia as part of the Embedded Systems Week, 2008.
  - Organized the DaNES Mini-Case Workshop in Denmark.
  - Organized the Embedded Software track at DATE 2008.
  - Organized the 9 Special Sessions at DATE 2008.
  - Organized a PhD course on Advanced Topics in Embedded Systems, Lyngby, Denmark (This was partly done together with ARTIST2)
  - Guest editor of the ACM TEC special issue on Model-Driven Embedded Systems Design.
  - Gave tutorial at Casteness 2008 Workshop in Rome, Italy.
  - Gave 4 invited talks at the 8th International Forum on Application Specific Multi-Processor SoC, Aachen, Germany.
- Yearly target is 1 workshop, 1 PhD course/school, 2-3 conference tutorials and special sessions.

- Integration of tools existing at the partner sites, and definition of tool flows integrating tools from the different partners.
    - The tool integration work started in ARTIST2 is being continued in ArtistDesign. This covers both integration of tools within the cluster, between clusters of ArtistDesign and with external partners.
- Mobility, i.e. the number of PhD student and faculty exchanges. This integration activity will also introduce the concept of "student clusters", where more than two PhD students from different partners will work together in a single location.
    - 6 PhD student visits
    - 4 faculty/researcher visits
    - 6 focused meetings (including "student clusters")
- Impact on industrial practice in the area of MPSoC design and analysis. This objective will leverage student internships at associated industrial partner's sites.
    - No student internships have been carried out during year 1.
    - 3 PhD students are working closely with industry partners.

3.4 Long-Term Vision

Embedded systems are growing more software and communication centric. As a consequence, new models and new analysis and design space exploration tools are needed in order to support optimal implementation of applications on distributed embedded architectures such as MPSoC. Embedded systems are characterized by continuously increasing complexity and strong constraints on safety, performance, power consumption, and costs. To be able to design such systems, it is needed to (1) consider the hardware platform and software components of MPSoC systems in their interaction, in order to produce a system which satisfies the requirements at low cost, (2) support the designer with tools for accurate estimation of certain design parameters (power, performance) based on appropriate models for hardware and software components and (3) provide the designer with adequate support for design space exploration and optimization.

Embedded architectures and heterogeneous distributed embedded systems have grown to extremely complex computation and communication patterns, and to an increasing level of reconfigurability (including adaptivity and run-time resource management). New performance models and a corresponding theory are urgently needed.

The long-term vision for this activity is to advance the theory, methods and tools for the modeling, analysis and design of embedded systems and to disseminate this to advance academic excellence, education and industrial innovation.

3.5 Tools and Platforms

3.5.1 Tool: SymTA/S

Objectives

SymTA/S is a tool for the development and verification of embedded multiprocessor real-time systems. The existing technology is mainly suitable for event or time-driven systems with message passing as the main task interaction. The tool shall be extended to cover the timing implications of multicore processors, or multiprocessor-systems-on-chip.

Main Results

In several previous projects (funded by German DFG, “Sureal”, funded by German BMBF, ARTIST2, and others), the compositional analysis approach has been transferred into a tool framework which is now also commercially available. The available modelling options capture typical problems in today’s automotive systems (CAN bus utilization, end-to-end deadlines,…). This addresses a growing need for formal methods in the industry. The topics currently under research (see below) address future problems which can be expected to become of increasing industrial interest in the future.

Current work

The research version of the tool framework is currently being developed into several new directions: Modeling of shared resources for multiprocessor-system-on-chips (see ArtistDesign Activity 6.2: Platform and MpSoC Analysis), the modelling of hierarchical event models (in the scope of the COMBEST project), and the demonstrator platform for adaptive systems (see ArtistDesign 7.1: Design for Adaptivity). Besides the extension of the applicability into new domains, a major focus within ArtistDesign is the synergetic coupling of tools, as well as the corresponding development of models.

Participating partners:

- TU Braunschweig.

  TU Braunschweig investigates synergies in the coupling of methods and implements prototypical implementations of the research results.

- Symtavision GmbH.

  Symtavision is the commercial co-developer of the tool framework. A focus within ArtistDesign is the coupling of with other industrially available tools (such as aiT).

- ETHZ.

  Collaboration on the coupling of MPA and SymTA/S with respect to modelling of hierarchical event models.

- AbsInt GmbH.

  The aiT tool supplies task timing models, which are required for system level analysis.

Web
http://www.symtavision.com/
http://www.ida.ing.tu-bs.de/index.php?id=symtas
http://www.ida.ing.tu-bs.de/en/research/projects/accord/

Related Publications

Simon Schliecker and Arne Hamann and Razvan Racu and Rolf Ernst. "Formal Methods for System Level Performance Analysis and Optimization." In *Proc. of the Design Verification Conference (DVCon)*, San José, CA, February 2008.

Jonas Rox and Rolf Ernst. "Modeling Event Stream Hierarchies with Hierarchical Event Models." In *Proc. Design, Automation and Test in Europe (DATE 2008)*, March 2008.

3.5.2 Tool: Analysis and optimisation framework for fault tolerant distributed embedded systems

Objectives

Linköping University and DTU are working on an environment and tool-set for the analysis and design optimisation of safety critical, fault tolerant real-time embedded applications. The emphasis is on the issue of transient faults and the goal is to develop tools for scheduling, mapping, and system optimisation.

Main results

A strategy for the synthesis of fault tolerant schedules has been developed. It can handle both hard and soft real-time tasks. The goal is to guarantee the deadlines for the hard processes even in the case of faults, while maximizing the overall utility. Time/utility functions are used to capture the utility of soft processes. Process re-execution is employed to recover from multiple faults. A single static schedule computed off-line is not fault tolerant and is pessimistic in terms of utility, while a purely online approach, which computes a new schedule every time a process fails or completes, incurs an unacceptable overhead. Thus, a quasi-static scheduling strategy is used, where a set of schedules is synthesized off-line and, at run time, the scheduler will select the right schedule based on the occurrence of faults and the actual execution times of processes. An optimisation technique for the generation of schedule tables supporting such a quasi-static scheduling approach has been developed and implemented.

Current work

Ongoing work is towards development of cost-optimisation techniques by considering processors with various hardening levels and the associated tradeoffs.

Participating partners

Linköping: Scheduling techniques, fault tolerant systems, design optimisation.

DTU: System level optimisation techniques

Publications

23. Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng, “Synthesis of Flexible Fault-Tolerant Schedules with Preemption for Mixed Soft and Hard Real-Time Systems”, 11th EUROMICRO CONFERENCE on DIGITAL SYSTEM DESIGN (DSD 2008), Parma, Italy, September 3-5, 2008, pp. 71-80.
24. Petru Eles, Viacheslav Izosimov, Paul Pop, Zebo Peng, “Synthesis of Fault-Tolerant Embedded Systems”, Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, pp. 1117-1122.

25. Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng, “Scheduling of Fault-Tolerant Embedded Systems with Soft and Hard Timing Constraints”, Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, 915-920.

3.5.3 Tool: IMEC MPA + MH MPSoC mapping framework

Objectives

The main objectives of the framework is to offer an automatic source code parallelization (MPA tool) and memory hierarchy management (MH tool) in order to map efficiently embedded software application on MPSoC platforms.

Main Results

Prototype versions of the MPSoC Parallelization Assistant (MPA) and Memory Hierarchy (MH) management tools were developed and tested on video codec embedded sosftware applications (i.e., MPEG-4, AVC etc.).

Current work

Currently, the affiliated partners of IMEC (ie, DUTH/ICCS and TU/e) and core partners (TUDortmund/ICD and KTH) are trying to integrate their tool and design flows with the IMEC MPA + MH MPSoC mapping framework in the memory and interconnect specific context of the MNEMEE and MOSART FP7 projects, respectively.

Participating partners:

- DUTH/ICCS
  This partner is integrating the dynamic data type and dynamic memory management tools and design flows with the IMEC MPSoC mapping tool flows.
- TU Dortmund/ICD
  This partner is integrating its pre-compiler and compiler framework to the static MH tool of IMEC.
- TU/e
  This partner is integrating its SDF3 framework in the context of system scenarios with the IMEC MPSoC mapping tool flows.
- KTH
  This partner is integrating its NoC simulation and exploration framework with the MPA tool of IMEC.

Web
http://www.mnemee.org/
http://www.mosart-project.org/

Related Publications

IMEC vzw. & TU/e

- ‘A System Scenario based Approach to Dynamic Embedded Systems’, S.V. Gheorghita, M. Palkovic, J. Hamers, A. Vandecappelle, S. Mamagkakis, T. Basten, L.

Eeckhout, H. Corporaal, F. Catthoor, F. Vandeputte, K. De Bosschere, ACM Transactions on Design Automation of Electronic Systems, ToDAES. To appear in 2009.

IMEC vzw. & TU/e & DUTH & TU Dortmund (at ICD)

- 'MNEMEE: Memory management technology for adaptive and efficient design of embedded systems' S.Mamagkakis, P.Lemmens, D.Soudris, T.Basten, P.Marwedel, D.Kritharidis, G.Guilmin, 16th IFIP/IEEE International Conference on Very Large Scale Integration - VLSI-SOC, 2008.

IMEC vzw. & KTH & DUTH

- 'MOSART: Mapping Optimisation for Scalable multi-core ARchiTecture', B. Candaele, A. Jantsch, T. Ashby, K. Tiensyrjä, F. Ieromnimon, B. Vanthournout, P. Di Crescenzo, D. Soudris, 16th IFIP/IEEE International Conference on Very Large Scale Integration - VLSI-SOC, 2008.

4. Cluster Participants

4.1 Core Partners

Cluster Leader Activity Leader & Team Leader	
	Jan Madsen (Technical University of Denmark)
Technical role(s) within ArtistDesign	Member of the Strategic Management Board Leads Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Participates in Intercluster activity: Integration Driven by Industrial Applications Leader of the JPRA Activity: “Platform and MPSoC Analysis”
Research interests	Research interests include high-level synthesis, hardware/software codesign, System-on-Chip design methods, and system level modelling, integration and synthesis for embedded computer systems.
Role in leading conferences/journals/etc in the area	Program Chair and Vice-Chair of Design Automation and Test in Europe Conference. Tutorial Chair and Special Sessions Chair of Design Automation and Test in Europe Conference. General Chair, Program Chair and Workshop Chair of CODES+ISSS Conference Member of the editorial board of the journal “IEE Proceedings – Computers and Digital Techniques” Member of the technical program committee and organizing committee of several technical conferences, including the Design Automation and Test in Europe Conference, the Real-Time Systems Symposium, the Symposium on Hardware-Software Codesign, and the International Workshop on Applied Reconfigurable Computing. Danish delegate in the Governing Board of ARTEMIS JU
Awards / Decorations	In 1995 he received the Jorck's Foundation Research Award for his research in hardware/software codesign

Team Leader

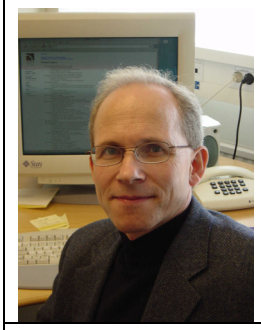
	Lothar Thiele (ETH Zurich)
Technical role(s) within ArtistDesign	Main areas of research: Embedded Systems and Software Participates in Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Participates in Intercluster activity: Design for Predictability and Performance
Research interests	Research interests include models, methods and software tools for the design of embedded systems, embedded software and bio-inspired optimization techniques.
Awards / Decorations	In 1986 he received the "Dissertation Award" of the Technical University of Munich, in 1987, the "Outstanding Young Author Award" of the IEEE Circuits and Systems Society, in 1988, the Browder J. Thompson Memorial Award of the IEEE, and in 2000-2001, the "IBM Faculty Partnership Award". In 2004, he joined the German Academy of Natural Scientists Leopoldina. In 2005-2006, he was the recipient of the Honorary Blaise Pascal Chair of University Leiden, The Netherlands.

Team Leader	
	Prof. Luca Benini, University of Bologna http://www-micrel.deis.unibo.it/%7Ebenini/
Technical role(s) within ArtistDesign	Member of the Strategic Management Board Co-leads Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Participates in Intercluster activity: Design for Predictability and Performance Leader of the JPRA Activity: “Platform and MPSoC Design”
Research interests	(i) Development of power modeling and estimation framework for systems-on-chip. (ii) Development of optimal allocation and scheduling techniques for energy-efficient mapping of multi-task applications onto multi-processor systems-on-chips. (iii) Development of energy-scavenging techniques for ultra-low power sensor network platforms.

Role in leading conferences/journals/etc in the area	▪ Program chair and vice-chair of Design Automation and Test in Europe Conference. ▪ Member of the 2003 MEDEA+ EDA roadmap committee 2003. ▪ Member of the IST Embedded System Technology Platform Initiative (ARTEMIS): working group on Design Methodologies ▪ Member of the Strategic Management Board of the ARTIST2 Network of excellence on Embedded Systems ▪ Member of the Advisory group on Computing Systems of the IST Embedded Systems Unit. ▪ Member of the technical program committee and organizing committee of several technical conferences, including the Design Automation Conference, International Symposium on Low Power Design, the Symposium on Hardware-Software Codesign. He is Associate Editor of the IEEE Transactions on Computer-Aided Design of Circuits and Systems and of the ACM Journal on Emerging Technologies in Computing Systems. ▪ Fellow of the IEEE.
Notable past projects	ICT-Project **REALITY - *Reliable and variability tolerant system-on-a-chip design in more-moore technologies.*** Funded under 7th FWP (Seventh Framework Programme). ICT-2007.3.1 Next-Generation Nanoelectronics Components and Electronics Integration. Start date: 01/01/2008; Duration: 30 months; Contract Type: Collaborative project; Project Reference: 216537; Project Cost: 4.45 million euro; Project Funding: 2.9 million euro. ICT-Project **PREDATOR - *Design for predictability and efficiency.*** Funded under 7th FWP (Seventh Framework Programme). ICT-2007.3.3 Embedded Systems Design. Start date: 01/02/2008; Duration: 36 months; Contract Type: Collaborative project; Project Reference: 216008; Project Cost: 3.93 million euro; Project Funding: 2.8 million euro. ICT-Project **GALAXY - *interface for complex digital system integration.*** Funded under 7th FWP (Seventh Framework Programme). ICT-2007.3.3 Embedded Systems Design. Start date: 01/12/2007; Duration: 36 months; Contract Type: Collaborative project; Project Reference: 214364; Project Cost: 4.08 million euro; Project Funding: 2.9 million euro. ICT-Project **DINAMICS - *Diagnostic Nanotech and Microtech Sensors.*** Funded under 6th FWP (Sixth Framework Programme). FP6-NMP 'Nanotechnologies and nanosciences, knowledge-based multifunctional materials and new production processes and devices'. Contract Type: Integrated project; Project Reference:IP 026804-2. Start date: 01/04/2007. Duration: 18 + 30 months. Project Cost:7276856 Euro. Project Funding: 4499542 Euro. http://www.dinamics-project.eu/ ICT-Project **SHARE - *Sharing open source software middleware to improve industry competitiveness in the embedded systems domain.*** Funded under 7th FWP (Seventh Framework Programme). ICT-2007.3.7 Network embedded and control systems. Start date: 01/05/2008; Duration: 24 months; Contract Type: Coordination and

	support actions; Project Reference: 224170; Project Cost: 1.1 million euro; Project Funding: 590000.00 euro.

Team Leader	
	Rolf Ernst (TU Braunschweig)
Technical role(s) within ArtistDesign	Main areas of research: Embedded Systems Participates in Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Participates in Intercluster activity: Design for Predictability and Performance Participates in Intercluster activity: Integration Driven by Industrial Applications
Research interests	Research interests include embedded architectures, hardware-/software co-design, real-time systems, and embedded systems engineering.
Role in leading conferences/journals/etc in the area	He chaired major international events, such as the International Conference on Computer Aided Design of VLSI (ICCAD), or the Design Automation and Test in Europe (DATE) Conference and Exhibition, and was Chair of the European Design Automation Association (EDAA), which is the main sponsor of DATE. He is a founding member of the ACM Special Interest Group on Embedded System Design (SIGBED), and was a member of the first board of directors. He is an elected member (Fachkollegiat) and Deputy Spokesperson of the "Computer Science" review board of the German DFG (corresponds to NSF). He is an advisor to the German Ministry of Economics and Technology for the high-tech entrepreneurship program EXIST (www.exist.org).

Team Leader	
	Petru Eles (Linköping University)
Technical role(s) within Artist2	Main areas of research: Embedded Systems Participates in Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Participates in Intercluster activity: Design for Predictability and Performance Participates in Intercluster activity: Integration Driven by Industrial Applications
Research interests	Research interests include electronic design automation, hardware/software co-design, real-time systems, design of embedded systems and design for testability.
Role in leading conferences/journals/etc in the area	- Associate Editor, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems; - Associate Editor, IEE Proceedings - Computers and Digital Techniques; - TPC Chair and General Chair, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS). - Topic chair, Design Automation and Test in Europe (DATE). - Topic Chair, Int. Conference on Computer Aided Design (ICCAD). - Program chair of the Hw/Sw Codesign track, IEEE Real-Time Systems Symposium (RTSS). - TPC Chair IEEE Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia). - Steering Committee Chair, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS).
Awards / Decorations	- Best paper award, European Design Automation Conference (EURO-DAC), 1992. - Best paper award, European Design Automation Conference (EURO-DAC), 1994. - Best paper award, Design Automation and Test in Europe (DATE), 2005. - Best presentation award, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS), 2003.

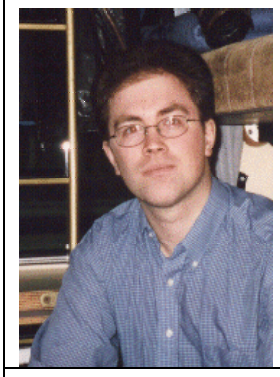
	- IEEE Circuits and Systems Society Distinguished Lecturer, for 2004 - 2005.

Team Leader	
	Dr. Stylianos Mamagkakis IMEC vzw. http://www.imec.be
Technical role(s) within ArtistDesign	Representing IMEC Nomadic Embedded Systems (NES) division in: -Cluster: SW Synthesis, Code Generation and Timing Analysis -Cluster: Operating Systems and Networks -Cluster: Hardware Platforms and MPSoC Design -Intercluster activity: Design for Adaptivity -Intercluster activity: Design for Predictability and Performance -Intercluster activity: Integration Driven by Industrial Applications
Research interests	Stylianos Mamagkakis received his Master and Ph.D. degree in Electrical and Computer Engineering from the Democritus Uni. Thrace (Greece) in 2004 and 2007, respectively. Since 2006, he coordinates a team of PhD students within the NES division at IMEC, Leuven, Belgium. His research activities mainly belong to the field of system-level exploration, with emphasis on MPSoC run-time resource management and system integration.
Role in leading conferences/journals/etc in the area	Stylianos Mamagkakis has published more than 35 papers in International Journals and Conferences. He was investigator in 9 research projects in the embedded systems domain funded from the EC as well as national governments and industry.
Notable past projects	Project leader of MNEMEE IST project www.mnemee.org Project leader of OptiMMA IWT project www.imec.be/OptiMMA Participation in: 1 international IMEC project (M4), 3 European IST projects (AMDREL, EASY, ARTIST2), 2 Greek projects (PRENED, DIAS)
Awards	1st prize in 'Technogenesis' Competition for Business Innovation, Greece, June'06 3rd prize in 'Otenet Innovation 2006' Competition for Business Innovation, Greece, November'06
Further Information	http://www2.imec.be/imec_com/nomadic-embedded-systems.php

Team Leader	
	Professor Axel Jantsch KTH http://web.it.kth.se/~axel/
Technical role(s) within ArtistDesign	A. Jantsch contributes to KTH participation and to the work on formal models of computation and communication and the ForSyDe framework. Furthermore, he also contributes to Hardware Platforms and MPSOC Design with focus on run-time environments and analysis techniques.
Research interests	A. Jantsch's main research topics are models of computation, modelling and analysis of embedded systems and SoCs, networks on chip.
Role in leading conferences/journals/etc in the area	
Notable past projects	**ANDRES** (Analysis and Design of run-time Reconfigurable, heterogeneous Systems) Project) – EU FP6 (http://andres.offis.de/) **SPRINT** (Open SoC Design Platform for Reuse and Integration of IPs): EU FP6 (http://www.ecsi-association.org/sprint) **MOSART** (Mapping Optimization for Scalable multi-core ARchiTecture) – EU FP7 (http://www.mosart-project.org/)

Team Leader	
	Thierry Collette, Ph.D (CEA LIST)
Technical role(s) within ArtistDesign	As a new partner, focus on new collaborations on reliable architectures.
Research interests	Embedded computing architectures, Many cores architectures reconfigurable computing and embedded reliability.

4.2 Affiliated Industrial Partners

	Daniel Karlsson (Volvo Technology Corporation)
Technical role(s) within ArtistDesign	Architecture and Design of Automotive Embedded Systems

	Kai Richter (SymTAVision GmbH)
Technical role(s) within ArtistDesign	Formal Performance Analysis and Optimization of Embedded Systems, Reliable System Integration, Early Architecture Exploration

	Dr. Arne Hamann (Robert Bosch GmbH)
Technical role(s) within ArtistDesign	Automotive Software Architectures

	Matthias Gries (Intel Germany)
Technical role(s) within ArtistDesign	Microprocessor Technology Lab, new computer architecture for embedded systems

	Rune Domsteen (Prevas A/S)
Technical role(s) within ArtistDesign	Embedded systems platform development

	Bjørn Sand Jensen (Bang & Olufsen ICEpower)
Technical role(s) within ArtistDesign	Execution platforms for audio signal processing

	Dr. Valter Bella (Telecom Italia Lab)
Technical role(s) within ArtistDesign	Architecture and Design of Wireless Sensor Networks and Embedded Systems for Ambient Intelligence

4.3 Affiliated Academic Partners

	Ass. Professor Dimitrios Soudris (NTUA/ formerly DUTH) www.microlab.ntua.gr www.ee.duth.gr
Technical role(s) within ArtistDesign	Collaboration with IMEC vzw.and contribution to the Hardware Platforms and MPSoC cluster and the Software Synthesis, Code Generation and Timing Analysis cluster.
Research interests	Dimitrios Soudris received his Diploma in Electrical Engineering from the University of Patras, Greece, in 1987. He received the Ph.D. Degree in Electrical Engineering, from the University of Patras in 1992. He is currently working as Assistant Professor in Electrical and Computer Engineering, National Technical University of Athens (NTUA), Greece. His research interests include low power design, parallel architectures, embedded systems design, and VLSI signal processing. He was leader and principal investigator in numerous research projects funded from the Greek Government and Industry as well as the European Commission (ESPRIT II-III-IV and 5th, 6th and 7th IST). He is a member of the IEEE, the VLSI Systems and Applications Technical Committee of IEEE CAS and the ACM.
Role in leading conferences/journals/etc in the area	Dimitrios Soudris has (co-)authored over 180 papers in international journals and conferences, and has coauthored and edited 4 text books. He has served as General Chair and Program Chair for PATMOS' 99 and 2000 and General Chair IEEE/CEDA VLSI-SOC 2008. He received an award from INTEL and IBM for the project results of LPGD #25256 (ESPRIT IV) and 4th position in ASP-DAC 2005 Design Contest for AMDREL IST-34793.
Notable past projects	LPGD project Design of a low power GFSK/GMSK modulator/demodulator for DECT receivers. AMDREL project Development of dynamic memory management design methodologies for emebedded syetems. Design of a low energy FPGA and a software supported design flow.
Awards / Decorations	Dimitrios Soudris received an award from INTEL and IBM for the project results of LPGD #25256 (ESPRIT IV) and 4th position in ASP-DAC 2005 for AMDREL IST-34793.
Further Information	Dimitrios Soudris is also member at the Institute of Communications and Computer Systems

	Prof. David Atienza (EPFL, Switzerland, and Complutense University of Madrid, Spain) http://esl.epfl.ch/
Technical role(s) within ArtistDesign	Collaboration with IMEC vzw.and contribution to the Hardware Platforms and MPSoC cluster and the Software Synthesis, Code Generation and Timing Analysis cluster.
Research interests	David Atienza received his MSc and PhD degrees in Computer Science from Complutense University of Madrid (UCM), Spain, and Inter-University Micro-Electronics Center (IMEC), Belgium, in 2001 and 2005, respectively. Currently he is Professor and Director of the Embedded Systems Laboratory (ESL) at Ecole Polytechnique Fédérale de Lausanne, Switzerland, and Adjunct Professor at the Computer Architecture and Automation Department of UCM. His research interests focus on design methodologies for high-performance embedded systems and Systems-on-Chip (SoC), including new thermal management techniques for Multi-Processor SoCs, dynamic memory management and memory hierarchy optimizations for embedded systems, novel architectures for logic and memories in forthcoming nano-scale electronics, Networks-on-Chip interconnection design, and low-power design of embedded systems.
Role in leading conferences/journals/etc in the area	In these fields, David Atienza is co-author of more than 90 publications in prestigious journals and international conferences, such as, IEEE TCAD, IEEE Micro, IEEE T-VLSI Systems, ACM TODAES, Elsevier-Integration: The VLSI Journal, DAC, ICCAD, DATE, ASP-DAC, etc. Also, he is part of the Technical Program Committee of the DATE, ICCAD, GLSVLSI, VLSI-SoC, RTAS, SBCCI and PATMOS conferences, and Associate Editor of IEEE Transactions on CAD (in the area of System-Level Design) and Elsevier Integration: The VLSI Journal. He is the general chair of VLSI-SoC 2010 and organizer of several conferences including GLSVLSI ‘09, ISVLSI ‘09 and SBCCI ’09.
Notable past projects	MDDTNSB-B22: “Materials, Devices and Design Technologies for Nanoelectronic Systems Beyond 22 nm CMOS” project Development of reliability-aware design methodologies for emerging nano-scale electronics. CMOSAIC project Design of design 3D stacked processing architectures with interlayer cooling. TIN2005-ARCHITECT project HW/SW technologies for the design of high-performance processing systems

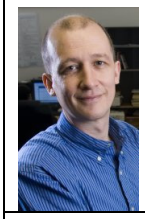
Awards / Decorations	David Atienza received the nomination as co-author for the "2004 DAC Best Paper Award" and the "2006 ICCAD Best Paper Award". In September 2008 he was named IEEE Young Gold Member Coordinator in the area of EDA.
Further Information	Since 2008, he an elected member of the Executive Committee of the IEEE Council of Electronic Design Automation (CEDA).

	Associate Professor Per Gunnar Kjeldsberg (NTNU) www.iet.ntnu.no/en
Technical role(s) within ArtistDesign	Collaboration with IMEC vzw.and contribution to the Hardware Platforms and MPSoC cluster and the Software Synthesis, Code Generation and Timing Analysis cluster.
Research interests	Per Gunnar Kjeldsberg received his Sivilingeniør degree (MSc) in electrical engineering in 1992 from the Norwegian Institute of Technology. In 2001 he received the degree of Doktor ingeniør (PhD) from the same institution (now Norwegian University of Science and Technology, NTNU). During his doctoral studies, he focused on storage requirement estimation and optimization for data intensive applications. The research was performed in close cooperation with IMEC, in Leuven, Belgium, where he was a visiting researcher for nine months in all. His research interests are embedded hw/sw systems, with a focus on multi-media and digital signal processing applications. Between October 2005 and June 2006, Kjeldsberg was a visiting researcher at University of California, Irvine, Center for Embedded Computer Systems.
Role in leading conferences/journals/etc in the area	Kjeldsberg has (co-)authored a large number of conference and journal papers, and has been coauthor of a book in his field of interest. He is frequently used as reviewer for several international journals and conferences.
Notable past projects	CUBAN project Co-optimized Ubiqutious Broadband Access Networks with focus on cross-layer optimized implementation of DSP algorithms. CoDeVer/Embla Codesign, verification, and languages for embedded systems in close cooperation with industry partners
Further Information	Between 1992 and 1996 Kjeldsberg worked as a design engineer at Eidsvoll Electronics, designing communication control equipment based on embedded hw/sw solutions. Currently he is an Associate Professor at the Department of Electronics and

	Telecommunications, NTNU. Here he teaches several extensive undergraduate and graduate courses, and supervises a number of students at master and PhD level. Kjeldsberg is and has been a member of the board of directors both at the Faculty and in private companies.

4.4 Affiliated International Partners

	Prof. Krishnendu (Krish) Chakrabarty, Department of Electrical and Computer Engineering, Duke University, USA
Technical role(s) within ArtistDesign	Collaboration with DTU on microfluidics-based biochips. Contributions to the Hardware Platforms and MPSoC cluster.
Research interests	Design and test of system-on-chip integrated circuits, microfluidics-based biochips (digital microfluidics, microelectrofluidics), and wireless/sensor networks.
Role in leading conferences/journals/etc in the area	He is an Editor of the Journal of Electronic Testing: Theory and Applications (JETTA), an Associate Editor of IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on VLSI Systems, IEEE Transactions on Biomedical Circuits and Systems, and ACM Journal on Emerging Technologies in Computing Systems. He serves on the editorial board of IEEE Design & Test of Computers. During 2006-2007, he served as an Associate Editor of IEEE Transactions on Circuits and Systems I, and before that as an Associate Editor of IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing.
Awards / Decorations	Prof. Chakrabarty is currently serving as an ACM Distinguished Speaker. He served as a Distinguished Visitor of the IEEE Computer Society for 2005-2007, and a Distinguished Lecturer of the IEEE Circuits and Systems Society for 2006-2007. He is also a recipient of the Humboldt Research Fellowship, awarded by the Alexander von Humboldt Foundation, Germany, in 2003.
Further Information	http://people.ee.duke.edu/~krish/

	Assist. Prof. Patrick Schaumont, Department of Electrical and Computer Engineering, Virginia Tech, USA
Technical role(s) within ArtistDesign	Collaboration with DTU on hardware description languages for MPSoC platforms. Contributions to the Hardware Platforms and MPSoC cluster.
Research interests	Design methods and architectures for secure embedded systems.
Further Information	http://www.ece.vt.edu/schaum/

5. Internal Reviewers for this Deliverable

Prof. Paul Pop (Technical University of Denmark)

Prof. Bengt Jonsson (Uppsala University)