214373 ArtistDesign
Network of Excellence
on Embedded Systems Design

Periodic Activity Report for Year 1

Executive Summary

Joseph Sifakis – ArtistDesign Scientific Coordinator
Bruno Bouyssounouse – ArtistDesign Technical Coordinator

ArtistDesign Consortium

1. Project Objectives

The ArtistDesign NoE is the visible result of the ongoing integration of a community.

The central objective for ArtistDesign is to build on existing structures and links forged in the ARTIST2 NoE, to become a virtual Centre of Excellence in Embedded Systems Design. This is achieved through tight integration between the central players of the European research community. Also, the consortium is smaller, and integrates several new partners. These teams have already established a long-term vision for embedded systems in Europe, which advances the emergence of Embedded Systems as a mature discipline.

ArtistDesign is becoming the main focal point for dissemination in Embedded Systems Design, leveraging on well-established infrastructure and links. It will extend its dissemination activities, including Education and Training, Industrial Applications, as well as International Collaboration. ArtistDesign will establish durable relationships with industry and SMEs in the area.

ArtistDesign builds on existing international visibility and recognition, to play a leading role in structuring the area.

The research effort aims to integrate topics, teams, and competencies, grouped into 4 Thematic Clusters: “Modelling and Validation”, “Software Synthesis, Code Generation, and Timing Analysis”, “Operating Systems and Networks”, “Platforms and MPSoC”. “Transversal Integration” covering both industrial applications and design issues aims for integration between clusters.

2. Contact Details and Contractors Involved

2.1 Core Partners

For a complete description including web links, see:
http://www.artist-embedded.org/artist/-ArtistDesign-Participants-.html

Scientific Coordinator:
Joseph Sifakis
Tel: +33 4 56 52 03 51
Joseph.Sifakis@imag.fr

Technical Coordinator:
Bruno Bouyssounouse
Tel: +33 4 56 52 03 68
Bruno.Bouyssounouse@imag.fr

N°	Beneficiary name	Beneficiary short name	Country
1	UJF FILIALE	FLORALIS	France
2	UNIVERSITE JOSEPH FOURIER GRENOBLE 1	UJF/VERIMAG	France
3	RHEINISCH-WESTFAELISCHE TECHNISCHE HOCHSCHULE AACHEN	AACHEN	Germany
4	AALBORG UNIVERSITET	AALBORG	Denmark
5	UNIVERSIDADE DE AVEIRO	AVEIRO	Portugal
6	ALMA MATER STUDORIUM - UNIVERSITA DI BOLOGNA	BOLOGNA	Italy
7	TECHNISCHE UNIVERSITAET BRAUNSCHWEIG	TUBS	Germany
8	UNIVERSIDAD DE CANTABRIA	CANTABRIA	Spain
9	COMMISSARIAT À L'ENERGIE ATOMIQUE	CEA	France
10	DANMARKS TEKNISKE UNIVERSITET	DTU	Denmark
11	UNIVERSITAET DORTMUND	DORTMUND	Germany
12	ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE	EPFL	Switzerland
13	EMBEDDED SYSTEMS INSTITUTE	ESI	Netherlands
14	EIDGENOESSISCHE TECHNISCHE HOCHSCHULE ZUERICH	ETH Zurich	Switzerland
15	INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM VZW	IMEC	Belgium
16	INSTITUT NATIONAL DE RECHERCHE EN INFORMATIQUE ET AUTOMATIQUE	INRIA	France
17	TECHNISCHE UNIVERSITAET KAISERSLAUTERN	TUKL	Germany
18	KUNGLIGA TEKNIKA HOGSKOLAN	KTH	Sweden
19	LINKÖPINGS UNIVERSITET	LINKOPING	Sweden
20	LUNDS UNIVERSITET	ULUND	Sweden
21	MAELARDALENS HOEGSKOLA	MDH	Sweden
22	OFFIS E.V.	OFFIS	Germany
23	PROJECT FOR ADVANCED RESEARCH OF ARCHITECTURE AND DESIGN OF ELECTRONIC SYSTEMS	PARADES	Italy
24	UNIVERSITAET PASSAU	PASSAU	Germany
25	SCUOLA SUPERIORE DI STUDI UNIVERSITARI E DI PERFEZIONAMENTO SANT'ANNA	SSSA-PISA	Italy
26	INSTITUTO SUPERIOR DE ENGENHARIA DO PORTO	PORTO	Portugal
27	UNIVERSITAET DES SAARLANDES	SAARLAND	Germany
28	UNIVERSITAET SALZBURG	PLU-SALZBURG	Austria
29	UPPSALA UNIVERSITET	UPPSALA	Sweden
30	TECHNISCHE UNIVERSITAET WIEN	VIENNA	Austria
31	UNIVERSITY OF YORK	YORK	UK

2.2 Affiliated Partners

Affiliated partners play a very strong role in the Spreading Excellence from the core partners to the research and industrial communities at large.

Affiliated partners generally play an active role in the research activities, either participating directly in research, or transferring the results directly to industry.

Each of the JPRA and JPIA activities' deliverables provides the list of the corresponding affiliated partners and roles.

Affiliated Industrial Partners

The complete set of Affiliated Industrial partners, including web links, is available online, here: http://www.artist-embedded.org/artist/-Affiliated-Industrial-Partners-.html

Christer Norström Göran Arinder	ABB	Peter Mårtensson	NOKIA Connecting People
David Lesens	EADS Astrium Space (EADS)	Dirk Ziegenbein	BOSCH Robert Bosch AG
Thomas Thurner Matthias Grochtmann	DaimlerChrysler	Sven Holme Sørensen	SIEMENS
Dr Joachim Stroop	dSPACE	Roberto Zafalon	ST
Alain Ourghanlian	EDF Electricité de France	Dr. Kai Richter	SYMTA VISION
Jan Lindblad	ENEA	Thomas Hune	TERMA
Johan Eker	ERICSSON	Dominique Potier, Philippe Kajfasz	THALES

Philippe Baufreton	Hispano-Suiza Groupe SAFRAN
Vladimir Havlena	Honeywell
Dr. Michael Winokur	IAI Israel Aircraft Industries
Dr. Matthias Gries	intel Intel Gmbh
Peter Mårtensson	MAQUET Maquet Critical Care
Fabian Wolf	VW
Magnus Hellring	VOLVO
Magnus Hellring	VOLVO
Jakob Axelsson	VOLVO for life

Affiliated SME Partners

Alan Moore	ARTiSAN SOFTWARE
Dr. Monica Donno	BullDAST Design Automation Services and Tools
Joachim Stroop	dSPACE
Jan Lindblad	ENEA
Bernard Dion	ESTEREL Technologies
Paolo Gai	Evidence
Carl von Platen	IAR SYSTEMS
António Garrido	LIFTECH LIFT TECHNOLOGIES
Fernando Santos	Micro I/O www.microio.pt
	VALIOSYS

Affiliated Academic Partners

Prof. Ahmed Bouajjani

LIAFA - Université Paris 7 & CNRS UMR 7089

Tel: +33 (0) 1 4427 7819

Dr. Frédéric Boulanger

Ecole supérieure d'électricité (Supélec), Computer Science Department
Component-Based Design of Heterogeneous Systems

Tel: +33 1 69 85 14 84

Prof. Lubos Brim

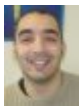
Masaryk University Brno

Tel: +420 549 493 647

Prof. Dr. Dr. h.c. Manfred Broy

TU München

Tel: +49 89 289-17304



Ass. Prof. Salvatore Carta

Università degli Studi di Cagliari

Tel: +39 070-675-8780

Dr. Francky Catthoor

IMEC

Tel: +32 16 281202

Prof. Lucia Lo Bello

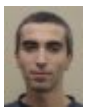
University of Catania

Tel: +39 095 7382386

Prof. Dr. Miroslaw Malek

Humboldt University Berlin

Tel: +49 30 2093 3027



Dr. Pau Martí Colom

Universitat Politècnica de Catalunya

Tel: +34 93 401 1679

Dr. Fabio Martinelli

Istituto di Informatica e Telematica

National Research Council C.N.R.

Tel: +39.050.315.3425

Dr. Marius Minea

Timisoara - Institute e-Austria Timisoara

Tel: +40-256-403284

Associate Prof. Laurent Pautet

ENST

Tel: +33 1-45-81-73-22

Prof. Geert Deconinck

Katholieke Universiteit Leuven

Tel: +32 16 32.11.26

Prof. Giovanni DeMicheli

EPFL Lausanne

Tel: (+41 21) 693-0911

Prof. Ivo De Lotto

Università degli studi di Pavia
Team leader

Tel: +39 0382 98 53 57

Prof. Dr. Ed Deprettere

Leiden University

Tel: +31 (0)71 5275776

Prof. Luca Fanucci

University of Pisa

Prof. Dr. Marisol Garcia-Valls

Universidad Carlos III de Madrid

Tel: +34 91-624-8783

Julián Proenza

University of the Balearic Islands

Tel: (+34) 971 17 29 92

Dr. Isabelle Puaut

IRISA

Tel: +33 02 99 84 73 10

Michael Rusinowitch

INRIA
Formal methods on embedded systems – in particular on verification of security properties.

Tel: +33 03 83 59 30 20

Prof. Pablo Pedro Sanchez

Universidad de Cantabria
Design and Implementation of Embedded H/S Systems

Tel: +34 942 201548

Dr. Markus Schordan

TU Vienna

Prof. Donatella Sciuto

Politecnico di Milano

Tel: +39-02-2399 3662


Prof. José Maria Giron-Sierra
University Complutense of Madrid
Tel: +34913944387


Prof. Axel Jantsch
Royal Institute of Technology (KTH)
Tel: +46 8 790 4124; +46 70 713 7428


Prof. Christoph Kirsch
University of Salzburg
Tel: +43 (0) 662 8044-6328


Prof. Stefan Kowalewski
RWTH Aachen
Tel: +49 241 80 21150


Prof. Andreas Krall
TU Vienna


Prof. Luciano Lavagno
Politecnico di Torino
Tel: +39-011-5644150


Prof. Johan Lilius
Åbo Akademi University


Ass. Prof. Dimitrios Soudris
Democritus University of Thrace
Tel: +30 25410 79557


Prof. Neeraj Suri
TU Darmstadt
Tel: +49 6151 16 3513


Prof. Dr.-Ing. Jürgen Teich
University of Erlangen-Nuremberg
Design Methodology for Embedded Systems
Tel: +49 9131 85 25150


Dr. ir. Jan Tretmans
University of Nijmegen
Tel: +31 24 365 2069


Prof. Pierre Verbaeten
Katholieke Universiteit Leuven
Tel: +32 (0)16 32 75 66


Prof. Eugenio Villar
Universidad de Cantabria
Design and Implementation of Embedded H/S Systems
Tel: +34 942 201398

Tel: +358-40-544 0741	

Affiliated International Collaboration Partners

Prof. Tarek Abdelzaher

University of Illinos at Urbana-Champaign
Technical expert

Tel: +1 217 265-6793

Prof. Zhou Chaochen

Chinese Academy of Sciences

Prof. Giovanni De Micheli

EPF Lausanne

Tel: +41 21 693-0911

Assoc. Prof. Stephen A. Edwards

Columbia University

Tel: +1 212 939 7019

Prof. Sharon Hu

University of Notre Dame - Indiana USA
Design for Low Power

Tel: +1 574 631-6015

Shankar Sastry

Berkeley University

Tel: +1 (510) 643-2200

Prof. Heinz Schmidt

Monash University (Australia)

Tel: +61 3 9905-2479

Prof. Lui Sha

University of Illinos at Urbana-Champaign
Technical expert.

Tel: +1 244-1887

Assoc. Prof. Mircea R. Stan

University of Virginia
Power and thermal modeling at the device, circuit and system level.
Self-consistent power modeling by taking into account thermal effects.
Temperature-aware circuit design.
Automotive computing applications.
Participates in the activity on Design for Low Power.

Tel: +1 434 924 3503

Prof. Mathai Joseph

Tata Research Development & Design Centre (TRDDC)

Prof. Edward A. Lee

UC Berkeley

Tel: +1-510-642-0253

Prof. Xiaojian Liu

Zhiming Liu

UNU-IIST Macau
Co-organiser of the Artist2 / UNU-IIST School in China - 2007

Tel: +853 712930

Prof. Kang Shin

University of Michigan

Tel: +1 (734) 763-0391

Prof. John Stankovic

University of Virginia

Tel: +1 (434) 982-2275

Prof. Janos Sztipanovits

Vanderbilt University USA

Tel: +1 615-343-7572

Prof. P.S. Thiagarajan

National University of Singapore

Tel: (65) 6516 7998

3. Vision and Assessment of the Work Performed

ArtistDesign finances durable integration between teams and not the concrete elements of the JPA which most often belong to other projects. These specific technical objectives may or may not be attained (this is the essence of research as opposed to development), but we feel that the main product of ArtistDesign is the emergence of a lasting European research community, that has a significantly enhanced capacity for preparing Europe's future.

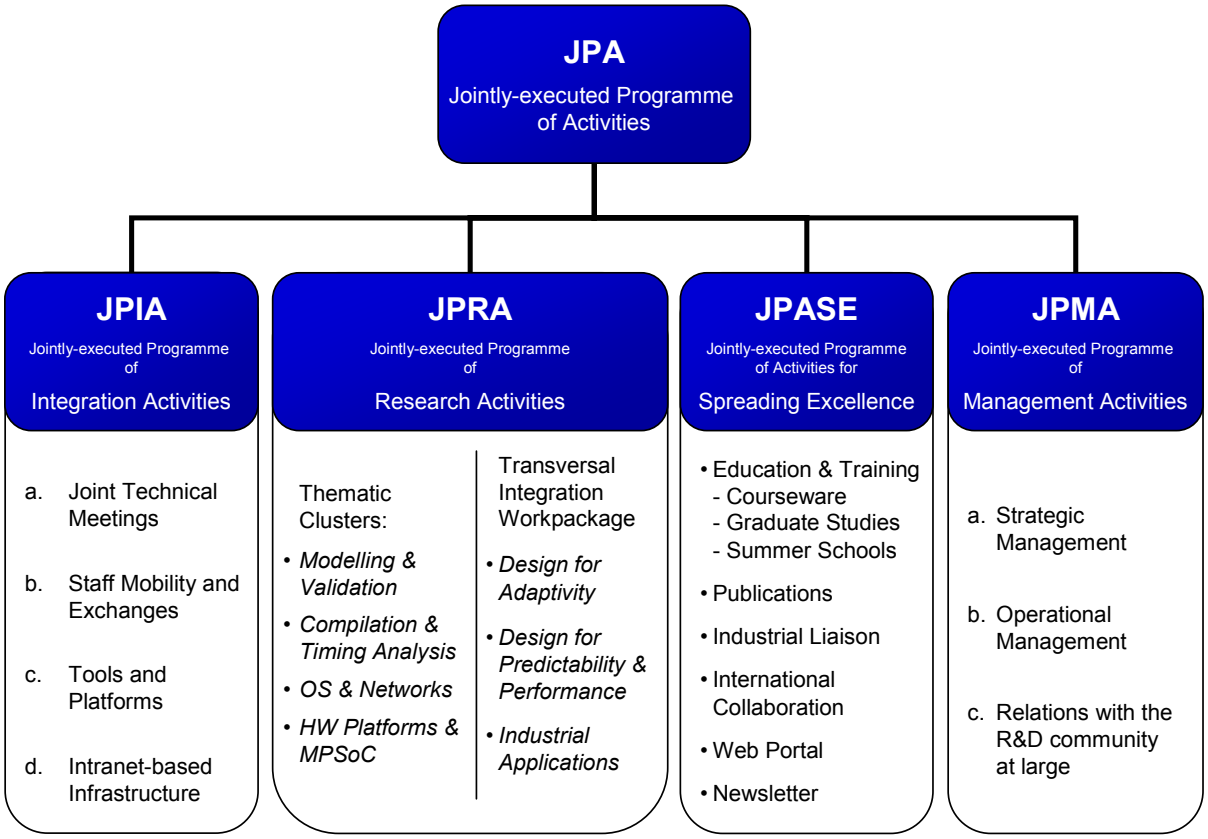
The research is completed by work in the JPIA (Jointly Executed Programme of Integration Activities) workpackage, which aim to transform research results in tangible tools and components, and bring teams closer together on a day to day basis.

We believe that the topics chosen provide a good coverage of the area, for embedded software and systems.

The ArtistDesign NoE is a complex construction assembled from world-leading communities, teams, and individuals. This is certainly an asset, but also a source of complexity in management. Each team has two essential characteristics: world-class excellence and strong interaction with top industrial players. ArtistDesign partners play a leading role in the different communities in embedded systems design, and they advance the state of the art in each of these.

It is difficult to abstract out a global synthesis of the overall technical achievements. This is due to the diversity and the low granularity of the actions to be covered (meetings, publications, attendance at workshops, visits, and platforms).

The following is a certainly non-exhaustive assessment of the work in the Joint Programme of Activities' 4 main branches.



3.1 Joint Programme of Research Activities (JPRA)

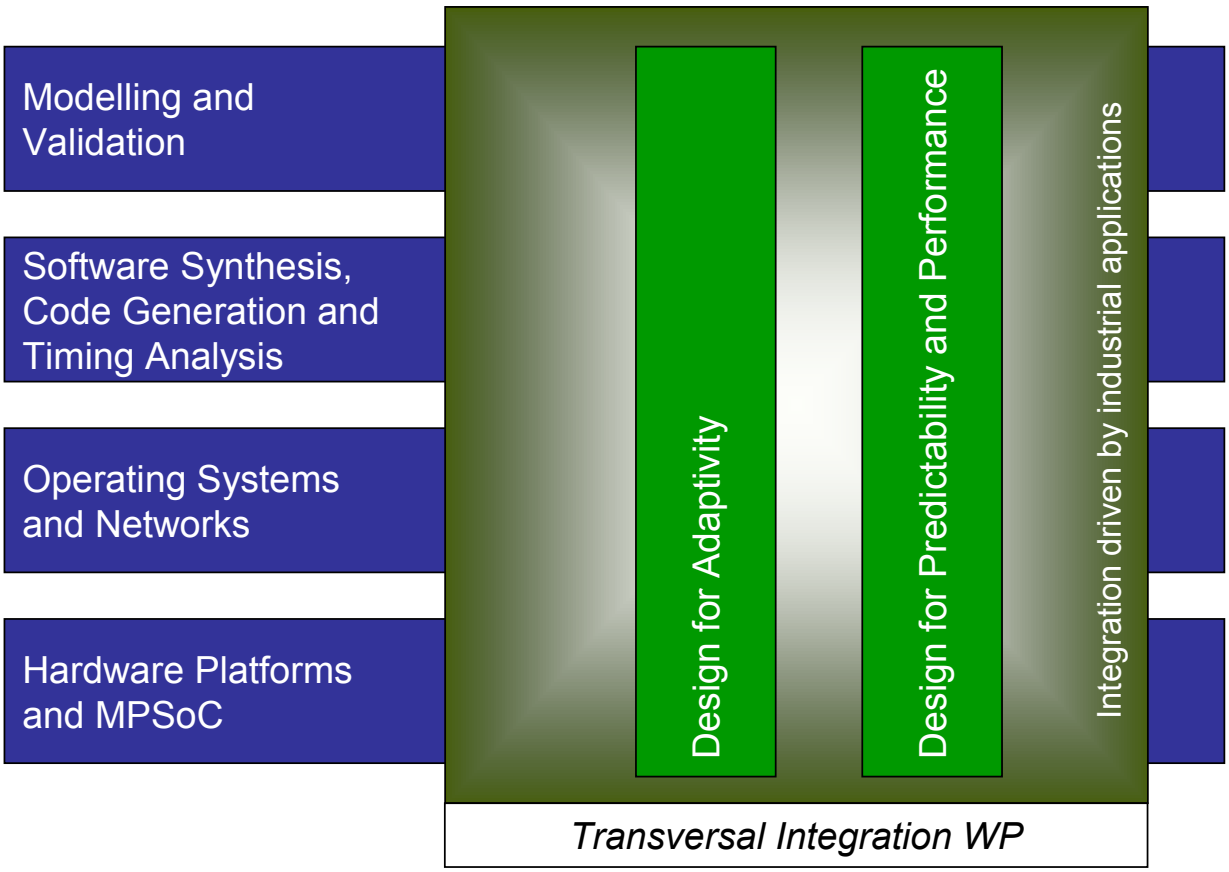
3.1.1 Structure of the Research Effort

The JPRA is composed of intra and inter-cluster research activities on cutting-edge topics in embedded systems design. While the main bulk of financing for these activities is taken up by outside programmes (Integrated Projects, National Programmes, Industrial Contracts, etc), the ArtistDesign NoE finances the extra burden due derived from integrating these into a single coherent research programme.

Thus, the essential ingredient within ArtistDesign is the JPRA, which motivates the participating research teams far more than the actual financing, which is tiny in comparison with the overall research aims. It is completed by the Joint Programme of Integrating Activities (JPIA), and the Joint Programme of Activities for Spreading Excellence (JPASE), and overseen by the Joint Programme of Management Activities (JPMA).

The structure of the research activities reflects the following decomposition of the embedded systems design flow.

This design flow is composed of the following cooperating activities, starting with component-based modelling and leading to implementation. These activities must be well coordinated, and supported by tools and methods to ensure satisfactory levels of productivity and quality. Accordingly, we have structured the area of embedded systems design into the following topics.



Modelling and Validation. Unlike other computer systems, embedded systems are strongly connected with a physical environment. A scientific foundation for embedded systems must therefore deal simultaneously with software, hardware resources, and the physical environment, in a quantitative manner. In order to gain independence from a particular target platform, embedded system design must be model-based. In order to scale to complex applications, embedded system design must be component-based. The overall objective of this activity is develop model and component based theories, methods, and tools that establish a coherent family of design flows spanning the areas of computer science, control, and hardware. The activity brings together the most important teams in the area of model and component based design in Europe.

SW Synthesis, Code Generation and Timing Analysis. There is a continuing demand for higher performance of information processing, which stimulates using a growing amount of parallelism (including using multiple processors). This trend affects the design of embedded systems. We address issues related to multiple heterogeneous processors on a chip, also containing memory hierarchies and communication interfaces. Such processors can only be exploited if (sets of) applications can be efficiently mapped to heterogeneous processors. Timing analysis is also affected by the trend toward the new platforms. Timing analysis has to cope with the kind of memory hierarchies found in MPSoCs. Also, timing analysis beyond the single processor is required. Hence, timing analysis will also consider the timing of communication. The overall objective is to provide safe timing guarantees for systems consisting of local memories hierarchies and multiple processors.

Operating Systems and Networks. We investigate how current real-time operating systems have to be extended or modified to support emerging real-time embedded systems characterized by a high degree of complexity, highly variable resource requirements and parallel processing such as multicores. Most embedded systems are often characterized by scarce resources in terms of processing power, memory, space, weight, energy, and cost. Hence, another objective is to investigate kernel mechanisms that can efficiently manage the available resources, taking multiple constraints into account, whilst guaranteeing isolation properties. Also, to support dynamic applications with variable resource requirements or to cope with unpredictable resource availability, feedback control techniques for resource management at the operating system and application level are also investigated.

Hardware Platforms and MPSoC Design. While hardware platforms for embedded applications will continue to be multi-core, with increasing degrees of parallelism, the evolution trajectory on programming models, design-time and run-time application environments is much less clear. The consequence is fragmentation: while many research teams are working on one or more of these domains, there is little communication and integration, this leads to duplication of results and overall slow progress. The teams involved in this activity have a wide-ranging research experience which covers all the key areas in MPSoC application specification mapping. The integration activity supported by ArtistDesign will help the participants to the cluster in strengthening the coherency of their approaches and focus on addressing complementary issues in a synergistic fashion.

Design for Adaptivity. An embedded hardware-software system is adaptive, if it can modify its behaviour and/or architecture to changing requirements. Adaptivity is increasingly important as the complexity and autonomy of embedded systems increases. Adaptivity is a cross-cutting system characteristic that affects both hardware and software. At the software-level adaptivity is mainly concerned with flexible and adaptive resource scheduling, e.g., CPU time scheduling. At the hardware-level adaptivity includes both adaptation of operation modes, e.g., supply voltage and clock frequency, processor instruction sets, and dynamic management of hardware resources, e.g., processing elements and memory.

Design for Predictability and Performance. Many applications have strict requirements on timing, and limited resources (memory, processing power, power consumption, etc.). All systems also have increasing demands on (average) performance, which has motivated the introduction of features such as caching, pipelining, and (now becoming very prominent) multiprocessor platforms. Almost all such efficiency-increasing features drastically increase variability and decrease analyzability of response-times, etc. and thus have a detrimental effect on predictability. Since the introduction of new architectural features is inevitable, it is important to: a) develop technology and design techniques for achieving predictability of systems built on modern platforms, and b) investigate the trade-offs between performance and predictability.

Integration Driven by Industrial Applications. To have a strong impact on industry and society at large, the results of the Thematic Clusters need to be harmonized in an overall design flow that can sustain the embedded design chain from conception of the product to its implementation. The design chains vary in length and players according to the industrial segment addressed: for example, the design chain in automotive electronics starts with the car maker (e.g., BMW, Daimler Chrysler, Peugeot, Fiat), goes through the Tier 1 suppliers (e.g., Contiteves, Bosch, Magneti Marelli) and connects to the Tier 2 suppliers (e.g., FreeScale, ST, Infineon, Hitachi). It often includes IP providers such as programmable cores, RTOS and software development tool providers and design service companies. In the mobile communication domain, the chain starts with the application developers (e.g., gaming and video content), includes the telecommunication operators (e.g., Telecom Italia and Telefonica), the device makers (e.g., Nokia and Ericsson), the silicon makers (e.g., TI, Qualcomm and ST) and outsourcing manufacturing companies (e.g., Flextronics). Today, there is stress in the chain as the technology advances may create opportunities to redefine the roles of the various players. In addition, the system integrators are often faced with an almost impossible task of composing their design out of parts supplied by companies whose design methods and standards are widely different and about which they have limited or no information. There is a need for an all-encompassing approach to system design that can make an entire industrial segment work as a virtual vertically integrated company.

3.1.2 *Overview of the Year1 Research Results*

We present an overall vision integrating aspects from both the Artist2 European Network of Excellence (ended Sept 30th 2008) and ArtistDesign. This more complete vision is not necessarily followed in the Cluster and Activity deliverables, to avoid “double reporting”.

3.1.2.1 Modeling and Validation

Modeling

On modelling heterogeneous systems, we have obtained some very significant results:

- Work by INRIA, PARADES, and VERIMAG, on the theory of tagged systems provides conditions for correct implementation of synchronous systems on “less synchronous” architectures. Work by INRIA on new models of computation, the Kahn-extended Event Graph (KEG), which adds “static control” in the Model of Computation of Marked Graphs.
- Work on the BIP component framework, introduces a notion of expressiveness for component-based formalisms, which provides a basis for their comparison. This notion

drastically differs from the usual one, as it takes into account the expressive power of composition operators (glue operators).

- Significant progress has been achieved in methods for distributed implementation of non-distributed specifications. VERIMAG studied a method for the automatic generation of distributed implementations of BIP models. INRIA, PARADES and VERIMAG studied the concept of loosely time-triggered architectures, implementing time-triggered architectures. Finally, fully asynchronous implementations of synchronous systems have been studied.
- Other results on distributed implementations include reliability, new heuristics in scheduling for reliability, design of communication architectures and time-triggered system-on-chip architectures.

Validation

At the crossroads between Modeling and Validation, we have obtained significant results on Interfaces and Composability, including:

- The development of interface theories supporting component reuse (EPFL). We have shown that existing interface theories provide no formal support for component reuse. We enriched interface theories with a new operation allowing the same component to implement several different interfaces in a design.
- The development of contract-based verification techniques for the heterogeneous rich component (HRC) model (INRIA, PARADES, VERIMAG), in the framework of the SPEEDS project. The techniques allow handling multiparty interaction, as well as many different languages for describing notions of refinement under contexts. These results found application in the verification and analysis of HRC models.
- In joint work, ETHZ and Uppsala propose modular performance analysis techniques, based on the real-time calculus and timed automata. A prototype tool name CATS for compositional timing and performance analysis has been developed.
- VERIMAG has continued the work on compositional deadlock verification of BIP programs, and its implementation in the DeadlockFinder tool. Other results include the enhancement of existing component models, such as the synthesis of controllers from specifications and the generation of component models from their observed behaviour.
-

On qualitative validation, work has been carried out in the following directions:

- Significant contributions to game-theoretic approaches to real-time system testing. By modelling the systems as timed game automata and specifying the test purposes as formulas, we developed a timed game solver Tiga to synthesize testing strategies.

  We studied games for different extensions of timed automata such as weighted timed automata, priced timed automata, multi-priced timed automata. The results relate to the complexity of decision problems for these automata, as well as model checking and synthesis algorithms. The notion of timed parity games has been studied, with a focus on robustness and complexity. We have also studied reachability in timed games.

- Continuing on work from previous years, we have extended and improved the functionality of the UPPAAL tool, including the use of slicing techniques for model optimization as well as features supporting interface theory for real-time systems.

- We have studied quantitative testing techniques. In particular, we have developed a theory allowing testing of systems in the presence of measurement imprecisions. We also studied testing methods for probabilistic processes.

- We have studied quantitative model checking techniques for timed models, including timed automata, linear hybrid automata and general non-linear hybrid systems. The work on verification has been applied to non-trivial case studies and systems, in particular in collaboration with industry.

Finally, we have studied compositional synthesis and verification techniques. These include modular supervisory control, as well as the verification of component-based systems.

3.1.2.2 Software Synthesis, Code Generation and Timing Analysis

Software Synthesis and Code Generation

We developed research in the following directions:

- We studied the influence of scratchpad memory allocation techniques on worst case execution times (WCET). We developed integer linear programming models to decide which parts of a program's code or data can be moved onto the highly predictable scratchpad. First experiments show WCET reductions of more than 50% for several benchmarks.
  We also investigated WCET-aware register allocation techniques, by extending existing techniques based on graph colouring.

- We continued work on scalable source-level analysis and annotation-based timing analysis methods. The SATIrE infrastructure allows building analysers that take source code annotations as additional input, and generate output as annotations. This allows a significant increase in productivity, by requiring the user to annotate the relevant timing information that cannot be automatically computed. The integration of PAG was instrumental in investigating the scalability of analyses.

- We studied polyhedral loop parallelisation techniques for multi-core systems.

Regarding tools and platforms, we developed work in the following directions:

- We designed a Static Loop Analyzer, allowing to estimate loop iteration bounds. This information is essential for a large number program analyses. Our analyser improves analysis techniques based on conventional abstract interpretation by integrating a new static polytope-based loop evaluation method.
  We have demonstrated the applicability of the analyser on benchmarks taken from the benchmark suites MRTC, DSPStone, MiBench, UTDSP and MediaBench. Our loop analyser was the only tool able to answer all questions related to flow fact during the WCET tool challenge 2008.

- In continuation of work performed in Year 3, we developed a new WCET-aware procedure positioning and cloning technique. The compiler optimisations obtained were exploited for WCET reduction. Results on real-world benchmarks show WCET reductions of 10% on average, while ACET is reduced by 2 on average.

The cooperation between ACE and Aachen on the retargetable code optimizations has been continued. The conditional execution engines have been extended by a strong retargeting formalism.

Timing Analysis

In addition to experimental work, we developed important results on Timing Analysis.

We have studied a notion of time predictability of cache architectures, which is the first precise notion found in the literature. Four different cache replacement strategies were compared and the LRU strategy was found to be optimal. This research is related to work within the PREDATOR FP7 project, which attempts to reconcile performance and predictability.

The study of Timing anomalies, where local worst-case choices may not lead to the global worst-case scenario, is essential for time predictability. We have studied techniques for handling timing anomalies for efficient WCET analysis, as well as for measuring the impact of timing anomalies on WCET analysis.

Other work on Timing Analysis includes parametric Timing Analysis, where some parameters of the program can remain unknown until execution. We also developed Timing Analysis techniques, in collaboration with BOSCH, taking into account operating modes of programs, computed semi-automatically. Finally, we developed WCET analysis for systems with preemptive scheduling.

Work on the AIR format has continued. The format was extended and adapted to the needs of the partners. The attribute database was extended with new attributes.

We also worked on the development and improvement of formats for ensuring the interoperability of the tools. The work on formats includes ALF for computation semantics representation, conversion of the ABSINT AIR format to SWEET format, and the definition of common flow description attributes.

As was the case last year, the WCET Challenge 2008 consisted of a set of benchmark programs and analysis tasks to be performed by the contestants.
http://www.artist-embedded.org/artist/-WCET-08-.html

3.1.2.3 Operating Systems and Networks

Resource-aware Operating Systems

In addition to work done in Artist2, we developed work in the following directions:

- Modeling and analysis of control-driven tasks. The standard design of control is based on the periodic sampling. We studied a model which saves a considerable amount of computational resources which samples the inputs when needed.
- Implementation of a flexible scheduling framework called FRSH that is capable of handling multiple concurrent activites with different criticality and timing in the same system. The framework has been designed to be implemented on different platforms.
- ERIKA support for the EasyBee radio transceiver has been developed.
- We studied issues relating to the operating system support needed by advanced users of a real-time specification for Java. In particular, two issues have been addresses: how to handle systems that contain a large number of events; and how to measure blocking time.

Scheduling and Resource Management

We have had a large volume of activity on this topic:

- All the partners, under the leadership of York, have worked for establishing a taxonomy of resource usage. The taxonomy distinguishes between different classes of resources - each class being subdivided into a number of resource types.
- The architectural model of a Flexible Scheduling Framework developed in the FRESCOR and FIRST EU-IST projects has been extended to include a contract model. Contracts represent complex requirements of the applications which can be managed by the underlying system to provide the required level of service.
- Several activities on scheduling, in particular multi-resource scheduling for multi-core platforms, schedulability for CAN-based control applications, sensitivity analysis, flexible scheduling on low-cost microcontrollers.
- Other work related to the Transversal Activity: “Design for Adaptivity” has been carried out, including dynamic runtime adaptability, optimal period selection and scheduling for embedded controllers.

Real-Time Networks

We have carried out work on:

- Analysis techniques, including Worst Case analysis and dimensioning of cluster-tree Wireless Sensor Networks, as well as analysis for specific networks.
- We studied techniques for supporting real-time communication and QoS for Wireless Sensor Networks. These include work around the use of IEEE 802.15.4 and ZigBee as federating communication protocols for Wireless Sensor Network applications, as well as supporting real-time communication of the Erika real-time operating system.
- We have also furthered work, started in Artist2, on student design competitions in the scope of the IEEE Real Time Systems symposium.

3.1.2.4 Hardware Platform and MPSoC Design

Platform and MPSoC Design

The work has included:

- Study of system design methodologies handling the dynamic nature of embedded systems and allowing predictability and optimal use of resources.
  Bologna, with ETHZ, has studied optimalisation-centric MPSoC design techniques. The main goal of this work was to establish a common understanding of the MPARM framework developed in Bologna, and the DOL framework developed at ETHZ.
  Bologna and Linkoping have studied a temperature power-optimization system. A temperature-aware dynamic voltage selection technique has been developed for energy minimisation.
  Other work on design optimization for fault-tolerant distributed embedded systems is developed by Linkoping and DTU.

- Bologna and ETHZ have improved the design of a scavenger prototype, to perform automatic maximum power point tracking. They developed a compact model for small solar modules that accurately describes their behaviour over a wide range of irradiance conditions. Furthermore, they improved the efficiency of the DC-CD converter at the solar harvester.
- We (DTU) have studied programming models for MPSoC architectures as well as investigated the hardware/software interface between the processing elements and the interconnect network. We also have studied a component-based service model for early design space exploration and performance estimation.

Platform and MPSoC Analysis

Work on analysis complete the design techniques above, with simulation, and performance analysis techniques:

- We studied techniques for performance estimation of distributed real-time systems, based on simulation, in particular for applications using heterogeneous task scheduling policies. We also studied performance analysis techniques for a MPSoC in collaboration with ST Microelectronics.
- An important work direction is modelling and performance analysis for multi-processor and/or networked systems.

  We studied relations between simulation-based and analytical methods for performance evaluation of distributed real-time systems. Based on experimental simulation results, we were able to draw interesting conclusions regarding the pessimism of formal approaches. The experiments were performed on FlexRay and CAN-based distributed systems.

  We also studied interesting relations between MPA (Modular Performance Analysis) and Timed Automata.
- We have extended the fault-tolerant process model, to consider a combination of hardware and software fault-tolerant techniques. We have proposed a method for computing the reliability of a system, taking into account: a) hardening levels in hardware; b) the re-execution levels in software; c) scheduling for sharing recovery slacks.
- We have worked on modelling and optimisation of a miniaturized solar energy harvester. We focused on the optimisation of two important metrics: a) maximisation of the energy harvesting efficiency and b) the minimisation of the energy used for ineffective operations. A hierarchical control solution has been designed which overcomes several drawbacks of previously proposed approaches. A novel algorithm for approximate multi-parametric linear programming has also been proposed.
- We studied scheduling-based energy optimisation techniques for energy-scavenging wireless sensor networks.

3.1.2.5 Design for Adaptivitty (Transversal Integration activity)

We have worked mainly in two complementary directions: a) Study of architectures and algorithms for ensuring adaptivity; b) Study of modelling and analysis techniques for adaptive systems:

- We studied a symbolic quality control technique for multi-media applications. Adaptivity is ensured by using a controller, which moniotors system execution and adapts quality parameters of its functions so as to meet hard real-time contraints.
- We studied adaptive energy management techniques in clusters of wireless sensor nodes. They allow tuning the application parameters according to the time-varying amount of harvested energy.
- We studied a reference architecture for self-configuring embedded systems in collaboration with Volvo. Algorithms suitable for runtime configuration management, load balancing, and quality of service have been developed and adapted to automotive applications.
- We designed adaptive techniques to enhance real-time support of IEEE 802.11.e networks. For such networks, we developed protocols to enhance the resilience to interference, and to provide an estimation of a relative localisation based on the radio frequency signal.
- We studied techniques allowing the design and performance analysis for multi-mode systems. We also studied online performance analysis techniques for distributed systems. A novel distributed algorithm for control of the global analysis flow has been proposed.
- Several partners have collaborated in the STREP projects FRESCOR and ACTORS to develop an infrastructure for adaptive scheduling of real-time applications.

3.1.2.6 Design for Predictability (Transversal Integration activity)

The technical work on Predictability has intersected work in all the Thematic Clusters.

Modeling and Validation of component –based systems

- We studied the concept of predictability in relation with robustness, and identified two major challenges in embedded systems design. These challenges require a rethinking of the conventional, purely discrete and purely functional foundation of computing.
- We worked on modular performance analysis techniques, based on real-time calculus for systems with cyclic dependencies. We integrated a contract-based scheduling framework with a component-based technology.

Timing Analysis and Compiler Techniques

- The main contribution is work on relations between Timing Analysis and Timing Predictability. A definition of predictability for cache architectures has been proposed, and the relative competitiveness of 4 different cache replacement strategies has been analysed.
- We also investigated WCET analysis techniques for cooperative task scheduling. A method guiding developers of an embedded system to select optimal pre-emption points is under development.
- We also studied parameteric timing analysis techniques that overcome usual limitations of analysis techniques requiring the maximum number of loop iterations to be known statically.

OS/MW/Networks

Our work addressed various issues, including: Integrating scheduling analysis and model checking; influence of abstractions on the schedulability analysis of distributed real-time systems, time-predictable operating systems.

Architecture and System Design

- We studied techniques allowed predictability for fault-tolerant embedded systems and predictability for multi-processor MPSoC architectures.
- We also developed a set of parametyerisable models of L2 Caches and integrated them in an accurate virtual platform environment.
- Finally, we are designing a Precision Timed (PRET) architecture based on a reactive processor, coupled with a MicroBlaze general purpose processor.

3.1.2.7 Industrial Integration (Transversal Integration activity)

This activity groups a set of industrial interactions and collaborations with ArtistDesign teams. The long-term goal is to understand industrial design methodologies and identify the research results that could be applied in these methodologies.

The work this year has consisted in organising a few high-profile meetings with industry (eg: Embedded Systems: Industrial Applications ’08) as well as joint workshops and technical meetings.

At this point, these constitute a rich set of events and interactions, which need to be structured and which need a more specific focus.

3.2 Joint Programme of Integration Activities (JPIA)

3.2.1 Structure of the Integration Effort

The JPIA activities promote integration of geographically dispersed teamsand have long-lasting effects:

Joint Technical Meetings. Joint Technical meetings aim to present, discuss and integrate the ongoing work, and exchange points of view with other teams. They also serve to identify future work directions.

Staff Mobility and Exchanges. This is essential for integration within the NoE, including mobility of students and/or researchers, between core teams, or between core teams and affiliated teams. Mobility is justified by and refers to involvement in an activity from the JPRA or JPIA, or one of the following: co-funded scholarships with industry; exchange of students and personnel within the consortium.

Tools and Platforms. A research platform is composed of competencies, resources, and tools targeting specific technical and scientific objectives around a chosen topic. These are at the state-of-the-art, and are made available to the R&D community for experimentation, demonstration, evaluation, and teaching.

The research platforms, tools and facilities are an essential tool for implementing the JPIA. They will lay the groundwork for the JPRA, allowing common research to occur and capitalisation on research results. Platforms are used as the basis for transfer of research results to industry. They allow teaching practical knowledge of the concepts and techniques.

ArtistDesign platforms are not defined from scratch – they integrate the results of long-term efforts, and are meant to be durable, evolving with the state of the art. The partners are committed to durability, and have invested significant resources into their development. The construction of ArtistDesign has provided the opportunity to assemble existing pieces into a rationally-structured set of platforms, covering the area of embedded systems design.

Some of the ArtistDesign platforms have international visibility, and the ambition is for these to serve as world-wide references in their respective topics.

The detailed information regarding the JPIA activities is available in the JPIA deliverable.

3.2.2 Assessment

The ArtistDesign Network of Excellence is a significant evolutionary step for integrating the leading embedded systems design research teams in Europe. The clusters are more tightly woven together, and each represents a significantly greater critical mass than did the clusters in the Artist2 Network of Excellence, which ended Sept 30th 2008, and has nearly the same consortium.

Despite this strong overlap with the Artist2 NoE, the overall assessment for the WP at the end of ArtistDesign Y1 (Jan–Dec 2008) is positive - both in terms of impact on the overall structuring and lasting integration within the consortium and more generally within the area in Europe.

- The ArtistDesign clusters have been actively pursuing operational integration through joint meetings, staff mobility, and shared platforms and tools.
- The level of activity shows that the Cluster / Activity structure and research topics defined for ArtistDesign make sense, and are viable vehicles for integrating the area. In operational terms, they generate sufficient interest for the partners and individual researchers to participate actively in the joint meetings, to exchange personnel, and to orient the tools and platforms developed to make sense within this structure.
- There is clearly a greater level of maturity for tools and platforms than had been the case at the start of the Artist2 NoE – and the partner teams are actively pursuing a policy of implementing tools, demontrators, and in many cases their accompanying methodologies.
- Nonetheless, it is important to remember that these are tools and platforms for research. The aim is not necessarily always for these to lead to commercially viable tools and start-up companies. In general, they are the concrete realisation of the state-of-the-research, allowing to explore possibilities for future research and later tools (some of which may in turn lead to commercially viable products).
- The level of activity varies according to individual clusters / activities, which is normal. We believe this is partly due to the remaining overlap with Artist2 – which should no longer be the case in Y2.

3.3 Jointly-executed Programme of Activities for Spreading Excellence *(JPASE)*

ArtistDesign leverages on the worldwide visibility of the ARTIST2 NoE. It is progressively creating a European embedded systems design community and spreading the "Artist culture" in all major research institutions.

To ensure that the next generation of researchers will continue in this direction we, as a consortium, devote a great deal of effort to Spreading Excellence, in both academic and industrial circles. Furthermore, through our links with both core and affiliated partners, we actively set up permanent links between industry and public research, based on existing partner collaborations with major industrial players in the area.

The JPASE activities are intended to spread excellence and structure the community at large. They are planned by the Strategic Management Board, and are implemented by ArtistDesign core and affiliated partners.

The NoE will leverage on its members and teams, who play a main role in the organisation of world-class scientific events, to disseminate results in the area. We expect that the NoE's structured and authoritative dissemination will have a strong effect on the community as a whole, for orienting and creating synergy for research.

3.3.1 Education and Training

- Courseware – The NoE has the ambition to serve as a resource and point of reference for the area, including by collecting and disseminating course materials for teaching embedded systems design.
- Graduate Studies – The NoE will provide support for selected graduate studies programmes, as the means for training engineers and researchers in embedded systems design.
- Summer Schools – The NoE will actively support and participate in summer schools and seminars in embedded systems design.
- International Workshop on Embedded Systems Education – We will continue this series of international workshops, started in ARTIST2. York has accepted to lead this activity.
- Implement a high-visibility International Summer School. The ArtistDesign NoE will organise each year a high-visibility international Summer School, drawing top European lecturers in Embedded Systems Design. The audience is researchers, PhD students, and engineers. The following group of core partners will lead this activity: Luca Benini (Bologna), Giorgio Buttazzo (SSSA-Pisa), Petru Eles (Linkoping), Kim Larsen (Aalborg), Peter Marwedel (Dortmund).
- Training Engineers – Many partners are already active in this area, such as IMEC, EPFL, ESI, and Aalborg's CSI. The ArtistDesign NoE will provide logistical, financial dissemination through the Web Portal and newsletter.

3.3.2 Publications in Conferences and Journals

The ArtistDesign consortium is very active in publishing in scientific journals and conferences, as attested by the list of significant publications by the partners' teams.

The NoE leverages on its members and teams, who are strongly implicated in collaboration with industry, to organize and structure industrial relations, and develop mutually beneficial

interactions. Furthermore, through Industrial Liaison, ArtistDesign receives useful feedback about the relevance of work directions and priorities.

3.3.3 Links to Artemisia

ArtistDesign seeks a tight interaction with the Artemis community, through the **Artemisia Liaison Task Force**. This is composed of the following prominent ArtistDesign members, also active in ARTEMIS/ARTEMISIA: Luca Benini, Ed Brinksma, Werner Damm, Jean-Luc Dormoy, Rudy Lauwereins, and Joseph Sifakis. Amongst these, 3 are elected members of the ARTEMIS Steering Board. Joseph Sifakis is the chair of ARTEMISIA's Chamber B.

ArtistDesign partners will be encouraged to join ARTEMISIA.

3.3.4 International Collaboration

The ArtistDesign "*International Collaboration*" activities allow ArtistDesign to be visible internationally, and to monitor the evolution of the state of the art in the area worldwide.

International Collaboration fits into a global win-win strategy for achieving the participants' long-range aims. Examples of activities include:

- **High-level meetings** gathering top representatives from industry, funding agencies, and research, to discuss avenues for International Collaboration, including on R&D and standards e.g. IST/NSF Workshop on Component-based Engineering (Paris, June 05).
- International Collaboration **Working Groups** for exploring possible avenues for research and education in a chosen topic and producing white papers and reports e.g. joint EU/US Working Groups: on Timing Validation, Adaptive Real-Time Systems for Dynamic Applications, Semantic Platform for Hard Real Time (2002 – 2003).
- Organization and sponsoring of international conferences and schools, to disseminate recent research results, and promote the emergence of embedded systems as a discipline e.g. Embedded Systems Week, New Jersey, October 2005.
- International Collaboration **Publications**.
- **Joint international projects**. Set up joint collaborative projects e.g. Columbus project or extend existing projects, by allotting them an extra budget.

International Collaborations is implemented mainly in collaboration with the USA, building on existing links between IST and the US funding agencies (mainly NSF).

ArtistDesign leverages on and extend the successful International Collaboration activities initiated in the ARTIST2 NoE.

3.3.5 Web Portal

The ArtistDesign Web Portal is a major tool for Spreading Excellence within the Embedded Systems Community. It aims to be the focal point of reference for events and announcements of interest to the embedded systems community.

This will play a key supporting role for collaboration and Integration, such as interaction between clusters, management information, such as scholarships, internal events, and progress of the work. The web portal will also be used to disseminate any relevant information to the community at large. We believe the web portal will be an essential mechanism for achieving integration.

It acts as a repository of knowledge in the area, including courseware, information about standards, methods and tools, research publications and results. This web portal will be made available within the NoE core and affiliated partners, and to other parties.

This repository is to be the reference for the embedded systems design community. It builds on the existing ARTIST2 Portal, which includes several features that help keep it coherent and up to date:

- Authorised users (principally, the ARTIST2 partners) can access the back end of the site to modify and update information directly. The changes are immediately visible on the site, which greatly streamlines the updating process.
- It's possible to track changes and go back to previous versions of individual web pages.
- Events are automatically sorted by date, and transferred to 'Past Events'. When appropriate.
- Structural information (hierarchy of pages) is maintained automatically.
- Ergonomics are set for the entire site. The "look and feel" of the site is always homogeneous throughout the site. It's possible to change these ergonomics, and these changes are applied homogeneously throughout the site, via automated mechanisms.

The ArtistDesign Web Portal offers information about:

- **Workshops, Conferences, Schools and Seminars**
  Provide information about the main scientific events in the area, and in particular those organised by ArtistDesign.
- **International Collaboration**
  Advertise the ArtistDesign International Collaboration events, and provide pointers to the most visible International Projects (either about significant projects outside Europe, or joint International Collaboration projects.
- **Publications**
  Publications from core partners, with emphasis on Position Papers, White Papers, etc. that may have a particularly deep impact.
- **Course Materials Available Online**
  The web portal will centralize course materials from as many sources as possible, to make them available to the general public.

3.4 Managing the Network of Excellence (JPMA)

We believe that the current two-tiered Management structure - dividing the management amongst cluster leaders and the Strategic Management Board composed of both cluster leaders and a limited number of other selected prominent core partners – has been the right one for managing such a large research entity. It has provided the right combination of flexibility and accountability, while leaving room for innovation and evolution.

This management structure is reproduced with adaptations in the ArtistDesign NoE. The adaptations reflect the greater cohesion between partners, and move to capitalize on and strengthen the integration achieved in Artist2.

4. End Results

We are achieving a significantly more integrated scientific community. Initially, there was a strong fragmentation by topics and communities, with little interaction between them. Over the course of the NoE, the clusters have evolved and merged. A gradually cohesion has taken

place, through transversal “NoE Integration” activities, and more importantly through strategic alliances.

We are seeing a convergence of interests, and the gradual emergence of recognized leaders.

214373 ArtistDesign
Network of Excellence
on Embedded Systems Design

Periodic Activity Report for Year 1

Joseph Sifakis – ArtistDesign Scientific Coordinator
Bruno Bouyssounouse – ArtistDesign Technical Coordinator

ArtistDesign Consortium

Table of Contents

1. Overview

1.1 Project Objectives and Major Achievements

A detailed description of objectives, and particularly the main aims for integration, is provided for each cluster in the sections labelled « State of Integration in Europe ».

1.1.1 Historical Perspective: Artist FP5, then Artist2 in FP6

Within IST FP5, a subset of the current consortium implemented an Accompanying Measure, whose objectives were to:

- Coordinate the R&D effort in the area of Advanced Real-time Systems
- Improve awareness of academics and industry in the area
- Define innovative and relevant work directions

This was achieved through work along 3 axes:

- Roadmaps for selected actions: (Hard Real Time, Component-based Design, Adaptive Real Time, Execution Platforms)
- International Collaboration
- Education

Information about these results is publicly available:

http://www.artist-embedded.org/Roadmaps/

Within IST FP6, a consortium very similar to the current one implemented the highly successful ARTIST2 NoE. The main changes between Artist2 and ArtistDesign are :

- An evolution of the clusters to reflect the ongoing integration.
  There are now 4 clusters instead of 6, and they are significantly larger.
- Reinforced role of the Transversal Activities (called NoE Integration activities in Artist2). In ArtistDesign these now have nearly the same role and autonmy as did the clusters in Artist2.
- Tighter consortium. The number of partners in the consortium has been reduced by approximately 25%. The “departing” partners continue interaction with the NoE, as Affiliated Partners. This allows them to participate in the technical meetings and occasionally claim some costs for travel, but none for manpower.
- Tools and procedures continue to evolve. The tools (eg web) and procedures developed within Artist2 contionue to evolve within ArtistDesign.
- Change of Coordinator. The Financial and Legal Issues handled by the CDC in Artist2 are now handled by Floralis in ArtistDesign.

1.2 Workpackage progress of the period

Given the size of this NoE, and the structuring by clusters, this information is provided in detail in separate physical sections of this document (chapters 2-5 of the Project Activity Report).

1.3 Deliverables for the Reporting Period

WP0: Joint Programme of Management Activities (JPMA)

Floralis	D1-(0.1)-Y1	**Project Management Report**
	D2-(0.2)-Y1	Project Activity Report
UJF/Verimag	D2-(0.2a)-Y1	*ch. 1* - **Executive Summary and Overview**
Aalborg	D2-(0.2b)-Y1	*ch. 2* - **Modelling and Validation**
Dortmund	D2-(0.2c)-Y1	*ch. 3* - **SW Synthesis, Code Generation and Timing Analysis**
Pisa	D2-(0.2d)-Y1	*ch. 4* - **Operating Systems and Networks**
DTU	D2-(0.2e)-Y1	*ch. 5* - **Hardware Platforms and MPSoC Design**

WP1: Joint Programme of Integration Activities (JPIA)

UJF/Verimag	D3-(1.0)-Y1	**Integration Activities Report**

WP2: Joint Programme of Activities for Spreading Excellence (JPASE)

UJF/Verimag	D4-(2.0)-Y1	**Spreading Excellence Report**

WP3: Modeling and Validation (JPRA)

EPFL	D5-(3.1)-Y1	**Modelling**
Aalborg	D6-(3.2)-Y1	**Validation**

WP4: Software Synthesis, Code Generation and Timing Analysis (JPRA)

Dortmund	D7-(4.1)-Y1	**Software Synthesis, Code Generation**
Saarland	D8-(4.2)-Y1	**Timing Analysis**

WP5: Operating Systems and Networks (JPRA)

Pisa	D9-(5.1)-Y1	**Resource-aware Operating Systems**
York	D10-(5.2)-Y1	**Scheduling and Resource Management**
Aveiro	D11-(5.3)-Y1	**Embedded Real-Time Networking**

WP6: Hardware Platforms and MPSoC (JPRA)

Bologna	D12-(6.1)-Y1	**Platform and MPSoC Design**
DTU	D13-(6.2)-Y1	**Platform and MPSoC Analysis**

WP7: Transversal Integration (JPRA)

Lund	D14-(7.1)-Y1	**Design for Adaptivity**
Uppsala	D15-(7.2)-Y1	**Design for Predictability**
PARADES	D16-(7.3)-Y1	**Integration Driven by Industrial Applications**

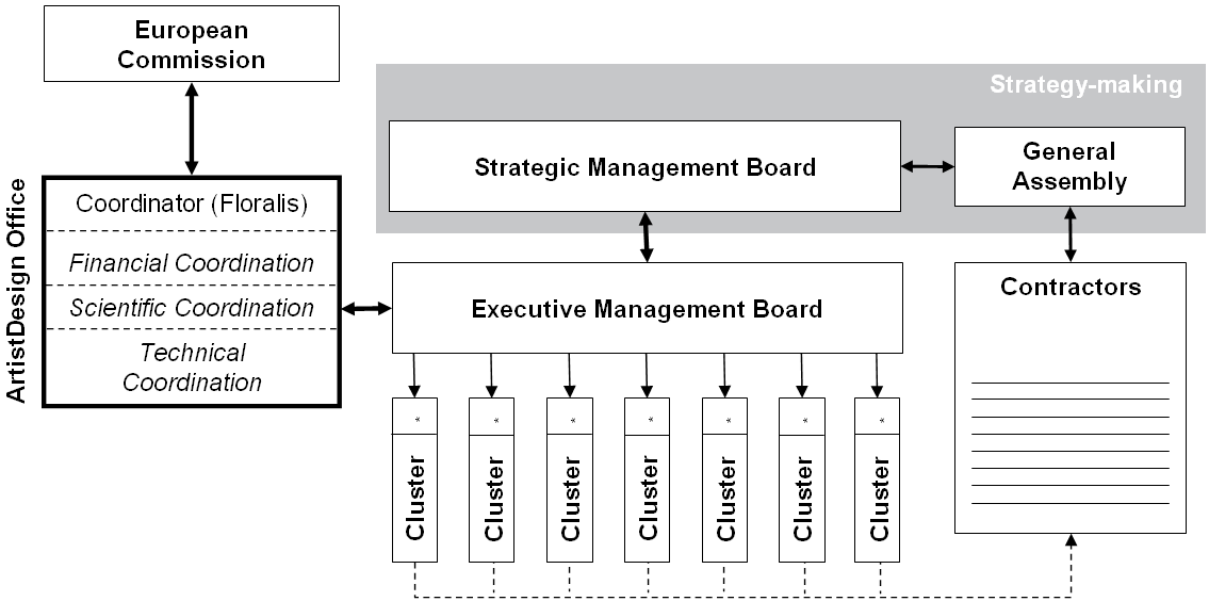
1.4 Consortium Management

This is unchanged from Artist2.

1.4.1 Governance Structure

Scientific Coordinator: Joseph Sifakis Tel: +33 4 56 52 03 51 Joseph.Sifakis@imag.fr	Technical Coordinator: Bruno Bouyssounouse Tel: +33 4 56 52 03 68 Bruno.Bouyssounouse@imag.fr
Mailing address: Verimag Laboratory - Centre Equation - 2, ave de Vignate - 38610 Gières - France	

The methodology adopted for achieving the JPA objectives follows the same lines as for managing a laboratory. The activities, their objectives, their technical description, the partners involved, their roles, and the resources available have been clearly defined in the initial Description of Work, and updated in the deliverables. This will be monitored and guided by a tight and rigorous management, as defined in the diagram below:



The main governance bodies are:

The **General Assembly** is composed of one representative per core partner. It is convened at the beginning of the project and meets once per year. It is chaired by the Scientific Manager.

The **Strategic Management Board** is initially composed of the NoE cluster leaders, and a representative of the Coordinator – who attends, with no voting rights. It is chaired by the Scientific Manager, assisted by the Technical Manager. It meets at least once per year – close to the General Assembly meeting. Its members are elected by the General Assembly every two years, according to modalities to be determined in the Consortium Agreement.

The **Cluster Leaders** (who compose the Executive Management Board) are responsible for the overall coordination of the activities led by their cluster. A cluster functions as a virtual team – with a degree of autonomy for defining its internal meetings and day to day management.

1.4.2 Partners Involved

This is provided in the publishable Executive Summary, in the first part of this document.

1.4.3 Contractors

There are no changes to the consortium at the end of Year 1.

1.4.4 Project Timetable

The JPA is organized into activities. The activities should not be considered as tasks of a workprogramme, with begin/end and synchronisation dependencies. Of course, the detailed description of an activity could be decomposed into sub-tasks and intermediate milestones, but this would imply a granularity that is too fine for research activities.

1.4.5 Other Issues

None

1.4.6 Plan for using and disseminating the knowledge

The main instruments for using and disseminating knowledge are:

- Workshops and Schools organised.
  The list is quite impressive, and is provided in the deliverable on “Spreading Excellence”.
- ArtistDesign Web Portal.
  Here also, the quantity of information made available to the greater embedded systems community is quite impressive, and continuously growing. This is possible through the efforts of the entire consortium, who now have direct access for updating the contents.
- Course Materials.
  There is a growing body of course materials made available via the Artist2 web portal.
- Publications.
  The ArtistDesign consortium is very prolific in publishing research articles, surveys, textbooks, roadmaps, and position papers.

1.5 Metrics

It should be noted that these metrics are imperfectly measured, relying on voluntary feedback from partners.

1.5.1 Excellence Indicators

Indicator	number	*Method used*
Number of publications (journals, proceedings, etc) by ARTIST Partners in Embedded System Design over Year 1	668	*from partners, (web form)*
Number of course books published by ArtistDesign Partners in the area in Year 1.	20	*from partners, (web form)*
Number of public keynotes, conferences, seminars and workshop in the area by ArtistDesign partners in Year 1. *NB: Due to differing definitions and data collection methods from one partner to the next, it should be noted that this figure is probably not very reliable.*	178	*From JPASE deliverable, section 5*
Number of white papers published in the area by ArtistDesign Partners in Year 1.	31	*from partners, (web form)*

1.5.2 Integration indicators

Indicator	number	*Method used*
Number of EC-funded projects in embedded systems, involving two or more ArtistDesign partners over Year 1 *NB: Due to differing definitions and data collection methods from one partner to the next, it should be noted that this figure is probably not very reliable.*	32	*from partners, (web form)*
[ICT-2007.1.2] IRMOS; [IST FP6] ACTORS (2008-2011), [ST] WASP (2008-2011), [FP6] HYCON NoE, [FP6] PREDATOR, [FP6] RIMACS, [FP7] COMBEST (2007-2010), [FP7] Speeds (2006/2009), [FP6] WASP (2006-2010), [FP6]FRESCOR (May 2006 May 2009), [FP7] MNENEE (2007-2010), [IST] ASSERT (2004-2007), [IST] MORE (2006-2009), [ITEA]ES_PASS (2007-2009), [ITEA2] TECOM (2007/2010), [NABIIT] MoDES (2006-2009), [VTU] D-ARTEMIS (2007-2009), ALL-TIMES 2008-2009, EU FP7 CONET (2008/2011), EU MORE 6/2006-5/2009, FP6 HiPEAC (2004-2008), FP7 HiPEAC (2008 – 2011), FP6 SHAPES (2006-2009), FRESCOR (2007-2010), [IST-FP7] Genesys FP7 18 months, [IST] ATESST, 04/01/2006 => 03/31/2008, KKS WCET 2006-2008, Quasimodo (Jan 2008-Dec2010), SPEEDS, Verisoft (03-10), VINNOVA FISS2 May 2007 - Dec 2009;; [FP7] FEEEDNETBACK; FP7 INTERESTED		

Number of other source funded projects in embedded system design, implying two or more ArtistDesign partners in year 1. *NB: Due to differing definitions and data collection methods from one partner to the next, it should be noted that this figure is probably not very reliable.*	18	*from partners, (web form)*
[CH] FIRE, [CH] MICS, [CH] PerformanceEvaluation, [ESA] Prototype Execution Time Analyzer for SPARC (Sept 2006/Feb 2007), [HTF] DaNES (2007-2010), [NABIIT] MoDES (2006-2009), [Spain PN] THREAD (2005-2008), [Spanish Government]THREAD (05/08), [Spanish project]THREAD (Jan 2005, Dec 2008) [Swedish Foundation for Strategic Research] SAVE(2003-2008), [US DARPA and Industry]: GSRC, [US NSF] CHESS, [VTU] D-ARTEMIS (2007-2009), ALL-TIMES 2008-2009, KKS WCET 2006-2008, SuReal (German BMBF, 2006-2008), Verisoft (03-10), VINNOVA FISS2 May 2007 - Dec 2009; EUROSYSLIB (Summer2007 - Dec2009)		
Number of PhD visiting other partners in the network in year 1	68	*from partners, (web form)*
Number of joint PhDs over year 1	34	*from partners, (web form)*
Number of visits between teams over year 1	48	*from partners, (web form)*
Number of public conferences, special sessions and workshop organised by ARTIST in year 1.	26	*from website*
Number of jointly published papers from two or more partners from ArtistDesign in year 1. *NB: Due to differing definitions and data collection methods from one partner to the next, it should be noted that this figure is probably not very reliable.*	156	*From JPASE deliverable section 9*
Number of research platforms or facilities shared for research	27	*JPIA*

1.5.3 Indicators about Spreading Excellence

Indicator	**number**	***Method used***
Large Summer Schools organised and funded by ARTIST in year 1.	3	*from website,*
Smaller Summer Schools organised and funded by ARTIST in year 1.	3	*from website,*

Other Summer Schools with ArtistDesign funding or participation in Year 1.	1	*from website*
Education: International seminars / training sessions organised specifically on Education WESE'08: WS on Embedded Systems Education *October 23rd, 2008 Atlanta, Georgia - USA (within ESWEEK)*	1	
Other international seminars / training sessions organised:	180	*from JPASE deliverable, section 5*
Number of papers published in top international journals and conferences	*Very large. This is very difficult to measure with any meaningful degree of accuracy.*	
Number of hits on the ARTIST2 web portal	2759886	*from JPASE deliverable, section 6*
International collaboration : nb of projects defined at the events	*This is impossible to measure.*	
Number of external links referring to ARTIST2 web portal	161	
Obtained from google, by searching for: `link:www.artist-embedded.org`		

1.5.4 Indicators on the financial independence from EC funding and from other sources

Indicator	**number**	***Method used***
Number of affiliated industrial partners	22	*from website*
Number of spinoff companies created	12	*from partners, (web form)*
Percentage of the ARTIST2 funding, respective to the partners' overall operating budget	*This is absolutely impossible to measure any meaningful way.*	
Number of affiliated partners willing to pay for membership in ARTIST2 *This would depend on the cost of membership, and the benefits they would get. Part of the benefits is the "seal of approval" involved in obtaining EC funding.*		
Overall revenue from membership dues from affiliated partners. *See previous question.*		

1.5.5 Indicators for Integrating the Gender Dimension

Indicator	**number**
Number of women currently active in the NoE	4
Number of women initially active in the NoE	1
Promotion of women in the area	No statistics