IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Cluster - Progress Report for Year 1

Cluster:

Software Synthesis, Code Generation and Timing Analysis

Cluster Leader:

Prof. Dr. Peter Marwedel (TU Dortmund)
http://ls12-www.cs.tu-dortmund.de/~marwedel

Policy Objective (abstract)

The objective of this activity is to provide software synthesis, code generation and timing analysis tools which are required for modern embedded architectures. A particular focus is on multi-processor systems. The parallelism and communication structures found in such architectures pose a particular challenge.

Versions

number	comment	date
1.0	First version delivered to the reviewers	December 19th 2008

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1. Overview

1.1 High-Level Objectives

There is a continuing demand for higher performance of information processing. This growing demand stimulates using a growing amount of parallelism (including using multiple processors), due to limitations of increasing clock speeds any further. This trend also affects the design of embedded systems. Hardware platforms, containing connected processors, are becoming increasingly parallel. Actually, there are various kinds of connectivity. In multi-processors in a system on a chip (MPSoC), processors are tightly connected and communication is fast. In other cases, networked processors may be less tightly connected and communication may be slower. In this project, we would like to address the issues resulting from the use of multiple processors, in particular in the form of multiple heterogeneous processors on a chip, also containing memory hierarchies and communication interfaces.

These processors can only be exploited if (sets of) applications can be efficiently mapped to heterogeneous processors. Mapping techniques can be either based on task graphs or on sequential applications. The latter require the use of automatic parallelization techniques. In this cluster, we want to provide at least partial solutions to the problem of mapping specifications of embedded systems to networks of embedded processors. These networks will be characterized by different speed parameters reflecting the communication and memory architectures. These parameters will be considered during the mapping. We will focus on mappings from simple sequential code from C or C-like languages. However, we will also look at the generation of code from other specifications, being based, for example, on MATLAB or UML. Such languages could simplify the mapping since such specifications might be inherently parallel (and also more appropriate for embedded systems). In general, mapping techniques will be indispensable for using future architectures.

Timing analysis is also affected by the trend toward the new platforms. Also, timing analysis beyond single processors is required. Timing analysis has to cope with the kind of memory hierarchies found in MPSoCs. Hence, timing analysis will also consider the timing of communication. The overall objective is to provide safe timing guarantees for systems consisting of local memories hierarchies and multiple processors. In addition, overcoming the traditional separation between compilers and timing analysis continues being on the agenda.

The design of efficient embedded systems also requires additional work. In particular, minimizing the energy consumption, addressing the memory wall problem and customizing instruction sets are hot topics, for which integrated approaches from various partners are being extended and exploited.

Partners in this cluster also participate in the activities of the thematic activities of the Transversal Integration workpackage, where they address adaptivity and predictability of complex systems comprising MPSoCs. Predictability is also to be addressed in the cooperation between partners of the two activities of this cluster.

It is understood that the current project can only help integrating work that provides potential solutions. The actual work on those solutions is mostly paid through other projects.

1.2 Industrial Sectors

Software Synthesis and Code Generation: The work performed in the cluster is relevant for all industrial sectors using embedded software. This includes semiconductor houses, system houses, companies working on audio processing, video processing, data streaming

applications in the TV, Set Top boxes, DVD players and recorders, mobile phones, base stations, printers and disk drives. Efficiency of embedded software, in particular the efficiency of memories, is relevant for high-speed embedded systems. It is expected that most mobile devices will provide some kind of multimedia processing.

Timing Analysis: WCET estimations are relevant for all industrial sectors using hard real-time systems. Therefore, industrial sectors in this case include avionics, automotive, defence and some areas where control systems are applied. Especially in the automotive and the aeronautical domains, there is a need to have precise knowledge on the worst-case timing behaviour of safety critical software. Therefore, timing-analysis tools entered industrial practice and are in routine use in the aeronautics and automotive industry. This need is underlined by the fact that the worst-case timing of large parts of the software used within the new Airbus A380 has been analyzed using AbsInt's aiT. AbsInt's timing analysis tool, aiT, has been used in the certification of time-critical subsystems of the Airbus A380 and has thus acquired the status of a *validated* tool.

Link between timing analysis and compilers: The availability of precise timing analyses does not fulfil all industrial needs. Since the code of safety critical applications is typically generated by a compiler, the compiler should also be aware of worst-case timings. This work is relevant in all areas for which a physical environment is integrated with software. The focus is on sectors having safety critical applications.

1.3 Main Research Trends

Mapping of applications to MPSoCs can be considered as an extension of scheduling. Traditionally, scheduling mostly focused on independent tasks. This assumption is not valid for most applications of embedded systems. Additional research is performed in the multi-core context. Multi-core processors are usually considered to be homogeneous. For embedded systems, this assumption is also not valid. Therefore, new mapping techniques are required. Some papers have been published in this area (for example, there will be a session on this topic at the forthcoming DATE 2009 conference). It is a trend to combine the mapping problem with non-traditional objectives. For example, minimization of the operating temperatures, maximization of the life-time of processors, and dependability in the presence of failing processors etc are considered. However, these approaches mostly consider tasks as black boxes with little information, for example, on the memory access characteristics. This can lead to sub-optimum mappings. This trend is important in all industrial areas in which high performance embedded computing is required.

Taking the well-known (frequently negative) results on automatic parallelization in high-performance computing into account, automatic parallelization is being experimented with in a way which is appropriate for embedded systems. Results obtained (for example at the University of Edinburgh and the University of Passau) indicate that this parallelization is feasible within a restricted scope of applications and architectures. This trend is also important in all industrial areas in which high performance embedded computing is required.

Energy efficiency, initially mostly a topic considered for embedded systems, is now becoming mainstream. Energy availability is continuing to be the most challenging constraint for embedded system design, but performance constraints also exist. Therefore, the design of efficient embedded systems continues being important. Constraints are most dominating for small, mobile products.

The importance of timing is slowly being recognized by larger groups of people. For example, there is increasing interest in the automotive domain. At the same time, researchers are also giving timing issues more attention. In-line with this, the first compiler including a fully

integrated WCET estimator was designed in the Artist2 project. This research direction is finding more attention recently.

WCET analysis has so far almost exclusively dealt with sequential code running on uni-processors. The main trend has been towards managing more complex sequential hardware architectures. Increasing the level of automation, e.g., by more advanced analyses constraining the possible program flows, is also a topic of active research. As multi-core and MPSoC architectures arise, the research focus will have to shift towards analysis of parallel systems.

2. State of the Integration in Europe

2.1 Brief State of the Art

Software Synthesis and Code Generation: Mapping applications to MPSoCs is an important topic in various places in the world, due to its extreme relevance for industry. In Europe, Ed Deprettere (U. Leiden) performed significant work, working together with adjacent universities on the DEADALUS tool. Also, the group of Jürgen Teich from the University of Erlangen Nürnberg is proposing the SystemCoDesigner tool. In the automotive context, additional work has been performed at TU Braunschweig. METROPOLIS by Sangiovanni-Vincentelli et al. is a tool working on a global level. CHARMED by Bhattacharyya places an emphasis on signal processing applications. Recent tools try to combine task allocation with non-standard cost functions such as energy (e.g. Chang at DAC 2008), temperature (e.g. Ciskun at DATE 2007), lifetime or dependability.

The design of efficient embedded systems is the target of numerous optimization tools. There are clearly too many tools to make any attempt to present a survey in limited space useful. Even within the more restricted area of optimization the memory structure, many approaches have been proposed by computer architects. Due to the increasing speed gap between processors and memories, efforts for improving the performance of systems have been predicted to hit the "memory wall". Work was done in the context of caches (loop caches, filter caches etc.). However, these approaches have mostly focussed on hardware approaches for reaching the goals. For these approaches, compilers were considered to be black boxes and untouchable. Only few authors (e.g. Barua, Catthoor, Dutt, Kandemir, Egger) have taken a holistic approach, looking at hardware and software issues.

Timing Analysis: Several commercial WCET tools are available. They have experienced positive feedback from extensive industrial use in the automotive and aeronautics industry. The existing tools serve some particular and highly relevant points in this space. AbsInt's tool for example has been used in the development and the certification of safety-critical systems in the Airbus A380. However, they currently do not serve distributed architectures well.

2.2 Main Aims for Integration and Building Excellence through ArtistDesign

The Compiler and Timing Analysis Cluster and the Execution Platforms Cluster aim at developing a common methodology to enable resource aware design and compilation and to increase predictability while retaining a performant system. The main aim of using the ArtistDesign network is to get access to competences, knowledge and tools which are not available locally at each of the institutions. The cooperation provides the required size of research teams, necessary to handle the complexity of today's technology. Furthermore, a major goal is the combination of areas of excellence of the different partners by defining and implementing interfaces between their design flows and tools in order to achieve compilation platforms applicable to a wider problem scope.

WCET analysis of parallel systems, including MPSoC, is a more or less novel research area. However, it is becoming rapidly important as MPSoC's become increasingly used. Therefore, it is urgently needed to initiate more research in this area, and the ArtistDesign network will be used for this. The network will also be used for research initiation activities within the WCET analysis area. Contacts with other clusters, such as the HW Platform and MPSoC design cluster, will also be of importance since the success of the cluster's activities depends critically on the properties of the underlying hardware design.

2.3 Other Research Teams

For mapping applications to MPSoCs, section 2.1 contains a brief description of the work of other research teams in this area. Ed Deprettere (U. Leiden), Jürgen Teich and two of their students participated in the working meeting at Düsseldorf in November 2008. They are clearly candidates for being added as affiliates.

Essentially three more research teams have competed with Europe in the area of Timing Analysis, one at Seoul National University (SNU), one at Florida State University, now with some branches in North Carolina etc., and Singapore National University. Seoul has turned to power-aware computing, and flash memory based components research. Singapore and Florida have cooperated with the ArtistDesign partners in writing a survey paper. Singapore has participated in the WCET Tool Challenge, arranged within ArtistDesign, with their academic prototype. There is a continuous exchange of PhD students and PostDocs with the team of Prof. Sang Lyul Min at SNU.

Only few groups have been working on the integration of worst-case execution times and compilers. Smaller, apparently volatile efforts have been reported from Sweden and South Korea. Some work was performed in the group of David Whalley at the Computer Science Department of the Florida State University. However, only very simplified timing models and highly predictable processor architectures are considered at Florida.

Additional work has been performed at INRIA by Isabelle Puaut et al. More information about the work of other teams is available in section 1.5 of the two related activity reports.

2.4 Interaction of the Cluster with Other Communities

For mapping application to MPSoCs, links have been established with the execution platform cluster of ArtistDesign, where some related work is being performed, for example, at Zürich, Bologna and TU Denmark. For timing analysis, the same applies for the modelling and validation cluster. The three clusters were represented by Lothar Thiele, Nicolas Halbwachs and Peter Marwedel at the South American Summer School on Embedded System Design at Florianopolis in 2008. Cluster members Peter Marwedel and Rainer Leupers performed further teaching activities at ALARI, Lugano, together with ArtistDesign members like Luca Benini (Bologna), Rudy Lauwereins (IMEC) and Lothar Thiele (Zürich). Further links of ArtistDesign members existed to the SHAPES project and to the HiPEAC Network of Excellence.

TU Dortmund:

The interaction with the local technology transfer centre ICD (see http://www.icd.de/index_eng.html) is key for interacting with industry. ICD is headed by Peter Marwedel. ICD is used for transferring research results to industry. The group promoted education in embedded systems through a published text book and through courses at ALARI (Lugano) and at spring or summer schools in Brazil, Portugal, Korea, and France. TU Dortmund organizes the SCOPES series of workshops on compilation for embedded systems.

IMEC:

IMEC is integrated in European research networks, including HiPEAC. Moreover, IMEC is the central partner of a Marie Curie Host Fellowship project that involves more than 10 universities across Europe. IMEC also has many industry co-operations including most large European multi-media and communication systems oriented companies. Additionally, several news sites featured the launch of the CleanC tools for source code parallelization assistance. Articles talking about the launch of the tools could be found on sites like EETimes, EDN, Electronics Weekly, Azonano, EDACafé.com, EDA_DesignLine, Electronic Design, Topix, SOCCentral, Ugens Erhverv, or Global-Electronics.net.

U. Passau:

The group at the University of Passau is internationally well connected in parallelism and programming methodology. This is most visibly documented by Christian Lengauer's chairmanship of the steering committee of the yearly international conference series Euro-Par (Parallel Computing in Europe) and the IFIP Working Group 2.11 on Program Generation. Here, the paradigm of feature orientation is receiving special interest.

Passau is also a member of the CoreGRID network of excellence which terminated in August 2008 bur will continue as an informal interest group. Some of the software engineering and parallelization issue of CoreGRID are also relevant to ArtistDesign.

In the past year, Lengauer has spear-headed the submission of a proposal for a national research activity ("*Schwerpunktprogramm*") to the German Research Foundation ("*Deutsche Forschungsgemeinschaft*") with the title "Manycore: Parallelism for everybody. One of several application areas is the use of multi-cores and many-cores in embedded systems. The national research activity programme is highly competitive, and an acceptance of the proposal is not certain. If granted, funding of €10+ million can be expected for a period of 6 years, funding up to 25 research projects. A decision will have been made by May 2009.

RWTH Aachen:

A close cooperation existed with the ArtistDesign Execution Platforms cluster, in particular between Dortmund, Aachen, and Bologna University. RWTH Aachen participated in the HiPEAC network of excellence and worked on cooperations related to code optimization, e.g. with Edinburgh University. Furthermore, Aachen maintained tight industry cooperations, e.g. with CoWare, ACE, and Infineon. Since Oct 2006, RWTH Aachen is running the UMIC research cluster (http://www.umic.rwth-aachen.de) of the German excellence initiative.

Mälardalen:

The WCET analysis group maintains close contacts with several industrial partners, and has conducted a number of case studies using their production codes. The group also interacts heavily with the Component-based Software Engineering community through the national centre PROGRESS for research on component-based software design for embedded systems.

Saarland University:

Timing-Analysis activities in the cluster interacted closely with the Execution-Platform cluster in the area of increasing the timing-predictability of real-time systems. Airbus and Bosch participated in the Predator FP7 proposal aimed at reconciling performance with predictability. The PREDATOR project started in 2008. Saarland University worked on modularizations of the Sagiv/Reps/Wilhelm shape analysis together with Mooly Sagiv, Tel Aviv University, and Arnd Poetzsch-Heffter, University of Kaiserslautern.

ACE:

ACE worked closely with ST and with Philips having both a commercial relationship with them as well as being co-members of EU project consortia – in one case along with Verimag. ACE has been working closely with Aachen in this domain for some time. One of the results of this cooperation has been the integration of compiler technology in a start-up company that span out of the university. Cooperation with Imperial College and Edinburgh has also started.

AbsInt:

Within the EmBounded Project (IST-510255), AbsInt was also involved in the development of the Hume compiler. Hume is a domain-specific high-level programming language for real-time embedded systems.

TU Berlin:

TU Berlin is generally involved in methods and tools for software engineering for embedded systems. TU Berlin has cooperated with Edinburgh University (Björn Franke) concerning the optimization of compilers based on machine learning techniques. Furthermore, TU Berlin has done research on the verification of embedded operating systems, also by cooperating with the Fraunhofer institute FIRST. Finally, TU Berlin visited and was visited by other cluster members, e.g. ACE, RWTH Aachen and TU Vienna.

Tidorum, York:

Tidorum (and partially York through Rapita Systems) were engaged in a project for the European Space Agency to study the timing and verification aspects of cache memories in space systems. The PEAL project ended in February 2007. An extension was started in late 2007. The main partner from the aerospace domain was Thales Alenia Space, France.

TU Vienna:

TU Vienna worked on measurement-based timing analysis together with TU Munich. It also maintained a close interaction with the Lawrence Livermore National Laboratory, CA, USA, in optimizing high-level abstractions.

3. Overall Assessment and Vision for the Cluster

3.1 Assessment for Year 1

The partners promised starting with a joint workshop, at which the directions of the work on the mapping of applications should be set. This workshop (held at Rheinfels castle) found a wider interest than initially conceived: both activities decided to be present at the workshop. The announcement of the workshop also found the interest of people outside ArtistDesign. At the workshop, attendees agreed to cooperate. Slides from the workshop are available at the ArtistDesign website (http://www.artist-embedded.org/artist/Mapping-of-Applications-to-MPSoCs.html). A summary of the workshop was presented at the CASA workshop (see http://www.esweek.org). An invitation to turn this summary into a survey in some journal was received. A follow-up meeting, more details about the cooperation were fixed. In this sense, the partners are working on the problems, but no tool integration could be expected in this new area in the very first year.

The integration of timing analysis and compilers is building on top of worked performed during the lifetime of the Artist2 network. Hence, tool integration is essentially complete and can now be exploited. A major number of papers reflect the fact that the current work was built on top of earlier work. Also, separate funding through the PREDATOR project allowed increasing the man power in this area.

Within Timing Analysis, work has been initiated in the area of timing predictability. Results for cache replacement policies have been obtained for individual cores: the plan is to extend these to multiple core systems. The influence of scheduling on cache contents has also been studied. For measurement-based timing analysis methods, joint work is carried out regarding test-case generation and learning techniques to identify timing model features.

An important part of the timing analysis work will be the formulation of design principles for architectures with predicable behaviour. This work is now being initiated. The immediate plan is to have a joint workshop with the HW Platforms and MPSoC Design cluster, and to write a white paper explaining the timing predictability problem for MPSoC from a timing analysis perspective.

The generation of efficient embedded systems is a second area where we could build on top of tools integrated during the lifetime of Artist2. Work in this area continues. Additional funding is available, for example through the MNEMEE project, in which IMEC and TU Dortmund's spin-off ICD are involved. The work on scratchpads is now widely recognized. For example, a previously published paper of TU Dortmund has been found to be the second most frequently cited paper at the CODES and ISSS symposia between 1996 and 2006 [F. Vahid, T. Givargis: Highly-cited ideas in system codesign and synthesis, *Proceedings of the 6th IEEE/ACM/IFIP international Conference on Hardware/Software Codesign and System Synthesis, p.* 191-196].

Software synthesis was represented at the Rheinfels workshop. It will be included in our considerations in the future. However, software synthesis is a wide area and the cluster has only few members. Therefore, the full breadth of this area could not and will not be covered.

3.2 Overall Assessment since the start of the ArtistDesign NoE

Support for various multi-processor systems has been selected as the key new topic for ArtistDesign. The importance of this topic has increased since the description of the work was written. It is now even more clear that clock speeds can hardly be increased and that performance increases have to rely on using parallel processors. There is still the **risk that missing tools will stop further increases of the performance of embedded systems** and

that huge investments into parallel architectures will be partially lost. Hence, **this topic is of outmost importance**. It turns out that the two activities of this cluster have joint interests in this area. Code generation tools are clearly needed and timing analysis is also mandatory. An early warning by timing analysis specialists is needed. Otherwise, architects might select architectures having absolutely non-acceptable WCET bounds. Therefore, code generation and timing analysis specialists decided to have a joint workshop.

The importance of timing for embedded system design is being recognized more widely. Ed Lee formulated this importance in a very well memorizable way. He wrote "The lack of timing in the core abstraction (of computer science) is a flaw" [Edward A. Lee: *Building Unreliable Systems out of Reliable Components: The Real Time Story*, University of California at Berkeley, Technical Report No. UCB/EECS-2005-5, 2005]. In the US, the term "cyber-physical systems" has been introduced. This term is intended to denote embedded systems and the introduction was mainly a marketing issue. Nevertheless, the explicit link to physics demonstrates the importance of timing. Accordingly, the keynote by F. Vahid and T. Givargis at the Workshop on Embedded system Education (WESE), supported by ArtistDesign, was called "Timing Is Everything – Embedded Systems Demand Early Teaching of Structured Time-Oriented Programming". It is now more widely recognized that the inclusion of timing is the key differentiator between embedded and non-embedded software. This insight demonstrates the importance of the work on timing analysis and WCET-aware compilation.

Efficiency of embedded systems continues being a key concern. The trend for higher resolution images in many industrial sectors continues. As a result, tight performance constraints exist for many advanced applications. The importance of energy efficient computing (initially just considered for embedded computing) has reached the attention of the general public. The carbon (-dioxide) footprint left by various technologies, including embedded systems, is now considered in most countries. Research on energy-efficient computing is counter-acting against increasing footprints.

3.3   Indicators for Integration

Partners promised the following Interactions:

- Partners announced an integration of techniques developed by the high-performance computing community and the compiler for embedded systems community. They predicted having at least one tool flow demonstrating the advantages of combining these approaches and having examples demonstrating the power of the integrated techniques for MPSoCs. According to the "description of the work", compilation techniques will be made available to the MPSoCs community. Along these lines, a common workshop and a meeting were held and plans for a cooperation conceived. The actual integration will require more time.

- The partners promised integrating at least one timing analysis tool with an experimental compiler, to design optimizations within this compiler considering multiple objectives (including worst-case execution times) and to generate a detailed set of results demonstrating the advantages and limitations of such an integration. This promise was kept: the integration of aiT and WCC has been completed. The results are being demonstrated in an increasing list of papers (see references). Tradeoffs between multiple objectives have not yet been studied.

  http://ls12-www.cs.tu-dortmund.de/research/activities/wcc/

- The partners promised organizing at least one open, internationally visible workshop on software generation, compilers and timing analysis per year. This promise was kept: the SCOPES workshop was held in March 2008. In addition, the WCET Workshop was held in July 2008.

- ▪ The partners promised publishing at least four joint papers per year. This promise was kept even in the very first year, despite the latency of the whole process from research to publications. There are six joint papers for the software synthesis and code generation activity (including submitted papers) and four joint papers for the timing analysis activity

- ▪ The Timing Analysis partners conducted the second WCET Challenge, WCET 2008. This is an effort in tool evaluation, where WCET anaysis tools are evaluated with respect to a number of criteria on a common set of benchmarks. The WCET Challenge has now been established as an ongoing activity.

3.4 Long-Term Vision

The long term vision of the project is to have an impact on the tool landscape supporting embedded computing. We intend to contribute to programming tools for MPSoCs, to timing predictability for all kinds of platforms (including MPSoCs) and to resource-aware platform mapping techniques. We predict that an increasing amount of industrial areas will require a guaranteed timing. However, the trend toward higher performances and the use of multi-processor systems with shared resources is working in the opposite direction. It will be required to raise the awareness of timing issues.

4. Cluster Participants

4.1 Core Partners

<table>
<tr><td colspan="2" align="center">Cluster Leader
Activity Leader for "Software Synthesis and Code Generation"</td></tr>
<tr><td></td><td>Prof. Dr. Peter Marwedel (TU Dortmund)
http://ls12-www.cs.tu-dortmund.de/~marwedel/</td></tr>
<tr><td>Technical role(s) within ArtistDesign</td><td>Cluster leader, activity leader SW Synthesis and Code Generation

Improved code quality for embedded applications is the main goal of the work at Dortmund University. Due to the widening gap between processor and memory speeds, emphasis has been on improving the efficiency of memory accesses, in terms of average and worst case execution time and in terms of the energy consumption.</td></tr>
<tr><td>Research interests</td><td>Peter Marwedel's Embedded Systems Group focuses on embedded software. Particular emphasis is on compilers for embedded processors. One of the very first publications in this area, the book "Compilers for Embedded Processors", edited by Peter Marwedel and Gert Goossens, was the result of the CHIPS project, funded by the European Commission. The group's current focus is on advanced optimizations for embedded processors (e.g. by using bit-level data flow analysis) and energy-aware compilation techniques. Current research also includes high-level transformations of algorithms as well as WCET-aware code generation.</td></tr>
<tr><td>Role in leading conferences/journals/etc in the area</td><td>Member of the EDAA (European Design and Automation Association) Main Board.

Editorial Board Member of the Journal of Embedded Computing.

Editorial Board Member of the Microelectronics Journal.

Co-Founder and Steering Board Chair of the SCOPES Workshop (Software and Compilers for Embedded Systems) Series.

>14 years of service for the DATE conference and its predecessors (program chair: 3 times, chairman of the steering committee, European representative to ASPDAC)

DAC: Topic chair and reviewer

Various other conferences</td></tr>
<tr><td>Notable past projects</td><td>MAMS:
Multi-Access modular-services framework, national project</td></tr>
</table>

	funded by the German Federal Ministry of Education and Research (BMBF)
	MORE: Network-centric Middleware for group communications and resource sharing across heterogeneous embedded systems, supported by the European Commission http://www.ist-more.org
	HiPEAC: European NoE on High-Performance Embedded Architecture and Compilation; http://www.hipeac.net
	Others: Various earlier projects supported by the EC, DFG etc.
Awards / Decorations	Teaching award, TU Dortmund, 2003 DATE fellow, 2008
Further Information	CEO of the Informatik Centrum Dortmund (ICD), a technology transfer centre founded in 1989.

Activity Leader for "Timing Analysis"	
	Prof. Björn Lisper (Mälardalen University) http://www.idt.mdh.se/personal/blr/
Technical role(s) within ArtistDesign	Activity for "Timing Analysis" Timing analysis, program analysis.
Research interests	Timing analysis, static program analysis, language design for embedded and real-time systems, program transformations, parallelism
Notable past projects	FP7 STREP ALL-TIMES, Integrating European Timing Analysis Technology (coordinator). http://www.all-times.org Several national projects, funded by Swedish Research Council, VINNOVA, KKS, SSF, Ericsson

	Dr. Stylianos Mamagkakis IMEC vzw. http://www.imec.be

Technical role(s) within ArtistDesign	Representing IMEC Nomadic Embedded Systems (NES) division in: -Cluster: SW Synthesis, Code Generation and Timing Analysis -Cluster: Operating Systems and Networks -Cluster: Hardware Platforms and MPSoC Design -Intercluster activity: Design for Adaptivity -Intercluster activity: Design for Predictability and Performance -Intercluster activity: Integration Driven by Industrial Applications
Research interests	Stylianos Mamagkakis received his Master and Ph.D. degree in Electrical and Computer Engineering from the Democritus Uni. Thrace (Greece) in 2004 and 2007, respectively. Since 2006, he coordinates a team of PhD students within the NES division at IMEC, Leuven, Belgium. His research activities mainly belong to the field of system-level exploration, with emphasis on MPSoC run-time resource management and system integration.
Role in leading conferences/journals/etc in the area	Stylianos Mamagkakis has published more than 35 papers in International Journals and Conferences. He was investigator in 9 research projects in the embedded systems domain funded from the EC as well as national governments and industry.
Notable past projects	Project leader of MNEMEE IST project ωωω.μνεμεε.οργ Project leader of OptiMMA IWT project ωωω.ιμεχ.βε/ΟπτιΜΜΑ Participation in: 1 international IMEC project (M4), 3 European IST projects (AMDREL, EASY, ARTIST2), 2 Greek projects (PRENED, DIAS)
Awards	1st prize in 'Technogenesis' Competition for Business Innovation, Greece, June'06 3rd prize in 'Otenet Innovation 2006' Competition for Business Innovation, Greece, November'06
Further Information	http://www2.imec.be/imec_com/nomadic-embedded-systems.php

	Prof. Dr. Christian Lengauer http://www.infosun.fim.uni-passau.de/cl/staff/lengauer
Technical role(s) within ArtistDesign	Strengthen link between high-performance computing and parallel programming and embedded systems
Research interests	Parallel systems, program analysis, programming methods
Role in leading conferences/journals/etc in the area	Journal editor for: *Parallel Processing Letters*, World Scientific Publ. Co. ; *Science of Computer Programming*, Elsevier Science B.V. ; *Scientific Programming*, IOS Press; *Int. J. of Parallel, Emergent and*

	Distributed Systems, Taylor & Francis; Chair of the Euro-Par steering committee, Chair of the IFIP WG 2.11 on Program Generation, programme committee member of various conferences
Notable present and past projects	LooPo: a loop parallelizer based on the polytope model (past and present DFG funding); FeatureFoundation: Feature-Oriented Program Synthesis (DFG: 2008-2010, renewable); Meta-Programming (DAAD: 2004-2005, EC FP6: from 2004) PolyAPM: abstract parallel machines for the polytope model (DFG: 2000-2002); HDC: a language for parallel higher-order divide&conquer (DFG: 1996-2000) ; SAT: performance-directed parallel programming (1994-98) ; PLR: parallel linear recursion (1994-98) ; OSIDRIS: object-oriented specification of distributed systems (DFG: 1993-97)

	Prof. Dr. Rainer Leupers http://www.iss.rwth-aachen.de
Technical role(s) within ArtistDesign	SW Synthesis and Code Generation, code optimization
Research interests	Compilers, ASIP design tools, MPSoC design tools
Role in leading conferences/journals/etc in the area	TPC member of DAC, DATE, ICCAD etc. Co-founder of SCOPES workshop General Co-Chair of MPSoC Forum 2008 (www.mpsoc-forum.org)
Notable past projects	HiPEAC NoE, SHAPES IP, several DFG-funded projects Industry-funded projects with Infineon, Philips, Microsoft, CoWare, ACE, Tokyo Electron etc.
Awards / Decorations	Several IEEE/ACM best paper awards
Further Information	Co-founder of LISATek Inc. (acquired by CoWare Inc.) European Commission expert in FP7 Editor of "Customizable Embedded Processors", Morgan Kaufmann, 2006 Vice Coordinator of UMIC (Ultra High-Speed Mobile Information and Communication) research cluster (www.umic.rwth-aachen.de)

	Prof. Dr. Reinhard Wilhelm (Saarland University) http://rw4.cs.uni-sb.de/users/wilhelm/wilhelm.html
Technical role(s) within ArtistDesign	Timing Analysis
Research interests	Compilers, Static Analysis, Timing Analysis
Role in leading conferences/journals/etc in the area	EMSOFT 2007 program co chair.
Notable past projects	DAEDALUS
Awards / Decorations	Prix Gay-Lussac-Humboldt

	Prof. Dr. Peter Puschner (TU Vienna) Real-Time Systems Group Institute of Computer Engineering Vienna University of Technology http://www.vmars.tuwien.ac.at/people/puschner.html
Technical role(s) within ArtistDesign	Peter Puschner and his group are participating in the Timing-Analysis activities of the Compilation and Timing Analysis cluster. Within ArtistDesign the contributions are in the area of path-description languages for static WCET analysis, compilation support for WCET analysis, methods and problems of measurement-based execution-time analysis, and on software and hardware architectures that support time predictability.
Research interests	Peter Puschner's main research interest is on real-time systems. Within this area he focuses on Worst-Case Execution-Time Analysis and Time-Predictable Architectures.
Role in leading conferences/journals/et	Member of the Euromicro Technical Committee on Real-Time Systems, the steering committee of the Euromicro Conference

c in the area	on Real-Time Systems (ECRTS)
	Member of the advisory board and organizers committee of the IEEE International Symposium on Object- and Component-Oriented Distributed Computing (ISORC) conference series
	Chair of the Steering Committee of the Euromicro Workshop on Worst-Case Execution-Time Analysis (WCET) series
Notable past projects	DECOS - Dependable Embedded Components and Systems Develop the basic enabling technology to move from a federated distributed architecture to an integrated distributed architecture. http://www.decos.at
	MoDECS - Model-Based Development of Distributed Embedded Control Systems Model-based construction of distributed embedded control systems: shift from a platform-oriented towards a domain-oriented, *platform-independent* development of composable, distributed embedded control systems. http://www.modecs.cc
	NEXT TTA Enhance the structure, functionality and dependability of the time-triggered architecture (TTA) to meet the cost structure of the automotive industry, while satisfying the rigorous safety requirements of the aerospace industry. http://www.vmars.tuwien.ac.at/projects/nextta/

	Dr. Iain Bate (University of York) http://www-users.cs.york.ac.uk/~ijb/
Technical role(s) within ArtistDesign	Responsible for the WCET cluster at University of York. Also involved in the Design for Adaptivity cluster.
Research interests	Worst-case execution time analysis. Design and certification of critical real-time systems. Design for flexibility. Search-based systems engineering. Use of novel computation techniques, e.g. Artificial Immune Systems.
Further Information	Also director of Origin Consulting (York) Ltd. a spin-off company providing consultancy on the design and certification of critical systems.

4.2 Affiliated Industrial Partners

	Joseph van Vlijmen (ACE, Netherlands)
Technical role(s) within ArtistDesign	The design and construction of extensions to CoSy required for ArtistDesign projects.
Research interests	The development and exploitation of compilation techniques and development systems in the wider contexts of SoC and EDA supported by descriptions of the system including application and target architectures. Particular interests include MPSoC and highly parallel system.
Role in leading conferences/journals/etc in the area	Programme Committees of SCOPES and DATE.
Notable past projects	COMPARE/PREPARE ESPRIT projects: These projects, particularly COMPARE, were precursors for CoSy. PREPARE focused on retargetable compilation for Fortran 90 and High Performance Fortran using massively parallel MIMD machines. MESA/NEVA (ongoing): Framework IPs addressing the challenges of designing and constructing multi-processor systems.
Further Information	Principal architect of the CoSy. Previously, architect of ACE's shared memory heterogeneous multiprocessor UNIX OS.

	Dr. Marco Bekooj (NXP)
Technical role(s) within ArtistDesign	Strengthen link to work on code synthesis and industry
Research interests	Design of predictable systems

	Dr.ir. Bart Kienhuis (Compaan Design B.V., Leiden) http://www.liacs.nl/~kienhuis/
Technical role(s) within ArtistDesign	Strengthen link to work on code synthesis and industry
Research interests	Design of predictable systems

	Dr. Niklas Holsti (Tidorum Ltd) http://www.tidorum.fi
Technical role(s) within ArtistDesign	Participate in the definition of the common WCET tool-set architecture, the analysis modules and the interchange representations (languages, file formats). Adapt Tidorum's WCET tool, Bound-T, to integrate with the architecture and interchange formats defined in ArtistDesign
Research interests	Static analysis of the worst-case execution time of embedded programs.

	Dr. Christian Ferdinand (AbsInt Angewandte Informatik GmbH) http://www.absint.com/
Technical role(s) within ArtistDesign	Christian Ferdinand coordinates the activities of AbsInt within Artist Design.
Research interests	Timing analysis, program optimization, compiler construction.
Notable past projects	Transferbereich 14 "Run-time Guarantees for modern Processor Architectures" of the German DFG. DAEDALUS RTD project IST-1999-20527 of the European FP5 program on the validation of software components embedded in future generation critical concurrent systems by exhaustive semantic-based static analysis and abstract testing methods based on abstract interpretation. http://www.di.ens.fr/~cousot/projects/DAEDALUS/index.shtml INTEREST EU Framework VI Specific Targeted Research Project IST-033661 aiming at overcoming the lack of integration and interoperability of tools for developing Embedded Systems software.

	http://www.interest-strep.eu/
Awards / Decorations	Dr. Ferdinand received the Dr. Eduard Martin Preis in 1999 (award for best Ph.D Thesis in computer science at Saarland University).
	AbsInt has been awarded a 2004 European Information Society Technology (IST) Prize for its timing analyzer aiT.

4.3 Affiliated Academic Partners

	Prof. Dr. Sabine Glesner (Technical University of Berlin) www.pes.cs.tu-berlin.de
Technical role(s) within ArtistDesign	Activity Leader for Compiler Platform Compiler Verification
Research interests	Compilers, Verification, Embedded Systems and Software, Formal Semantics
Role in leading conferences/journals/etc in the area	PC Member of Compiler Construction 2007 Date'06, Design, Automation and Test in Europe, TPC Member of Topic B9 on Formal Verification Workshop Compiler Optimization meets Compiler Verification COCV, ETAPS Conferences, PC Member in 2005 and 2006, Program Co-Chair in 2007 Workshop Formal Foundations of Embedded Software and Component-Based Software Architectures (FESCA), ETAPS Conferences, PC Member 2005 and 2006 Editorial Board Member of "Informatik – Forschung und Entwicklung" by Springer, starting with Vol. 21, No. 1
Notable past projects	VATES (Verification and Transformation of Embedded Systems), funded by DFG Aktionsplan Informatik (Emmy Noether-Program), funded by DFG, support for young researchers to build a research group, with a focus on optimization and verification in the compilation of higher programming languages, from 2004 to 2009 Correct and Optimizing Compilers for Modern Processor Architectures, funded by a postdoc excellence program of Baden-Württemberg, Germany, 2003-2005

	Grant in the Wrangell-Habilitation Program of Baden-Württemberg, Germany, 2001-2005
Awards / Decorations	Award of the "Forschungszentrum Informatik" for one of the two best PhD theses of the Faculty for Computer Science, University of Karlsruhe, 1998/99
	Member of the "Studienstiftung des deutschen Volkes", the German national scholarship organization, 1991-1996
	Fulbright grant to study at the University of California, Berkeley, 1993-1994
	Member of the Siemens Internationaler Studenten / Doktorandenkreis, 1993-1999

	Dr. Björn Franke (Lecturer, University of Edinburgh) http://homepages.inf.ed.ac.uk/bfranke/Welcome.html
Technical role(s) within ArtistDesign	Provide a link to work on program analysis and parallelization
Research interests	Compilers, embedded systems

	Prof. Paul Kelly (Imperial College, London) http://www.doc.ic.ac.uk/~phjk/
Technical role(s) within ArtistDesign	Provide a link to work on program analysis and parallelization
Research interests	Software performance optimization

	Dr. Alain Darte Scientific leader of Inria Project Compsys (Compilation and Embedded Computing Systems) Laboratoire de l'Informatique du Parallélisme CNRS, Inria, UCBL, ENS-Lyon http://perso.ens-lyon.fr/alain.darte
Technical role(s) within ArtistDesign	Activity in automatic parallelization, source to source transformations for high-level synthesis of hardware accelerators, possibly WCET.
Research interests	Code optimizations for embedded computing systems: back-end code optimizations (SSA form, register allocation, static/JIT compilation), source-to-source code transformations for HLS tools (code rewriting, memory and communication optimizations).
Role in leading conferences/journals/etc in the area	Editorial board of ACM Transactions on Embedded Computing Systems (ACM TECS). Program committees in 2008-09: SCOPES 2009, PLDI 2008, CC 2008. Before 2008: many DATE, CASES, ASAP, ICS, CGO, etc.
Notable past projects	Minalogic project SCEPTRE Collaboration with STMicroelectronics, funded by French Ministry of Research and Région Rhône-Alpes
Awards / Decorations	Best paper awards: IPDPS 2002, CGO 2007

4.4 Affiliated International Partners

None.

5. Internal Reviewers for this Deliverable

Prof. Dr. Olaf Spinczyk (TU Dortmund)

Prof. Dr. Christian Lengauer (U. Passau)