IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Transversal Activity - Progress Report for Year 1

Cluster:
Hardware Platform and MPSoC Design

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Policy Objective (abstract)

The purpose of this cluster is to integrate different view points and approaches to MPSoC design and programming. The cluster will consider the hardware architecture and software components in their interaction, investigate tools for accurate estimation of certain design parameters (power, performance), and provide the designer with adequate support for design space exploration and optimization.

Versions

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1. Overview

In relation to the ArtistDesign network, it is the overall goal of the topic on hardware platforms and MPSoC design to extend the current state in composability towards issues like modelling of non-functional constraints, power and energy, end-to-end real-time behaviour, timing and performance analysis and heterogeneous models of computation.

Many application domains require adaptive real-time embedded systems that can change their functionality over time. In such systems it is not only necessary to guarantee timing constraints in every operating mode, but also during the transition between different modes. Therefore, it is one of the goals to develop new methods for the design and analysis of adaptive multi-mode systems.

One of the most critical issues to be faced in the research on execution platform is their rapidly growing complexity. Complexity increase is pushed by Moore's law, and by the ever-increasing demand for high performance computing. In addition, the boundaries between hardware and software domains are getting more blurred (dynamically re-configurable hardware, adaptable embedded systems, breakthrough in power consumption and performance) and challenging questions are at the border (trade-offs in mapping applications to hardware and software components, re-configurable hardware, WCET, performance of distributed computer and communication systems).

The cluster attempts to combine the diverse knowledge and to integrate different approaches in the area of execution platforms for embedded systems available in Europe and beyond.

1.1 High-Level Objectives

The purpose of this cluster is to integrate different view points and approaches to MPSoC design and programming. Therefore, the work is based on existing and future hardware platforms and their expected properties as well as anticipated application domains. The cluster will consider the hardware architecture and software components in their interaction, investigate tools for accurate estimation of certain design parameters (power, performance) based on appropriate models for hardware and software components, and provide the designer with adequate support for design space exploration and optimisation.
The importance of resource awareness in embedded systems is growing very rapidly. One major aspect is predictability, in particular concerning the timing behaviour. With the growing software content in embedded systems, and the diffusion of highly programmable and re configurable platform, software is given an unprecedented degree of control on resource utilization. Therefore, the major focus of the combined activities is to establish a design methodology that;

- scales to massively parallel and heterogeneous multiprocessor architectures,
- allows for predictable system properties
- uses the available hardware resources in an efficient manner.

Promising approaches are based on increasing the adaptivity on various levels and on composable frameworks.

1.2 Industrial Sectors

As hardware platforms are the backbone of embedded systems, the activities of this cluster spans all industrial sectors. A recent and accelerating trend is the move towards multicore platforms.

In the automotive domain, the increasing number of functions has led to automotive networks with a large number of distributed ECUs and increasing complexity with several busses and gateways that is difficult to handle. In next generation systems, large automotive OEMs are therefore proposing new structured hardware topologies, that focus on the application of powerful domain controllers connected over a high speed bus and several dedicated busses for the different functional domains. Multicore control units (MCUs) are perceived as a co-enabler for this technology, by allowing the integration of a large number of functions, at relatively low power and with various reliability and fail-safe options.

A similar trend can be observed in the aerospace domain, where multicore components need to be integrated into complex networks with commonly very high reliability requirements.

In the multimedia domain, the emerging trend for multimedia applications on mobile terminals, combined with a decreasing time-to-market and a multitude of standards have created the need for flexible and scalable computing platforms that are capable of providing considerable (application specific) computational performance at a low cost and a low energy budget. Platforms like TI OMAP, ST Nomadik, Philips Nexperia and IBM/Toshiba/Sonys CELL, contain multiple heterogeneous, flexible processing elements, a memory hierarchy and I/O components. All these components are linked to each other by a flexible on-chip interconnect structure. These architectures meet the performance needs of multimedia applications, while limiting the power consumption.

Also in the mechatronics domain, which traditionally was a rather sequential process, there is a trend towards multi-core platforms and the need to support the designer to make well-founded choices for an execution platform. Techniques from the multimedia domain are now being extended and adapted to deal with control-dominated high-tech applications as well.

Another clear trend is towards reconfigurable architectures, in general, and configurable processors, in particular. The generic goal is to achieve a high degree of flexibility (traditionally available only with software implementation) at an power consumption, which is much lower than achievable with a traditional software implementation using general purpose processors.

1.3 Main Research Trends

Many embedded system applications are implemented today using distributed architectures, consisting of several hardware nodes interconnected in a network. Each hardware node can consist of a processor, memory, interfaces to I/O and to the network. The networks are using specialized communication protocols, depending on the application area. For example, in the automotive electronics area communication protocols such as CAN, FlexRay and TTP are used. One important trend today is toward the integration of multiple cores on the same chip, hence embedded systems are not only distributed across multiple boards or chips, but also within the same chip.

As the complexity of the functionality increases, the way it is distributed has changed. If we take as an example the automotive applications, initially, each function was running on a dedicated hardware node, allowing the system integrators to purchase nodes implementing required functions from different vendors, and to integrate them into their system. Currently, number of such nodes has reached more than 100 in a high-end car, which can lead to large cost and performance penalties. Moreover, with the advent of poly-core (i.e. high cardinality multi-core) single-chip platforms, the effective number of processing nodes tends to grow in a “fractal” way, and future distributed systems with thousands of processing nodes are not a far away dream.

Not only the number of nodes has increased, but the resulting solutions based on dedicated hardware nodes do not use the available resources efficiently in order to reduce costs. For example, it should be possible to move functionality from one node to another node where

there are enough resources (e.g., memory) available. Moreover, emerging functionality, such as brake-by-wire, is inherently distributed, and achieving an efficient fault-tolerant implementation is very difficult in the current setting.

Moreover, as the communications become a critical component, new protocols are needed that can cope with the high bandwidth and predictability required. The trend is towards hybrid communication protocols, such as the FlexRay protocol, which allows the sharing of the bus by event-driven and time-driven messages. Time-triggered protocols have the advantage of simplicity and predictability, while event-triggered protocols are flexible and have low cost. A hybrid communication protocol like FlexRay offers some of the advantages of both worlds. The need for scalable and predictable communication is not only a characteristic of automotive designs, but even multimedia and signal processing systems are increasingly communication dominated.

While computation and communication are clear targets, common consensus has been growing on the criticality of memory architecture and related memory management software challenges. Even predictable and efficient processors and communication fabrics are not sufficient to provide a predictable and efficient application level view of the platform if not adequately supported by a memory system.

The trend towards distributed architectures introduces a new challenge. A lot, if not most of the traditional software is sequential in nature. Major reason for this is that most modern programming languages are sequential and do not have adequate language-level concurrency support. Traditionally the timing performance of software increased as a result of the increase in clock speed of the individual processing cores. However, this free lunch is over because clock speeds have hardly increased since 2003. Multi-core and hyperthreading techniques are now used to boost platform performance. Modern compilers based on sequential programming languages are not able to sufficiently utilize these additional computational resources. New languages, techniques and tools are required that seamlessly match modern execution platforms, for instance by adequate application-level concurrency support. Although a number potential techniques already exist, getting more momentum in these directions is crucial to deal with future complexity and performance requirements.

With growing embedded system complexity more and more parts of a system are reused or supplied, often from external sources. These parts range from single hardware components or software processes to hardware-software (HW-SW) subsystems. They must cooperate and share resources with newly developed parts such that the design constraints are met. There are many software interface standards such as CORBA, COM or DCOM, to name just a few examples that are specifically designed for that task. Nevertheless in practice, software integration is not a solved but a growing problem. This is especially true when performance and energy efficiency can be achieved only if a sufficient degree of parallelism in application execution is achieved.

New design optimization tools are needed to handle the increasing complexity of such systems, and their competing requirements in terms of performance, reliability, low power consumption, cost, time-to-market, etc. As the complexity of the systems continues to increase, the development time lengthens dramatically, and the manufacturing costs become prohibitively high. To cope with this complexity, it is necessary to reuse as much as possible at all levels of the design process, and to work at higher and higher abstraction levels, not only for specification of overall system functionality, but also for supporting communication among a number of parallel executing nodes.

One of the most significant achievements in the cultural landscape of low-power embedded systems design is the consensus on the strategic role of power management technology. It is now widely acknowledged that resource usage in embedded system platforms depends on application workload characteristics, desired quality of service and environmental conditions.

System workload is highly non-stationary due to the heterogeneous nature of information content. Quality of service depends on user requirements, which may change over time. In addition, both can be affected by environmental conditions such as network congestion and wireless link quality.

Power management is viewed as a strategic technology both for integrated and distributed embedded systems. In the first area, the trend is toward supporting power management in multi-core architectures, with a large number of power-manageable resources. Silicon technology is rapidly evolving to provide an increased level of control of-on chip power resources. Technologies such as multiple power distribution regions, multiple power-gating circuits for partial shutdown, multiple variable-voltage supply circuits are now commonplace. The challenge now is how to allocate and distribute workload in an energy efficient fashion over multiple cores executing in parallel. Also, one open issue is how to cope with the increasing amount of leakage in nanometer technologies, which tends to over-emphasize the cost of inactive logic, unless it can be set in a low-power idle state (which in many cases implies storage losses and high wakeup cost).

In the area of distributed low-power systems, wireless sensor networks are the key technology drivers, given their tightly power constrained nature. One important trend in this area is toward “battery free” operation. This can be achieved through energy storage devices (e.g. super-capacitors) coupled with additional devices capable of harvesting energy from environmental sources (e.g. solar energy, vibrational energy). Battery-free operation requires carefully balancing harvested energy and stored energy against the energy consumed by the system, in a compromise between quality of service and sustainable lifetime.

The concept of Multiprocessors-on-a-chip (MPSoC) has been discussed since some years but it appears that recently, the area has gained much more interest. In terms of industrial support, an increasing number of companies are active in the design of corresponding architectures as well as introducing the first products in the market. Whereas there are major breakthroughs in terms of new hardware architectures, corresponding programming environment are still at their infancy. In particular, ease of application specification, scalability, predictability of the overall system, parallelization, low power operation, efficiency and support of legacy code are just some of the main problems the community is facing.

A major industrial concern that comes with the integration of previously independent functions onto a single multicore or multiprocessor-system-on-chip is the resulting reliability of the individual functions. Depending on the criticality of a function, OEMs and indirectly their suppliers deliver guarantees to lawmakers on the overall failure rate of the system or component, with higher cost associated with the certification of higher level of reliability. Integration of functions with different reliability levels is then not cost efficient, if the resulting system needs to be verified for the highest level of reliability. A major research direction is therefore the investigation of methods that allow the co-integration of such functions. The researchers in ArtistDesign investigate countermeasures to this problem, for example by orthogonalization of the shared memory (e.g. Linköping University), or conservative bounds on the use of shared resources (e.g. TU Braunschweig).

2. State of the Integration in Europe

2.1 Brief State of the Art

Modern embedded systems for multimedia, imaging, and signal processing are characterized by high performance requirements on the one hand and stringent power requirements on the other hand. Often, these requirements can no longer be satisfied by embedded system architectures based on a single processor. Thus, emerging embedded system-on-chip platforms are increasingly becoming multiprocessor architectures. To compensate the high nonrecurring costs for designing and manufacturing multiprocessor chips, however, they need to be flexible such that they can be reused in different systems. This flexibility calls for programmability and sometimes reconfigurability. As a result, embedded systems platforms often have a heterogeneous architecture consisting of fully dedicated hardware components and different programmable processor cores.

A considerable number of multi-processor design frameworks have been proposed in the past, such as Artemis, Distributed Operation Layer (DOL), Embedded System-Level Platform Synthesis and Application Mapping (ESPAM), Koski, or StreamIt. While all frameworks provide an automated path from application specification to system implementation, they focus on different aspects of the design flow. In ArtistDesign, we attempt to unify the approaches developed by the various partners and extend them towards new methods for performance analysis, design space exploration and adaptivity.

The past several years have seen an increasing interest in wireless sensor nodes which are scavenging energy from their environment. In [5], several technologies have been discussed how, e.g., solar, thermal, kinetic or vibrational energy may be extracted from a node‘s physical environment. In particular, techniques to harvest energy via photovoltaic cells have attracted the interest of the sensor network community [6]. Solar energy is certainly one of the most promising energy sources and typical environmental monitoring applications have access to solar energy. If sensor nodes are equipped with photovoltaic cells as energy transducers, the autonomy of sensor nodes is increased substantially since frequent recharging and replacement of the batteries becomes unnecessary. Ideally, sensor nodes once deployed in a harsh environment benefit from a drastically increased operating time and become virtually immortal.

Clearly, the power generated by small solar cells is limited. Sensor nodes executing a given application may frequently run out of energy in times with insufficient illumination. If one strives for predictable, continuous operation of a sensor node, common power management techniques have to be reconceived. In addition to perform classical power saving techniques, the sensor node has to adapt to the stochastic nature of solar energy. Goal of this adaptation is to maximize the utility of the application in a long-term perspective. The resulting mode of operation is sometimes also called energy neutral operation: The performance of the application is not predetermined a priori, but adjusted in a best effort manner during runtime and ultimately dictated by the power source. Therefore, storage devices like batteries are solely used as energy buffers to compensate the variations of the underlying energy source. It is the goal of the interaction in ArtistDesign to improve the state-of-the-art in energy scavenging and the corresponding algorithms to adapt the running applications so as to optimize a long-term reward function.

2.2 Main Aims for Integration and Building Excellence through ArtistDesign

Following the activities presented in the previous section, the cluster on execution platforms follows the following strategy and uses the following mechanisms to spread the knowledge and integration achieved so far:

- Summer Schools and Training Activities to distribute the knowledge acquired in ArtistDesign to (a) other countries, (b) other communities and (c) young researchers.
- Tutorials at major conferences to reach new and larger research communities.
- Joint publications between partners, which not only show the integration within the cluster but are an excellent instrument to disseminate the integration results.
- New research projects with industrial partners, which allow us to apply the obtained results at an industrial scale. This way, we also receive feedback and ideas for new research directions.
- Cooperation with other research groups, especially outside the EU (mostly USA and Asia). In this case, spreading excellence is not the only objective. The cluster participants can be exposed to new research problems and new approaches that can be then explored and improved within the cluster.

2.3 Other Research Teams

It appears that main research groups in Europe dealing with execution platforms for embedded systems are in the ArtistDesign network, either as full or as affiliated partners. There are some exceptions though, caused by the fact that not all are accepting a European network of Excellence as a viable funding instrument. In the following, some of these groups are listed together with their relation to ArtistDesign.

The University of North Carolina at Chapel Hill, Sanjoy Baruah and Jim Anderson. Sanjoy Baruah and Jim Anderson are known in particular for their research in the domain of multiprocessor real-time scheduling.

University of Dresden, Hermann Härtig. Hermann Härtig is a leading researcher in the domain of micro-kernel based real-time operating systems.

Low power embedded systems design: In the area of low power embedded systems design, several new and relevant research themes are explored by other teams, not included in the ARTIST2 network. In particular research groups in the USA have a long tradition of excellence in low power research. We can mention the group lead by prof. Jan Rabaey in UC Berkeley, which is carrying out ground-breaking work on hardware platforms for wireless sensor networks. In the same area, several other groups are performing top-level research, e.g. Anantha Chandrakasan's group at MIT and David Blaauw's group at University of Michigan. Low power execution platforms are not relevant only for wireless sensor network, but also for mobile computing and even for servers and traditional computing infrastructure (e.g. servers). In these areas, the groups lead by Profs. Vijaykrishnan Narayanan, Mahmut Kandemir and Mary Jane Irwin at Penn State University, has produced a large number of interesting results in the last few years. We mention in particular their work on power issues for 3D integration and their analysis of power vs. reliability tradeoffs in high-performance computing. In this area, very interesting work is also performed by the group of prof. Kevin Skadron. The focus of this group is on thermal issues, which are very significant for high-performance system.

Universita degli Studi di Verona/Electronic Design Automation (EDA) group, Prof. Franco Fummi. Main research activities of the EDA group concern system verification, system synthesis and optimization, hardware description languages, power consumption, language

abstraction, and system testing. Interactions with members of the execution platforms cluster are, for example, by participation in European projects (e.g. the STRP "Vertigo") together with the Linköping group.

University of Southampton,/Electronic Systems Design Group, Prof. Bashir Al Hashimi. The Electronic Systems Design (ESD) Research Group is internationally recognized in two main areas - the development of novel algorithms and methodologies for Electronic Design Automation to support the design and test of large systems, and for intelligent sensor micro-systems. The group is working in the areas of system modelling, simulation, and synthesis, SoC design and testing, as well as smart sensors. Several cooperation projects have been undertaken, in particular with the Linköping group.

Carnegie Mellon University/System Level Design Group/Prof. Radu Marculescu. The System Level Design group performs research on formal methods for system-level design of embedded applications. They, in particular, focus on fast methods for power and performance analysis that can guide the design process of portable information systems. Important results have been obtained with regard to the communication-centric SOC design, providing formal support for analysis and optimization of novel on-chip communication architectures. In particular, this work addresses fundamental research problems for defining scalable and flexible communication schemes via the Network-on-Chip (NoC) approach. Interaction has been by, for example, PhD student exchanges with the Linköping group.

2.4 Interaction of the Cluster with Other Communities

Casteness 2008 Workshop; location: Rome, Italy; date: 15th-18th of January 2008: The objectives of CASTNESS workshops and schools are, first, to provide training about the future of multi-processor/adaptable embedded systems (system SW, HW architectures, applications) and second, the cross-dissemination among European projects. ETHZ presented an overview and a SW demonstration of the Distributed Operation Layer framework, included in a complete MPSoC design flow, as well as detailed information about the design space exploration and mapping optimization steps within this framework.

Invited Talk L. Thiele (ETHZ): MPSOC Conference. Aachen, Germany, June 23-27, 2008: Lothar Thiele described a new approach for mapping algorithms onto MPSoC architectures. It is a result of a cooperation between ArtistDesign partners from Aachen, TIMA and LETI. The design methodology is named DOL (distributed operation layer) and targets predictable and efficient multiprocessor systems and applications.

Summer School: Course on Embedded Systems (ETHZ, L. Thiele), Florianopolis, Brazil, August 25-2, 2008. The summer school was dedicated to promote the interaction between the embedded system communities in Europe and South America. Lothar Thiele was presenting a wide range of subjects, starting from basic methods to design predictable software of embedded systems. In addition, he presented methods for real-time scheduling and performance analysis of distributed embedded systems.

Tutorial L. Thiele (ETHZ): Analysis of Distributed Embedded Systems. CASTENESS WORKSHOP ROMA, Jan. 15-18, 2008. During the CASTNESS Workshop, ETHZ gave a tutorial on the different methods to estimate the performance of distributed embedded systems, including computation, communication and resource sharing.

TU Braunschweig and TU Eindhoven are guest editors of the ACM TECS special issue on Model-driven Embedded System Design (http://acmtecs.acm.org/mesd.htm).

Linköping has given an invited talk at the DATE 2008 Conference, as part of the special day on Dependable Embedded Systems. With this occasion several results obtained in the ARTIST

context have been made accessible to an international audience. They are related, in particular, to fault tolerance aspects of distributed real-time systems like those used in automotive applications.

Linköping has organised the 6th IEEE Workshop on Embedded Systems for Real-Time Multimedia, as part of the ARTIST sponsored Embedded Systems Week 2008.

UNIBO has been very active in the Multi-core Systems-on-Chip community and in the computer architecture community which is now aggressively targeting multi-core systems. UNIBO has become active member of the HIPEAC2 network of excellence and participated to several events in this area. Prof. Benini has been an HIPEAC instructor at the ACACES summer school, in L'Acquila. Members of the UNIBO team have participated to the main HIPEAC events in 2008.

DTU has become an active member of the HIPEC2 network of excellence and is participating in the chapter on programming models. Prof. Sven Karlsson from DTU has participated en several HIPEAC2 events.

DTU has been organizing the DaNES Mini-Case Workshop on industrial case-studies at DTU on May 22-23, 2008.

TU Braunschweig has been organizing the Embedded Software Track at the major European conference on design automation DATE (Design Automation and Test in Europe) that took place March 10-14, 2007. The track was devoted to modelling, analysis, design and deployment of embedded software, including formal methods, tools, methodologies and development environments. Thereby, the emphasis was on embedded software platforms, software integration and portability issues.

DTU has established collaboration with Duke University on design tools for biochips based on digital microfluidics. A PhD student from DTU has visited Duke for 6 months.

DTU has extended its long term relationship with Virginia Tech on hardware design using the Gezel hardware description language. A PhD student from DTU has visited Virginia Tech for 1 month.

DTU has been organizing the Special Sessions of the DATE 2008 conference. A total of 9 sessions were organized.

UNIBO, TU Braunschweig and DTU gave invited talks at the 8th International Forum on Application Specific Multi-Processor SoC, Aachen, Germany.

3. Overall Assessment and Vision for the Cluster

The research in embedded systems is still fragmented. This not only is true within a single subject but also between several sub-disciplines. It is one of the major goals of the cluster on 'Hardware Platforms and MPSoC Design' to establish closer links to the other communities and to take advantage of the scientific results and insights.

Cross-layer design is a key issue in embedded systems. The classical view of a strict layering according to chosen abstraction levels does not work any more because of the importance of non-functional constraints and limited resources. Therefore, completely new concepts are necessary that enable the integrated modelling and design under predictability and efficiency constraints. It is expected that this move towards a resource-aware design trajectory involves all current layers and a breakthrough can be obtained by integration only.

3.1 Assessment for Year 1

LINKÖPING-DTU: Interaction between Linköping and DTU has been in the area of fault tolerant embedded systems. Solutions have been developed in cooperation and publications have been written together. Prof. Paul Pop from DTU has visited Linköping.

LINKÖPING-BOLOGNA: Interaction between Linköping and Bologna has been in the area of predictable multiprocessor systems. Paolo Burgio has visited Linköping for 10 months and has worked on the elaboration of bus controllers. In this period he has also written his Master Thesis. Experiments at Linköping has been run using the MPARM tool from Bologna.

LINKÖPING-TUBS: Interaction between Linköping and Braunschweig has been in the area of performance analysis for distributed systems and predictable multiprocessors. The Symta/P worst case execution time analysis tool from Braunschweig has been further developed at Linköping and has been integrated in a predictable analysis and scheduling tool for multiprocessors.

ETHZ has been mainly involved in cooperations with University Bologna and University Dortmund. In particular, we looked at new approaches to map algorithms onto highly parallel MPSoC platforms. To this end, we linked the specification and mapping environment DOL (distributed operation layer) from ETHZ to the MPARM simulation platform from University Bologna. Major efforts have been invested into the corresponding alignment of the semantics, the generation of appropriate hardware-dependent software and the implementation of predictable communication fabrics. This work just started and will continue during the next phase of ArtistDesign. Together with University Dortmund, we are starting to investigate the influence of memory mapping on the whole MPSoC design process. A first visit of a PhD student from Dortmund to ETHZ took place which resulted in a first problem specification.

DTU-BOLOGNA: Interaction between DTU and Bologna has been in the area of networked embedded systems. Focus has been on power management in wireless sensor networks supported by energy harvesting. To this end, the sensor node scheduler based on Lazy-scheduling has been integrated in the wireless sensor network simulator from DTU, which provides a dynamic power-aware routing protocol. Two visits of a student from DTU to Bologna took place, resulting in a first integration and a definition of a case study.

DTU-KTH: Interaction between DTU and KTH has been in the area of system modelling suited for raising the level of abstraction for SMEs working with Embedded Systems, either as technology providers or as technology users. The result was a joint application to the ARTEMIS JU together with Tampare University of Technology and 8 SMEs. The project, called SYSMODEL, was accepted and will be started in the beginning of 2009.

DTU-AAU: Interaction between DTU and AAU (Modeling and Validation cluster) has been in the area of formalizing the ARTS system-level simulation model using timed automata based on UPPAAL. This work was started in ARTIST2. The result has been a prototype modelling framework (MoVES), which allows to experiment with different models-of-computation. In order to support designers of industrial applications, the timed-automata model is hidden for the user, allowing the designer to work directly with the abstract system-level model of embedded systems.

3.2 Overall Assessment since the start of the ArtistDesign NoE

Simulation platform for distributed embedded systems (Linköping, DTU)

A simulation environment is designed and implemented for distributed real-time systems such as those used in automotive applications. The ARTS environment, developed at DTU and targeting System-on-chip applications, has been used as a starting point by the Linköping team.

Modeling and response-time/buffer analysis for NoC (Linköping)

The Linköping group has developed a system model, based on which worst case response times and worst case buffer need for hard real-time applications implemented on NoCs can be calculated. On top of this analysis approach, an optimization tool for buffer space minimization has been implemented, for real-time NoC applications.

Predictability in Multiprocessor SoC architectures (Linköping, Bologna, Braunschweig)

The Linköping group has developed a framework for predictable WCET analysis, scheduling, and bus access optimisation for multiprocessors. With regard to the "classical" aspect of WCET analysis the group is building on the Symta/P tool from the Braunschweig group. The Linköping group is also interacting with the Bologna group with regard to the issues of bus control for predictable multiprocessors.

Power optimization via system-level resource allocation and scheduling (Linköping, Bologna)

The main objective here is to develop techniques for optimally mapping multi-task (parallel) applications onto System-on-chip (SoC) platforms with multiple processors (MP-SoCs). This is an industry-relevant problem, as most high-end embedded computing platforms in a number of target markets (automotive, multimedia, networking) are evolving toward multi-core architectures. The most critical challenge in this area is the complexity of the problem of optimally mapping tasks onto cores (and storage resources), while selecting frequency and voltage assignments for the various cores.

Optimization and analysis of distributed embedded systems (Linköping)

In the context of optimization and analysis of distributed embedded systems the following issues:

- Analysis of hierarchically scheduled systems
- Timing analysis of distributed task sets communicating through the FlexRay protocol
- Analysis and optimization mixed time and event triggered systems

Fault Tolerant Distributed Embedded Systems (Linköping, DTU)

Linköping and DTU have addressed the issue of fault tolerant distributed embedded systems, with special emphasis on handling transient faults. There are two main aspects of interest here:

- Analysis of timing properties in the presence of faults and possible guarantees regarding worst case behaviour
- System optimization, such that timing and fault tolerance requirements are satisfied given a certain, limited amount of resources.

An approach for scheduling and worst case analysis with fault tolerance has been developed. On top of this analysis approach, an optimization technique for task mapping and fault tolerance policy assignment has been elaborated and implemented.

Integration of Symta/S - MPA and unifying approaches for hierarchical scheduling (ETHZ together with University Braunschweig)

In a recently published paper J. Rox and R. Ernst from University Braunschweig introduced the hierarchical event model that is going to be implemented in the SymTA/S framework. Alternative approaches to deal with merged event streams should be found for the MPA framework used at the ETH Zurich. In a first step, ETHZ analyzed the formalism by Braunschweig and are now considering various solutions how to embed the hierarchical event model into MPA. The major issue here is to also allow an extraction of single event streams from previously merged – and transformed event streams. The transformation is hereby due to the fact that incoming streams can be combined via OR-operation and may pass different system components, which may buffer these streams due to scheduling policies. In a next step, analysis and comparisons of the different approaches will be done. To this end, a PhD student from ETHZ visited University Braunschweig for a week (6th of Oct until 10th of Oct. 2008). A technical report has been written that will be submitted for publication.

Optimization-centric MPSoC Design (University Bologna together with ETHZ)

The technical achievements are based on a set of joint meetings and visits. The primary goal of this activity was to establish a mutual understanding of the MPARM framework (developed at University of Bologna), on one hand, and the DOL framework (developed at ETHZ), on the other hand.

One main outcome of the meetings was to establish the design of the Modular Performance Analysis (MPA) analytic model for the MPARM platform. For this goal, the input specification and the API of the Distributed Operation Layer (DOL) framework, developed by ETHZ, was ported to the MPARM environment. This work is still under way. In particular, further phone conferences on the 22nd and 24th of October have been devoted to a refinement of the approach. These phone meetings had as main goal the identification of the basic design factors impacting on predictable communication fabrics.

Photovoltaic scavenging systems from the model to the optimized design (University Bologna, ETHZ)

University of Bologna and ETHZ have improved the design of a scavenger prototype which exploits miniaturized photovoltaic modules to perform automatic maximum power point tracking. We propose a detailed model of the solar cell that predicts the instantaneous power collected by the panel and improves the simulation of harvester systems. Furthermore, we focused on a methodology for optimizing the design of MPPT solar harvesters for self-powered

embedded systems and presented innovations in the circuit architecture with respect to our previous implementation. We verified that energy consumption and efficiency of the MPP tracker are very important design criteria in energy scavengers for sensor nodes, therefore we analyzed two important metrics: (i) maximization of the energy harvesting efficiency; (ii) minimization of the energy used for ineffective operations.

To this end the technical achievements can be summarized as follow:

(a) We presented a compact model for small solar modules that accurately describes the behaviour over a wide range of irradiance conditions, cell temperature variation and incident angle with out numerical approaches typically adopted;

(b) We improved the design process of the DC–DC converter at the solar harvester input stage boosting its efficiency

(c) We addressed the powering a sensor node with miniaturized photovoltaic modules of a few mm2 proposing a new inductor-less architecture for the harvesting process suitable for on-chip integration.

Energy Harvesting Aware Routing with Scheduling optimization (DTU, UoB)

DTU and Bologna have started a collaboration on energy-scavenging wireless sensor networks. Renewable energy sources can potentially lead to perpetual operation, but not without careful management of the energy both in the individual node and in the whole network. DTU has developed a simulator for wireless sensor networks, which is capable of capturing nodes with energy harvesting. Bologna and DTU have made the first attempts towards integrating lazy-scheduling with energy-aware routing within the simulator.

Modeling and Verification of Embedded Systems (DTU, AAU)

DTU has continued the work from ARTIST2 on formalizing the ARTS simulation model and to make it usable for designers early in the design process. In order to support designers of industrial applications, the timed-automata model is hidden for the user, allowing the designer to work directly with the abstract system-level model of embedded systems. The designer provides an application consisting of a set of task graphs, an execution platform consisting of processing elements interconnected by a network and a mapping of tasks to processing elements. The system model is then translated into a timed-automata model which enables schedulability analysis as well as being able to verify that memory usage and power consumption are within certain limits. In the case where a system is not schedulable, the tool provides useful information about what caused the missed deadline. DTU does not propose

3.2.1 List of Joint Publications

The following list contains publications, where authors are in different research sites which are participating in the ArtistDesign network and where at least one author is in the cluster on Execution Platforms. It clearly shows the degree of integration that has been achieved. The following list collects all joint publications since the start of ArtistDesign:

1. Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng, “Synthesis of Flexible Fault-Tolerant Schedules with Preemption for Mixed Soft and Hard Real-Time Systems”, 11th EUROMICRO CONFERENCE on DIGITAL SYSTEM DESIGN (DSD 2008), Parma, Italy, September 3-5, 2008, pp. 71-80.
2. Petru Eles, Viacheslav Izosimov, Paul Pop, Zebo Peng, “Synthesis of Fault-Tolerant Embedded Systems”, Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, pp. 1117-1122.

3. Wu, K., Madsen, J., Kanstein, A., Mladen, B., *MT-ADRES: Multithreading on Coarse-Grained Reconfigurable Architecture*, Intel. Journal of Electronics (IJE), Volume 95, Issue 7, July 2008. Page(s): 761-776.
4. Anders Tranberg-Hansen, Jan Madsen, Bjørn Sand Jensen, A Service Based Estimation Method for MPSoC Performance Modelling, to appear in the proceedings of the 3rd International Symposium on Industrial Embedded Systems, June 2008.
5. A Reactive and Cycle-True IP Emulator for MPSoC Exploration Mahadevan, S.; Angiolini, F.; SparsSparso, J.; Benini, L.; Madsen, J. Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Volume 27, Issue 1, Jan. 2008 Page(s):109 – 122
6. **'**Enabling run-time memory data transfer optimizations at the system level with automated extraction of embedded software metadata information', Bartzas, A.; Peon-Quiros, M.; Mamagkakis, S.; Catthoor, F.; Soudris, D. and Mendias, J., Asia and South Pacific Design Automation Conference - ASP-DAC, 2008
7. 'Optimization Methodology of Dynamic Data Structures based on Genetic Algorithms for Multimedia Embedded Systems', Baloukas, C.; Risco Martin, J.; Atienza, D.; Poucet, C.; Papadopoulos, L.; Mamagkakis, S.; Soudris, D.; Hidalgo, J.; Catthoor, F. and Lancares, J., Elsevier Journal of Systems and Software (JSS), 2008
8. 'MNEMEE: Memory management technology for adaptive and efficient design of embedded systems' S.Mamagkakis, P.Lemmens, D.Soudris, T.Basten, P.Marwedel, D.Kritharidis, G.Guilmin, 16th IFIP/IEEE International Conference on Very Large Scale Integration - VLSI-SOC, 2008.
9. 'MOSART: Mapping Optimisation for Scalable multi-core ARchiTecture', B. Candaele, A. Jantsch, T. Ashby, K. Tiensyrjä, F. Ieromnimon, B. Vanthournout, P. Di Crescenzo, D. Soudris, 16th IFIP/IEEE International Conference on Very Large Scale Integration - VLSI-SOC, 2008.
10. Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng, "Scheduling of Fault-Tolerant Embedded Systems with Soft and Hard Timing Constraints", Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, 915-920.
11. Traian Pop, Paul Pop, Petru Eles, Zebo Peng, Alexandru Andrei, "Timing Analysis of the FlexRay Communication Protocol", Real-Time Systems Journal, Volume 39, Numbers 1-3, August, 2008, pp 205-235.
12. Traian Pop, Paul Pop, Petru Eles, Zebo Peng, Alexandru Andrei, "Analysis and Optimisation of Hierarchically Scheduled Multiprocessor Embedded Systems", Intl. Journal of Parallel Programming, Volume 36, Number 1, February, 2008, pp. 37-67.
13. Bengt Jonsson, Simon Perathoner, Lothar Thiele, Wang Yi: Cyclic Dependencies in Modular Performance Analysis. ACM & IEEE International Conference on Embedded Software (EMSOFT), ACM Press, Atlanta, Georgia, USA, pages 179-188, October, 2008.
14. Simon Perathoner, Ernesto Wandeler, Lothar Thiele, Arne Hamann, Simon Schliecker, Rafik Henia, Razvan Racu, Rolf Ernst, Michael González Harbour: Influence of Different Abstractions on the Performance Analysis of Distributed Hard Real-Time Systems Design Automation for Embedded Systems, Springer Science+Business Media, LLC, 2008.
15. Davide Brunelli, Clemens Moser, Luca Benini, Lothar Thiele: An Efficient Solar Energy Harvester for Wireless Sensor Nodes. Design, Automation and Test in Europe (DATE 08), Munich, Germany, March, 2008.

16. Clemens Moser, Lothar Thiele, Davide Brunelli, Luca Benini: Robust and Low Complexity Rate Control for Solar Powered Sensors Design, Automation and Test in Europe (DATE 08), Munich, Germany, March, 2008.
17. Tolga Ovatman, Aske Brekling, and Michael R. Hansen. Cost analysis for embedded systems: Experiments with Priced Timed Automata. In proceedings of FESCA 2008.
18. 'Enabling run-time memory data transfer optimizations at the system level with automated extraction of embedded software metadata information', Bartzas, A.; Peon-Quiros, M.; Mamagkakis, S.; Catthoor, F.; Soudris, D. and Mendias, J., Asia and South Pacific Design Automation Conference - ASP-DAC, 2008
19. 'Storage estimation and design space exploration methodologies for the memory management of signal processing applications', Balasa, F.; Kjeldsberg, P.; Vandecappelle, A.; Palkovic, M.; Hu, Q.; Zhu, H. and Catthoor, F.Journal, Journal of VLSI Signal Processing Systems, 2008
20. Iyad Al Khatib, Francesco Poletti, Davide Bertozzi, Luca Benini, Mohamed Bech ara, Hasan Khalifeh, Axel Jantsch, and Rustam Nabiev, "A Multiprocessor System-on-Chip for Real-Time Biomedical Monitoring and Analysis: ECG Prototype Arc hitectural Design Space Exploration", ACM Transactions on Design Automation of Embedded Systems, vol. 13, no. 2, April 2008.
21. 'A System Scenario based Approach to Dynamic Embedded Systems', S.V. Gheorghita, M. Palkovic, J. Hamers, A. Vandecappelle, S. Mamagkakis, T. Basten, L. Eeckhout, H. Corporaal, F. Catthoor, F. Vandeputte, K. De Bosschere, ACM Transactions on Design Automation of Electronic Systems, ToDAES. To appear in 2009.
22. V. Izosimov, P. Pop, P. Eles, Z. Peng, "Design Optimization of Time- and Cost-Constrained Fault-Tolerant Embedded Systems with Checkpointing and Replication", IEEE Trans. on Very Large Scale Integrated (VLSI) Systems (accepted for publication).

3.3 Indicators for Integration

During year 1 we have done the following interactions between partners:

- *22 joint publications* have been produced. The plan was 10 Joint publications / year describing the results in terms of new methods and tools.
- Joint organization of workshops, tutorials, special sessions in international highly recognized conferences. In year 1 the following was accomplished:
  - Organized the 6th IEEE Workshop Embedded Systems for Real-Time Multimedia as part of the Embedded Systems Week, 2008.
  - Organized the DaNES Mini-Case Workshop in Denmark.
  - Organized the Embedded Software track at DATE 2008.
  - Organized the 9 Special Sessions at DATE 2008.
  - Organized a PhD course on Advanced Topics in Embedded Systems, Lyngby, Denmark (This was partly done together with ARTIST2)
  - Guest editor of the ACM TEC special issue on Model-Driven Embedded Systems Design.
  - Gave tutorial at Casteness 2008 Workshop in Rome, Italy.
  - Gave 4 invited talks at the 8th International Forum on Application Specific Multi-Processor SoC, Aachen, Germany.
- Yearly target is 1 workshop, 1 PhD course/school, 2-3 conference tutorials and special sessions.

- Integration of tools existing at the partner sites, and definition of tool flows integrating tools from the different partners.
    - The tool integration work started in ARTIST2 is being continued in ArtistDesign. This covers both integration of tools within the cluster, between clusters of ArtistDesign and with external partners.
- Mobility, i.e. the number of PhD student and faculty exchanges. This integration activity will also introduce the concept of "student clusters", where more than two PhD students from different partners will work together in a single location.
    - 6 PhD student visits
    - 4 faculty/researcher visits
    - 6 focused meetings (including "student clusters")
- Impact on industrial practice in the area of MPSoC design and analysis. This objective will leverage student internships at associated industrial partner's sites.
    - No student internships have been carried out during year 1.
    - 3 PhD students are working closely with industry partners.

3.4 Long-Term Vision

Embedded systems are growing more software and communication centric. As a consequence, new models and new analysis and design space exploration tools are needed in order to support optimal implementation of applications on distributed embedded architectures such as MPSoC. Embedded systems are characterized by continuously increasing complexity and strong constraints on safety, performance, power consumption, and costs. To be able to design such systems, it is needed to (1) consider the hardware platform and software components of MPSoC systems in their interaction, in order to produce a system which satisfies the requirements at low cost, (2) support the designer with tools for accurate estimation of certain design parameters (power, performance) based on appropriate models for hardware and software components and (3) provide the designer with adequate support for design space exploration and optimization.

Embedded architectures and heterogeneous distributed embedded systems have grown to extremely complex computation and communication patterns, and to an increasing level of reconfigurability (including adaptivity and run-time resource management). New performance models and a corresponding theory are urgently needed.

The long-term vision for this activity is to advance the theory, methods and tools for the modeling, analysis and design of embedded systems and to disseminate this to advance academic excellence, education and industrial innovation.

3.5 Tools and Platforms

3.5.1 Tool: SymTA/S

Objectives

SymTA/S is a tool for the development and verification of embedded multiprocessor real-time systems. The existing technology is mainly suitable for event or time-driven systems with message passing as the main task interaction. The tool shall be extended to cover the timing implications of multicore processors, or multiprocessor-systems-on-chip.

Main Results

In several previous projects (funded by German DFG, “Sureal”, funded by German BMBF, ARTIST2, and others), the compositional analysis approach has been transferred into a tool framework which is now also commercially available. The available modelling options capture typical problems in today’s automotive systems (CAN bus utilization, end-to-end deadlines,…). This addresses a growing need for formal methods in the industry. The topics currently under research (see below) address future problems which can be expected to become of increasing industrial interest in the future.

Current work

The research version of the tool framework is currently being developed into several new directions: Modeling of shared resources for multiprocessor-system-on-chips (see ArtistDesign Activity 6.2: Platform and MpSoC Analysis), the modelling of hierarchical event models (in the scope of the COMBEST project), and the demonstrator platform for adaptive systems (see ArtistDesign 7.1: Design for Adaptivity). Besides the extension of the applicability into new domains, a major focus within ArtistDesign is the synergetic coupling of tools, as well as the corresponding development of models.

Participating partners:

- TU Braunschweig.

  TU Braunschweig investigates synergies in the coupling of methods and implements prototypical implementations of the research results.

- Symtavision GmbH.

  Symtavision is the commercial co-developer of the tool framework. A focus within ArtistDesign is the coupling of with other industrially available tools (such as aiT).

- ETHZ.

  Collaboration on the coupling of MPA and SymTA/S with respect to modelling of hierarchical event models.

- AbsInt GmbH.

  The aiT tool supplies task timing models, which are required for system level analysis.

Web
http://www.symtavision.com/
http://www.ida.ing.tu-bs.de/index.php?id=symtas
http://www.ida.ing.tu-bs.de/en/research/projects/accord/

Related Publications

Simon Schliecker and Arne Hamann and Razvan Racu and Rolf Ernst. "Formal Methods for System Level Performance Analysis and Optimization." In *Proc. of the Design Verification Conference (DVCon)*, San José, CA, February 2008.

Jonas Rox and Rolf Ernst. "Modeling Event Stream Hierarchies with Hierarchical Event Models." In *Proc. Design, Automation and Test in Europe (DATE 2008)*, March 2008.

3.5.2 Tool: Analysis and optimisation framework for fault tolerant distributed embedded systems

Objectives

Linköping University and DTU are working on an environment and tool-set for the analysis and design optimisation of safety critical, fault tolerant real-time embedded applications. The emphasis is on the issue of transient faults and the goal is to develop tools for scheduling, mapping, and system optimisation.

Main results

A strategy for the synthesis of fault tolerant schedules has been developed. It can handle both hard and soft real-time tasks. The goal is to guarantee the deadlines for the hard processes even in the case of faults, while maximizing the overall utility. Time/utility functions are used to capture the utility of soft processes. Process re-execution is employed to recover from multiple faults. A single static schedule computed off-line is not fault tolerant and is pessimistic in terms of utility, while a purely online approach, which computes a new schedule every time a process fails or completes, incurs an unacceptable overhead. Thus, a quasi-static scheduling strategy is used, where a set of schedules is synthesized off-line and, at run time, the scheduler will select the right schedule based on the occurrence of faults and the actual execution times of processes. An optimisation technique for the generation of schedule tables supporting such a quasi-static scheduling approach has been developed and implemented.

Current work

Ongoing work is towards development of cost-optimisation techniques by considering processors with various hardening levels and the associated tradeoffs.

Participating partners

Linköping: Scheduling techniques, fault tolerant systems, design optimisation.

DTU: System level optimisation techniques

Publications

23. Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng, “Synthesis of Flexible Fault-Tolerant Schedules with Preemption for Mixed Soft and Hard Real-Time Systems”, 11th EUROMICRO CONFERENCE on DIGITAL SYSTEM DESIGN (DSD 2008), Parma, Italy, September 3-5, 2008, pp. 71-80.
24. Petru Eles, Viacheslav Izosimov, Paul Pop, Zebo Peng, “Synthesis of Fault-Tolerant Embedded Systems”, Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, pp. 1117-1122.

25. Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng, “Scheduling of Fault-Tolerant Embedded Systems with Soft and Hard Timing Constraints”, Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, 915-920.

3.5.3 Tool: IMEC MPA + MH MPSoC mapping framework

Objectives

The main objectives of the framework is to offer an automatic source code parallelization (MPA tool) and memory hierarchy management (MH tool) in order to map efficiently embedded software application on MPSoC platforms.

Main Results

Prototype versions of the MPSoC Parallelization Assistant (MPA) and Memory Hierarchy (MH) management tools were developed and tested on video codec embedded sosftware applications (i.e., MPEG-4, AVC etc.).

Current work

Currently, the affiliated partners of IMEC (ie, DUTH/ICCS and TU/e) and core partners (TUDortmund/ICD and KTH) are trying to integrate their tool and design flows with the IMEC MPA + MH MPSoC mapping framework in the memory and interconnect specific context of the MNEMEE and MOSART FP7 projects, respectively.

Participating partners:

- DUTH/ICCS
  This partner is integrating the dynamic data type and dynamic memory management tools and design flows with the IMEC MPSoC mapping tool flows.
- TU Dortmund/ICD
  This partner is integrating its pre-compiler and compiler framework to the static MH tool of IMEC.
- TU/e
  This partner is integrating its SDF3 framework in the context of system scenarios with the IMEC MPSoC mapping tool flows.
- KTH
  This partner is integrating its NoC simulation and exploration framework with the MPA tool of IMEC.

Web
http://www.mnemee.org/
http://www.mosart-project.org/

Related Publications

IMEC vzw. & TU/e

- ‘A System Scenario based Approach to Dynamic Embedded Systems’, S.V. Gheorghita, M. Palkovic, J. Hamers, A. Vandecappelle, S. Mamagkakis, T. Basten, L.

Eeckhout, H. Corporaal, F. Catthoor, F. Vandeputte, K. De Bosschere, ACM Transactions on Design Automation of Electronic Systems, ToDAES. To appear in 2009.

IMEC vzw. & TU/e & DUTH & TU Dortmund (at ICD)

- 'MNEMEE: Memory management technology for adaptive and efficient design of embedded systems' S.Mamagkakis, P.Lemmens, D.Soudris, T.Basten, P.Marwedel, D.Kritharidis, G.Guilmin, 16th IFIP/IEEE International Conference on Very Large Scale Integration - VLSI-SOC, 2008.

IMEC vzw. & KTH & DUTH

- 'MOSART: Mapping Optimisation for Scalable multi-core ARchiTecture', B. Candaele, A. Jantsch, T. Ashby, K. Tiensyrjä, F. Ieromnimon, B. Vanthournout, P. Di Crescenzo, D. Soudris, 16th IFIP/IEEE International Conference on Very Large Scale Integration - VLSI-SOC, 2008.

4. Cluster Participants

4.1 Core Partners

Cluster Leader Activity Leader & Team Leader	
	Jan Madsen (Technical University of Denmark)
Technical role(s) within ArtistDesign	Member of the Strategic Management Board Leads Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Participates in Intercluster activity: Integration Driven by Industrial Applications Leader of the JPRA Activity: “Platform and MPSoC Analysis”
Research interests	Research interests include high-level synthesis, hardware/software codesign, System-on-Chip design methods, and system level modelling, integration and synthesis for embedded computer systems.
Role in leading conferences/journals/etc in the area	Program Chair and Vice-Chair of Design Automation and Test in Europe Conference. Tutorial Chair and Special Sessions Chair of Design Automation and Test in Europe Conference. General Chair, Program Chair and Workshop Chair of CODES+ISSS Conference Member of the editorial board of the journal “IEE Proceedings – Computers and Digital Techniques” Member of the technical program committee and organizing committee of several technical conferences, including the Design Automation and Test in Europe Conference, the Real-Time Systems Symposium, the Symposium on Hardware-Software Codesign, and the International Workshop on Applied Reconfigurable Computing. Danish delegate in the Governing Board of ARTEMIS JU
Awards / Decorations	In 1995 he received the Jorck's Foundation Research Award for his research in hardware/software codesign

Team Leader

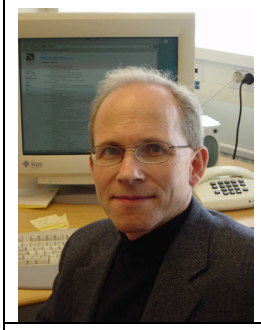
	Lothar Thiele (ETH Zurich)
Technical role(s) within ArtistDesign	Main areas of research: Embedded Systems and Software Participates in Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Participates in Intercluster activity: Design for Predictability and Performance
Research interests	Research interests include models, methods and software tools for the design of embedded systems, embedded software and bio-inspired optimization techniques.
Awards / Decorations	In 1986 he received the "Dissertation Award" of the Technical University of Munich, in 1987, the "Outstanding Young Author Award" of the IEEE Circuits and Systems Society, in 1988, the Browder J. Thompson Memorial Award of the IEEE, and in 2000-2001, the "IBM Faculty Partnership Award". In 2004, he joined the German Academy of Natural Scientists Leopoldina. In 2005-2006, he was the recipient of the Honorary Blaise Pascal Chair of University Leiden, The Netherlands.

Team Leader	
	Prof. Luca Benini, University of Bologna http://www-micrel.deis.unibo.it/%7Ebenini/
Technical role(s) within ArtistDesign	Member of the Strategic Management Board Co-leads Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Participates in Intercluster activity: Design for Predictability and Performance Leader of the JPRA Activity: “Platform and MPSoC Design”
Research interests	(i) Development of power modeling and estimation framework for systems-on-chip. (ii) Development of optimal allocation and scheduling techniques for energy-efficient mapping of multi-task applications onto multi-processor systems-on-chips. (iii) Development of energy-scavenging techniques for ultra-low power sensor network platforms.

Role in leading conferences/journals/etc in the area	▪ Program chair and vice-chair of Design Automation and Test in Europe Conference. ▪ Member of the 2003 MEDEA+ EDA roadmap committee 2003. ▪ Member of the IST Embedded System Technology Platform Initiative (ARTEMIS): working group on Design Methodologies ▪ Member of the Strategic Management Board of the ARTIST2 Network of excellence on Embedded Systems ▪ Member of the Advisory group on Computing Systems of the IST Embedded Systems Unit. ▪ Member of the technical program committee and organizing committee of several technical conferences, including the Design Automation Conference, International Symposium on Low Power Design, the Symposium on Hardware-Software Codesign. He is Associate Editor of the IEEE Transactions on Computer-Aided Design of Circuits and Systems and of the ACM Journal on Emerging Technologies in Computing Systems. ▪ Fellow of the IEEE.
Notable past projects	ICT-Project **REALITY - *Reliable and variability tolerant system-on-a-chip design in more-moore technologies.*** Funded under 7th FWP (Seventh Framework Programme). ICT-2007.3.1 Next-Generation Nanoelectronics Components and Electronics Integration. Start date: 01/01/2008; Duration: 30 months; Contract Type: Collaborative project; Project Reference: 216537; Project Cost: 4.45 million euro; Project Funding: 2.9 million euro. ICT-Project **PREDATOR - *Design for predictability and efficiency.*** Funded under 7th FWP (Seventh Framework Programme). ICT-2007.3.3 Embedded Systems Design. Start date: 01/02/2008; Duration: 36 months; Contract Type: Collaborative project; Project Reference: 216008; Project Cost: 3.93 million euro; Project Funding: 2.8 million euro. ICT-Project **GALAXY - *interface for complex digital system integration.*** Funded under 7th FWP (Seventh Framework Programme). ICT-2007.3.3 Embedded Systems Design. Start date: 01/12/2007; Duration: 36 months; Contract Type: Collaborative project; Project Reference: 214364; Project Cost: 4.08 million euro; Project Funding: 2.9 million euro. ICT-Project **DINAMICS - *Diagnostic Nanotech and Microtech Sensors.*** Funded under 6th FWP (Sixth Framework Programme). FP6-NMP 'Nanotechnologies and nanosciences, knowledge-based multifunctional materials and new production processes and devices'. Contract Type: Integrated project; Project Reference:IP 026804-2. Start date: 01/04/2007. Duration: 18 + 30 months. Project Cost:7276856 Euro. Project Funding: 4499542 Euro. http://www.dinamics-project.eu/ ICT-Project **SHARE - *Sharing open source software middleware to improve industry competitiveness in the embedded systems domain.*** Funded under 7th FWP (Seventh Framework Programme). ICT-2007.3.7 Network embedded and control systems. Start date: 01/05/2008; Duration: 24 months; Contract Type: Coordination and

	support actions; Project Reference: 224170; Project Cost: 1.1 million euro; Project Funding: 590000.00 euro.

Team Leader	
	Rolf Ernst (TU Braunschweig)
Technical role(s) within ArtistDesign	Main areas of research: Embedded Systems Participates in Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Participates in Intercluster activity: Design for Predictability and Performance Participates in Intercluster activity: Integration Driven by Industrial Applications
Research interests	Research interests include embedded architectures, hardware-/software co-design, real-time systems, and embedded systems engineering.
Role in leading conferences/journals/etc in the area	He chaired major international events, such as the International Conference on Computer Aided Design of VLSI (ICCAD), or the Design Automation and Test in Europe (DATE) Conference and Exhibition, and was Chair of the European Design Automation Association (EDAA), which is the main sponsor of DATE. He is a founding member of the ACM Special Interest Group on Embedded System Design (SIGBED), and was a member of the first board of directors. He is an elected member (Fachkollegiat) and Deputy Spokesperson of the "Computer Science" review board of the German DFG (corresponds to NSF). He is an advisor to the German Ministry of Economics and Technology for the high-tech entrepreneurship program EXIST (www.exist.org).

Team Leader	
	Petru Eles (Linköping University)
Technical role(s) within Artist2	Main areas of research: Embedded Systems Participates in Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Participates in Intercluster activity: Design for Predictability and Performance Participates in Intercluster activity: Integration Driven by Industrial Applications
Research interests	Research interests include electronic design automation, hardware/software co-design, real-time systems, design of embedded systems and design for testability.
Role in leading conferences/journals/etc in the area	- Associate Editor, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems; - Associate Editor, IEE Proceedings - Computers and Digital Techniques; - TPC Chair and General Chair, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS). - Topic chair, Design Automation and Test in Europe (DATE). - Topic Chair, Int. Conference on Computer Aided Design (ICCAD). - Program chair of the Hw/Sw Codesign track, IEEE Real-Time Systems Symposium (RTSS). - TPC Chair IEEE Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia). - Steering Committee Chair, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS).
Awards / Decorations	- Best paper award, European Design Automation Conference (EURO-DAC), 1992. - Best paper award, European Design Automation Conference (EURO-DAC), 1994. - Best paper award, Design Automation and Test in Europe (DATE), 2005. - Best presentation award, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS), 2003.

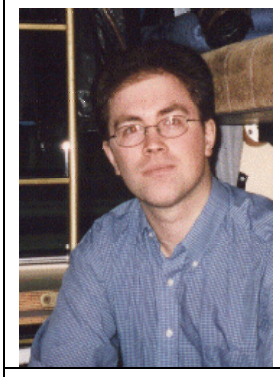
	- IEEE Circuits and Systems Society Distinguished Lecturer, for 2004 - 2005.

Team Leader	
	Dr. Stylianos Mamagkakis IMEC vzw. http://www.imec.be
Technical role(s) within ArtistDesign	Representing IMEC Nomadic Embedded Systems (NES) division in: -Cluster: SW Synthesis, Code Generation and Timing Analysis -Cluster: Operating Systems and Networks -Cluster: Hardware Platforms and MPSoC Design -Intercluster activity: Design for Adaptivity -Intercluster activity: Design for Predictability and Performance -Intercluster activity: Integration Driven by Industrial Applications
Research interests	Stylianos Mamagkakis received his Master and Ph.D. degree in Electrical and Computer Engineering from the Democritus Uni. Thrace (Greece) in 2004 and 2007, respectively. Since 2006, he coordinates a team of PhD students within the NES division at IMEC, Leuven, Belgium. His research activities mainly belong to the field of system-level exploration, with emphasis on MPSoC run-time resource management and system integration.
Role in leading conferences/journals/etc in the area	Stylianos Mamagkakis has published more than 35 papers in International Journals and Conferences. He was investigator in 9 research projects in the embedded systems domain funded from the EC as well as national governments and industry.
Notable past projects	Project leader of MNEMEE IST project www.mnemee.org Project leader of OptiMMA IWT project www.imec.be/OptiMMA Participation in: 1 international IMEC project (M4), 3 European IST projects (AMDREL, EASY, ARTIST2), 2 Greek projects (PRENED, DIAS)
Awards	1st prize in 'Technogenesis' Competition for Business Innovation, Greece, June'06 3rd prize in 'Otenet Innovation 2006' Competition for Business Innovation, Greece, November'06
Further Information	http://www2.imec.be/imec_com/nomadic-embedded-systems.php

Team Leader	
	Professor Axel Jantsch KTH http://web.it.kth.se/~axel/
Technical role(s) within ArtistDesign	A. Jantsch contributes to KTH participation and to the work on formal models of computation and communication and the ForSyDe framework. Furthermore, he also contributes to Hardware Platforms and MPSOC Design with focus on run-time environments and analysis techniques.
Research interests	A. Jantsch's main research topics are models of computation, modelling and analysis of embedded systems and SoCs, networks on chip.
Role in leading conferences/journals/etc in the area	
Notable past projects	**ANDRES** (Analysis and Design of run-time Reconfigurable, heterogeneous Systems) Project) – EU FP6 (http://andres.offis.de/) **SPRINT** (Open SoC Design Platform for Reuse and Integration of IPs): EU FP6 (http://www.ecsi-association.org/sprint) **MOSART** (Mapping Optimization for Scalable multi-core ARchiTecture) – EU FP7 (http://www.mosart-project.org/)

Team Leader	
	Thierry Collette, Ph.D (CEA LIST)
Technical role(s) within ArtistDesign	As a new partner, focus on new collaborations on reliable architectures.
Research interests	Embedded computing architectures, Many cores architectures reconfigurable computing and embedded reliability.

4.2 Affiliated Industrial Partners

	Daniel Karlsson (Volvo Technology Corporation)
Technical role(s) within ArtistDesign	Architecture and Design of Automotive Embedded Systems

	Kai Richter (SymTAVision GmbH)
Technical role(s) within ArtistDesign	Formal Performance Analysis and Optimization of Embedded Systems, Reliable System Integration, Early Architecture Exploration

	Dr. Arne Hamann (Robert Bosch GmbH)
Technical role(s) within ArtistDesign	Automotive Software Architectures

	Matthias Gries (Intel Germany)
Technical role(s) within ArtistDesign	Microprocessor Technology Lab, new computer architecture for embedded systems

	Rune Domsteen (Prevas A/S)
Technical role(s) within ArtistDesign	Embedded systems platform development

	Bjørn Sand Jensen (Bang & Olufsen ICEpower)
Technical role(s) within ArtistDesign	Execution platforms for audio signal processing

	Dr. Valter Bella (Telecom Italia Lab)
Technical role(s) within ArtistDesign	Architecture and Design of Wireless Sensor Networks and Embedded Systems for Ambient Intelligence

4.3 Affiliated Academic Partners

	Ass. Professor Dimitrios Soudris (NTUA/ formerly DUTH) www.microlab.ntua.gr www.ee.duth.gr
Technical role(s) within ArtistDesign	Collaboration with IMEC vzw.and contribution to the Hardware Platforms and MPSoC cluster and the Software Synthesis, Code Generation and Timing Analysis cluster.
Research interests	Dimitrios Soudris received his Diploma in Electrical Engineering from the University of Patras, Greece, in 1987. He received the Ph.D. Degree in Electrical Engineering, from the University of Patras in 1992. He is currently working as Assistant Professor in Electrical and Computer Engineering, National Technical University of Athens (NTUA), Greece. His research interests include low power design, parallel architectures, embedded systems design, and VLSI signal processing. He was leader and principal investigator in numerous research projects funded from the Greek Government and Industry as well as the European Commission (ESPRIT II-III-IV and 5th, 6th and 7th IST). He is a member of the IEEE, the VLSI Systems and Applications Technical Committee of IEEE CAS and the ACM.
Role in leading conferences/journals/etc in the area	Dimitrios Soudris has (co-)authored over 180 papers in international journals and conferences, and has coauthored and edited 4 text books. He has served as General Chair and Program Chair for PATMOS' 99 and 2000 and General Chair IEEE/CEDA VLSI-SOC 2008. He received an award from INTEL and IBM for the project results of LPGD #25256 (ESPRIT IV) and 4th position in ASP-DAC 2005 Design Contest for AMDREL IST-34793.
Notable past projects	LPGD project Design of a low power GFSK/GMSK modulator/demodulator for DECT receivers. AMDREL project Development of dynamic memory management design methodologies for emebedded syetems. Design of a low energy FPGA and a software supported design flow.
Awards / Decorations	Dimitrios Soudris received an award from INTEL and IBM for the project results of LPGD #25256 (ESPRIT IV) and 4th position in ASP-DAC 2005 for AMDREL IST-34793.
Further Information	Dimitrios Soudris is also member at the Institute of Communications and Computer Systems

	Prof. David Atienza (EPFL, Switzerland, and Complutense University of Madrid, Spain) http://esl.epfl.ch/
Technical role(s) within ArtistDesign	Collaboration with IMEC vzw.and contribution to the Hardware Platforms and MPSoC cluster and the Software Synthesis, Code Generation and Timing Analysis cluster.
Research interests	David Atienza received his MSc and PhD degrees in Computer Science from Complutense University of Madrid (UCM), Spain, and Inter-University Micro-Electronics Center (IMEC), Belgium, in 2001 and 2005, respectively. Currently he is Professor and Director of the Embedded Systems Laboratory (ESL) at Ecole Polytechnique Fédérale de Lausanne, Switzerland, and Adjunct Professor at the Computer Architecture and Automation Department of UCM. His research interests focus on design methodologies for high-performance embedded systems and Systems-on-Chip (SoC), including new thermal management techniques for Multi-Processor SoCs, dynamic memory management and memory hierarchy optimizations for embedded systems, novel architectures for logic and memories in forthcoming nano-scale electronics, Networks-on-Chip interconnection design, and low-power design of embedded systems.
Role in leading conferences/journals/etc in the area	In these fields, David Atienza is co-author of more than 90 publications in prestigious journals and international conferences, such as, IEEE TCAD, IEEE Micro, IEEE T-VLSI Systems, ACM TODAES, Elsevier-Integration: The VLSI Journal, DAC, ICCAD, DATE, ASP-DAC, etc. Also, he is part of the Technical Program Committee of the DATE, ICCAD, GLSVLSI, VLSI-SoC, RTAS, SBCCI and PATMOS conferences, and Associate Editor of IEEE Transactions on CAD (in the area of System-Level Design) and Elsevier Integration: The VLSI Journal. He is the general chair of VLSI-SoC 2010 and organizer of several conferences including GLSVLSI ‘09, ISVLSI ‘09 and SBCCI ’09.
Notable past projects	MDDTNSB-B22: “Materials, Devices and Design Technologies for Nanoelectronic Systems Beyond 22 nm CMOS” project Development of reliability-aware design methodologies for emerging nano-scale electronics. CMOSAIC project Design of design 3D stacked processing architectures with interlayer cooling. TIN2005-ARCHITECT project HW/SW technologies for the design of high-performance processing systems

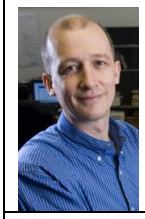
Awards / Decorations	David Atienza received the nomination as co-author for the "2004 DAC Best Paper Award" and the "2006 ICCAD Best Paper Award". In September 2008 he was named IEEE Young Gold Member Coordinator in the area of EDA.
Further Information	Since 2008, he an elected member of the Executive Committee of the IEEE Council of Electronic Design Automation (CEDA).

	Associate Professor Per Gunnar Kjeldsberg (NTNU) www.iet.ntnu.no/en
Technical role(s) within ArtistDesign	Collaboration with IMEC vzw.and contribution to the Hardware Platforms and MPSoC cluster and the Software Synthesis, Code Generation and Timing Analysis cluster.
Research interests	Per Gunnar Kjeldsberg received his Sivilingeniør degree (MSc) in electrical engineering in 1992 from the Norwegian Institute of Technology. In 2001 he received the degree of Doktor ingeniør (PhD) from the same institution (now Norwegian University of Science and Technology, NTNU). During his doctoral studies, he focused on storage requirement estimation and optimization for data intensive applications. The research was performed in close cooperation with IMEC, in Leuven, Belgium, where he was a visiting researcher for nine months in all. His research interests are embedded hw/sw systems, with a focus on multi-media and digital signal processing applications. Between October 2005 and June 2006, Kjeldsberg was a visiting researcher at University of California, Irvine, Center for Embedded Computer Systems.
Role in leading conferences/journals/etc in the area	Kjeldsberg has (co-)authored a large number of conference and journal papers, and has been coauthor of a book in his field of interest. He is frequently used as reviewer for several international journals and conferences.
Notable past projects	CUBAN project Co-optimized Ubiqutious Broadband Access Networks with focus on cross-layer optimized implementation of DSP algorithms. CoDeVer/Embla Codesign, verification, and languages for embedded systems in close cooperation with industry partners
Further Information	Between 1992 and 1996 Kjeldsberg worked as a design engineer at Eidsvoll Electronics, designing communication control equipment based on embedded hw/sw solutions. Currently he is an Associate Professor at the Department of Electronics and

	Telecommunications, NTNU. Here he teaches several extensive undergraduate and graduate courses, and supervises a number of students at master and PhD level. Kjeldsberg is and has been a member of the board of directors both at the Faculty and in private companies.

4.4 Affiliated International Partners

	Prof. Krishnendu (Krish) Chakrabarty, Department of Electrical and Computer Engineering, Duke University, USA
Technical role(s) within ArtistDesign	Collaboration with DTU on microfluidics-based biochips. Contributions to the Hardware Platforms and MPSoC cluster.
Research interests	Design and test of system-on-chip integrated circuits, microfluidics-based biochips (digital microfluidics, microelectrofluidics), and wireless/sensor networks.
Role in leading conferences/journals/etc in the area	He is an Editor of the Journal of Electronic Testing: Theory and Applications (JETTA), an Associate Editor of IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on VLSI Systems, IEEE Transactions on Biomedical Circuits and Systems, and ACM Journal on Emerging Technologies in Computing Systems. He serves on the editorial board of IEEE Design & Test of Computers. During 2006-2007, he served as an Associate Editor of IEEE Transactions on Circuits and Systems I, and before that as an Associate Editor of IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing.
Awards / Decorations	Prof. Chakrabarty is currently serving as an ACM Distinguished Speaker. He served as a Distinguished Visitor of the IEEE Computer Society for 2005-2007, and a Distinguished Lecturer of the IEEE Circuits and Systems Society for 2006-2007. He is also a recipient of the Humboldt Research Fellowship, awarded by the Alexander von Humboldt Foundation, Germany, in 2003.
Further Information	http://people.ee.duke.edu/~krish/

	Assist. Prof. Patrick Schaumont, Department of Electrical and Computer Engineering, Virginia Tech, USA
Technical role(s) within ArtistDesign	Collaboration with DTU on hardware description languages for MPSoC platforms. Contributions to the Hardware Platforms and MPSoC cluster.
Research interests	Design methods and architectures for secure embedded systems.
Further Information	http://www.ece.vt.edu/schaum/

5. Internal Reviewers for this Deliverable

Prof. Paul Pop (Technical University of Denmark)

Prof. Bengt Jonsson (Uppsala University)