IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Workpackage Progress Report for Year 1

# Jointly-executed Programme of Integrating Activities (JPIA) Report

With input from all clusters.

Workpackage Leader:

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*Policy Objective (abstract)*

Each ArtistDesign research activity has work within both the JPIA and the JPRA workpackages. The JPIA activities are carried out on a global, NoE level, transcending the clusters. They form the supporting background for integration of the NoE, and are executed in phase and in interplay with the JPRA research activities. For instance, funds for staff mobility will be allocated taking into account the needs for research.

The activities listed here will promote integration of geographically dispersed teams. All these activities will have long-lasting effects, well beyond the duration of the initial EC funding.

These activities include Joint Technical Meetings, Staff Mobility and Exchanges, Tools and Platforms.

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# 1. Overview of the Workpackage

## *1.1 ArtistDesign Participants and Affiliated Partners*

Each ArtistDesign research activity contributes to achieving both research and integration goals. Thus, each has work within both the JPIA and the JPRA workpackages, and all partners and affiliated partners participate in the Joint Programme of Integration Activities.

## *1.2 Starting Date, and Expected Ending Date*

These activities are intimately related to the JPRA (Joint Programme of Research Activities) and run for the entire duration of the NoE.

## *1.3 Policy Objective*

The JPIA activities are carried out on a global, NoE level, transcending the clusters. They form the supporting background for integration of the NoE, and are executed in phase and in interplay with the JPRA research activities. For instance, funds for staff mobility will be allocated taking into account the needs for research.

The activities listed here will promote integration of geographically dispersed teams. All these activities will have long-lasting effects, well beyond the duration of the initial EC funding.

These activities include Joint Technical Meetings, Staff Mobility and Exchanges, Tools and Platforms.

# 2. Joint Technical Meetings

Joint Technical meetings aim to present, discuss and integrate the ongoing work, and exchange points of view with other teams. They also serve to identify future work directions.

They are often organized around the annual General Assembly and Review, or around some of the main conferences in the area (most of which are piloted by a majority of ArtistDesign partners).

Depending on the context and in particular on the maturity of the topics under discussion, these Joint Technical Meetings may be open to the public, or by invitation (which implicitly includes all interested ArtistDesign partners).

## *2.1 Modelling and Validation Cluster*

**Organization of the workshop**, **Veronique Bruyere and Jean-Francois Raskin.** "Automata and Verification", University of Mons-Hainaut, Belgium, August 25-26, 2008.

**Summer school: Movep 08:** Co-organization of the Movep school (http://www.univ-orleans.fr/movep2008/) about modelling and verifying parallel processes in June 2008, partially funded by Artist 2.

**RTSS08 track on Design and Verification of Embedded Real-Time Systems**, the 29th IEEE Real-Time Systems Symposium. Barcelona, Spain. November 30 - December 3, 2008. This is one of the four tracks of RTSS 2008.

The objective is to promote research on design and analysis, and verification of embedded real-time systems. It intends to cover the whole spectrum from theoretical results to concrete applications with an emphasis on practical and scalable techniques and tools providing the designers with automated support for obtaining high-quality software and hardware systems. A particular goal is to provide a forum for interaction between different research communities, such as scheduling, hardware/software co-design, and formal techniques. http://www.rtss.org

**Workshop : SafeCert 2008, International Workshop on the Certification of Safety-Critical Software Controlled Systems**, ETAPS 2008 Budapest, Hungary, 29 March, 2008, organized by TU Braunschweig and OFFIS.

The need for certification, like for instance in the rail sector, imposes the burden of not only validating a system, but also proving in a juridical sense, that the validation can be trusted. The major question addressed in the workshop was how to embed formal methods and tools in a seamless design process which covers several development phases and which includes an efficient construction of a safety case for the product.
http://safecert08.offis.de/

**Workshop FIT 2008: Foundation of Interface Theories** ETAPS 2008 Budapest, Hungary, 29 March, 2008, organized by CISS, Aalborg University and ITU, Copenhagen. Invited presentations from INRIA, Rennes, and Twente U.

Component-based design is widely considered as a major approach to developing systems in a time and cost effective way. Central in this approach is the notion of an interface. Interfaces summarize the externally visible properties of a component and are seen as a key to achieving

component interoperability and to predict global system behavior based on the component behavior. To capture the intricacy of complex software products, rich interfaces have been proposed. These interfaces do not only specify syntactic properties, such as the signatures of methods and operations, but also take into account behavioral and extra-functional properties, such as quality of service, security and dependability. Rich interfaces have been proposed for describing, e.g., the legal sequences of messages or method calls accepted by components, or the resource and timing constraints in embedded software. The development of a rigorous framework for the specification and analysis of rich interfaces is challenging. The aim of this workshop is to bring together researchers who are interested in the formal underpinnings of interface technologies.

**Workshop: 1st International Workshop on Model Based Architecting and Construction of Embedded Systems**
*Toulouse -- September 29th, 2008*

This ARTIST workshop is held in conjunction with MODELS 2008 as a follow-up workshop of the SVERTS and MARTE workshops organised in previous years, the objective of this workshop is to bring together researchers and practitioners interested in model-based software engineering for real-time embedded systems. We are seeking contributions relating to this subject at different levels, from modelling languages and semantics to concrete application experiments, from model analysis techniques to model-based implementation and deployment. Given the criticality of the application domain, we particularly focus on model-based approaches yielding efficient and provably correct designs. Concerning models and languages, we welcome contributions presenting novel modelling approaches as well as contributions evaluating existing ones. The organisers of this workshop are partners from the ASSERT and SPICES project; the ARTIST partners are CEA and Verimag.
http://www.artist-embedded.org/artist/ACES-MB-08.html

**Workshop SLA++P 2008: Model-driven High-level Programming of Embedded Systems European Joint Conference on Theory and Practice of Software ETAPS 2008**
*Budapest, Hungary – April 5th,* 2008

SLA++P is a workshop dedicated to synchronous languages and the model-driven high-level programming of reactive and embedded systems. Firmly grounded in clean mathematical semantics, synchronous languages are receiving increasing attention in industry ever since they emerged in the 80s. Lustre, Esterel, Signal are now widely and successfully used to program real-time and safety critical applications, from nuclear power plant management layer to Airbus air flight control systems. At the same time, model-based programming is making its way in other fields of software engineering, too, often involving cycle-based synchronous paradigms. The purpose of the SLA++P workshop is to bring together researchers and practitioners who work in the field of languages and tools for the model-driven development of embedded applications both in hardware and software. The workshop is not limited to synchronous approaches but open to other engineering design approaches with strong semantical foundations providing a way to go from a high-level description to provable executable code.
http://www.artist-embedded.org/artist/SLA-P-2008,1231.html

**Workshop : ACESMB 2008, 1st Int. Workshop on Model Based Architecting and Construction of Embedded Systems**
**ACM/IEEE 11th Int. Conf. on Model Driven Engineering Languages and Systems**
*Toulouse, France - September 29th, 2008*

New real-time systems have increasingly complex architectures because of the intricacy of the multiple interdependent features they have to manage. They must meet new requirements of reusability, interoperability, flexibility and portability. These new dimensions favour the use of an architecture description language that offers a global vision of the system, and which is particularly suitable for handling real-time characteristics. Due to the even more increased complexity of distributed, real-time and embedded systems (DRE), the need for a model-driven approach is more obvious in this domain than in monolithic RT systems. The purpose of this workshop is to provide an opportunity to gather researchers and industrial practitioners to survey existing efforts related to behaviour modelling and model-based analysis of DRE systems. This workshop sought contribution from researchers and practitioners interested in all aspects of the representation, analysis, and implementation of DRE system behaviour and/or architecture models.
http://www.artist-embedded.org/artist/ACES-MB-08.html

**Workshop : UML & AADL 2008**
**13th IEEE International Conference on Engineering of Complex Computer Systems**
*Belfast, Northern Ireland - April 2nd, 2008*

New real-time systems have increasingly complex architectures because of the intricacy of the multiple interdependent features they have to manage. They must meet new requirements of reusability, interoperability, flexibility and portability. These new dimensions favour the use of an architecture description language that offers a global vision of the system, and which is particularly suitable for handling real-time characteristics. Due to the even more increased complexity of distributed, real-time and embedded systems (DRE), the need for a model-driven approach is more obvious in this domain than in monolithic RT systems. The purpose of this workshop is to provide an opportunity to gather researchers and industrial practitioners to survey existing efforts related to behaviour modelling and model-based analysis of DRE systems. This workshop sought contribution from researchers and practitioners interested in all aspects of the representation, analysis, and implementation of DRE system behaviour and/or architecture models.
http://www.artist-embedded.org/artist/Topics,1199.html

## *2.2 Software Synthesis, Code Generation and Timing Analysis cluster*

**Course: Peter Marwedel, Rainer Leupers: Retargetable Compilation**

*Lugano, Switzerland, Feb. 25-29., 2008*

The course consisted of two parts: the first part (by Peter Marwedel) focused on memory-architecture aware compilation. The second part (by Rainer Leupers, RWTH Aachen) focused on processor retargetability. The course was supported by ALARI.

http://www.alari.ch

**Tutorial: Peter Marwedel, Embedded Systems in a Nutshell, Spring School on Knowledge Discovery in Ubiquitous Systems**,
*Porto, Portugal, March 2, 2008*

This tutorial provided a brief overview over specification techniques, hardware, scheduling and optimization of embedded systems for a community without any pre-existing knowledge on embedded systems.

http://www.kdubiq.org

**Tutorial: Rainer Leupers, Gerd Ascheid (RWTH Aachen), Wilfried Verachtert, Tom Ashby, Arnout Vandecappelle (IMEC): System-Level Design and Application Mapping for Wireless and Multimedia MPSoC Architectures**
**DATE 2008**
*Munich, Germany, March 10, 2008*

Advanced embedded devices such as multi-standard mobile terminals demand ever-increasing performance and energy efficiency. Simultaneously, a high degree of flexibility and programmability is required due to increasing software complexity and fast changing protocol and codec standards. This has led to the concept of MPSoC (Multi-Processor System-on-Chip) platforms. In many cases, MPSoCs are simply assembled in "best effort" manner from existing legacy IP components, and programming the platform presents a major bottleneck. As Moore´s Law permits us to enter the "many core" MPSoC area, what is needed is a systematic approach that builds on well-proven technologies, but also innovates with novel classes of electronic system-level (ESL) design automation tools.

This tutorial discussed several key questions with significant impact on the future of MPSoC: What are the MPSoC killer applications? Is homogeneous or heterogeneous architecture the right choice? What are the key tools, methodologies and programming models for successfully designing and programming MPSoC platforms? In the end, will there be only a few survivor platforms that everyone has to accept? Based on their extensive research and industry experience, the presenters provided their answers from a practical, application-oriented perspective.

http://www.date-conference.com/archive/conference/proceedings/PAPERS/2008/DATE08/PDFFILES/TUTORIALS.PDF

**Workshop: Software & Compilers for Embedded Systems (SCOPES) 2008**
*Munich, Germany – March 13-14, 2008*

SCOPES focuses on the software generation process for modern embedded systems. Topics of interest include all aspects of the compilation process, starting with suitable modelling and specification techniques and programming languages for embedded systems. The emphasis of the workshop lies on code generation techniques for embedded processors. The exploitation of specialized instruction set characteristics is as important as the development of new optimizations for embedded application domains. Cost criteria for the entire code generation and optimization process include runtime, timing predictability, energy dissipation, code size and others. Since today's embedded devices frequently consist of a multi-processor system-on-chip, the scope of this workshop is not limited to single-processor systems but particularly covers compilation techniques for MPSoC architectures.

In addition, this workshop puts a spotlight on the interactions between compilers and other components in the embedded system design process. This includes compiler support for e.g. architecture exploration during HW/SW codesign or interactions between operating systems and compilation techniques. Finally, techniques for compiler aided profiling, measurement,

debugging and validation of embedded software were also covered by this workshop, because stability of embedded software is mandatory.

SCOPES 2008 was the 11th workshop in a series of workshops initially called "International Workshop on Code Generation for Embedded Processors". The name SCOPES has been used since the 4th workshop. The scope of the workshop remains software for embedded systems with emphasis on code generation (compilers) for embedded processors.

SCOPES 2008 was organized by Heiko Falk from TU Dortmund and was held as DATE Friday Workshop. There were many discussions between cluster members at SCOPES (starting already on the eve before the sessions), at DATE and during an Artist2 meeting during the same week, making the entire week the key joint event in spring.

http://www.scopesconf.org/scopes-08

**Keynote: Rainer Leupers: ESL Design Technologies for Wireless and Multimedia MPSoC Architectures**
**3rd International Symposium on Industrial Embedded Systems (SIES 2008)**
*La Grande Motte, June 11-13, 2008*
http://www.lirmm.fr/SIES2008/

**Meeting: 1st Workshop on Mapping Applications to MPSoCs, 2008**
St. Goar*, Germany – June 16-17, 2008*

Objectives for the meeting: The goal of the ArtistDesign workshop was to identify requirements and partial solutions for the problem of mapping applications to MPSoCs. It was considered to be the starting point for more intensive cooperations in the ArtistDesign framework. Also, members of other projects (hipeac2, ACOTES) were invited.
Organizer: Peter Marwedel (TU Dortmund)
Other participants: there were a total of 37 participants.
Conclusions: The topic was partitioned into two related areas: mapping and code generation. Working groups were formed and it was agreed to have joint follow-up workshops.

http://www.artist-embedded.org/artist/Mapping-of-Applications-to-MPSoCs.html

**Meeting: Working Meeting IFIP 2.11 (Program Generation)**
**Passau***, Germany – Jun. 19-21, 2008*
Objectives for the meeting: General discussion on the future of program generation.
Organizer: Christian Lengauer (U. Passau)
Other participants: IFIP 2.11.

**Forum: 8th International Forum on Application-Specific Multi-Processor SoC, 2008**
*Aachen, Germany, 23 - 27 June 2008,*

MPSoC is a pluridisciplinary forum bringing together key R&D actors from the different fields required to design heterogeneous multiprocessor SoC (MPSoC). MPSoC '08, 8th event of the forum series, was held on 23-27 June 2008 at Château St. Gerlach (near Aachen) and was organized by ISS/SSS, RWTH Aachen University. Rainer Leupers from RWTH Aachen was one of the general co-charis of this premier event. The full week format and the quality of both attendees and speakers made MPSoC '08 a unique occasion for executives and senior managers to explore new ideas and refine strategic thinking. The program brought together key actors from IP, fabless, semiconductor, system houses and design industry to build a vision of the next step in integrated system design. More than 50 world class R&D speakers discussed fundamental and strategic issues to master multi-processor SoC design. This year's technical sessions presented strategic directions and state-of-the-art research, covering topics like MPSoC Architecture, MPSoC Application Platforms, MPSoC Programming, MPSoC

Design methodologies, etc. The detailed program and the slides from the speakers can be found in the event's website.

Organizer: Rainer Leupers, Heinrich Meyr (RWTH Aachen)

http://www.mpsoc-forum.org

**Workshop: 8th Int'l Workshop on Worst-Case Execution Time Analysis (WCET'08)**
*Prague, Czech Republic – July 1st, 2008*

The 8th International Workshop on Worst-Case Execution Time Analysis (WCET 2008) was held as a satellite event to the 20th Euromicro Conference on Real-Time Systems (ECRTS 2008). The goal of the workshop is to bring together people from academia, tool vendors and users in industry that are interested in all aspects of timing analysis for real-time systems. The workshop fosters a highly interactive format with ample time for in-depth discussions. It provides a relaxed forum to present and discuss new ideas, new research directions, and to review current trends in this area. The presentations are kept short to leave plenty of time for interaction of attendees.

The WCET 2008 event of this workshop has gained on popularity, it had 45 registered participants. This tendency may be interpreted that the real-time community becomes increasingly aware of the importance of WCET analysis. The workshop program included four regular sessions with 13 talks on WCET analysis. Additionally an invited talk on timing analysis at system level was given by Prof. Rolf Ernst and the current results of the WCET Tool Challenge 2008 were presented by the organizer, Niklas Holsti.

http://www.artist-embedded.org/artist/WCET-08.html

**Keynote: Constructing Time-Critical Embedded Systems: Use Your Intelligence before Runtime**
**6th Workshop on Intelligent Solutions in Embedded Systems**

*Regensburg, Germany – July 10-11, 2008*

This presentation, given by Peter Puschner, examined the complexity of contemporary hardware and software architectures and demonstrated how the sophisticated mechanisms used lead to difficulties in understanding and analysing the timing of embedded real-time applications. It was argued that a new trend towards simplicity is needed that avoids speculation and minimizes the number of dynamic decisions taken at runtime. Following these principles one can eliminate timing variations, system timing becomes easy to understand, and proofs for temporal correctness turn out to be almost trivial.

http://fbim.fh-regensburg.de/~wises08/index.htm

**Tutorial: Timing Analysis and Timing Predictability**
**Embedded Networked Systems: Theory and Applications**

*Heraklion, Crete – July 21–25, 2008*

The 2008 Lectures in Computer Science of the Onassis Foundation were dedicated to theory and applications of Embedded Systems. Among the talks by leading researchers was a two-part tutorial by Reinhard Wilhelm on Timing Analysis and Timing Predictability.

http://www.forth.gr/onassis/lectures/2008-07-21/lecturers.html

**Invited Course: Peter Marwedel, Heiko Falk, Embedded Systems with Emphasis on the Exploitation of the Memory Hierarchy**

**Advanced Institute of Information Technology**
*Seoul, Korea – August 11-15, 2008*

The goal of this course is to provide an overview over key areas in embedded system design which should be taught at Universities. After attending the course, the attendees should be able to compare different approaches to embedded system design education and their advantages and limitations. The attendees will also become familiar with the contents of a course on embedded system design which aims targets second or third year students. The course should enable attendees to design the structure of embedded system education at their universities. In the last third of the course, attendees will be introduced to research topics regarding embedded system optimization. In particular, this last third will address the so-called memory wall problem (the problem resulting from the small performance improvements of memories). This problem is frequently seen as the key problem for further performance enhancements of future systems. This material would be appropriate for an advanced course in embedded system design.

Peter Marwedel and Heiko Falk from TU Dortmund lectured this one-week course for Korean professors (CS and EE) after an invitation by the (South) Korean Advanced Institute of Information Technology.

http://ttt.aiit.or.kr

**Tutorial: Peter Marwedel: Memory architecture aware compilation for Embedded Systems**
**Artist South American Summer School**
*Florianopolis, Brazil, Aug. 25.-29., 2008*

The tutorial focused on compilation techniques exploiting descriptions of the memory architecture.

http://www.artist-embedded.org/artist/Objectives,1365.html

**ARTIST2 Summer School 2008 in Autrans:**

*Autrans, France, Sept. 8th-12th, 2008*

- **Tutorial/Invited Talk: Peter Marwedel, Heiko Falk: Memory architecture aware compilation**
  This talk gave an overview over compilation for scratchpad memories and linked it to worst case execution time aware compilation.
- **Tutorial/Invited Talk: Reinhard Wilhelm: Timing Analysis and Timing Predictability**
  This talk gave an overview over recent techniques for timing analysis.

http://www.artist-embedded.org/artist/ARTIST2-Summer-School-2008.html

**Invited talk: Peter Marwedel: Mapping of Applications to MPSoCs**
**4th Compiler Assisted SoC Assembly Workshop (CASA08)**
*Atlanta, USA – Oct. 19th, 2008*

The talk summarized the presentations of the "1st workshop on the mapping of applications to MPSoCs" for a wider audience.

http://www.esweek.org/

**Workshop: 4th Workshop on Embedded Systems Education, 2008**
*Atlanta, US, – October 23rd, 2008*

Embedded system education is still a very young area and frequently restricted to teaching the details of microcontroller programming. A long-term objective of this workshop is to stimulate the introduction of broader curricula. Also, there will be more emphasis on publishing the results of the workshop online and in journals.

http://www.esweek.org/

**Meeting: Working Meeting on Mapping Applications to MPSoCs (*Fall Activity meeting*).**
Düsseldorf, *Germany – Nov. 27th-28th, 2008*
Objectives for the meeting: The goal of the ArtistDesign meeting was to intensify the discussions started at the Rheinfels workshop and to advance the cooperation between the partners.
Organizer: Peter Marwedel (TU Dortmund)
Other participants: there were a total of 25 participants.
Conclusions: Details of the cooperation between the partners were fixed.

**Keynote: Rainer Leupers: Advanced MPSoC design technologies in the UMIC project J-CING (Japan – CoWare Innovators Group) 2007**
*Tokyo, Nov. 30th, 2007*
http://www.coware.co.jp/J-CING/keynote2.html

## *2.3 Operating Systems and Networks cluster*

**Meeting: APRES 2008: Workshop on Adaptive and Reconfigurable Embedded Systems**
*St. Louis, MO, USA – April 21st, 2008*

Objectives for the meeting: The purpose of the workshop was to discuss new and on-going research that is centered on the idea of adaptability as first class citizen and consider the involved tradeoffs. The workshop provided an open forum to discuss ideas and approaches, and intended to give the attendees a chance to discuss them in a relaxed environment. The target audience included people from academia, tool vendors, system suppliers, and users in industry interested in the all aspects of the mentioned topics. The workshop was based on presentations of selected works with sufficient time for feedback from the audience and discussions. Participants have been encouraged to submit short papers, workin-progress reports, or position papers.

Organizers:

- Luis Almeida, Univ. of Aveiro, Portugal
- Sebastian Fischmeister, Univ. of Pennsylvania, USA
- Insup Lee, Univ. of Pennsylvania, USA
- Julian Proenza, Univ. of the Balearic Islands, Spain

URL: http://www.artist-embedded.org/artist/APRES08.html

**Meeting: Training Course on Real-Time Kernels for Microcontrollers: Theory and Practice**
*Pisa, Italy – June 23-25, 2008*

Objectives for the course: The course was aimed at:

1. providing the fundamentals concepts of real-time computing systems, including scheduling, resource management and timing analysis;

2. introducing the OSEK/VDX standards, taking as a reference implementation the Erika Enterprise kernel;
3. showing how to apply such concepts in practice, with examples based on the Altera Nios II and the Microchip dsPIC DSC microcontrollers;
4. teaching participants how to develop simple control applications using Erika Enterprise with code generation from functional models.

Organizers:

- Giorgio Buttazzo - Scuola Superiore Sant'Anna, Italy
- Paolo Gai, Evidence Srl
- Tullio Facchinetti, University of Pavia, Italy
- Ettore Ricciardi – ISTI-CNR, Pisa

URL: http://www.artist-embedded.org/artist/Real-Time-Kernels-for.html

**Meeting: Operating Systems and Networks**
*Pisa, Italy – October 2-3, 2008*

Objectives for the meeting: The purpose of the meeting was to refine the research objectives of the cluster on Operating Systems and Networks and coordinate the collaboration among the different groups. Discussed topics included: architecture effects on worst-case execution times, taxonomy of resources, real-time networks, and real-time and control issues.

Organizers:

- Giorgio Buttazzo - Scuola Superiore Sant'Anna, Italy
- Alan Burns – University of York, UK
- Luis Almeida, Univ. of Aveiro, Portugal

**Meeting: OSPERT 2008 - Fourth International Workshop on Operating Systems Platforms for Embedded Real-Time Applications**
*Prague, Czech Republic – July 1st, 2008*

Objectives for the meeting: This workshop was intended as a forum for researchers and practitioners of RTOS to discuss the recent advances in RTOS technology and the challenges that lie ahead. The workshop consisted of submitted papers as well as invited presentations about academic state-of-the-art and industrial state-of-practice within the area of real-time operating systems architectures and services.

Organizers:

- Jim Anderson, University of North Carolina, Chapel Hill, USA

URL: http://www.cs.unc.edu/~anderson/meetings/ospert08/OSPERT.html

**Meeting: WCET 2008: Worst Case Execution Time Analysis**
*Prague, Czech Republic – July 1st, 2008*

Objectives for the meeting: The goal of the workshop was to bring together people from academia, tool vendors and users in industry interested in all aspects of timing analysis for real-time systems. The workshop fostered a highly interactive format with ample time for in-depth discussions. It provided a relaxed forum to present and discuss new ideas, new research

directions, and to review current trends in this area. The presentations were kept short to leave plenty of time for interaction of attendees.

Organizers: Jim Anderson, University of North Carolina, Chapel Hill, USA

URL: http://www.cs.unc.edu/~anderson/meetings/ospert08/OSPERT.html

**Meeting: RTN 2008: Real-Time Networks**
*Prague, Czech Republic – July 1st, 2008*

Objectives for the meeting: The Real Time Networks (RTN, formerly RTLIA) workshop was the seventh on the series of workshops that started at the 2002 ECRTS conference. RTN focuses on the current technological challenges of developing communication infrastructures that are real-time, reliable, pervasive and interoperable. The goal of this workshop was to bring together people from industry and academia that are interested in all aspects of real-time communication. The workshop provided a relaxed forum to present and discuss new ideas, new research directions and to review current trends in this area.

Organizers: Anis Koubâa, IPP-HURRAY Research Group, ISEP-IPP, Portugal.

URL: http://www.hurray.isep.ipp.pt/rtn08/index.php

**Meeting: Course on Real-Time Control Systems: Theory and Practice**
*Pisa, Italy – April 2-18, 2008*

Objectives: The objective of the course was to introduce classical control notions applied to real-time computing systems. Topics included Discrete time systems, Exact Real-time simulation, period selection, delayed models, controllability, observability and performance of discrete time controllers, real-time computing of control systems, timing and implementation, control of real-time systems, event-driven systems, scheduling of event driven systems.

Organizers:

- Giorgio Buttazzo - Scuola Superiore Sant'Anna, Italy
- Manel Velasco – University of Catalonia, Spain

**Meeting: A Multi-Processor Architectural Simulator (MPARM)**
*Pisa, Italy – November 5-6, 2008*

Objectives: The objective of the meeting was to discuss how to use the MPARM simulator developed at the University of Bologna for evaluating the effects of sheduling and cache memories on task execution times. Martino Ruggiero, who participated in the development of the simulator, gave a tutorial to explain the MPARM architecture, the available hardware modules, their profiling features, possible power models, how add new modules to MPARM, the software development flow, the application profiling, debugging features, the operating system interface, the communication library, and a few examples.

Organizers:

- Giorgio Buttazzo - Scuola Superiore Sant'Anna, Italy
- Luca Benini – University of Bologna, Italy
- Martino Ruggiero – University of Bologna, Italy

## *2.4 Hardware Platforms and MPSoC cluster*

**Workshop : Industrial Collaboration**
*Copenhagen, Denmark – June 5-6, 2008*
Objectives for the meeting: Main objective is to get the affiliated industrial partners of the cluster involved in the activities of the cluster.
Organizer: Jan Madsen (DTU)
Other participants: Matthias Gries (Intel), Daniel Karlsson (Volvo), Anders Tranberg-Hansen (B&O ICEpower), Michael R. Hansens (DTU), Sven Karlsson (DTU), Michael R. Boesen (DTU), Peter Sørensen (DTU), Elena Maftei (DTU), Petru Eles (LiU), Soheil Samii (LiU), Jakob Rosen (LiU), Rolf Ernst (TUBS), Simon Schliecker (TUBS), Simon Perathoner (ETHZ), Clemens Moser (ETHZ), Mamagkakis Stylianos (IMEC), Renaud De Landtsheer (IMEC), Luca Benini (UNIBO), David Brunelli (UNIBO), Thierry Collette (CEA), Huimin She (KTH).
Conclusions : The meeting consisted of three parts ; an industrial session, where the industrial partners presented the challenges of Embedded systems design as seen from their perspective. A Partner session, where each Partner presented their current research related to the cluster. Finally, a discussion session with the topic interaction with companies. The conclusion from the discussions was that it is very difficult to have the companies reveal their design flows, which would be of great interest for the academic partners. What would be possible, is to 1) have the companies defining industry cases for academia to study, and 2) to have design flows developed in academia to be reviewed by industry partners.

**Meeting : Cluster meeting on Analysis**
*Munich, Germany – March , 2008*
Objectives for the meeting: Short status and planning meeting for the Analysis activity.
Organizer: Jan Madsen (DTU)
Other participants: Matthias Gries (Intel), Petru Eles (LiU), Rolf Ernst (TUBS), Mamagkakis Stylianos (IMEC), Luca Benini (UNIBO), Thierry Collette (CEA), Axel Jantsch (KTH)
Conclusions : Main conclusion was to have a joint cluster and industry meeting in Copenhagen late spring or early summer. Also possible exchange visits were discussed.

**Meeting : Cluster meeting on Design**
*Munich, Germany – March , 2008*
Objectives for the meeting: Short status and planning meeting for the Design activity.
Organizer: Luca Benini (UNIBO)
Other participants: Petru Eles (LiU), Rolf Ernst (TUBS), Mamagkakis Stylianos (IMEC), Jan Madsen (DTU), Thierry Collette (CEA), Axel Jantsch (KTH)

**Workshop : Tools and Design Methodologies**
*Eindhoven, The Netherlands – March, 2008*
On March 27, 2008, a two day workshop tool place in TU/e where the ICD, IMEC, DUTH/ICCS and TU/e presented their individual tools and design methodologies. A common design and tool flow was drafted as a result of the workshop.

**Workshop : IMEC Tools**
*Athens, Greece – May, 2008*
During May 9, 2008, a one day workshop took place in ICCS, where IMEC researcher Dr. Stylianos Mamagkakis presented and discussed with the main ICCS and DUTH researchers the the MPSoC parallelization (MPA) and memory hierarchy mapping (MH) tools of IMEC

**Meeting: Scenario Cluster**
*Leuven, Belgium – April and November, 2008*
There were 2 meetings of the scenario cluster in April'08 and November'08 taking place in IMEC and Uni. Gent, respectively. The interaction focused on further improvements of the scenario extraction, identification, exploitation, switching and calibration steps.

**Meeting : Bologna**
*Bologna, Italy – March 6-7, 2008*
Objectives for the meeting: Discussing dynamic adaptation to changes in system behaviour and requirements. Use of appropriate resource abstractions and interfaces.
Organizer: University Bologna
Other participants: University Bologna, SSSA, ETHZ, University Dortmund, University Saarland.
Conclusions : The meeting lead to a cooperation between SSSA and ETHZ in the area of dynamic adaptations and hard real-time systems.

**Meeting : Application Model**
*Bologna, Italy – June 5, 2008*
Objectives for the meeting: Discussing an appropriate application model that serves as a basis for the joint work on adaptive changes.
Organizer: University Bologna
Other participants: University Bologna, SSSA, ETHZ.
Conclusions : A joint application model has been defined. It is the basis of the ongoing cooperation between University Bologna, SSSA (PISA) and ETHZ (Zurich).

**Meeting : BIP – DOL**
*Grenoble, France – September 15-16, 2008*
Objectives for the meeting: The main goal of this meeting was to define the collaboration between ETHZand VERIMAG on coupling DOL (Distributed Operation Layer) and BIP (Behavior Interaction Priority) frameworks.
Organizer: Verimag
Other participants: Veriamg, ETHZ
Conclusions : The main outcome of this meeting was the definition of a design flow as well as establishing the basic modeling aspects.

## *2.5 Design for Adaptivity in Embedded Systems (Transversal Integration WP)*

**Meeting: Lund May 13-14, 2008**
*City, Country – Lund, Sweden*
Objectives for the meeting: Provide the kick-off meeting for this activity. Present the work that is currently done by the individual partners. Discuss the ontology of adaptivity in embedded systems. Plan the work for the coming year.
Organizer: Karl-Erik Årzén (ULUND)
Other participants: Mälardalen, IMEC, York, SSSA, Aveiro, CEA, TUKL, NXP, Ericsson, KTH, IPP, UPC, UPM, UCatania (20 persons in all)
Conclusions

- The interpretation of the work adaptivity can be very wide depending on the community. Hence there is substantial need for strong definitions of the terminology used. This was initiated at the meeting

- The next formal meeting for the entire activity will be held in at SSSA, Pisa, 2-3 April 2009.
- A Wiki will be defined to act both as the platform for the internal work within the activity as well as the interface to the rest of the community. The wiki has been set up and is currently being filled with content. (http://www2.control.lth.se/ArtistAdapt/)
- It was decided to use the APRES workshop series to promote the work within the activity. It was decided to aim for organizing the next instance of APRES (Workshop on Adaptive and Reconfigurable Embedded Systems) in connection with ECRTS in Dublin in July 2009.
- Existing collaborations among the partners were identified. They include FRESCOR, ACTORS, MOSART, REALITY, and PREDATOR.

Meeting web: http://www.artist-embedded.org/artist/Design-for-Adaptivity.html

**Meeting : Bologna March 6-7, 2008**
*City, Country – Bologna, Italy*
Objectives for the meeting: Discussing dynamic adaptation to changes in system behavior and requirements. Use of appropriate resource abstractions and interfaces.
Organizer: University Bologna
Other participants: University Bologna, SSSA, ETHZ, University Dortmund, University Saarland.
Conclusions : The meeting lead to cooperation between SSSA and ETHZ in the area of dynamic adaptations and hard real-time systems.

**Meeting : Application Model, June 5, 2008**
*City, Country – Bologna, Italy*
Objectives for the meeting: Discussing an appropriate application model that serves as a basis for the joint work on adaptive changes.
Organizer: University Bologna
Other participants: University Bologna, SSSA, ETHZ.
Conclusions : A joint application model has been defined. It is the basis of the ongoing cooperation between University Bologna, SSSA (PISA) and ETHZ (Zurich).

**Meeting : BIP – DOL, 15$^{th}$-16$^{th}$ Sept. 2008**
*City, Country – Grenoble, France*
Objectives for the meeting: The main goal of this meeting was to define the collaboration between ETHZ and VERIMAG on coupling DOL (Distributed Operation Layer) and BIP (Behavior Interaction Priority) frameworks.
Organizer: Verimag
Other participants: Verimag, ETHZ
Conclusions : The main outcome of this meeting was the definition of a design flow as well as establishing the basic modeling aspects.

## *2.6 Design for Predictability (Transversal Integration WP)*

**Meeting: ArtistDesign meeting mapping of applications for MPSoCs**
*Düsseldorf, Germany; date: 27th and 28th of November 2008*:
Within the frame of this ArtistDesign meeting which addresses the mapping of applications to MPSoCs, ETHZ presents an overview and a SW demonstration of the Distributed Operation Layer framework.

## *2.7 Integration Driven by Industrial Applications (Transversal Integration WP)*

**Meeting: Workshop: From Embedded Systems to Cyber-Physical Systems: a Review of the State-of-the-Art and Research Needs, RTAS in St. Louis at the Renaissance Grand Hotel Saint Louis, USA, April 21st, 2008**

*Objectives for the meeting:*

To presentment an overarching view of methodologies and theories for the design of embedded and critical systems as it has emerged in the past five years and discuss the future in terms of the extension of the notion of embedded systems to Cyber-Physical Systems (CPS).

*Organizers:* Tom Henzinger (Berkeley, EPFL), Alberto Sangiovanni-Vincentelli (Berkeley, PARADES Roma), Jonathan Sprinkle (University of Arizona), Janos Sztipanovits (Vanderbilt)

*Other participants:* Werner Damm, OFFIS, EPFL, Roberto Passerone, U. Trento. Henzinger and Sangiovanni-Vincentelli were among the organizers of the meeting. All presented talks in their area of expertise and reflected the research work carried out in COMBEST and ArtistDesign.

*Conclusions:* In the overview of the present status of the discipline, the workshop addressed heterogeneous system composition, design methods based on abstraction and refinement, interface theories, mapping of abstract entities to implementation platforms and industrial applications. The presentations also featured industry representatives who gave their perspective of what are the gaping holes in the state of the art in their business segment and how to bridge academic accomplishments with industrial practice. The discussion about the extension of the theories and methodologies to the new generation of CPS reviewed the necessary steps and a possible roadmap for research. The discussion included public research organizations. European Community representatives provided the state-of-the-art and the research initiatives on embedded systems in the EU..Alberto Sangiovanni Vincentelli summarized the meeting and the conclusions. He called for the next steps in the EU-US collaboration to be coordinated between NSF and the EU research agencies.
http://ike.ece.cmu.edu/twiki/bin/view/CpsNCO/WebHome

**Meeting: Industrial Integration: Industrial Challenges and Design Drivers Selection, PARADES Offices, Rome, November 12 and 13, 2008**

*Objectives for the meeting:*

- To review with industrial partners and affiliates the challenges to be faced in embedded system design in several vertical industrial segments;
- Based on these inputs, to select the design drivers for the integration activity;
- To plan for next year activities choosing the leaders for each vertical industrial segment.

*Organizers*: Alberto Sangiovanni Vincentelli (PARADES), Ed Brinksma (ESI)

*Other participants*: 33 participants of which 27 were representing Artist Design partners (PARADES, OFFIS, ESI, University of Trento, University of Bologna, TU Braunschweig, TU Dortmund, Universidad de Cantabria, TU Wien, IMEC, Uppsala University, TU Denmark). Others were industrial participants working in international corporations (UTC) or in Artist Design affiliated companies (Danfoss, Phillips, Thales, Carmeq, Real-Time-at-Work and IAI). The participants are available on the Artist Design Web site.

*Conclusions:* After the two-day presentations, the following areas were selected as design drivers for the activity of the industrial integration transversal activity:

1. Transportation with emphasis on automotive and avionic. These two areas were combined since from a design flow point of view they shared enough common features to warrant a unified approach. The link to CESAR was emphasized as the Artemis project had exactly the same characteristics.OFFIS will drive and coordinate the activities in this area.
2. Health care with emphasis on equipments. Health care is one of the core research areas of the EU for the foreseeable future. Since we are using the applications as drivers, we decided to focus on well-developed products to demonstrate the use of Artist Design technology. ESI will drive and coordinate this activity.
3. Zero-energy buildings. This area is a growth domain for traditional industry such as construction, HVAC, monitoring and energy optimization. There is a strong push from the EU and the technical problems are challenging. The level of understanding of the academic partners in this domain is limited as it is a new area to most of them. PARADES will lead this effort.

We recommended having one-two yearly meetings per area at topical conferences and one-two plenary meetings at the annual Artist Design meeting and at one of the topical conferences such as Formal Methods where it is likely that most of the partners and a substantial contingent from industry will be present.
http://www.artist-embedded.org/artist/Agenda,1532.html

# 3. Staff Mobility and Exchanges

*From the Description of Work:*
Staff Mobility and Exchanges between teams are essential for integration within and beyond the NoE, including mobility of students and/or researchers, between core teams, or between core teams and affiliated teams.

Mobility should be justified by and refer to involvement in an activity from the JPRA or JPIA, or one of the following: co-funded scholarships with industry; exchange of students and personnel within the consortium.

## *3.1 Modelling and Validation Cluster*

Alberto Sangiovanni Vincentelli has visited VERIMAG. INRIA and VERIMAG researchers spent significant amount of time visiting Rome to carry out research work in the area of methodologies and tools for embedded system design. Alberto Ferrari has visited Grenoble and other locations to maintain connectivity with the rest of the research community.

Dr. Pierre America participated and provided a presentation during the ArtistDesign workshop Intercluster activity: Integration Driven by Industrial Applications. Title of his presentation was Embedded Systems in Healthcare.

Dr. Ir. Twan Basten participated in the ArtistDesign WFCD 2008 workshop, held on 19th of October during the Embedded Systems Week.

Dr. Michael Borth participated and provided a presentation during the ArtistDesign Workshop Intercluster activity: Integration Driven by Industrial Applications, 13-14 November, Rome. His presentation was titled: Future Car Platform Development.

Kim Larsen was awarded Doctor Honoris Causa at ENS Cachan acknowledging his regular collaboration with LSV. Kim Larsen also spent a month as an invited professor at LSV.

From Aalbrog to CFV (Brussels): one week visit of Prof. Kim Larsen to the team of Prof. JF Raskin.

From ENS Cachan to Aalborg: one week visit of Patricia Bouyer and Nicolas Markey.

From Aalborg to ENS Cachan: one week visit of Ulrich Fahrenberg.

Ghassan Oreiby wil after his position as PhD student at LSV go to Aalborg University for a post doc position starting November 1, 2008.

EPFL + CFV collaborated on efficient algorithms for classical decision problems in automata theory (emptiness, language inclusion, universality), with application to the model-checking of linear time properties.

EPFL + LSV collaborated on games with imperfect information. We work on building a tool to solve such games, with parity objectives.

From INRIA to LSV and CVF (Mons): one week visit of Nathalie Bertrand in each place on probabilistic semantics for timed automata.

From CFV (Brussels) to Inria Rennes: two month visit of Gabriel Kalyon and one month visit of Thierry Massart.

From INRIA to CFV (Brussels) one week visit of T. Legall to ULB followed by post-doc started in September 2008.

From ESI to Inria Rennes: one week visit of Jan Tretmans to Inria for participation to the summer school EJCP.

Uppsala has collaborated with ETH in Zurich on modular performance analysis. Jointly, we have established a fixed point theorem on the existence of fixed points for component networks containing feedback cycles. Uppsala has also initiated collaboration with North Eastern University in China, on multiprocessor scheduling.

The SPEEDS project lead to an important collaboration between INRIA, OFFIS, PARADES and VERIMAG on the definition of the SPEEDS metamodel HRC [BCSM07] which is the basis of an important analysis platform (platform 1). This collaboration continues for the definition of a verification methodology. From the collaboration in SPEEDS has started a broader collaboration on a general framework for the semantics of communication in distributed systems with INRIA, PARADES and VERIMAG with external collaboration of University of Columbia and Cadence Design Systems [BCC+].

In the Combest project several joint activities are being carried out. In particular, Verimag and ETHZ collaborate on the combination of analytical performance analysis via performance analysis of a corresponding more precise operational model in order to obtain more precise results.

Interaction between RWTH and Saarland University on design notations and model checking

Iinteraction between CISS and RWTHon quantitative versions of priced timed automata

From Aalbrog to CFV (Brussels): one week visit of Prof. Kim Larsen to the team of Prof. JF Raskin.

From CFV (Brussels) to EPFL (Henzinger): Dr. Laurent Doyen formerly in CFV is post-doct at EPFL.

From CFV (Brussels) to EPFL (Henzinger): several visits during 2007-2008 by Prof. JF Raskin.

From EPFL (Henzinger) to CFV (Brussels): several visits during 2007-2008 by Dr. L Doyen.

## *3.2 Software Synthesis, Code Generation and Timing Analysis cluster*

**Visiting student: Dipl.-Inf. Daniel Cordes** (TU Dortmund)
Team visited: IMEC design automation team, led by Stylianos Magmakhakis (IMEC)
Leuven*, Belgium – November 3rd-4th, 2008*
*Approximate cost for travel and lodging: 400 €*
Reason for the visit: The reason for the visit was to get hands-on experience for mapping and memory-optimization tools designed at IMEC.
Conclusions/objectives reached: The student was quite impressed by the power and the stability of the tools developed by IMEC. The conclusions will have an impact on the design of the memory-aware compilation tools as well as mapping tools being designed at TU Dortmund.

**Visiting student: Dipl.-Inf. Olivera Jovanovic** (TU Dortmund)
Team visited: ETH Zürich, TIK, led by Lothar Thiele (ETH Zürich)
Zürich*, Switzerland – November 13th-14th, 2008*
*Approximate cost for travel and lodging: 400 €*
Reason for the visit: The reason for the visit was to explore the feasibility of extending tools from ETH Zürich with a more detailed modelling of the memory requirements and access characteristics of applications.
Conclusions: Extensions are feasible, but there are tight constraints on what could be done.

**Visiting student: Max Ferger** (RWTH Aachen)
Team visited: ACE, led by ACE management (Amsterdam)
Amsterdam*, Netherlands – June-November, 2008*
Reason for the visit: Loop parallelization in the CoSy framework.

Conclusions/objectives reached: The student had an opportunity to work in ACE's CoSy compiler framework developing the loop vectorization techniques. This was a continuation of the collaboration between RWTH Aachen and ACE in the research of retargetable compilers for embedded processors.

**Visiting researchers:** Dr. Marco Bekooij et al. (NXP)
Team visited: ISS/software on silicon, led by Rainer Leupers (RWTH Aachen)
*Aachen, Germany – August 26th, 2008*
Reason for the visit: discussion of topics related to Real Time Scheduling for MPSoCs and the problem of multi-application mapping and scheduling under timing constraints.
Conclusions/objectives reached: Both sides exchanged their views and research progress on the MPSoC programming problem and the meeting led to a good discussion on the likely future co-operation between RWTH Aachen and NXP.

**Visiting student: Sven Bunte** (**TU Vienna**)
Team visited: Univ of York
*York, Great Britain –October, 6th-10th , 2008*
*Approximate cost for travel and lodging: 1000 €*
Reason for the visit: To look at general synergy between the two research groups specifically with respect to code coverage metrics.
Conclusions/objectives reached: Whilst there has been a great deal of research on dynamic and hybrid analysis for WCET, one fundamental issue has been overlooked. That is, without appropriate test data the quality of the results are questionable. Specifically it is important that the coverage of the code is sufficient to give good results with statistical confidence. Here coverage is considered to include not only the structure of the software but should also allow for hardware and data. In the spring 2009, a joint activity is to be performed (using resources from other funded projects) that will examine which coverage metrics are important and how this coverage can be achieved. The work would be both novel and timely.

### *3.3 Operating Systems and Networks cluster*

**Visiting researcher:** Paolo Costa (Vrije Universiteit - Amsterdam, NL)
Team visited: RETIS Lab, led by Giorgio Buttazzo (Scuola Superiore Sant'Anna)
*Pisa, Italy – February 12, 2008 to February 13, 2008*
Approximate cost for travel and lodging: 400 €
Reason for the visit: Discussion on Wireless Sensor Networks
Conclusions/objectives reached: Introduction to TeenyLIME package for a Tuple Space Middleware for Wireless Sensor Networks.

**Visiting researcher:** Yao Liang (Indiana Purdue University, Indianapolis, IN, USA)
Team visited: RETIS Lab, led by Giorgio Buttazzo (Scuola Superiore Sant'Anna)
*Pisa, Italy – March 10, 2008 to March 17, 2008*
Approximate cost for travel and lodging: 2000 €
Reason for the visit: Advanced communication protocols for sensor networks
Conclusions/objectives reached: Started a collaboration on multi-view vision systems deployed through wireless sensor networks.

**Visiting researcher:** Dr. Manel Velasco (University of Catalonia, Spain)
Team visited: RETIS Lab, led by Giorgio Buttazzo (Scuola Superiore Sant'Anna)
*Pisa, Italy – April 2, 2008 to April 18, 2008*
Approximate cost for travel and lodging: 2700 €
Reason for the visit: Real-Time Control Systems: Theory and Practice
Conclusions/objectives reached: Real-Time Control Systems: Theory and Practice

**Visiting researcher:** Paolo Pagano (Scuola Superiore Sant'Anna, Pisa)
Team visited: HIPP-HURRAY, led by Eduardo Tovar (Politechnical Institute of Porto, PT)
*Porto, Portugal – January 24, 2008 to January 31, 2008*
Approximate cost for travel and lodging: 800 €
Reason for the visit: decision on operating systems support for real-time wireless networking.
Conclusions/objectives reached: Porting of Open Zigbee package to Erika Enterprise operating system.

**Visiting student:** André Cunha (Politechnical Institute of Porto, PT)
Team visited: RETIS Lab, led by Giorgio Buttazzo (Scuola Superiore Sant'Anna)
*Pisa, Italy – February 1, 2008 to February 28, 2008*
Approximate cost for travel and lodging: 1200 €
Reason for the visit: Collaboration on Open Zigbee for wireless networks
Conclusions/objectives reached: Implementation of the physical and MAC layers for the IEEE 802.15.4 suit of protocols.

**Visiting student:** Ricardo Severino (Politechnical Institute of Porto, PT)
Team visited: RETIS Lab, led by Giorgio Buttazzo (Scuola Superiore Sant'Anna)
*Pisa, Italy – May 7, 2008 to May 14, 2008*
Approximate cost for travel and lodging: 800 €
Reason for the visit: Collaboration on Open Zigbee for wireless networks
Conclusions/objectives reached: Implementation of the GTS mechanisms for the IEEE 802.15.4 MAC layer.

**Visiting student:** Mangesh Chitnis (Scuola Superiore Sant'Anna, Pisa)
Team visited: HIPP-HURRAY, led by Eduardo Tovar (Politechnical Institute of Porto, PT)
*Porto, Portugal – January 24, 2008 to January 31, 2008*
Approximate cost for travel and lodging: 800 €
Reason for the visit: decision on operating systems support for real-time wireless networking.
Conclusions/objectives reached: Porting of Open Zigbee package to Erika Enterprise operating system.

**Visiting student:** Antonio Romano (Scuola Superiore Sant'Anna, Pisa)
Team visited: HIPP-HURRAY, led by Eduardo Tovar (Politechnical Institute of Porto, PT)
*Porto, Portugal – January 24, 2008 to January 31, 2008*
Approximate cost for travel and lodging: 800 €
Reason for the visit: decision on operating systems support for real-time wireless networking.
Conclusions/objectives reached: Porting of Open Zigbee package to Erika Enterprise operating system.

**Visiting student:** Mangesh Chitnis (Scuola Superiore Sant'Anna, Pisa)
Team visited: HIPP-HURRAY, led by Eduardo Tovar (Politechnical Institute of Porto, PT)
*Porto, Portugal – April 7, 2008 to April 11, 2008*
Approximate cost for travel and lodging: 800 €
Reason for the visit: porting of Open Zigbee package to Erika Enterprise operating system.
Conclusions/objectives reached: task management for networking in the Erika Enterprise operating system.

### *3.4 Hardware Platforms and MPSoC cluster*

**Visiting researcher :** Paul Pop (DTU)
Team visited: Duke, led by Krishnendu Chakrabarty (Duke University)
*Durham, USA – December 7, 2008 to December 14, 2008*
*Approximate cost for travel and lodging: 2000 €*
Reason for the visit: Planing further collaboration.
Conclusions/objectives reached: Not completed by the time this report was written.

**Visiting student :** Mikkel Koefoed Jacobsen (DTU)
Team visited: UNIBO, led by Luca Benini (UNIBO)
*Bologna, Italy – June 15, 2008 to June 21, 2008*
*Approximate cost for travel and lodging: 1000 €*
Reason for the visit: Develop a simulation framework able to address routing policies in wireless sensor network domain and scheduling algorithms on nodes.
Conclusions/objectives reached: A prototype of the framework has been created. It is able to apply for all kind of energy harvesting systems, which must schedule processes under deadline constraints.

**Visiting student :** Aske W. Brekling (DTU)
Team visited: Virginia Tech, led by Patrick Schaumont (Virginia Tech)
*Blacksburg, USA – October 26, 2008 to November 23, 2008*
*Approximate cost for travel and lodging: 2000 €*
Reason for the visit: The aim is to define a clear semantics of the language which allows to formulate the model-of-computation using timed automata, and hence, being able to formally reason about the hardware architecture. In particular, we will look at how metrics of power consumption can be incorporated.
Conclusions/objectives reached: Not completed by the time this report was written.

**Visiting student :** Elena Maftei (DTU)
Team visited: Duke, led by Krishnendu Chakrabarty (Duke University)
*Durham, USA – August 20, 2008 to December 15, 2008*
*Approximate cost for travel and lodging: 5500 €*
Reason for the visit: To get a better understanding of the physical aspects of biochips propose a more realistic biochip and biochemical application model, that can take into account the variability in the current biochip implementations, and the potential for contamination during operations.
Conclusions/objectives reached: Not completed by the time this report was written.

**Visiting researcher :** Prof. Paul Pop (DTU)
Team visited: Linköping, led by Petru Eles (Linköping University)
*Several short visits during 2008*
Reason for the visit: Common research on predictable fault tolerant systems.
Conclusions/objectives reached: Elaborated several approaches. Written two common publications for 2008.

**Visiting student :** Paolo Burgio (Bologna)
Team visited: Linköping, led by Petru Eles (Linköping University)
*January 2008 – April 2008*
Reason for the visit: Synthesis of bus controllers for predictable multiprocessor on chip.
Conclusions/objectives reached: Efficient infrastructure for the predictable implementation of multiprocessor systems has been designed.

**Visiting researcher :** Prof. Michael R,. Hansen (DTU)
Team visited: Oldenburg, led by Martin Franzle (University of Oldenburg)
*Oldenburg, Germany – October 6 – 10, 2008*
Reason for the visit: Common research on

**Visiting researcher :** Prof. Martin Franzle (University of Oldenburg)
Team visited: DTU, led by Jan Madsen (DTU)
*Lyngby, Denmark – June 16 - 20 and October 20 – 24, 2008*
Reason for the visit: Common research on

**Visiting researcher :** Luca Santinelli, SSSA PISA
Team visited: ETHZ, led by Lothar Thiele, Zurich
Time: November 2008 – April 2009.
Reason for the visit: Joint work on adaptive changes and real-time constraints
Conclusions/objectives reached: The visit just started.

**Visiting researcher :** Michele Magno, University Bologna
Team visited: ETHZ, led by Lothar Thiele, Zurich
Time: November July 2008 – January 2009.
Reason for the visit: Joint work on energy scavenging sensor networks.

### *3.5 Design for Adaptivity in Embedded Systems (Transversal Integration WP)*

**Visiting researcher :** Clara Otero-Perez (NXP)
Team visited: TUKL, led by Gerhard Fohler (<TUKL>)
*Kaiserslautern, Germany – 2008 11 12-14*
*Approximate cost for travel and lodging: 500 €*
Reason for the visit: regular visit within joint PhD which started in ARTIST2
Conclusions/objectives reached: Directions of further PhD work were outlined, next publications planned

**Visiting researcher :** Luca Santinelli, SSSA PISA
Team visited: ETHZ, led by Lothar Thiele, Zurich
Time: November 2008 – April 2009.
*Approximate cost for travel and lodging: 12.000*
Reason for the visit: Joint work on adaptive changes and real-time constraints
Conclusions/objectives reached: The visit just started.

**Visiting student :** Michele Magno (University of Bologna)
Team visited: TIK, led by Lothar Thiele (ETH Zurich)
*Zurich, Switzerland – June 30, 2008 to January 31, 2009*
*Approximate cost for travel and lodging: 2000 €*
Reason for the visit: Research on adaptive energy management in clusters of wireless sensor nodes
Conclusions/objectives reached: The visit investigated on adaptivity to systems which use energy harvesting modules. In particular we propose a model which run on the cluster-heads node and will decide the long-term objectives of each node adapting their parameters.

**Visiting researcher : PhD student Magnus Persson, Ass. Professor Ingo Sander, KTH**
Team visited: LTH, Karl-Erik Årzen
Lund workshop on the Design for Adaptivity workshop organized as part of ArtistDesign; May 13-14, 2008
Approximate cost for travel and lodging: 800 €

Reason for the visit: This was the kick-off for the adaptivity action in ArtistDesign.
Conclusions/objectives reached: A summary is available on the Artist web (http://www.artist-embedded.org/artist/Venue,1403.html)

**Visiting researcher : PhD student Magnus Persson, Prof. Martin Törngren, Ass. Professor DeJiu Chen, PhD student Tahir Naseer, PhD student Anders Sandberg, KTH**
Team visited: LTH, Sebastien Gerard, Francois Terrier, Paris, France
2008-04-07 - 2008-04-09
Approximate cost for travel and lodging: 2500 €
Reason for the visit: To discuss embedded systems modeling and component modeling. To plan for joint projects and papers.
Conclusions/objectives reached: Further exchange of information and openings for joint papers on component models and models of computation.

### *3.6 Design for Predictability (Transversal Integration WP)*

**Visiting researcher :** Prof. Paul Pop (DTU)
Team visited: Linköping, led by Petru Eles (Linköping University)
*Several short visits during 2008*
Reason for the visit: Common research on predictable fault tolerant systems.
Conclusions/objectives reached: Elaborated several approaches. Written two common publications for 2008.

**Visiting student :** Paolo Burgio (Bologna)
Team visited: Linköping, led by Petru Eles (Linköping University)
*January 2008 – April 2008*
Reason for the visit: Synthesis of bus controllers for predictable multiprocessor on chip.
Conclusions/objectives reached: Efficient infrastructure for the predictable implementation of multiprocessor systems has been designed.

**Visiting student: Dipl.-Inf. Olivera Jovanovic** (TU Dortmund)
Team visited: ETH Zürich, led by Lothar Thiele (ETH Zürich)
Zürich*, Switzerland – 13.11.2008 to 14.11.2008*
*Approximate cost for travel and lodging: 400 €*
Reason for the visit: The reason for the visit was to explore the feasibility of extending tools from ETH Zürich with a more detailed modelling of the memory requirements and access characteristics of applications.

### *3.7 Integration Driven by Industrial Applications (Transversal Integration WP)*

**Visiting researcher:** Ed Brinksma, ESI

Team visited: KTH led by Martin Torngren, KTH
Stockholm, Sweden, - Sept. 02-Sept. 03, 2008.
*Approximate cost for travel and lodging:* Approximate cost for travel and lodging: 500 €
Reason for the visit: Invited keynote for kick-off of the KTH Embedded Systems centre.
Conclusions/objectives reached: It was concluded that further contacts in relation to ArtistDesign and the Industrial Integration activity should be organized.

# 4. Tools and Platforms

*From the description of work :*
A research platform is composed of competencies, resources, and tools targeting specific technical and scientific objectives around a chosen topic. These are at the state-of-the-art, and are made available to the R&D community for experimentation, demonstration, evaluation, and teaching.

The research platforms, tools and facilities are an essential tool for implementing the JPIA. They will lay the groundwork for the JPRA, allowing common research to occur and capitalisation on research results. Platforms are used as the basis for transfer of research results to industry. They allow teaching practical knowledge of the concepts and techniques.

ArtistDesign platforms are not defined from scratch – they integrate the results of long-term efforts, and are meant to be durable, evolving with the state of the art. The partners are committed to durability, and have invested significant resources into their development. The construction of ArtistDesign has provided the opportunity to assemble existing pieces into a rationally-structured set of platforms, covering the area of embedded systems design.

Some of the ArtistDesign platforms have international visibility, and the ambition is for these to serve as world-wide references in their respective topics.

## *4.1 Modelling and Validation Cluster*

Here we list some of the stable, downloadable tools and platforms of the cluster. The cluster particpants are working on several other tools and platforms. For more and detailed information we refer to the reports of the activities *Modeling* and *Validation*.

### *4.1.1 AMT*

AMT (Analog Monitoring Tool) is a tool for checking the correctness of analog and mixed-signal simulation traces with respect to a formal specification expressed as an assertion. The specification language supported by the tool is STL/PSL, an extension of the temporal logic inspired by the PSL language, which allows to express properties of real-valued continuous-time behaviors.

http://www-verimag.imag.fr/~nickovic/index.php?id=nickovic&page=amt

### *4.1.2 IF TOOLBOX*

IF is a language for the structured representation of concurrent real-time systems and a set of tools allowing the analysis and verification of requirements on such systems. The tool evolved from the CADP toolset. Its development was motivated by the need for a structured representation of systems, allowing the application of simplifications for avoiding state explosion before its translation into a global (symbolic) transition relation. In particular, IF has frontends allowing the verification and analysis of models of real-time systems represented in SDL and UML.

http://www-if.imag.fr./

### 4.1.3 MARTE

MARTE consists in defining foundations for model-based description of real time and embedded systems. These core concepts are then refined for both modeling and analyzing concerns. Modeling parts provides support required from specification to detailed design of real-time and embedded characteristics of systems. MARTE concerns also model-based analysis. In this sense, the intent is not to define new techniques for analyzing real-time and embedded systems, but to support them. Hence, it provides facilities to annotate models with information required to perform specific analysis. Especially, MARTE focuses on performance and schedulability analysis. But, it defines also a general framework for quantitative analysis which intends to refine/specialize any other kind of analysis.

http://www.omgmarte.org/

### 4.1.4 METROPOLIS

Establishing formal design methodologies is imperative to effectively

manage complex design tasks required in modern-date system designs. It involves defining levels of abstraction to formally represent systems being designed, as well as formulating problems to be addressed at and across the abstraction levels. This calls for a design environment in which systems can be unambiguously represented throughout the abstraction levels, the design problems can be mathematically formulated, and tools can be incorporated to solve some of the problems automatically. Developing such an environment is precisely the goal of Metropolis.

Metropolis consists of an infrastructure, a tool set, and design methodologies for various application domains. The infrastructure provides a mechanism such that heterogeneous components of a system can be represented uniformly and tools for formal methods can be applied naturally.

http://embedded.eecs.berkeley.edu/metropolis/index.html

### 4.1.5 PHAVER

PHAVer is a tool for verifying safety properies of hybrid systems. It stands out from other tools with the following features:

- exact and robust arithmetic with unlimited precision,
- on-the-fly over-approximation of piecewise affine dynamics
- improved algorithms and termination heuristics
- support for compositional and assume-guarantee reasoning.

http://www-verimag.imag.fr/~frehse/phaver_web/index.html

### 4.1.6 UPPAAL

Uppaal is an integrated tool environment for modeling, validation and verification of real-time systems modeled as networks of timed automata, extended with data types (bounded integers, arrays, etc.).

The tool is developed in collaboration between the Department of Information Technology at Uppsala University, Sweden and the Department of Computer Science at Aalborg University in Denmark.

www.uppaal.com

### 4.1.7 UPPAAL TIGA

UPPAAL TIGA (Fig. 1) is an extension of UPPAAL [BDL04] and it implements the first efficient on-the-fly algorithm for solving games based on timed game automata with respect to reachability and safety properties. Though timed games for long have been known to be decidable there has until now been a lack of efficient and truly on-the-fly algorithms for their analysis.

http://www.cs.aau.dk/~adavid/tiga/

### 4.1.8 UPPAAL TRON

Uppaal TRON is a testing tool, based on Uppaal engine, suited for black-box conformance testing of timed systems, mainly targeted for embedded software commonly found in various controllers. By online we mean that tests are derived, executed and checked simultaneously while maintaining the connection to the system in real-time.

http://www.cs.aau.dk/~marius/tron/

### 4.1.9 SARTS

SARTS is a model based schedulability analysis tool used for hard real-time systems. SARTS is used to translate hard real-time systems, implemented in Java, to a finite state machine in the modeling tool Uppaal.

The system being analyzed must be implemented in SCJ2, a safety critical profile for Java developed in this project, based on SCJ. The target hardware is the time predictable Java processor JOP, developed specifically for hard real-time systems.

Several experiments have been conducted to illustrate the accuracy of SARTS compared to existing tools. It is shown how the model based approach can result in a more accurate analysis, than possible with traditional analyses.

http://sarts.boegholm.dk/

### 4.1.10 STG

STG (Symbolic Test Generator) generates conformance tests, based on this framework:

- Implementation: black-box, only input/output behavior is observable.
- Specification: IOSTS(input/output behavior + internal structure)
- Test Purpose: IOSTS, tells which part of the specification is to be tested
- Test Case: IOSTS generated by STG from a specification and a test purpose
  - Test Cases are symbolic, and possibly parameterized by constants
  - They take into account possible non-determinism of the Spec;
  - They include a verdict (no manual interpretation needed)

http://www.irisa.fr/prive/ployette/stg-doc/stg-web.html

### *4.1.11 TIMES*

TIMES is a **T**ool for **M**odeling and **I**mplementation of **E**mbedded **S**ystems. It is a tool set for modelling, schedulability analysis, synthesis of (optimal) schedules and executable code. It is appropriate for systems that can be described as a set of tasks which are triggered periodically or sporadically by time or external events.

http://www.timestool.com/

## *4.2 Software Synthesis, Code Generation and Timing Analysis cluster*

### *4.2.1 aiT*

**Objectives**

aiT is the leading tool for computing worst case execution times (WCETs).

**Main Results**

In a previous project, aiT was integrated with an experimental worst-case execution time aware compiler called WCC. During the last year, this integrated tool set was used for exploring the optimization potential for compiler optimizations using WCETs as the objective function.

**Current work**

Current work is performed in the PREDATOR project and extends work performed during the lifetime of the Artist2 NoE The current work explores the optimization potential of WCC.

**Participating partners:**

- AbsInt, Saarbrücken
  AbsInt provides aiT.
- TU Dortmund
  TU Dortmund integrates aiT into WCC and explores the optimization potential.

**Web**
http://ls12-www.cs.tu-dortmund.de/research/activities/wcc/

**Related Publications**

- Paul Lokuciejewski, Heiko Falk, Peter Marwedel: *WCET-driven Cache-based Procedure Positioning Optimizations*, Proceedings of the 20th Euromicro Conference on Real-Time Systems (ECRTS), Prague, Czech Republic, July, 2008.
- Paul Lokuciejewski, Fatih Gedikli, and Peter Marwedel: *Accelerating WCET-driven optimizations by the Cold Path Paradigm – a Case Study of Loop Unswitching*, Submitted to SCOPES, 2009.
- Paul Lokuciejewski, Daniel Cordes, Heiko Falk, Peter Marwedel: *A Fast and Precise Static Loop Analysis based on Abstract Interpretation, Program Slicing and Polytope Models*, International Symposium on Code Generation and Optimization (CGO), 2009.

- Sascha Plazar, Paul Lokuciejewski, Peter Marwedel: *A Retargetable Framework for Multi-objective WCET-aware High-level Compiler Optimizations*, IEEE Real-Time Systems Symposium (RTSS/WIP), 2009.
- Paul Lokuciejewski, Fatih Gedikli, Peter Marwedel, Katharina Morik: *Automatic WCET Reduction by Machine Learning Based Heuristics for Function Inlining,* Submitted to 3rd hipeac Workshop on Statistical and Machine Learning approaches applied to Architectures and Compilation (SMART) 2009

### *4.2.2 MAPS*

**Objectives**

MAPS (MPSoC Application Programming Studio) is proposed and developed in ISS, RWTH Aachen to tackle the challenge of programming future heterogeneous MPSoC platforms. It targets efficient code generation for multiple applications at a time and predefined heterogeneous MPSoC platforms.

**Main Results**

In collaboration with Prof. Isshiki's group in Tokyo Inst. of Tech., MAPS was coupled with TCT (Tightly-Coupled Thread) tools from Tokyo to successfully parallelize a number of applications. The results were reported in the DAC paper this year.

**Current work**

MAPS is currently under development in many aspects to enhance its capabilities, such as multi-application RT scenario, high-level simulation environment, dedicated task dispatching/scheduling, etc. MAPS is part of RWTW Aachen's Ultra high speed Mobile Information and Communication (UMIC) research cluster. RWTH Aachen has been actively discussing MAP with ArtistDesign partners at the Rheinfels workshop and at the working meeting at Düsseldorf.

**Participating partners:**

- RWTH Aachen
  RWTH Aachen is designing and developing the MAPS tools.

**Web**
http://www.iss.rwth-aachen.de/Projekte/Tools/MPSoC%20Application%20Programming%20Studio.html

**Related Publications**

Jianjiang Ceng, Jeronimo Castrillon, Weihua Sheng, Hanno Scharwächter, Rainer Leupers, Gerd Ascheid, Heinrich Meyr (RWTH Aachen Univ.), Tsuyoshi Isshiki, Hiroaki Kunieda (Tokyo Institute of Tech.), "MAPS: An Integrated Framework for MPSoC Application Parallelization", in 45th Design Automation Conference, Anaheim, CA, USA, June 2008

### *4.2.3 CoSy*

**Objectives**

CoSy is a mature commercial development compiler platform.

**Main Results**

RWTH integrated additional optimizations into CoSy. TU Berlin used CoSy for its research on compiler verification. IMEC used CoSy as a platform for generating compilers.

**Current work**

Work on additional optimizations continues at RWTH Aachen, and so does the work at TU Berlin and IMEC. There is the trend toward using MPSoCs as the target platform.

**Participating partners:**

- RWTH Aachen
- TU Berlin
- IMEC vzw

**Web**
http://www.ace.nl/compiler/cosy.html

**Related Publications**

M. Hohenauer, F. Engel, R. Leupers, G. Ascheid, H. Meyr, RWTH Aachen University; G. Bette, ACE; B. Singh, NXP Semiconductors Eindhoven: Retargetable Code Optimization for Predicated Execution,. In DATE, Munich, Germany, March 2008.

### *4.2.4 ICD-C*

**Objectives**

ICD-C is a recent development platform with special support for source-to-source transformations. Source-to-source transformations can be implemented without loosing any information about the original C program. It can also be used in cases where full control over the libraries is required.

**Main Results**

ICD-C was used for the integration of compilers with timing analysis and the impact of optimizing the WCET was studied in a number of cases.

**Current work**

Current work is extending the support for caches and aims at reducing the number of calls of the WCET estimator in order to speed-up optimization. Machine-learning techniques are being tried as a promising approach. Mnemee partners are starting to use ICD-C.

**Participating partners:**

- TU Dortmund
- ICD Dortmund (via the Mnemee project)
- TU Eindhoven

**Web**

http://www.icd.de/es/index.html

## *4.3 Operating Systems and Networks cluster*

### *4.3.1 Platform: Educational kit for Real-Time Embedded Systems*

**Objectives**

The goal of this initiative is to develop of an educational kit for embedded systems, based on Microchip dsPIC technology, consisting of a number of modules that can easily be composed depending on specific application purposes. The modules consist of:

1. The main processing platform (the FLEX mother board) with the dsPIC 16-bit microcontroller. It is designed to be composable with other boards (daughter boards) designed for specific applications and connected in a piggy-back fashion.
2. A set of dauther boards for specific applications, with specific sensors and actuators. Available special boards include a multi-bus connection board, an intertial system for flight control, a 4 axis motor controller, and a sound localization board.
3. A set of libraries to simplify the access to the hardware devices (sensors, servomotors, wireless modules),
4. A number of sample real-time control applications that can be easily replicated by the users.

All applications are developed in C language and run on the Erika operating system, which is an OSEK compliant real-time kernel for small embedded microcontrollers.

**Main Results**

In this first year, the system was used as a reference embedded platform for running real-time applications under severe resource constraints. The following control applications have been developed using Erika Enterprise as a real-time kernel and Flex as a hardware platform.

**Ball and plate balancing**. A two-degrees-of-freedom balancing device has been built at the Scuola Superiore Sant'Anna to control the trajectory of a ball on a plate actuated by two servomotors. The position of the ball is detected by a resistive touch screen mounted on the plate.

**Web link:** http://www.evidence.eu.com/content/view/276/266/

**Visual tracking**. A visual tracking application was developed at the Scuola Superiore Sant'Anna, where a moving ball was followed by a mobile CMOS camera using the FLEX board. The CMOS Camera is capable of returning JPEG images to the connected FLEX board

hosting a Microchip dsPIC. The Flex Board also controls two servomotors which are used to articulate the camera, thereby maintaining the focus on the rolling ball.

**Web link:** http://www.evidence.eu.com/content/view/277/266/

**Inverted Pendulum at SUSPI**. An inverted pendulum was controlled using the FLEX board with Scilab/Scicos at SUPSI (Scuola Universitaria Professionale della Svizzera Italiana), Lugano, Switzerland. The FLEX Base Board and the FLEX Multibus Board with a CAN module were used for swinging-up and maintaining the inverted equilibrium. The Source code was entirely generated using Scilab/Scicos, an automatic code generator for control systems.

**Web link:** http://www.evidence.eu.com/content/view/274/266/

**Inverted Pendulum at UPC**. An inverted pendulum was implemented using the FLEX board and Erika by the Distributed Control Systems group at the Automatic Control Department, Technical University of Catalonia, Barcelona, Spain. The FLEX Board and the FLEX Multibus Board with a RS232 module was used for both swinging-up and maintaining the inverted equilibrium.

**Web link:** http://paginespersonals.upcnet.es/~pmc16/08EvidenceNoteRTpend.zip

**DC Motor control**. A DC servomotor was controlled using the FLEX board with Scilab/Scicos at SUPSI (Scuola Universitaria Professionale della Svizzera Italiana), Lugano, Switzerland. The FLEX Base Board and the FLEX Multibus Board with a CAN module were used for Servo control of a DC Motor. The Source code was entirely generated using Scilab/Scicos, an automatic code generator for control systems.

**Web link:** http://www.evidence.eu.com/content/view/273/266/

**Hexapode robot control**. An 18-DOF hexapod robot was completly designed and developed at the University of Florence by Andrea Foschi in 2005. It was later tamed by Marco Natalini and Alessandro Mambelli using Evidence Srl's FLEX Light board and ERIKA kernel. The main purpose for adopting FLEX was due to its low-cost development kit that permits easy addition of features, i.e., sensors and behaviour. Since then, a number of students have worked on this hexapod.

**Web link:** http://www.evidence.eu.com/content/view/261/266/

**Educational experiments**. An embedded control systems was developed with the Erika+Flex platform at the Automatic Control Department of the Technical University of Catalonia (Spain), with the purpose of setting a laboratory experiment for educational purposes. A real-time control of dynamical system was designed to drive students to a better understanding and integration of the diverse theoretical concepts that often come from different disciplines such as real-time and control systems.

**Current work**

The current work includes the development of:

- new dauther boards for specific sensors and real-time control applications;
- schedulability analysis tools for real-time tasks with timing and resource constraints;
- energy-aware scheduling algorithms;

- medium access protocols for wireless communication under real-time constraints;
- code generation modules for the Scilab/Scicos environment;

**Participating partners:**

RETIS Lab - Scuola Superiore Sant'Anna, Pisa – Giorgio Buttazzo (http://retis.sssup.it/)
Role: Design of real-time algorithms, applications and sensor interfaces.

Evidence s.r.l. – Paolo Gai (http://www.evidence.eu.com/)
Role: Support for the Erika operating system.

Embedded Solutions – Daniele Sartorello (http://www.es-online.it/)
Role: Hardware design, board production, and testing.

Microchip Technology – Antonio Bersani (http://www.mchip.it/)
Role: Hardware components, support for the compiler and device libraries, dissemination.

University of Catalonia – Pau Marti (http://paginespersonals.upcnet.es/~pmc16/)
Role: Development of control applications.

University of Pavia – Tullio Facchinetti (http://robot.unipv.it/toolleeo/)
Role: Development of robotic applications.

**Web**

| | |
|---|---|
| ERIKA: | http://www.evidence.eu.com/content/view/27/254/ |
| FLEX: | http://www.evidence.eu.com/content/view/114/204/ |
| Applications: | http://www.evidence.eu.com/content/blogsection/6/266/ |
| | http://www.youtube.com/group/flexboards |

**Related Publications**

1. Pau Martí, Manel Velasco and Giorgio Buttazzo, "AN EMBEDDED REAL-TIME CONTROL SYSTEMS LABORATORY ACTIVITY", Research report ESAII-RR-08-03, Automatic Control Dept., Technical University of Catalonia, Barcelona, Spain, Aug. 2008.

### *4.3.2 Tool: Realistic Simulation of Wireless Sensor Networks*

**Objectives**

Networks simulators can play a key role, together with analytical models, for validating a distributed system against the QoS it must guarantee. Current network simulators, however, only concentrate on the communication activities of the network through the various layers, neglecting the concurrent computations that may occur within the nodes. The objective of this work is to integrate the simulation functions of the NS-2 network simulator with the operating system activities going on in a node, to evaluate the effects of the overheads and the scheduling mechanism on the overall performance of the network.

**Main Results**

The RETIS group of the Scuola Superiore Sant'Anna of Pisa is developing RTNS, a publicly available free tool, to simulate operating system aspects in wireless distributed applications. It extends the well-known NS-2 simulator with models of the CPU and real-time application tasks

to take into account delays introduced by scheduling and I/O interrupts. This package can be used to efficiently co-design the kernel and network profiles before deployment, especially when the number of nodes is high and analytical methods are too expensive.

**Web link:** http://rtns.sssup.it

**Participating partners:**

RETIS Lab - Scuola Superiore Sant'Anna, Pisa – Giorgio Buttazzo (http://retis.sssup.it/)
Role: Design of real-time algorithms, applications and sensor interfaces.

## *4.4 Design for Adaptivity in Embedded Systems (Transversal Integration WP)*

### *4.4.1 SWEET (SWEdish Execution Time tool)*

**Objectives**

SWEET is a WCET analysis tool. It is an academic prototype: the main objective is to use it as a test bench for methods in WCET analysis, and then mainly flow analysis to produce program flow constraints (upper bounds on # of loop iterations, information about infeasible paths, etc.).

**Main Results**

SWEET has been used to develop and test various methods for constraining program flow. It has also been used in industrial case studies. The results indicate that the developed methods do improve on the number of automatically detected program flow constraints, as well as on the precision of the resulting WCET bound.

**Current work**

SWEET is currently being reengineered to use new interface formats for code to analyze and resulting program flow constraints. A version of SWEET that performs parametric WCET analysis will also be created: this work is of relevance to the adaptivity activity since parametric WCET bounds can be used by adaptive scheduling methods.

**Participating partners:**

- Mälardalen University
  Maintains and develops SWEET, develops methods for parametric WCET analysis.
- Saarland University
  Collaboration partner for parametric WCET analysis.

**Web**
http://www.mrtc.mdh.se/projects/wcet/sweet.html

**Related Publications**


- Stefan Bygde and Björn Lisper. *Towards an Automatic Parametric WCET Analysis*. In Raimund Kirner (ed.) Proc. 8th International Workshop on Worst-Case Execution Time Analysis, (WCET'2008), pp. 9-17, Prague, Czech Republic, July 2008.
- Sebastian Altmeyer, Christian Hümbert, Björn Lisper, and Reinhard Wilhelm: Parametric timing analysis for complex architectures. Proc. 14th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 08), Kaohsiung, Taiwan, Aug. 2008


### *4.4.2 MPA (Modular Performance Analysis)*

**Objectives**

The MPA toolbox allows the analysis of distributed embedded real-time systems. It is based on the real-time calculus which allows a component-based investigation of essential system properties like throughput, end-to-end constraints and buffer space.

**Main Results**

During the first year of ArtistDesign, the tool box have been extended towards the modeling of hierarchical event streams (together with University Braunschweig) and coupled to the Symta/S tool from SymtaVision. In addition, it has been integrated into the MPSOC design environment DOL. As a result of activities in ArtistDesign, a design flow has been established that includes the MPARM simulation environment from University Bologna (Luca Benini). In the context of this activity, the semantics of DOL will be modeled in BIP (Verimag, Joseph Sifakis) in order to verify additional important system properties.

**Current work**

The integration of MPA and DOL with other tools of partners just started.

**Participating partners:**

- VERIMAG
  Link to BIP from Verimag.
- Braunschweig
  Link to Symta/S and the modeling of hierarchical event streams
- University Bologna
  Combining MPARM simulation and the DOL specification and mapping environment.
- Uppsala
  Providing insights into the analysis of cyclic systems which lead to an extension of the toolbox.

### 4.4.3 Hardware setup to demonstrate self-protection and adaptability of embedded Real-Time Systems

**Objectives**

A demonstrator for self-protection and adaptability in real-time systems is to be developed. It shall demonstrate feasibility and cost of run-time adaptation and protection with respect to performance metrics such as end-to-end latencies. Furthermore, the demonstrator acts as a platform to evaluate performance of the proposed methodologies.

**Main Results**

A demonstrator implementation of the achievements outlined in section 3.1 has been developed on different platforms. For once, a cycle-accurate model of an ARM-Bsed microprocessor is available, second, two MPC5200 based microcontroller evaluation boards exist in order to show properties of the implementation. On both prototypes, a uC/OS-II microkernel is running and communication between multiple instances is possible using a CAN bus.

The microcontroller boards have been extended by a time sensitive control application, in order to show effects of self-protection and adaptation with respect to performance metrics.

**Current work**

Currently, work is being done on integration of framework components in the demonstrator. Furthermore, the time-sensitive control application is being implemented.

**Participating partners:**

- TU Braunschweig
  Sole Developer of the demonstrator

**Related Publications**

Steffen Stein and Rolf Ernst. "Distributed Performance Control in Organic Embedded Systems." In *Autonomic and Trusted Computing (LNCS)*, Volume 5060/2008, pp 331-342, June 2008.

### 4.4.4 TrueTime

**Objectives**

To provide a flexible simulation platform for networked embedded real-time systems with a particular focus on control applications. TrueTime implements simulation models for a multi-tasking real-time kernel and data link layer network protocols that execute embedded in the Matlab/Simulink environment. Using TrueTime it is possible to experiment with adaptive resource management and network protocols and investigate how this influence application performance.

**Main Results**

TrueTime has been continuously developed since 1999. The version that will be released during fall 2008 (Version 1.6) will be released according to the GPL license. It also provides improved support for CBS-type reservation-based management.

**Current work**

The current development work on TrueTime is focused on providing support for multi-core kernels, to begin with using global scheduling. The development is currently mainly supported by the ACTORS project.

**Participating partners:**

- ULUND
  Toolbox development.
- SSSA, TUKL, Aveiro, KTH,....
  Users of the toolbox

**Web**

http://www.control.lth.se/truetime/

**Related Publications**

Gonzalo Farias, Anton Cervin, Karl-Erik Årzén, Sebastián Dormido, Francisco Esquembre: "Multitasking Real-Time Control Systems in Easy Java Simulations". In Proc. 17th IFAC World Congress, Seoul, Korea, July 2008.

Anton Cervin and Karl-Erik Årzén: “TrueTime: Simulation tool for performance analysis of real-time embedded systems”, Book chapter in forthcoming book “Model-Based Design of Heterogeneous Embedded Systems”, CRC Press, 2009.

### *4.4.5 SHARK RTOS*

**Objectives**

The SHARK (Soft and HArd Real-time Kernel) RTOS is a real-time operating system developed at the ReTiS Lab of the Scuola Superiore Sant’Anna of Pisa, with the collaboration of the Robotics Lab of the University of Pavia. It provides a number of internal kernel mechanisms specifically designed to facilitate the development of demonstrators and prototypes. It supports applications where computational tasks can have explicit timing constraints; it includes several advanced algorithms for task scheduling and shared resource management, which can be dynamically selected by the user through a configuration file. It includes drivers for the most common I/O peripherals and it complies with the POSIX standard, PSE51 profile. The objective is to use SHARK as a common platform for OS-based adaptivity research within the activity.

**Current work**

Shark has been used as a tool for evaluating the effects of periods, delays and jitter on control performance. Under Shark, we implemented a mechanism for injecting arbitrary delays in periodic control tasks and used to perform several tests with varying timing parameters.

**Participating partners:**

- SSSA
  SHARK development.

**Related Publications**

Yifan Wu, Enrico Bini, and Giorgio Buttazzo, "A Framework for Designing Embedded Real-Time Controllers", Proceedings of the 14th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2008), Kaohsiung, Taiwan, August 25-27, 2008.

### *4.4.6 ForSyDe – Formal System Design*

**Objectives**

ForSyDe is a modelling framework for studying models of computation and various modelling and analysis techniques. It has been developed at KTH for eight years and has been used in a number of research projects and in several courses.

**Main Results**

In ForSyDe four main models of computation (MoC) have been realized and seamlessly integrated: continuous MoC, discrete MoC, synchronous MoC and untimed NoC. Thus, heterogeneous systems can be modelled in ForSyDe in an integrated way.

A transfoprmational design method has been developed and realized in ForSyDe. A set of formal verification and retiming techniques, that are conncted to design transformations, have been developed as well.

Also, abstract concepts of adaptivity have been developed in ForSyDe and modelling mechanisms have been devised in realized. As a concrete application, dunamically reconfigurable systems have been modelled and a performance analysis technique has been developed that captures the reconfiguration time and the buffer requirements.

**Current work**

Todate, the ForSyDe team focuses on establishing a formal and sound relation for the ForSyDe MoCs to corresponding MoCs in SystemC. This will allow for a formal foundation of SystemC based design and it will make the design transformations and verification techniques, that have been developed in ForSyDe, available in SystemC. Also, the performance analysis methods, developed for reconfigyurable systems, are generalized for heterogeneous multicore SoCs.

**Participating partners:**

- KTH
  Main developer

- OFFIS
  Cooperates with KTH in developing the performance analysis method for dynamically reconfigurable systems.

**Web**
http://www.ict.kth.se/org/ict/ecs/sam/projects/forsyde/www/index.html

**Related Publications**

Tarvo Raudvere, Ingo Sander, and Axel Jantsch. Application and verification of local non-semantic-preserving transformations in system design. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 27(6):1091-1103, June 2008.

Axel Jantsch. Models of computation for distributed embedded systems. In Richard Zurawski, editor, *Networked Embedded Systems*. CRC Press/Taylor & Francis, 2008.

Deepak Mathaikutty, Hiren Patel, Sandeep Shukla, and Axel Jantsch. SML-Sys: A functional framework for multiple models of computation for heterogeneous system design. *Design Automation for Embedded Systems*, 2008.

Ingo Sander and Axel Jantsch, "Modelling Adaptive Systems in ForSyDe", Electronic Notes in Theoretical Computer Science, vol. 200, no. 2, pp. 39-54, February 2008.

Jun Zhu, Ingo Sander, and Axel Jantsch, "Performance Analysis of Reconfiguration in Adaptive Real-Time Streaming Applications", Proceedings of the 6th Workshop on Embedded Systems for Real-Time Multimedia, October 2008.

Jun Zhu, Ingo Sander, and Axel Jantsch, "Energy efficient streaming applications with guaranteed throughput on MPSoCs", Proceedings of the International Conference on Embedded Software, October 2008.

## *4.5 Integration Driven by Industrial Applications (Transversal Integration WP)*

### *4.5.1 Tool: IMEC MPA + MH MPSoC mapping framework for wireless and multimedia applications*

**Objectives**

The main objectives of the framework is to offer an automatic source code parallelization (MPA tool) and memory hierarchy management (MH tool) in order to map efficiently embedded software application on MPSoC platforms.

**Main Results**

Prototype versions of the MPSoC Parallelization Assistant (MPA) and Memory Hierarchy (MH) management tools were developed and tested on video codec embedded sosftware applications (i.e., MPEG-4, AVC etc.). The results will be used by THALES, INTRACOM, CoWare, ICD and Arteris industrial partners to improve their memory hierarchy, NoC interconnect and MPSoC mapping for wireless (software defined radio and WiMax) and multimedia (VoIP) applications.

**Current work**

Currently, the affiliated partners of IMEC (ie, DUTH/ICCS and TU/e) and core partners (TUDortmund/ICD and KTH) are trying to integrate their tool and design flows with the IMEC MPA + MH MPSoC mapping framework in the memory and interconnect specific context of the MNEMEE and MOSART FP7 projects, respectively.

**Participating partners:**

- DUTH/ICCS
  This partner is integrating the dynamic data type and dynamic memory management tools and design flows with the IMEC MPSoC mapping tool flows.
- TUDortmund/ICD
  This partner is integrating its pre-compiler and compiler framework to the static MH tool of IMEC.
- TU/e
  This partner is integrating its SDF3 framework in the context of system scenarios with the IMEC MPSoC mapping tool flows.
- KTH
  This partner is integrating its NoC simulation and exploration framework with the MPA tool of IMEC.

**Web**
http://www.mnemee.org/
http://www.mosart-project.org/

**Related Publications**

**IMEC vzw. & TU/e**

- 'A System Scenario based Approach to Dynamic Embedded Systems', S.V. Gheorghita, M. Palkovic, J. Hamers, A. Vandecappelle, S. Mamagkakis, T. Basten, L. Eeckhout, H. Corporaal, F. Catthoor, F. Vandeputte, K. De Bosschere, ACM Transactions on Design Automation of Electronic Systems, ToDAES. To appear in 2009.

**IMEC vzw. & TU/e & DUTH & TU Dortmund (at ICD)**

- 'MNEMEE: Memory management technology for adaptive and efficient design of embedded systems' S.Mamagkakis, P.Lemmens, D.Soudris, T.Basten, P.Marwedel, D.Kritharidis, G.Guilmin, 16th IFIP/IEEE International Conference on Very Large Scale Integration - VLSI-SOC, 2008.

**IMEC vzw. & KTH & DUTH**

- 'MOSART: Mapping Optimisation for Scalable multi-core ARchiTecture', B. Candaele, A. Jantsch, T. Ashby, K. Tiensyrjä, F. Ieromnimon, B. Vanthournout, P. Di Crescenzo, D. Soudris, 16th IFIP/IEEE International Conference on Very Large Scale Integration - VLSI-SOC, 2008.

## *4.5.2 COSI*

### Objectives

COSI (Communication Synthesis Infrastructure) is a software framework for interconnect infrastructure synthesis

### Main Results

The framework allows developing specialized flows and tools for communication synthesis as exemplified by the GSRC-internal release of COSI-NOC (Communication Synthesis Infrastructure for Network-on-Chips), a software toolkit for the automatic synthesis of synchronous networks-on-chip based on the platform-based design paradigm, and by COSI-BAD, for building automation design.

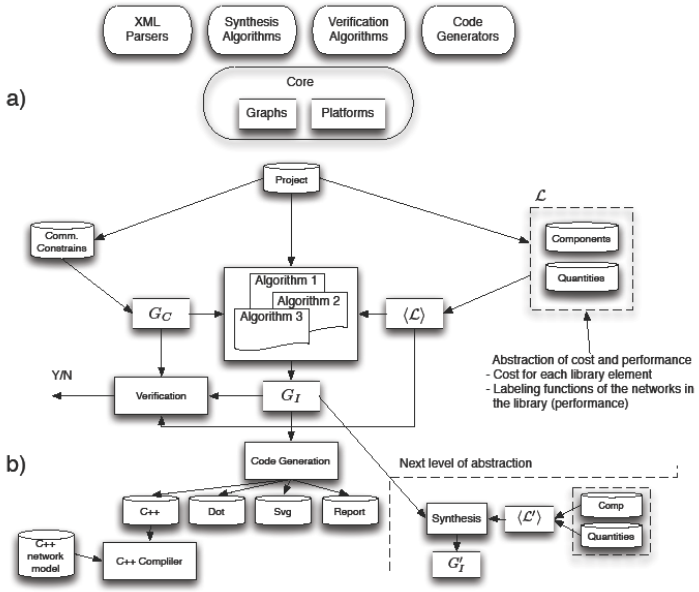


**Figure 1.** The COSI Platform-Based Design-like structure

| | Quantities | CommStructs | Library | Models | Rules | Platforms | Environment | I/O | Algorithms |
|---|---|---|---|---|---|---|---|---|---|
| Core | Ports<br>Bandwidth<br>Flows... | Graphs | | | | | | | ShortestPath<br>Tsp<br>SpanningTree<br>FacilityLocation<br>Kmedian |
| On-Chip Communication | Interface<br>ipGeometry<br>NodeParam | Specification<br>PItInstance<br>Implementation | Router<br>Link<br>Bus | Ho-Area<br>Ho-Power<br>Orion | Critical length<br>Deadlock | RouterLink<br>BusNoc | Rectangle | Parsers<br>SvgGen<br>Parquet interface<br>SyscGen | DegreeConstrained<br>LatencyConstrained<br>Hierarchical |
| Building Automation | Interface<br>NodeParam<br>Threads | Specification<br>PItInstance<br>Implementation | Sensor<br>Actuator<br>Controller<br>TwistedPair | TokenRing<br>802.15.4 | WiringRule<br>NodePosition | DaisyChain<br>TreeWireless | Walls<br>CableLadder | BuildingParser<br>SvgGen<br>Desyre interface | DaisyChainPartition<br>WirelessTree |

**Figure 2.** How the COSI framework has been used to generate specific synthesis tools.

**Current work**

We continue to work towards expanding COSI capabilities, including better models for router delays, bus models, and support for the generation of synthesizable RTL description of the synthesized on-chip interconnection network. In this domain, we are integrating Desyre developed at PARADES with COSI. Meanwhile, we also plan to continue our work on the extension of the communication synthesis approach to the design of large-scale network for distributed embedded systems such as those that can be found in smart buildings.

**Participating partners:**

- **PARADES**
  Setting the directions of the framework. Methodology and theory. Integrating COSI with Desyre.
- **UC Berkeley**
  Tool development and application to Network on Chip and intelligent buildings
- **Columbia**
  Participation in the development of the methodology.

**Web**
http://embedded.eecs.berkeley.edu/cosi/

**Related Publications**

[PCSV208] A. Pinto, L. Carloni and A. Sangiovanni Vincentelli, COSI: A Framework for the Design of Interconnection Networks, IEEE Design and Test of Computers, vol. 25, n. 5, Sept-Oct. 2008, pp. 402-415.

### *4.5.3 SymTA/S*

**Objectives**

SymTA/S is a tool for the development and verification of embedded multiprocessor real-time systems. The existing technology is mainly suitable for event or time-driven systems with message passing as the main task interaction. The tool shall be extended to cover the timing implications of multicore processors, or multiprocessor-systems-on-chip.

**Main Results**

In several previous projects (funded by german DFG, “Sureal”, funded by german BMBF, ARTIST2, and others), the compositional analysis approach has been transferred into a tool framework which is now also commercially available. The available modelling options capture typical problems in todays automotive systems (CAN bus utilization, end-to-end deadlines,…). This addresses a growing need for formal methods in the industry. The topics currently under research (see below) address future problems which can be expected to become of increasing industrial interest in the future.

**Current work**

The research version of the tool framework is currently being developed into several new directions: Modeling of shared resources for multiprocessor-system-on-chips (see ArtistDesign Activity 6.2: Platform and MpSoC Analysis), the modelling of hierarchical event models (in the scope of the COMBEST project), and the demonstrator platform for adaptive systems (see ArtistDesign 7.1: Design for Adaptivity). Besides the extension of the applicability into new domains driven by industrial applications, a major focus within ArtistDesign is the synergetic coupling of tools, as well as the corresponding development of models.

**Participating partners:**

- TU Braunschweig investigates synergies in the coupling of methods and implements prototypical implementations of the research results.

  Symtavision GmbH is the commercial co-developer of the tool framework. A focus within ArtistDesign is the coupling of with other industrially available tools (such as aiT).
- ETHZ. Collaboration on the coupling of MPA and SymTA/S with respect to modelling of hierarchical event models.
- Absint GmbH. The aiT tool supplies task timing models, which are required for system level analysis.

### *4.5.4 ICD-C*

**Objectives**

ICD-C is a recent development platform with special support for source-to-source transformations. Source-to-source transformations can be implemented without loosing any information about the original C program. It can also be used in cases where full control over the libraries is required.

**Main Results**

ICD-C was used for the integration of compilers with timing analysis and the impact of optimizing the WCET was studied in a number of cases.

**Current work**

Current work is extending the support for caches and aims at reducing the number of calls of the WCET estimator in order to speed-up optimization. Machine-learning techniques are being tried as a promising approach.

**Participating partners:**

- TU Dortmund
- ICD Dortmund (via the Mnemee project)
- TU Eindhoven

**Web**

http://www.icd.de/es/index.html

# 5. Assessment of the Workpackage at the end of Y1

The ArtistDesign Network of Excellence is a significant evolutionary step for integrating the leading embedded systems design research teams in Europe. The clusters are more tightly woven together, and each represents a significantly greater critical mass than did the clusters in the Artist2 Network of Excellence, which ended Sept 30th 2008, and has nearly the same consortium.

Despite this strong overlap with the Artist2 NoE, the overall assessment for the WP at the end of ArtistDesign Y1 (Jan–Dec 2008) is positive - both in terms of impact on the overall structuring and lasting integration within the consortium and more generally within the area in Europe.

- The ArtistDesign clusters have been actively pursuing operational integration through joint meetings, staff mobility, and shared platforms and tools.
- The level of activity shows that the Cluster / Activity structure and research topics defined for ArtistDesign make sense, and are viable vehicles for integrating the area. In operational terms, they generate sufficient interest for the partners and individual researchers to participate actively in the joint meetings, to exchange personnel, and to orient the tools and platforms developed to make sense within this structure.
- There is clearly a greater level of maturity for tools and platforms than had been the case at the start of the Artist2 NoE – and the partner teams are actively pursuing a policy of implementing tools, demontrators, and in many cases their accompanying methodologies.
- Nonetheless, it is important to remember that these are tools and platforms for research. The aim is not necessarily always for these to lead to commercially viable tools and start-up companies. In general, they are the concrete realisation of the state-of-the-research, allowing to explore possibilities for future research and later tools (some of which may in turn lead to commercially viable products).
- The level of activity varies according to individual clusters / activities, which is normal. We believe this is partly due to the remaining overlap with Artist2 – which should no longer be the case in Y2.