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Towards Model Checking Executable UML Specifications in mCRL2

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> Eindhoven University of Technology University of Twente

> > 8 December 2009

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Introducti	on				

Verification of railway safety systems (interlockings):

- Specification is highly declarative (not an implementation)
- Specification written in executable UML

Executable UML (xUML):

- Class diagrams and state machines
- Particular dialect comes with a simulator

Verification approach:

Instantiate the model based on the layout of a railway yard

- Transform into an mCRL2 specification (process algebra)
- Apply model checking (both explicit and symbolic)

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mCRL2					

mCRL2 is an ACP-based process algebra:

- Synchronous communication between processes
- Processes and actions may carry data

Data types

- Built-in data types: integers, lists, …
- Abstract data types: sort myState = struct Yes | No

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Sequential processes (with data)

- Recursive processes: $\operatorname{proc} A(\ldots) = \cdots A(\ldots) \cdots$;
- Actions: a(...)
- ullet Sequential and alternative composition: . and +
- If-then-else construct: $c \rightarrow s \diamond t$

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mCRL2 (cont	.)			

• Quantification over data: $\sum_{d:D} P(d)$

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$$ext{proc } \mathtt{A}(n:\mathbb{N}) = \sum_{m:\mathbb{N}} \mathtt{a}(m).(m=0) o \mathtt{A}(n+1) \diamond (\mathtt{A}(m) + \mathtt{A}(n))$$

Parallel processes and communication

- parallel composition:
- synchronous communication (multi-actions): $a_1 | \cdots | a_n \rightarrow b$

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Example

 $\operatorname{comm}(\{a|b \rightarrow c\}, a(m) \parallel b(m))$ we observe c(m)

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mCRL2	(cont.)				

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Class diagrams

Inheritance and associations between classes

No association classes (classes labelling associations)

(Nested) state machines

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(Nested) state machines

States:

- Concurrent and composite states (AND- and OR-states)
- Initial pseudo states (no history and final pseudo states)
- Transitions labelled with "trigger[condition]/action"-triples
 - Trigger needed to take the transition (signal or change even
 - Condition needed to be valid upon taking the transition
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Signal a	nd (hand	re Event	5		

Events are stored in event pools (buffers), one per class instance

Signal events

Signals can be sent to classes and their associated state machines

- Signals are sent asynchronously
- Once received signal event is added to an event pool

Change events

Change events are of the form

when(*cond*)

where *cond* is a boolean expression:

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Run-to-Completion Assumptions

Run-to-completion assumptions specify the allowed interleavings

Definition (Run-to-completion (RTC))
Local RTC All actions of a transition in a state machine S
are executed before a new transition is taken by S
Atomic RTC All actions of a transition in the system
are executed before any new transition is taken
Global RTC External events are only accepted by the system
in case (i) all event pools are empty
and (ii) no actions are being executed

Local RTC is minimally required by the UML standard The available simulator enforces both atomic and global RTC

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Translati	ng Class	Diagran	ns		

- Inheritance is dealt with by "flattening" the class hierarchy
 ⇒ Concurrent composition of state machines related to classes
- Associations become parameters of processes





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Translating Event Pools and State Machines

Each process representing a class consists of two parallel processes:

- Buffer process
 - \Rightarrow Represents event pool associated with an instance of a class
 - $\Rightarrow\,$ Asynchronous communication in synchronous environment
- Process representing the state machine related to the class
 - \Rightarrow States are represented as data parameters to the process
 - \Rightarrow Process is a message loop:

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Change events are translated by introducing "monitor" processes

- One monitor per occurring change event
- Inner workings:
 - If part of the state referred to by the change event changes, then a message is sent synchronously to the related monitor
 Monitor checks if condition is valid while it wasn't before
 If so, the state machine to which the event belongs is notified (message is put in buffer associated with the state machine)

Observations (without showing any mCRL2 specification):

- Monitors duplicate state data
- Communication with monitors increases number of transitions

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Model C	hecking				

- Unlimited buffer size in translation \Rightarrow Infinite state space
- Only local RTC in translation \Rightarrow Starvation

Mitigation:

- Limited buffer space (solves *only* infinite state space problem)
- Barrier synchronisation (solves both issues, but global RTC)

Small Toy Specification (7 class instances)VersionState spaceSymbolicExplicitbuffer size 1 61×10^{12} 113 secsnot feasiblebarrier sync 8×10^6 160 secs $9\frac{1}{2}$ minutes

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No atomic RTC: yields traces not observable in the simulator

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Translation from xUML to mCRL2:

- Not extremely difficult
- Except for change events (not completely satisfactory)

Model checking the translation:

- Measures needed to avoid infinite state space and starvation
- State space can be huge
- Traces depend on RTC assumptions (different for simulator)

Future work:

- Automatic translation using the Epsilon framework
- Extend the translation to other xUML constructs
- Re-consider the translation of change events (avoid them?)

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